

## NE5532x, SA5532x Dual Low-Noise Operational Amplifiers

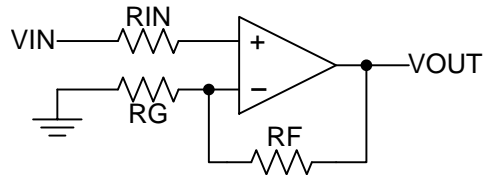
### 1 Features

- Equivalent Input Noise Voltage: 5 nV/ $\sqrt{\text{Hz}}$  Typ at 1 kHz
- Unity-Gain Bandwidth: 10 MHz Typ
- Common-Mode Rejection Ratio: 100 dB Typ
- High DC Voltage Gain: 100 V/mV Typ
- Peak-to-Peak Output Voltage Swing 26 V Typ With  $V_{CC\pm} = \pm 15$  V and  $R_L = 600 \Omega$
- High Slew Rate: 9 V/ $\mu\text{s}$  Typ

### 2 Applications

- AV Receivers
- Embedded PCs
- Netbooks
- Video Broadcasting and Infrastructure: Scalable Platforms
- DVD Recorders and Players
- Multichannel Video Transcoders
- Pro Audio Mixers

### 4 Simplified Schematic



### 3 Description

The NE5532, NE5532A, SA5532, and SA5532A devices are high-performance operational amplifiers combining excellent DC and AC characteristics. They feature very low noise, high output-drive capability, high unity-gain and maximum-output-swing bandwidths, low distortion, high slew rate, input-protection diodes, and output short-circuit protection. These operational amplifiers are compensated internally for unity-gain operation. These devices have specified maximum limits for equivalent input noise voltage.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
NE5532x, SA5532x	SOIC (8)	4.90 mm × 3.91 mm
NE5532x, SA5532x	PDIP (8)	9.81 mm × 6.35 mm
NE5532x	SO (8)	6.20 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	8.2 Functional Block Diagram .....	<b>7</b>
<b>2 Applications</b> .....	<b>1</b>	8.3 Feature Description .....	<b>7</b>
<b>3 Description</b> .....	<b>1</b>	8.4 Device Functional Modes .....	<b>7</b>
<b>4 Simplified Schematic</b> .....	<b>1</b>	<b>9 Application and Implementation</b> .....	<b>8</b>
<b>5 Revision History</b> .....	<b>2</b>	9.1 Typical Application .....	<b>8</b>
<b>6 Pin Configuration and Functions</b> .....	<b>3</b>	<b>10 Power Supply Recommendations</b> .....	<b>11</b>
<b>7 Specifications</b> .....	<b>4</b>	<b>11 Layout</b> .....	<b>11</b>
7.1 Absolute Maximum Ratings .....	<b>4</b>	11.1 Layout Guidelines .....	<b>11</b>
7.2 ESD Ratings .....	<b>4</b>	11.2 Layout Example .....	<b>11</b>
7.3 Recommended Operating Conditions .....	<b>4</b>	<b>12 Device and Documentation Support</b> .....	<b>13</b>
7.4 Thermal Information .....	<b>4</b>	12.1 Related Links .....	<b>13</b>
7.5 Electrical Characteristics .....	<b>5</b>	12.2 Trademarks .....	<b>13</b>
7.6 Operating Characteristics .....	<b>5</b>	12.3 Electrostatic Discharge Caution .....	<b>13</b>
7.7 Typical Characteristics .....	<b>6</b>	12.4 Glossary .....	<b>13</b>
<b>8 Detailed Description</b> .....	<b>7</b>	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	<b>13</b>
8.1 Overview .....	<b>7</b>		

## 5 Revision History

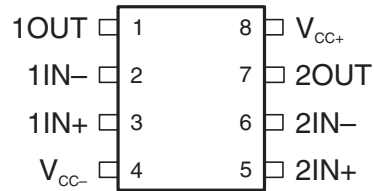
### Changes from Revision I (April 2009) to Revision J

**Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. .... **1**
- Deleted *Ordering Information* table. .... **1**

## 6 Pin Configuration and Functions

**NE5532, NE5532A . . . D, P, OR PS PACKAGE  
SA5532, SA5532A . . . D OR P PACKAGE  
(TOP VIEW)**



### Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN+	3	I	Noninverting input
1IN-	2	I	Inverting Input
OUT1	1	O	Output
2IN+	5	I	Noninverting input
2IN-	6	I	Inverting Input
2OUT	7	O	Output
VCC+	8	—	Positive Supply
VCC-	4	—	Negative Supply

## 7 Specifications

### 7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage <sup>(2)</sup>	V <sub>CC+</sub>	0	22	V
		V <sub>CC-</sub>	-22	0	V
Input voltage, either input <sup>(2)(3)</sup>		V <sub>CC-</sub>	V <sub>CC+</sub>	V	
Input current <sup>(4)</sup>		-10	10	mA	
Duration of output short circuit <sup>(5)</sup>		Unlimited			
T <sub>J</sub>	Operating virtual-junction temperature	150		°C	
T <sub>stg</sub>	Storage temperature range	-65	150	°C	

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltage values, except differential voltages, are with respect to the midpoint between V<sub>CC+</sub> and V<sub>CC-</sub>.
- The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
- Excessive input current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs, unless some limiting resistance is used.
- The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	1000	

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

		MIN	MAX	UNIT	
V <sub>CC+</sub>	Supply voltage	5	15	V	
V <sub>CC-</sub>	Supply voltage	-5	-15	V	
T <sub>A</sub>	Operating free-air temperature	NE5532, NE5532A	0	70	°C
		SA5532, SA5532A	-40	85	

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		NE5532, NE5532A, SA5532, and SA5532A			UNIT
		D	P	PS	
		8 PINS			
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(2)(3)</sup>	97	85	95	°C/W

- For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- The package thermal impedance is calculated in accordance with JESD 51-7.
- Maximum power dissipation is a function of T<sub>J(max)</sub>, θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> - T<sub>A</sub>) / θ<sub>JA</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.

## 7.5 Electrical Characteristics

 $V_{CC\pm} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	$V_O = 0$	$T_A = 25^\circ\text{C}$	0.5	4		mV
			$T_A = \text{Full range}^{(2)}$			5	
$I_{IO}$	Input offset current		$T_A = 25^\circ\text{C}$	10	150		nA
			$T_A = \text{Full range}^{(2)}$			200	
$I_{IB}$	Input bias current		$T_A = 25^\circ\text{C}$	200	800		nA
			$T_A = \text{Full range}^{(2)}$			1000	
$V_{ICR}$	Common-mode input-voltage range			$\pm 12$	$\pm 13$		V
$V_{OPP}$	Maximum peak-to-peak output-voltage swing	$R_L \geq 600\ \Omega$ , $V_{CC\pm} = \pm 15\text{ V}$		24	26		V
$A_{VD}$	Large-signal differential-voltage amplification	$R_L \geq 600\ \Omega$ , $V_O = \pm 10\text{ V}$	$T_A = 25^\circ\text{C}$	15	50		V/mV
			$T_A = \text{Full range}^{(2)}$	10			
		$R_L \geq 2\ \text{k}\Omega$ , $V_O = \pm 10\text{ V}$	$T_A = 25^\circ\text{C}$	25	100		
			$T_A = \text{Full range}^{(2)}$	15			
$A_{vd}$	Small-signal differential-voltage amplification	$f = 10\ \text{kHz}$		2.2		V/mV	
$B_{OM}$	Maximum output-swing bandwidth	$R_L = 600\ \Omega$ , $V_O = \pm 10\text{ V}$		140			kHz
$B_1$	Unity-gain bandwidth	$R_L = 600\ \Omega$ , $C_L = 100\ \text{pF}$		10			MHz
$r_i$	Input resistance			30	300		k $\Omega$
$z_o$	Output impedance	$A_{VD} = 30\ \text{dB}$ , $R_L = 600\ \Omega$ , $f = 10\ \text{kHz}$		0.3			$\Omega$
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\ \text{min}$		70	100		dB
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC\pm} = \pm 9\text{ V}$ to $\pm 15\text{ V}$ , $V_O = 0$		80	100		dB
$I_{OS}$	Output short-circuit current			10	38	60	mA
$I_{CC}$	Total supply current	$V_O = 0$ , No load		8	16		mA
	Crosstalk attenuation ( $V_{O1}/V_{O2}$ )	$V_{O1} = 10\text{ V}$ peak, $f = 1\ \text{kHz}$		110			dB

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified.

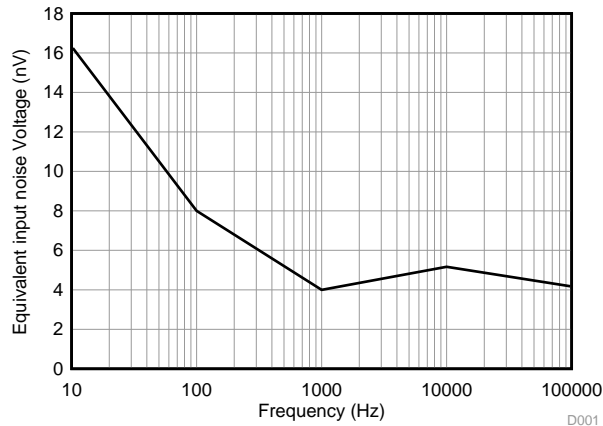
(2) Full temperature ranges are:  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  for the SA5532 and SA5532A devices, and  $0^\circ\text{C}$  to  $70^\circ\text{C}$  for the NE5532 and NE5532A devices.

## 7.6 Operating Characteristics

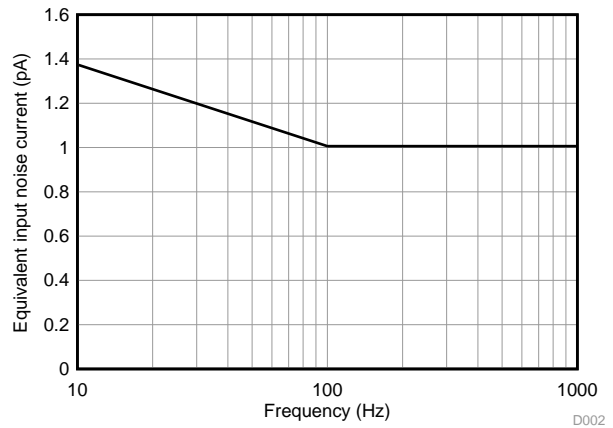
 $V_{CC\pm} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	NE5532, SA5532			NE5532A, SA5532A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain		9		9			V/ $\mu\text{s}$
	Overshoot factor	$V_I = 100\ \text{mV}$ , $R_L = 600\ \Omega$ , $A_{VD} = 1$ , $C_L = 100\ \text{pF}$		10		10		%
$V_n$	Equivalent input noise voltage	$f = 30\ \text{Hz}$		8		8	10	nV/ $\sqrt{\text{Hz}}$
		$f = 1\ \text{kHz}$		5		5	6	
$I_n$	Equivalent input noise current	$f = 30\ \text{Hz}$		2.7		2.7		pA/ $\sqrt{\text{Hz}}$
		$f = 1\ \text{kHz}$		0.7		0.7		

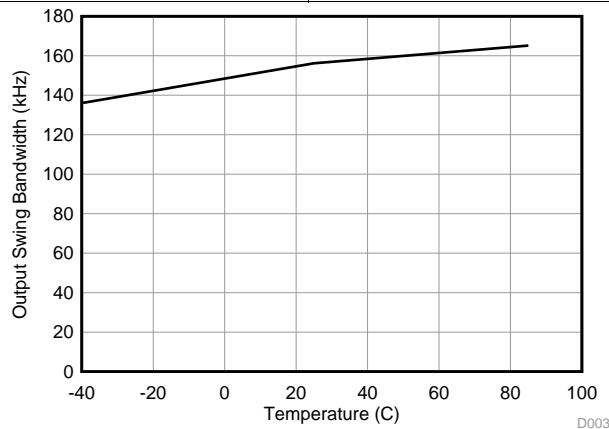
## 7.7 Typical Characteristics



**Figure 1. Equivalent Input Noise Voltage vs Frequency**



**Figure 2. Equivalent Input Noise Current vs Frequency**



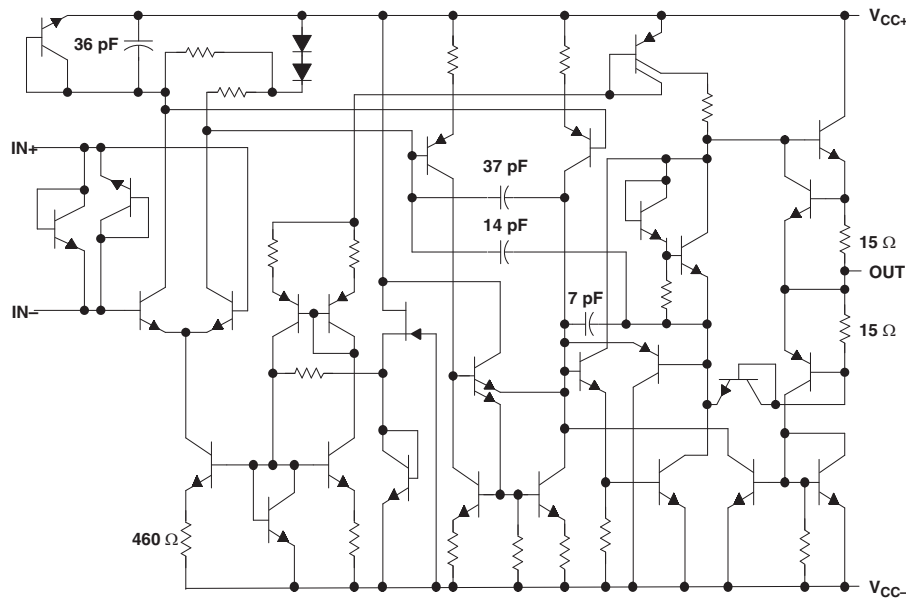
**Figure 3. Output Swing Bandwidth vs Temperature at V<sub>CC</sub> = ±10 V**

## 8 Detailed Description

### 8.1 Overview

The NE5532, NE5532A, SA5532, and SA5532A devices are high-performance operational amplifiers combining excellent dc and ac characteristics. They feature very low noise, high output-drive capability, high unity-gain and maximum-output-swing bandwidths, low distortion, high slew rate, input-protection diodes, and output short-circuit protection. These operational amplifiers are compensated internally for unity-gain operation. These devices have specified maximum limits for equivalent input noise voltage.

### 8.2 Functional Block Diagram



Component values shown are nominal.

### 8.3 Feature Description

#### 8.3.1 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. The NE5532, NE5532A, SA5532, and SA5532A devices have a 10-MHz unity-gain bandwidth.

#### 8.3.2 Common-Mode Rejection Ratio

The common-mode rejection ratio (CMRR) of an amplifier is a measure of how well the device rejects unwanted input signals common to both input leads. It is found by taking the ratio of the change in input offset voltage to the change in the input voltage and converting to decibels. Ideally the CMRR would be infinite, but in practice, amplifiers are designed to have it as high as possible. The CMRR of the NE5532, NE5532A, SA5532, and SA5532A devices is 100 dB.

#### 8.3.3 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. The NE5532, NE5532A, SA5532, and SA5532A devices have a 9-V/ms slew rate.

### 8.4 Device Functional Modes

The NE5532, NE5532A, SA5532, and SA5532A devices are powered on when the supply is connected. Each of these devices can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

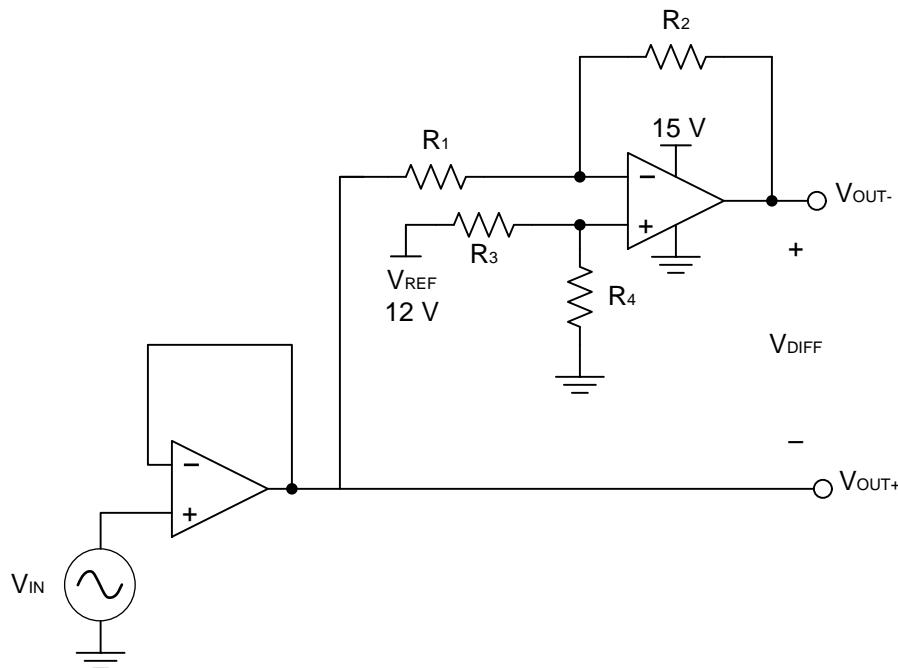
## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Typical Application

Some applications require differential signals. Figure 4 shows a simple circuit to convert a single-ended input of 2 V to 10 V into differential output of  $\pm 8$  V on a single 15-V supply. The output range is intentionally limited to maximize linearity. The circuit is composed of two amplifiers. One amplifier acts as a buffer and creates a voltage,  $V_{OUT+}$ . The second amplifier inverts the input and adds a reference voltage to generate  $V_{OUT-}$ . Both  $V_{OUT+}$  and  $V_{OUT-}$  range from 2 V to 10 V. The difference,  $V_{DIFF}$ , is the difference between  $V_{OUT+}$  and  $V_{OUT-}$ .



**Figure 4. Schematic for Single-Ended Input to Differential Output Conversion**

#### 9.1.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 15 V
- Reference voltage: 12V
- Input: 2 V to 10 V
- Output differential:  $\pm 8$  V



## Typical Application (continued)

### 9.1.2 Detailed Design Procedure

The circuit in [Figure 4](#) takes a single-ended input signal,  $V_{IN}$ , and generates two output signals,  $V_{OUT+}$  and  $V_{OUT-}$  using two amplifiers and a reference voltage,  $V_{REF}$ .  $V_{OUT+}$  is the output of the first amplifier and is a buffered version of the input signal,  $V_{IN}$  [Equation 1](#).  $V_{OUT-}$  is the output of the second amplifier which uses  $V_{REF}$  to add an offset voltage to  $V_{IN}$  and feedback to add inverting gain. The transfer function for  $V_{OUT-}$  is [Equation 2](#).

$$V_{OUT+} = V_{IN} \quad (1)$$

$$V_{out-} = V_{ref} \times \left( \frac{R_4}{R_3 + R_4} \right) \times \left( 1 + \frac{R_2}{R_1} \right) - V_{in} \times \frac{R_2}{R_1} \quad (2)$$

The differential output signal,  $V_{DIFF}$ , is the difference between the two single-ended output signals,  $V_{OUT+}$  and  $V_{OUT-}$ . [Equation 3](#) shows the transfer function for  $V_{DIFF}$ . By applying the conditions that  $R_1 = R_2$  and  $R_3 = R_4$ , the transfer function is simplified into [Equation 6](#). Using this configuration, the maximum input signal is equal to the reference voltage and the maximum output of each amplifier is equal to the  $V_{REF}$ . The differential output range is  $2 \times V_{REF}$ . Furthermore, the common mode voltage will be one half of  $V_{REF}$  (see [Equation 7](#)).

$$V_{DIFF} = V_{OUT+} - V_{OUT-} = V_{IN} \times \left( 1 + \frac{R_2}{R_1} \right) - V_{REF} \times \left( \frac{R_4}{R_3 + R_4} \right) \left( 1 + \frac{R_2}{R_1} \right) \quad (3)$$

$$V_{OUT+} = V_{IN} \quad (4)$$

$$V_{OUT-} = V_{REF} - V_{IN} \quad (5)$$

$$V_{DIFF} = 2 \times V_{IN} - V_{REF} \quad (6)$$

$$V_{cm} = \left( \frac{V_{OUT+} + V_{OUT-}}{2} \right) = \frac{1}{2} V_{REF} \quad (7)$$

#### 9.1.2.1 Amplifier Selection

Linearity over the input range is key for good dc accuracy. The common mode input range and the output swing limitations determine the linearity. In general, an amplifier with rail-to-rail input and output swing is required. Bandwidth is a key concern for this design. Since the NE5532 has a bandwidth of 10 MHz, this circuit will only be able to process signals with frequencies of less than 10 MHz.

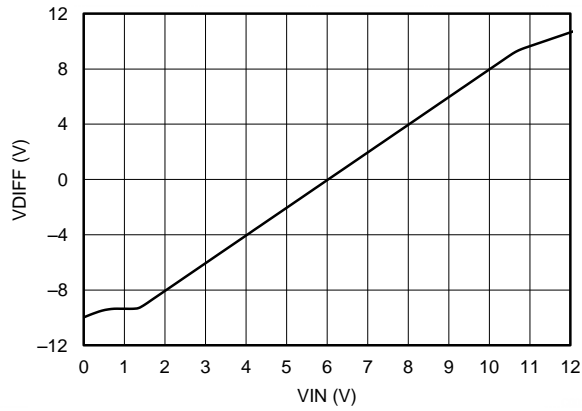
#### 9.1.2.2 Passive Component Selection

Because the transfer function of  $V_{OUT-}$  is heavily reliant on resistors ( $R_1$ ,  $R_2$ ,  $R_3$ , and  $R_4$ ), use resistors with low tolerances to maximize performance and minimize error. This design used resistors with resistance values of 36 k $\Omega$  with tolerances measured to be within 2%. But, if the noise of the system is a key parameter, the user can select smaller resistance values (6 k $\Omega$  or lower) to keep the overall system noise low. This ensures that the noise from the resistors is lower than the amplifier noise.

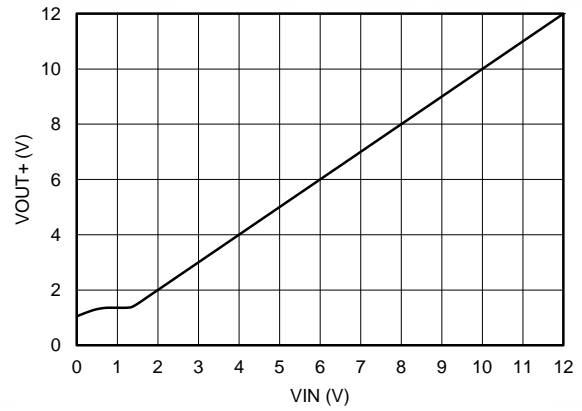
### 9.1.3 Application Curves

The measured transfer functions in [Figure 5](#), [Figure 6](#), and [Figure 7](#) were generated by sweeping the input voltage from 0 V to 12V. However, this design should only be used between 2 V and 10 V for optimum linearity.

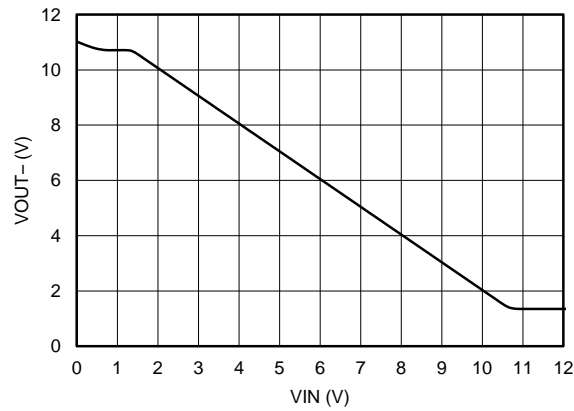
**Typical Application (continued)**



**Figure 5. Differential Output Voltage vs Input Voltage**



**Figure 6. Positive Output Voltage Node vs Input Voltage**



**Figure 7. Positive Output Voltage Node vs Input Voltage**

## 10 Power Supply Recommendations

The NE5532x and SA5532x devices are specified for operation over the range of  $\pm 5$  to  $\pm 15$  V; many specifications apply from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$  (NE5532x) and  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  (SA5532x). The [Typical Characteristics](#) section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

### CAUTION

Supply voltages outside of the  $\pm 22$  V range can permanently damage the device (see the [Absolute Maximum Ratings](#)).

Place 0.1- $\mu\text{F}$  bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the [Layout Guidelines](#).

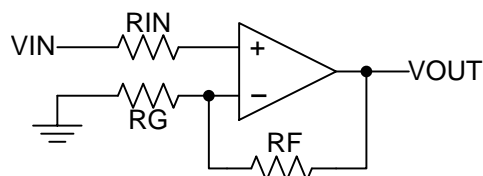
## 11 Layout

### 11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

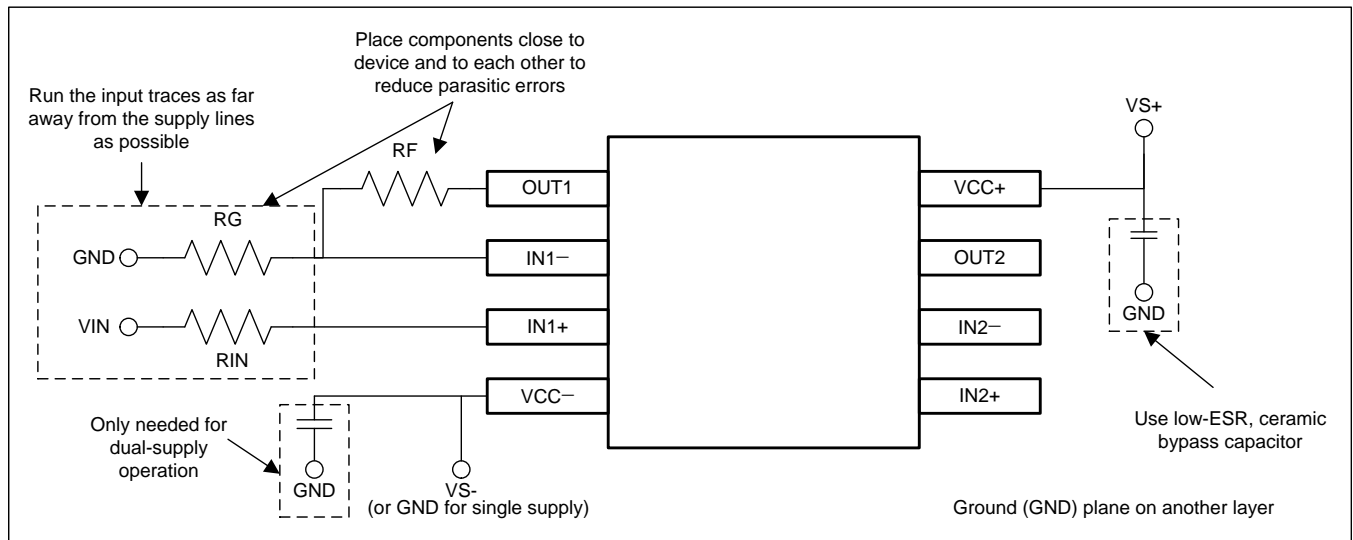
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu\text{F}$  ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to Circuit Board Layout Techniques, [SLOA089](#).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in [Layout Example](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

### 11.2 Layout Example



**Figure 8. Operational Amplifier Schematic for Noninverting Configuration**

**Layout Example (continued)**



**Figure 9. Operational Amplifier Board Layout for Noninverting Configuration**

## 12 Device and Documentation Support

### 12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 1. Related Links**

Parts	Product Folder	Sample & Buy	Technical Documents	Tools & Software	Support & Community
NE5532	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
NE5532A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
SA5532	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
SA5532A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.2 Trademarks

All trademarks are the property of their respective owners.

### 12.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
NE5532AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A	<a href="#">Samples</a>
NE5532ADE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A	<a href="#">Samples</a>
NE5532ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A	<a href="#">Samples</a>
NE5532ADRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A	<a href="#">Samples</a>
NE5532ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A	<a href="#">Samples</a>
NE5532AP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	NE5532AP	<a href="#">Samples</a>
NE5532APE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	NE5532AP	<a href="#">Samples</a>
NE5532APSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A	<a href="#">Samples</a>
NE5532APSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A	<a href="#">Samples</a>
NE5532D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532	<a href="#">Samples</a>
NE5532DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532	<a href="#">Samples</a>
NE5532DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	0 to 70	N5532	<a href="#">Samples</a>
NE5532DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532	<a href="#">Samples</a>
NE5532DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532	<a href="#">Samples</a>
NE5532P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU   CU SN	N / A for Pkg Type	0 to 70	NE5532P	<a href="#">Samples</a>
NE5532PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	NE5532P	<a href="#">Samples</a>
NE5532PSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
NE5532PSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532	<a href="#">Samples</a>
NE5532PSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532	<a href="#">Samples</a>
SA5532AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5532A	<a href="#">Samples</a>
SA5532ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5532A	<a href="#">Samples</a>
SA5532ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5532A	<a href="#">Samples</a>
SA5532ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5532A	<a href="#">Samples</a>
SA5532AP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SA5532AP	<a href="#">Samples</a>
SA5532APE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SA5532AP	<a href="#">Samples</a>
SA5532D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5532	<a href="#">Samples</a>
SA5532DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5532	<a href="#">Samples</a>
SA5532DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5532	<a href="#">Samples</a>
SA5532P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SA5532P	<a href="#">Samples</a>
SA5532PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SA5532P	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

---

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

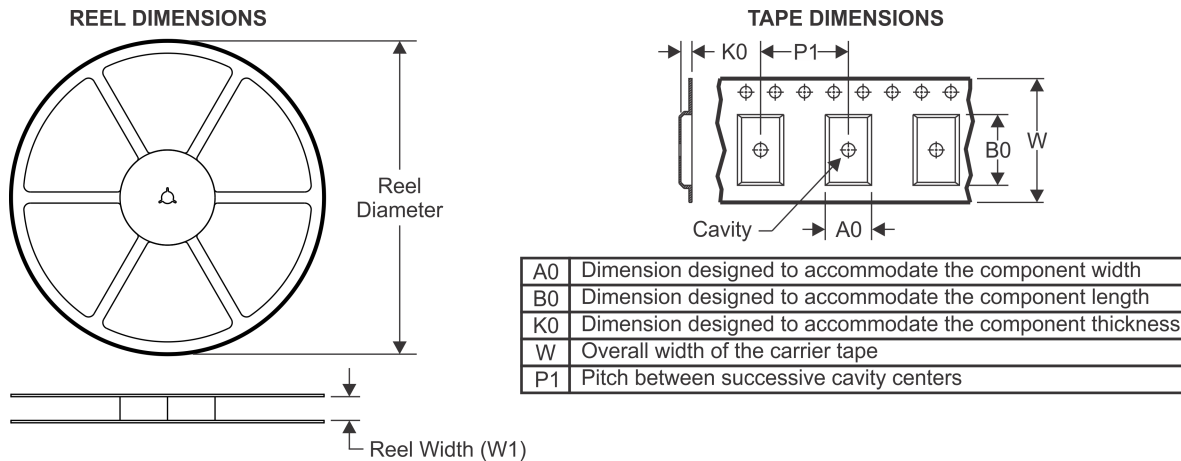
<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
NE5532ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE5532APSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
NE5532DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE5532DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
NE5532DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE5532PSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SA5532ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SA5532DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
NE5532ADR	SOIC	D	8	2500	340.5	338.1	20.6
NE5532APSR	SO	PS	8	2000	367.0	367.0	38.0
NE5532DR	SOIC	D	8	2500	340.5	338.1	20.6
NE5532DR	SOIC	D	8	2500	364.0	364.0	27.0
NE5532DRG4	SOIC	D	8	2500	340.5	338.1	20.6
NE5532PSR	SO	PS	8	2000	367.0	367.0	38.0
SA5532ADR	SOIC	D	8	2500	340.5	338.1	20.6
SA5532DR	SOIC	D	8	2500	340.5	338.1	20.6

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.  
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.  
 E. Reference JEDEC MS-012 variation AA.

# MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.