

DS90LV032A 3V LVDS Quad CMOS Differential Line Receiver

Check for Samples: [DS90LV032A](#)

FEATURES

- >400 Mbps (200 MHz) switching rates
- 0.1 ns channel-to-channel skew (typical)
- 0.1 ns differential skew (typical)
- 3.3 ns maximum propagation delay
- 3.3V power supply design
- Power down high impedance on LVDS inputs
- Low Power design (40mW @ 3.3V static)
- Interoperable with existing 5V LVDS networks
- Accepts small swing (350 mV typical) VID
- Supports open, short and terminated input fail-safe
- Compatible with ANSI/TIA/EIA-644
- Industrial temp. operating range (-40°C to +85°C)
- Available in SOIC and TSSOP Packaging

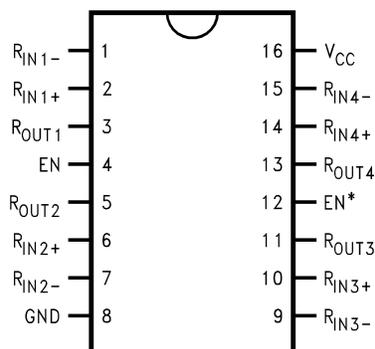
DESCRIPTION

The DS90LV032A is a quad CMOS differential line receiver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90LV032A accepts low voltage (350 mV typical) differential input signals and translates them to 3V CMOS output levels. The receiver supports a TRI-STATE[®] function that may be used to multiplex outputs. The receiver also supports open, shorted and terminated (100Ω) input Fail-safe. The receiver output will be HIGH for all fail-safe conditions.

The DS90LV032A and companion LVDS line driver (eg. DS90LV031A) provide a new alternative to high power PECL/ECL devices for high speed point-to-point interface applications.

Connection Diagram



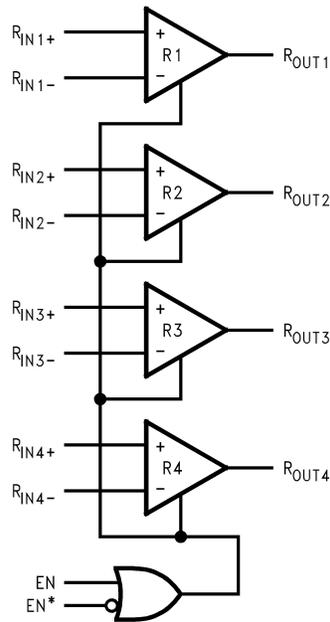
**Order Number DS90LV032ATM
or DS90LV032ATMTC
D-16 and PW-16 Packages**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TRI-STATE is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

Functional Diagram



Truth Table

| ENABLES | | INPUTS | OUTPUT |
|---|-----|---|------------------|
| EN | EN* | R _{IN+} – R _{IN-} | R _{OUT} |
| L | H | X | Z |
| All other combinations of ENABLE inputs | | $V_{ID} \geq 0.1V$ | H |
| | | $V_{ID} \leq -0.1V$ | L |
| | | Full Fail-safe OPEN/SHORT or Terminated | H |



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾

| | |
|---|------------------------------|
| Supply Voltage (V_{CC}) | -0.3V to +4V |
| Input Voltage (R_{IN+} , R_{IN-}) | -0.3V to +3.9V |
| Enable Input Voltage (EN, EN*) | -0.3V to ($V_{CC} + 0.3V$) |
| Output Voltage (R_{OUT}) | -0.3V to ($V_{CC} + 0.3V$) |
| Maximum Package Power Dissipation @ +25°C | |
| D Package | 1025 mW |
| PW Package | 866 mW |
| Derate D Package | 8.2 mW/°C above +25°C |
| Derate PW Package | 6.9 mW/°C above +25°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature Range | |
| (Soldering 4 sec.) | +260°C |
| Maximum Junction Temperature | +150°C |
| ESD Rating ⁽²⁾ | |
| (HBM 1.5 k Ω , 100 pF) | ≥ 4.5 kV |
| (EIAJ 0 Ω , 200 pF) | ≥ 250 V |

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. [Electrical Characteristics](#) specifies conditions of device operation.

(2) ESD Rating:

HBM (1.5 k Ω , 100 pF) ≥ 4.5 kV

EIAJ (0 Ω , 200 pF) ≥ 250 V

Recommended Operating Conditions

| | Min | Typ | Max | Units |
|-----------------------------|------|------|------|-------|
| Supply Voltage (V_{CC}) | +3.0 | +3.3 | +3.6 | V |
| Receiver Input Voltage | GND | | +3.0 | V |
| Operating Free Air | | | | |
| Temperature (T_A) | -40 | 25 | +85 | °C |

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. ⁽¹⁾

| Symbol | Parameter | Conditions | Pin | Min | Typ | Max | Units |
|-----------|--|---|-------------------------|---------------|---------|----------|---------|
| V_{TH} | Differential Input High Threshold | $V_{CM} = +1.2V^{(2)}$ | R_{IN+} R_{IN-} | | +20 | +100 | mV |
| V_{TL} | Differential Input Low Threshold | | | -100 | -20 | | mV |
| VCMR | Common-Mode Voltage Range | $VID = 200$ mV peak to peak ⁽³⁾ | | 0.1 | | 2.3 | V |
| I_{IN} | Input Current | $V_{IN} = +2.8V$ | $V_{CC} = 3.6V$ or $0V$ | -10 | ± 1 | +10 | μA |
| | | $V_{IN} = 0V$ | | -10 | ± 1 | +10 | μA |
| | | $V_{IN} = +3.6V$ | | $V_{CC} = 0V$ | -20 | | +20 |
| V_{OH} | Output High Voltage | $I_{OH} = -0.4$ mA, $V_{ID} = +200$ mV | R_{OUT} | 2.7 | 3.0 | | V |
| | | $I_{OH} = -0.4$ mA, Input terminated | | 2.7 | 3.0 | | V |
| | | $I_{OH} = -0.4$ mA, Input shorted | | 2.7 | 3.0 | | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 2$ mA, $V_{ID} = -200$ mV | | | 0.1 | 0.25 | V |
| I_{OS} | Output Short Circuit Current | Enabled, $V_{OUT} = 0V$ ⁽⁴⁾ | | -15 | -48 | -120 | mA |
| I_{OZ} | Output TRI-STATE Current | Disabled, $V_{OUT} = 0V$ or V_{CC} | | -10 | ± 1 | +10 | μA |
| V_{IH} | Input High Voltage | | EN, EN* | 2.0 | | V_{CC} | V |
| V_{IL} | Input Low Voltage | | | GND | | 0.8 | V |
| I_I | Input Current | $V_{IN} = 0V$ or V_{CC} , Other Input = V_{CC} or GND | | -10 | ± 1 | +10 | μA |
| V_{CL} | Input Clamp Voltage | $I_{CL} = -18$ mA | | -1.5 | -0.8 | | V |
| I_{CC} | No Load Supply Current | EN, EN* = V_{CC} or GND, Inputs Open | V_{CC} | | 10 | 15 | mA |
| | Receivers Enabled | EN, EN* = 2.4V or 0.5V, Inputs Open | | | 10 | 15 | mA |
| I_{CCZ} | No Load Supply Current Receivers Disabled | EN = GND, EN* = V_{CC} , Inputs Open | | | | 3 | 5 |

- (1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.
- (2) V_{CC} is always higher than R_{IN+} and R_{IN-} voltage. R_{IN-} and R_{IN+} are allowed to have a voltage range $-0.2V$ to $V_{CC} - VID/2$. However, to be compliant with AC specifications, the common voltage range is 0.1V to 2.3V
- (3) The VCMR range is reduced for larger VID. Example: if $VID = 400mV$, the VCMR is 0.2V to 2.2V. The fail-safe condition with inputs shorted is valid over a common-mode range of 0V to 2.3V. A VID up to $V_{CC} - 0V$ may be applied to the R_{IN+}/R_{IN-} inputs with the Common-Mode voltage set to $V_{CC}/2$. Propagation delay and Differential Pulse skew decrease when VID is increased from 200mV to 400mV. Skew specifications apply for $200mV \leq VID \leq 800mV$ over the common-mode range.
- (4) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.

Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. ⁽¹⁾ ⁽²⁾ ⁽³⁾ ⁽⁴⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|------------|---|---------------------------|-----|------|------|-------|
| t_{PHLD} | Differential Propagation Delay High to Low | $C_L = 10 \text{ pF}$ | 1.8 | | 3.3 | ns |
| t_{PLHD} | Differential Propagation Delay Low to High | $V_{ID} = 200 \text{ mV}$ | 1.8 | | 3.3 | ns |
| t_{SKD1} | Differential Pulse Skew $ t_{PHLD} - t_{PLHD} $ ⁽⁵⁾ | (Figure 1 and Figure 2) | 0 | 0.1 | 0.35 | ns |
| t_{SKD2} | Differential Channel-to-Channel Skew-same device ⁽³⁾ | | 0 | 0.1 | 0.5 | ns |
| t_{SKD3} | Differential Part to Part Skew ⁽⁴⁾ | | | | 1.0 | ns |
| t_{SKD4} | Differential Part to Part Skew ⁽⁶⁾ | | | | 1.5 | ns |
| t_{TLH} | Rise Time | | | 0.35 | 1.2 | ns |
| t_{THL} | Fall Time | | | 0.35 | 1.2 | ns |
| t_{PHZ} | Disable Time High to Z | $R_L = 2 \text{ k}\Omega$ | | 8 | 12 | ns |
| t_{PLZ} | Disable Time Low to Z | $C_L = 10 \text{ pF}$ | | 6 | 12 | ns |
| t_{PZH} | Enable Time Z to High | (Figure 3 and Figure 4) | | 11 | 17 | ns |
| t_{PZL} | Enable Time Z to Low | | | 11 | 17 | ns |
| f_{MAX} | Maximum Operating Frequency ⁽⁷⁾ | All Channels Switching | 200 | 250 | | MHz |

- (1) All typicals are given for: $V_{CC} = +3.3\text{V}$, $T_A = +25^\circ\text{C}$.
- (2) Generator waveform for all tests unless otherwise specified: $f = 1 \text{ MHz}$, $Z_O = 50\Omega$, t_r and t_f (0% to 100%) $\leq 3 \text{ ns}$ for R_{IN} .
- (3) t_{SKD2} , Channel-to-Channel Skew, is defined as the difference between the propagation delay of one channel and that of the others on the same chip with any event on the inputs.
- (4) t_{SKD3} , part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same V_{CC} , and within 5°C of each other within the operating temperature range.
- (5) t_{SKD1} is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel
- (6) t_{SKD4} , part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as $|\text{Max} - \text{Min}|$ differential propagation delay.
- (7) f_{MAX} generator input conditions: $t_r = t_f < 1\text{ns}$ (0% to 100%), 50% duty cycle, differential (1.05V to 1.35V peak to peak). Output Criteria: 60%/40% duty cycle, V_{OL} (max 0.4V), V_{OH} (min 2.7V), Load = 10 pF (stray plus probes)

PARAMETER MEASUREMENT INFORMATION

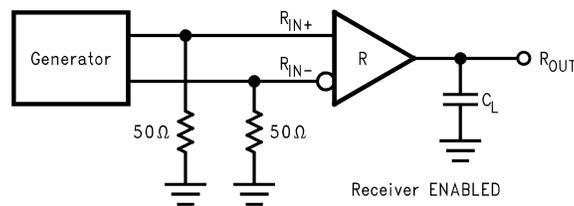


Figure 1. Receiver Propagation Delay and Transition Time Test Circuit

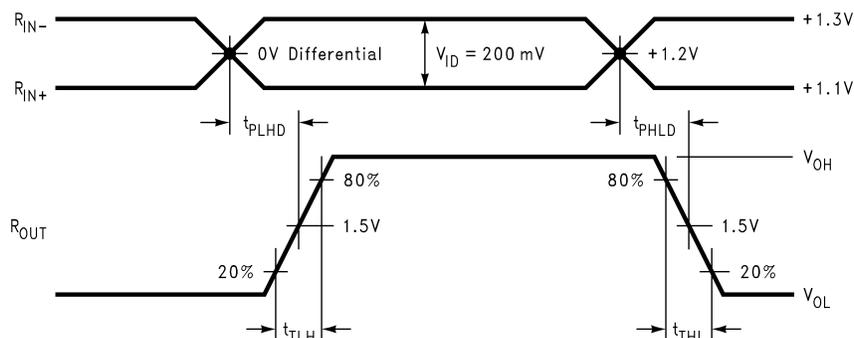
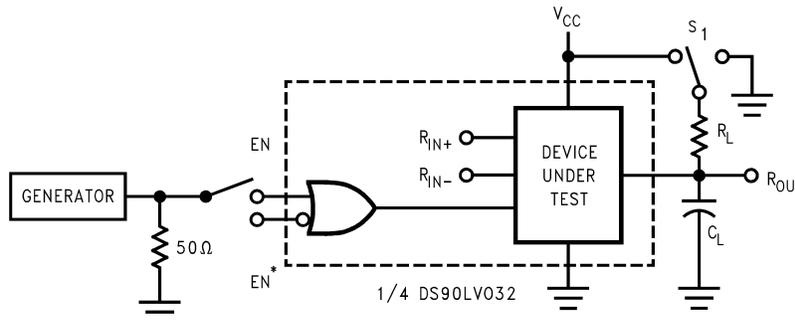


Figure 2. Receiver Propagation Delay and Transition Time Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



C_L includes load and test jig capacitance.
 $S_1 = V_{CC}$ for t_{PZL} and t_{PLZ} measurements.
 $S_1 = GND$ for t_{PZH} and t_{PHZ} measurements.

Figure 3. Receiver TRI-STATE Delay Test Circuit

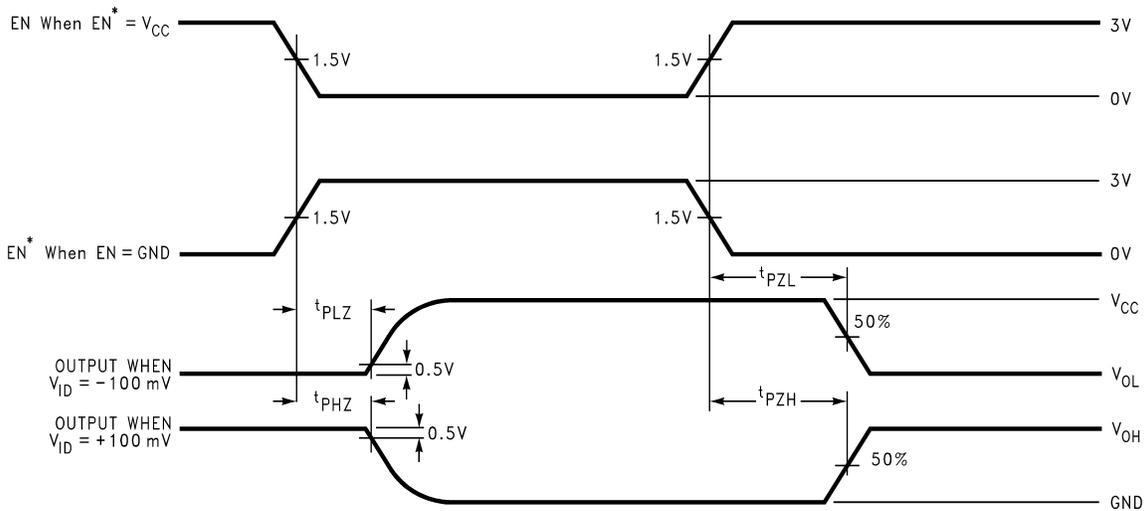


Figure 4. Receiver TRI-STATE Delay Waveforms

TYPICAL APPLICATION

Balanced System

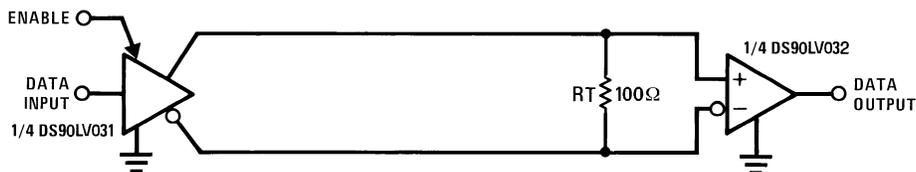


Figure 5. Point-to-Point Application

APPLICATION INFORMATION

General application guidelines and hints for LVDS drivers and receivers may be found in the application notes found at: <http://www.ti.com/ww/en/analog/interface/lvds.shtml>.

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in [Figure 5](#). This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the driver output (current mode) into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90LV032A differential line receiver is capable of detecting signals as low as 100 mV, over a ±1V common-mode range centered around +1.2V. This is related to the driver offset voltage which is typically +1.2V. The driven signal is centered around this voltage and may shift ±1V around this center point. The ±1V shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise, or a combination of the two. Both receiver input pins have a recommended operating input voltage range of 0V to +2.4V (measured from each pin to ground), exceeding these limits may turn on the ESD protection circuitry which will clamp the bus voltages.

Power Decoupling Recommendations

Bypass capacitors must be used on power pins. High frequency ceramic (surface mount is recommended) 0.1μF in parallel with 0.01μF, in parallel with 0.001μF at the power supply pin as well as scattered capacitors over the printed circuit board. Multiple vias should be used to connect the decoupling capacitors to the power planes. A 10μF (35V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board.

PC Board considerations

Use at least 4 PCB layers (top to bottom); LVDS signals, ground, power, TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s).

Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

Differential Traces

Use controlled impedance traces which match the differential impedance of your transmission medium (ie. cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be < 10mm long). This will help eliminate reflections and ensure noise is coupled as common-mode. Lab experiments show that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. Plus, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result. (Note the velocity of propagation, $v = c/Er$ where c (the speed of light) = 0.2997mm/ps or 0.0118 in/ps). Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

Termination

Use a resistor which best matches the differential impedance of your transmission line. The resistor should be between 90Ω and 130Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work without resistor termination. Typically, connect a single resistor across the pair at the receiver end.

Surface mount 1% to 2% resistors are best. PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be <10mm (12mm MAX)

Probing LVDS Transmission Lines

Always use high impedance (> 100kΩ), low capacitance (< 2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing will give deceiving results.

Cables and Connectors, General Comments

When choosing cable and connectors for LVDS it is important to remember:

Use controlled impedance media. The cables and connectors you use should have a matched differential impedance of about 100Ω. They should not introduce major impedance discontinuities.

Balanced cables (e.g. twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax.) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode (not differential mode) noise which is rejected by the receiver. For cable distances < 0.5M, most cables can be made to work effectively. For distances $0.5M \leq d \leq 10M$, CAT 3 (category 3) twisted pair cable works well, is readily available and relatively inexpensive.

Fail-Safe Feature

The LVDS receiver is a high gain, high speed device that amplifies a small differential signal (20mV) to CMOS logic levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal.

The receiver's internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated or shorted receiver inputs.

1. **Open Input Pins.** The DS90LV032A is a quad receiver device, and if an application requires only 1, 2 or 3 receivers, the unused channel(s) inputs should be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will ensure a HIGH, stable output state for open inputs.
2. **Terminated Input.** If the driver is disconnected (cable unplugged), or if the driver is in a TRI-STATE or power-off condition, the receiver output will again be in a HIGH state, even with the end of cable 100Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. Twisted pair cable will offer better balance than flat ribbon cable.
3. **Shorted Inputs.** If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0V differential input voltage, the receiver output will remain in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (GND to 2.4V). It is only supported with inputs shorted and no external common-mode voltage applied.

External lower value pull up and pull down resistors (for a stronger bias) may be used to boost fail-safe in the presence of higher noise levels. The pull up and pull down resistors should be in the 5kΩ to 15kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point should be set to approximately 1.2V (less than 1.75V) to be compatible with the internal circuitry.

The footprint of the DS90LV032A is the same as the industry standard 26LS32 Quad Differential (RS-422) Receiver.

PIN DESCRIPTIONS

| Pin No. | Name | Description |
|-----------------|------------------|--|
| 2, 6, 10, 14 | R _{IN+} | Non-inverting receiver input pin |
| 1, 7, 9, 15 | R _{IN-} | Inverting receiver input pin |
| 3, 5, 11, 13 | R _{OUT} | Receiver output pin |
| 4 | EN | Active high enable pin, OR-ed with EN* |
| 12 | EN* | Active low enable pin, OR-ed with EN |
| 16 | V _{CC} | Power supply pin, +3.3V ± 0.3V |
| 8 | GND | Ground pin |

Typical Characteristics

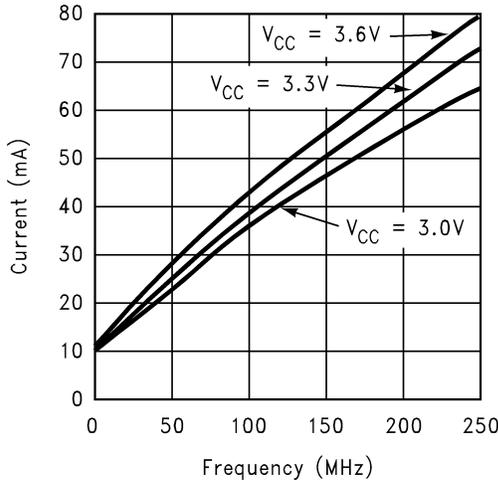


Figure 6. ICC vs Frequency, four channels switching

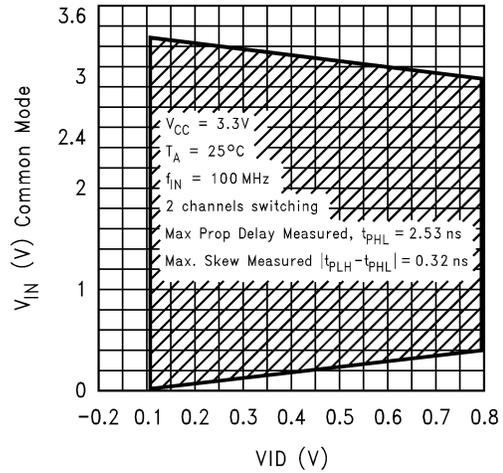


Figure 7. Typical Common-Mode Range variation with respect to amplitude of differential input

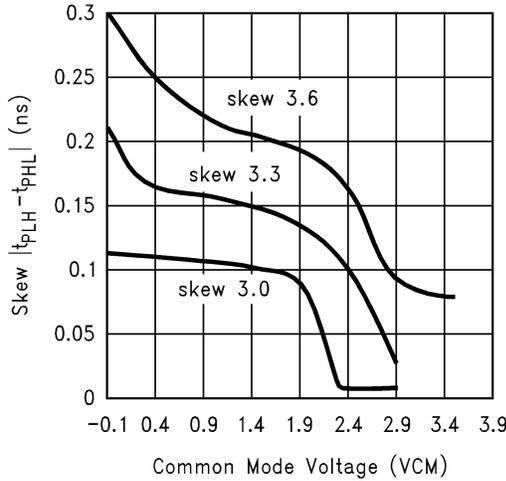


Figure 8. Typical Pulse Skew variation versus common-mode voltage

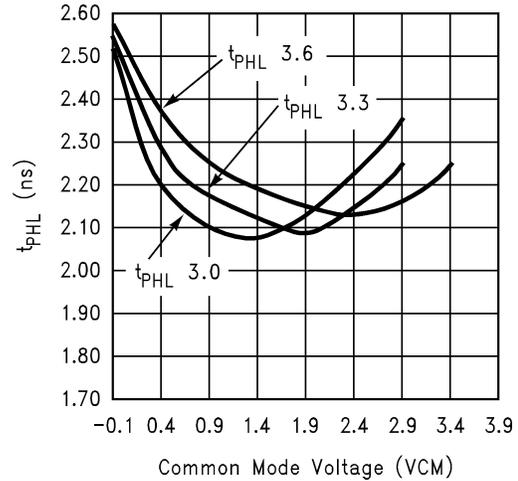


Figure 9. Variation in High to Low Propagation Delay versus VCM

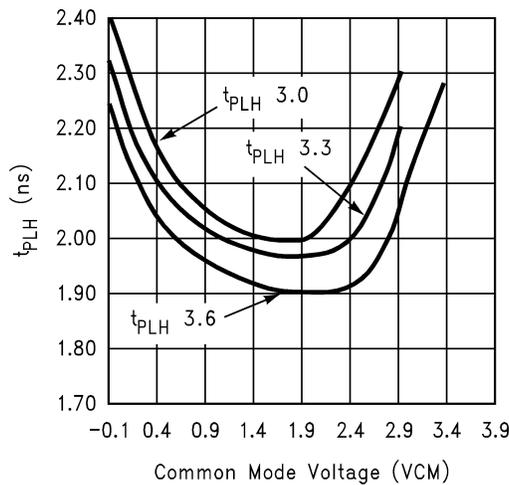


Figure 10. Variation in Low to High Propagation Delay versus VCM

REVISION HISTORY

| Changes from Revision B (April 2013) to Revision C | Page |
|--|--------------------|
| • Changed layout of National Data Sheet to TI format | 10 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|----------------------|---------------|--------------|-----------------|------|-------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|----------------|
| DS90LV032ATM | NRND | SOIC | D | 16 | 48 | TBD | Call TI | Call TI | -40 to 85 | DS90LV032A TM | |
| DS90LV032ATM/NOPB | ACTIVE | SOIC | D | 16 | 48 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | DS90LV032A TM | Samples |
| DS90LV032ATMTC | NRND | TSSOP | PW | 16 | 92 | TBD | Call TI | Call TI | -40 to 85 | DS90LV 032AT | |
| DS90LV032ATMTC/NOPB | ACTIVE | TSSOP | PW | 16 | 92 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | DS90LV 032AT | Samples |
| DS90LV032ATMTCX | NRND | TSSOP | PW | 16 | 2500 | TBD | Call TI | Call TI | -40 to 85 | DS90LV 032AT | |
| DS90LV032ATMTCX/NOPB | ACTIVE | TSSOP | PW | 16 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | DS90LV 032AT | Samples |
| DS90LV032ATMX | NRND | SOIC | D | 16 | 2500 | TBD | Call TI | Call TI | -40 to 85 | DS90LV032A TM | |
| DS90LV032ATMX/NOPB | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU SN Call TI | Level-1-260C-UNLIM | -40 to 85 | DS90LV032A TM | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

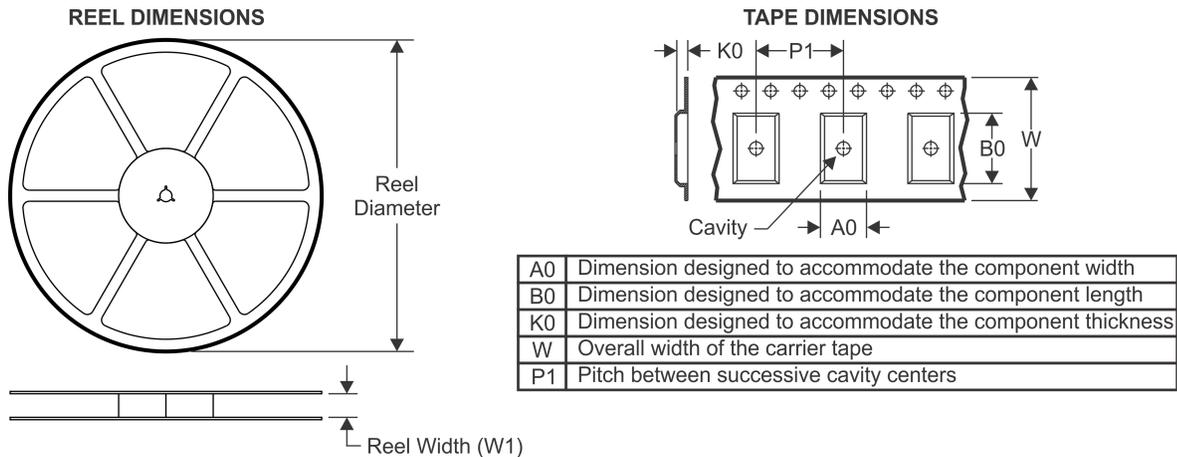
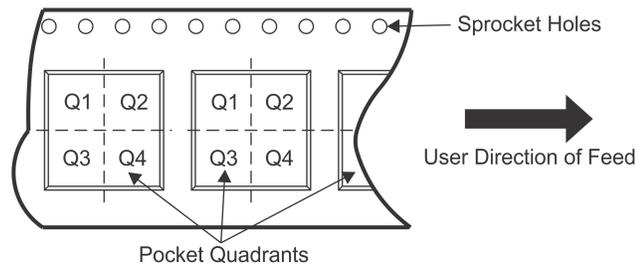
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

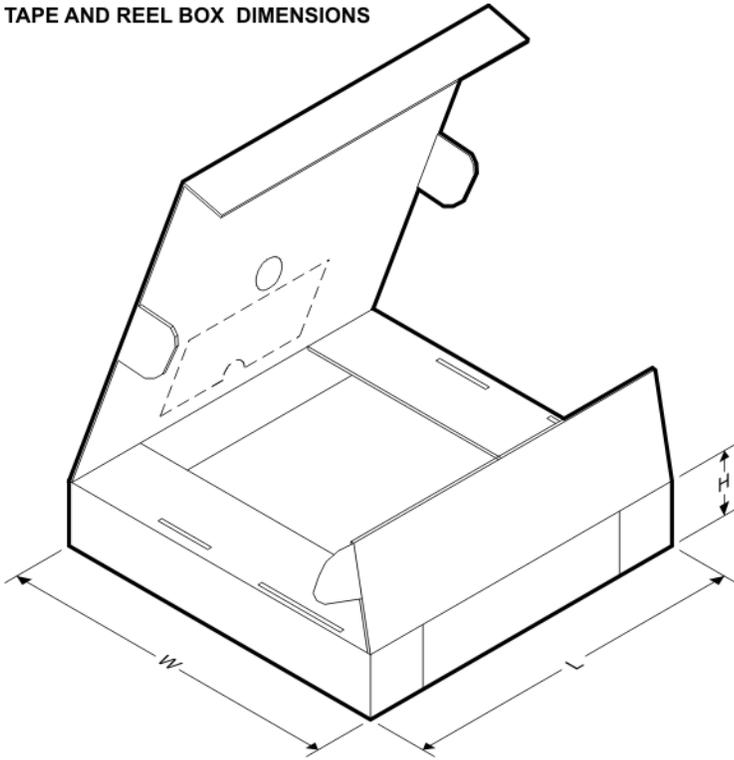
Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DS90LV032ATMTCX | TSSOP | PW | 16 | 2500 | 330.0 | 12.4 | 6.95 | 8.3 | 1.6 | 8.0 | 12.0 | Q1 |
| DS90LV032ATMTCX/NO PB | TSSOP | PW | 16 | 2500 | 330.0 | 12.4 | 6.95 | 8.3 | 1.6 | 8.0 | 12.0 | Q1 |
| DS90LV032ATMX | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.3 | 8.0 | 16.0 | Q1 |
| DS90LV032ATMX/NOPB | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.3 | 8.0 | 16.0 | Q1 |

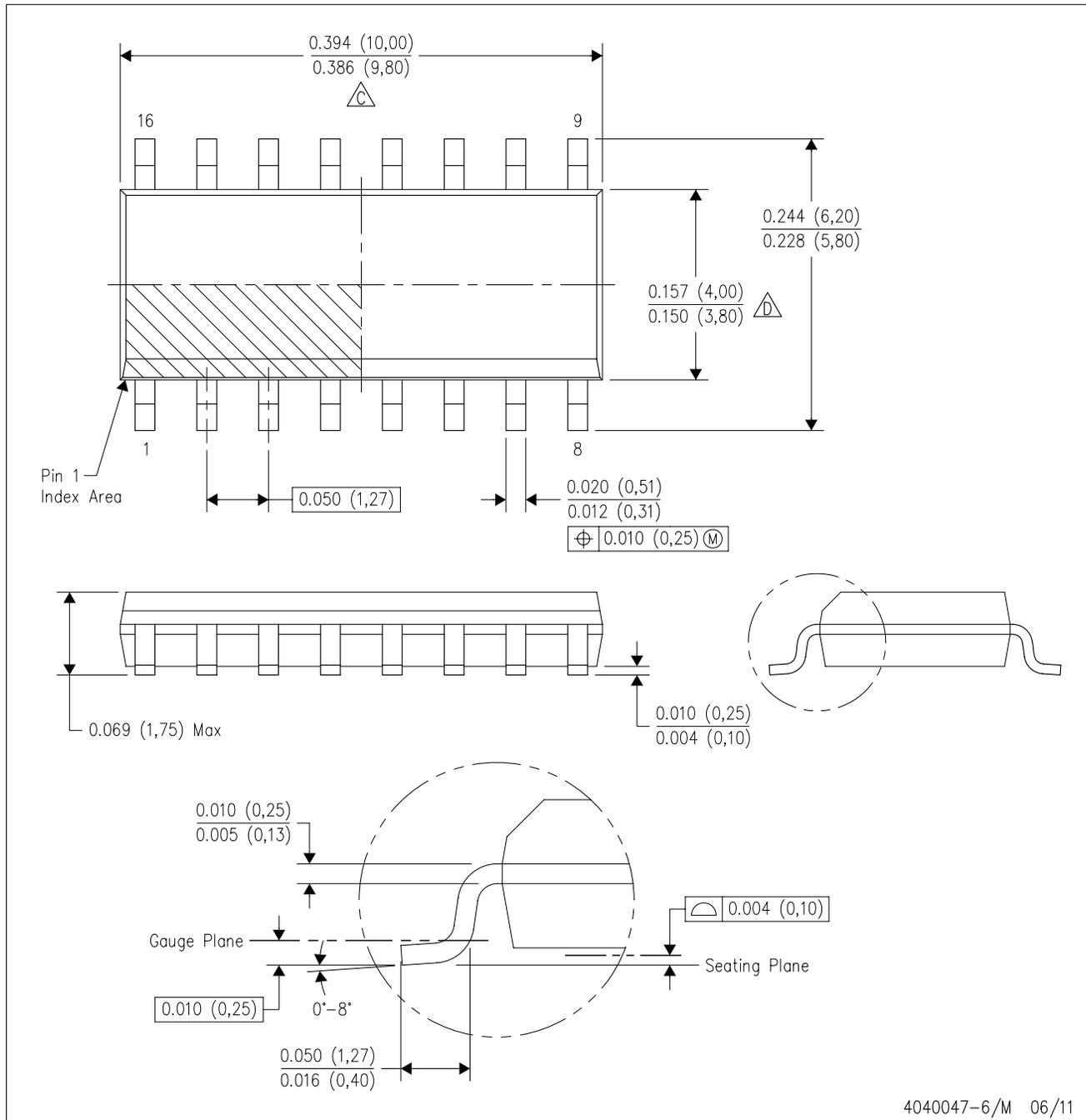
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DS90LV032ATMTCX | TSSOP | PW | 16 | 2500 | 367.0 | 367.0 | 35.0 |
| DS90LV032ATMTCX/NOPB | TSSOP | PW | 16 | 2500 | 367.0 | 367.0 | 35.0 |
| DS90LV032ATMX | SOIC | D | 16 | 2500 | 367.0 | 367.0 | 35.0 |
| DS90LV032ATMX/NOPB | SOIC | D | 16 | 2500 | 367.0 | 367.0 | 35.0 |

D (R-PDSO-G16)

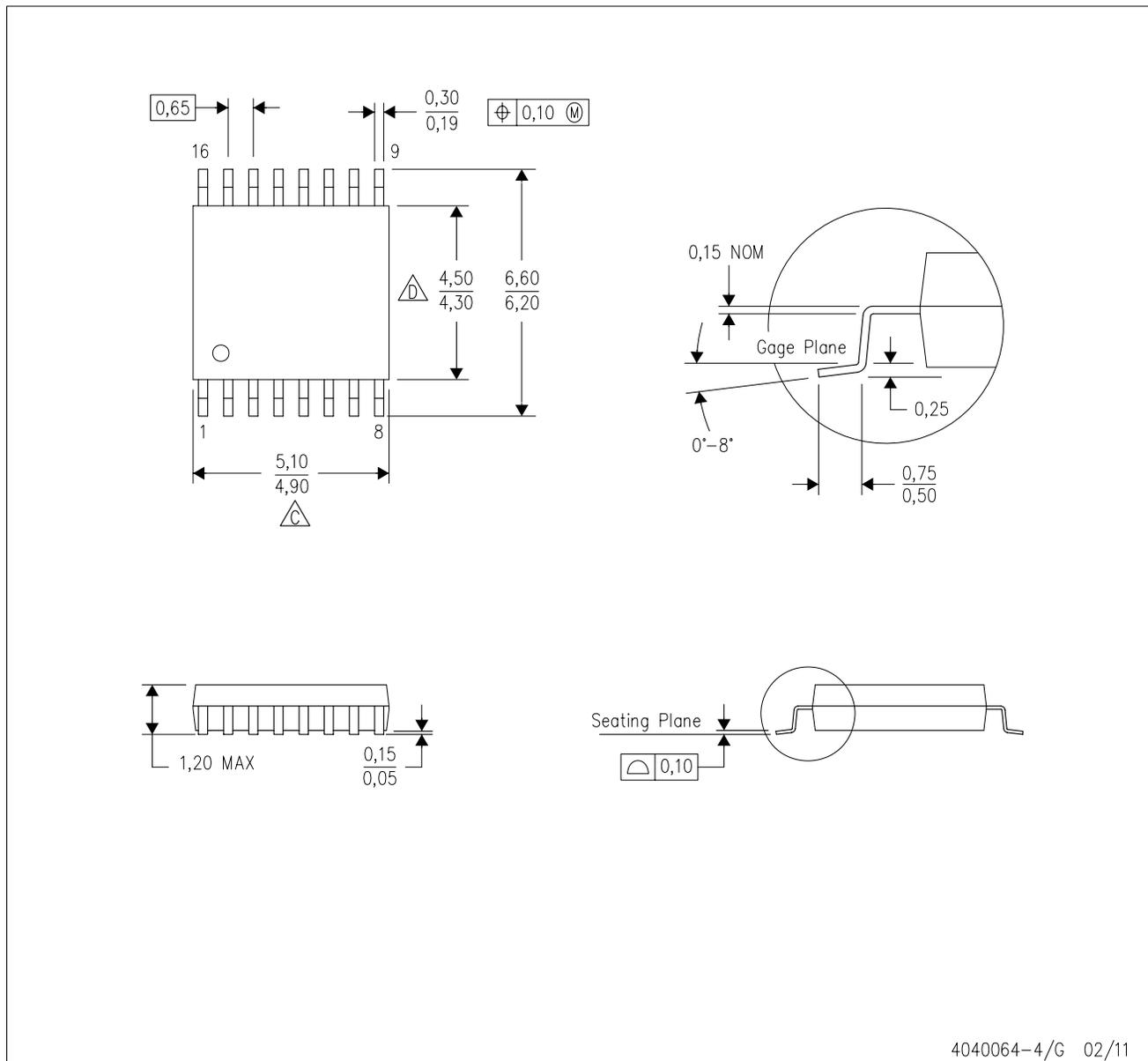
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

| | |
|------------------------------|--|
| Audio | www.ti.com/audio |
| Amplifiers | amplifier.ti.com |
| Data Converters | dataconverter.ti.com |
| DLP® Products | www.dlp.com |
| DSP | dsp.ti.com |
| Clocks and Timers | www.ti.com/clocks |
| Interface | interface.ti.com |
| Logic | logic.ti.com |
| Power Mgmt | power.ti.com |
| Microcontrollers | microcontroller.ti.com |
| RFID | www.ti-rfid.com |
| OMAP Applications Processors | www.ti.com/omap |
| Wireless Connectivity | www.ti.com/wirelessconnectivity |

Applications

| | |
|-------------------------------|--|
| Automotive and Transportation | www.ti.com/automotive |
| Communications and Telecom | www.ti.com/communications |
| Computers and Peripherals | www.ti.com/computers |
| Consumer Electronics | www.ti.com/consumer-apps |
| Energy and Lighting | www.ti.com/energy |
| Industrial | www.ti.com/industrial |
| Medical | www.ti.com/medical |
| Security | www.ti.com/security |
| Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Video and Imaging | www.ti.com/video |

TI E2E Community

e2e.ti.com