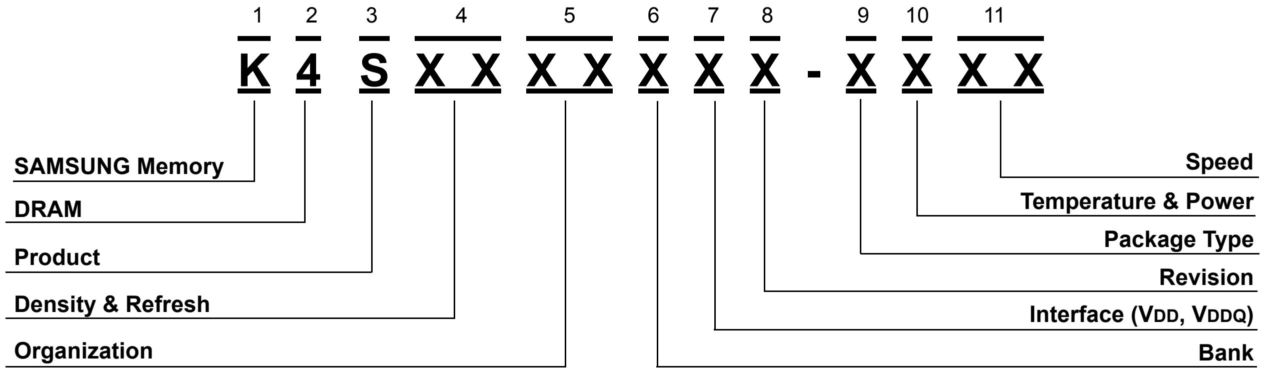
SDRAM Product Guide

November 2007

Memory Division

A. SDRAM Component Ordering Information



1. SAMSUNG Memory : K

2. DRAM : 4

3. Product

S : SDRAM

4. Density & Refresh

16 : 16Mb, 4K/64ms
64 : 64Mb, 4K/64ms
28 : 128Mb, 4K/64ms
56 : 256Mb, 8K/64ms
51 : 512Mb, 8K/64ms

5. Organization

04 : x 4
06 : x 4 Stack (Flex frame)
07 : x 8 Stack (Flex frame)
08 : x 8
16 : x16
32 : x32

6. Bank

2 : 2 Banks
3 : 4 Banks

7. Interface (V_{DD}, V_{DDQ})

2 : LVTTL (3.3V, 3.3V)

8. Revision

M : 1st Gen.
A : 2nd Gen.
B : 3rd Gen.
C : 4th Gen.
D : 5th Gen.
E : 6th Gen.
F : 7th Gen
H : 9th Gen
J : 11th Gen.
K : 12th Gen
N : 14th Gen

9. Package Type

T : TSOP II
N : sTSOP II
L : TSOP II(Lead-free & Halogen-free)[*1]
U : TSOP II (Lead-free)[*1]
V : sTSOP II (Lead-free)[*1]

Note 1: All of Lead-free or Halogen-free product are in compliance with RoHS

10. Temperature & Power

C : Commercial Temp.(0°C ~ 70°C) & Normal Power
L : Commercial Temp.(0°C ~ 70°C) & Low Power
I : Industrial Temp.(-40°C ~ 85°C) & Normal Power
P : Industrial Temp.(-40°C ~ 85°C) & Low Power

11. Speed (Default CL= 3)

75 : 7.5ns, PC133 (133MHz CL=3)
60 : 6.0ns (166MHz CL=3)
50 : 5.0ns (200MHz CL=3)

B. SDRAM Component Product Guide

Density	Bank	Part Number	Package[*1] & Power[*2] & Speed[*3]	Org.	Interface	Refresh	Power (V)	Package	Avail.
64Mb K-die	4Banks	K4S640832K	UC75 UL75	8M x 8	LVTTL	4K/64ms	3.3 ± 0.3V	Lead-free 54pin TSOP(II)	EOL DEC. '08
		K4S641632K	UC50/C60/C75 UL50/L60/L75	4M x 16					
64Mb N-die	4Banks	K4S640832N	LC75 LL75	8M x 8	LVTTL	4K/64ms	3.3 ± 0.3V	Lead-free & Halogen-free 54pin TSOP(II)	4Q'07 CS
		K4S641632N	LC50/C60/C75 LL50/L60/L75	4M x 16					
128Mb I-die	4Banks	K4S280432I	UC75 UL75	32M x 4	LVTTL	4K/64ms	3.3 ± 0.3V	Lead-free 54pin TSOP(II)	EOL AUG. '08
		K4S280832I	UC75 UL75	16M x 8					
		K4S281632I	UC60/C75 UL60/L75	8M x 16					
128Mb K-die	4Banks	K4S280432K	U[*4]C75 UL75	32M x 4	LVTTL	4K/64ms	3.3 ± 0.3V	Lead-free & Halogen-free 54pin TSOP(II)[*4]	Now
		K4S280832K	UC75 UL75	16M x 8					
		K4S281632K	UC60/C75 UL60/L75	8M x 16					
256Mb H-die	4Banks	K4S560432H	UC75 UL75	64M x 4	LVTTL	8K/64ms	3.3 ± 0.3V	Lead-free 54pin TSOP(II)	EOL SEP. '08
		K4S560832H	UC75 UL75	32M x 8					
		K4S561632H	UC60/C75 UL60/L75	16M x 16					
256Mb J-die	4Banks	K4S560432J	U[*4]C75 UL75	64M x 4	LVTTL	8K/64ms	3.3 ± 0.3V	Lead-free & Halogen-free 54pin TSOP(II)[*4]	Now
		K4S560832J	UC75 UL75	32M x 8					
		K4S561632J	UC60/C75 UL60/L75	16M x 16					
512Mb D-die	4Banks	K4S510432D	UC75 UL75	128M x 4	LVTTL	8K/64ms	3.3 ± 0.3V	Lead-free 54pin TSOP(II)	Now
		K4S510832D	UC75 UL75	64M x 8					
		K4S511632D	UC75 UL75	32M x 16					

Note 1 :
U : TSOP(II) (Lead-free)
L : TSOP(II) (Lead-free & Halogen-free)

Note 2 :

Temperature and Power	Description
C	Temperature, Normal Power
L	Temperature, Low Power

- Commercial Temp (0°C < Ta < 70°C)

Note 3 :

Speed	Description
75	7.5ns, PC133 (133Mhz @ CL=3)
60	6.0 ns (166Mhz @ CL=3)
50	5.0 ns (200Mhz @ CL=3)

* All products have backward compatibility with PC100.

Note 4 : 128Mb K-die SDR and 256Mb J-die SDR DRAMs support Lead-free & Halogen-free package with Lead-free package code(-U)

C. Industrial Temperature SDRAM Component Product Guide

Density	Bank	Part Number	Package[*1] & Power[*2] & Speed[*3]	Org.	Interface	Refresh	Power (V)	Package	Avail.
64Mb K-die	4Banks	KS641632K	UI60/I75 UP60/P75	4M x 16	LVTTL	4K/64ms	3.3 ± 0.3V	Lead-free 54pin TSOP(II)	EOL DEC.'08
64Mb N-die	4Banks	KS641632N	LI60/I75 LP60/P75	4M x 16	LVTTL	4K/64ms	3.3 ± 0.3V	Lead-free & Halogen-free 54pin TSOP(II)	1Q'08
128Mb I-die	4Banks	K4S281632I	UI60/I75 UP60/P75	8M x 16	LVTTL	4K/64ms	3.3 ± 0.3V	Lead-free 54pin TSOP(II)	EOL AUG.'08
128Mb K-die	4Banks	K4S281632K	U[*4]I60/I75 UP60/P75	8M x 16	LVTTL	4K/64ms	3.3 ± 0.3V	Lead-free & Halogen-free 54pin TSOP(II)[*4]	Now
256Mb H-die	4Banks	K4S561632H	UI60/I75 UP60/P75	16M x 16	LVTTL	8K/64ms	3.3 ± 0.3V	Lead-free 54pin TSOP(II)	EOL SEP.'08
256Mb J-die	4Banks	K4S561632J	U[*4]I60/I75 UP60/P75	16M x 16	LVTTL	8K/64ms	3.3 ± 0.3V	Lead-free & Halogen-free 54pin TSOP(II)[*4]	Now

Note 1 :
U : TSOP(II) (Lead-free)
L : TSOP(II) (Lead-free & Halogen-free)

Note 2 :

Temperature and Power	Description
I	Industrial Temperature, Normal Power
P	Industrial Temperature, Low Power

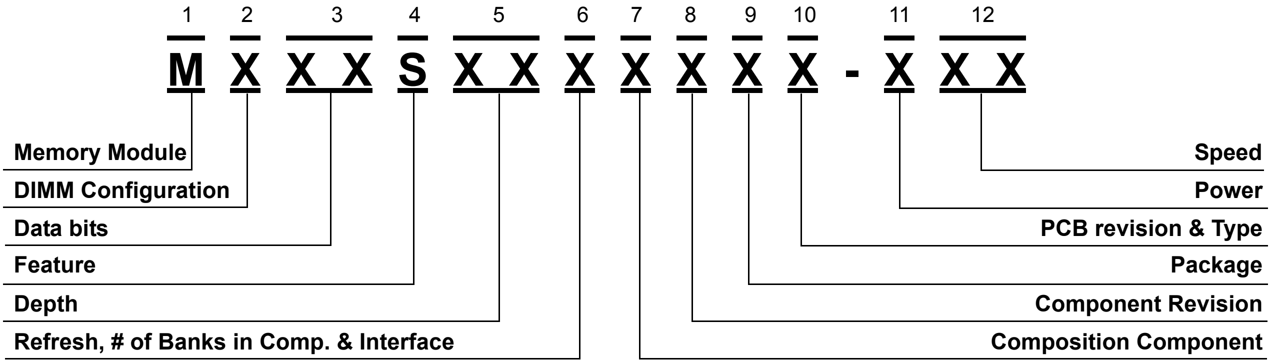
- Industrial Temp (-40°C < Ta < 85°C)

Note 3 :

Speed	Description
75	7.5ns, PC133 (133Mhz @ CL=3)
60	6.0 ns (166Mhz @ CL=3)
50	5.0 ns (200Mhz @ CL=3)

Note 4 : 128Mb K-die SDR and 256Mb J-die SDR DRAMs support Lead-free & Halogen-free package with Lead-free package code(-U)

D. SDRAM Module Ordering Information



1. Memory Module : M

2. DIMM Configuration

3 : DIMM
4 : SODIMM

3. Data Bits

63 : x63 PC100 / PC133 µSODIMM with SPD for 144pin
64 : x64 PC100 / PC133 SODIMM with SPD for 144pin (Intel/JEDEC)
66 : x64 Unbuffered DIMM with SPD for 144pin/168pin (Intel/JEDEC)
74 : x72 /ECC Unbuffered DIMM with SPD for 168pin (Intel/JEDEC)
77 : x72 /ECC PLL + Register DIMM with SPD for 168pin (Intel PC100)
90 : x72 /ECC PLL + Register DIMM with SPD for 168pin (JEDEC PC133)

4. Feature

S : SDRAM

5. Depth

16 : 16M
32 : 32M
64 : 64M
28 : 128M
56 : 256M

09 : 8M (for 128Mb/512Mb)
17 : 16M (for 128Mb/512Mb)
33 : 32M (for 128Mb/512Mb)
65 : 64M (for 128Mb/512Mb)
29 : 128M (for 128Mb/512Mb)
59 : 256M (for 128Mb/512Mb)

6. Refresh, # of Banks in comp. & Interface

2 : 4K/ 64ms Ref., 4Banks & LVTTL
5 : 8K/ 64ms Ref., 4Banks & LVTTL

7. Composition Component

0 : x 4
3 : x 8
4 : x16
8 : x 4 Stack (Flexframe)
9 : x 8 Stack (Flexframe)

8. Component Revision

M : 1st Gen.
A : 2nd Gen.
B : 3rd Gen.
C : 4th Gen.
D : 5th Gen.
E : 6th Gen.
F : 7th Gen.
H : 9h Gen.
J : 11h Gen.

9. Package

T : TSOP(II) (400mil)
N : sTSOP(II) (400mil)
U : TSOP(II) Lead-free (400mil)
V : sTSOP(II) Lead-free (400mil)

10. PCB Revision & Type

0 : Mother PCB
1 : 1st Rev.
2 : 2nd Rev.
3 : 3rd Rev.
U : Low Profile DIMM
S : 4Layer PCB.

11. Power

C : Commercial Normal (0°C ~ 70°C)
L : Commercial Low (0°C ~ 70°C)

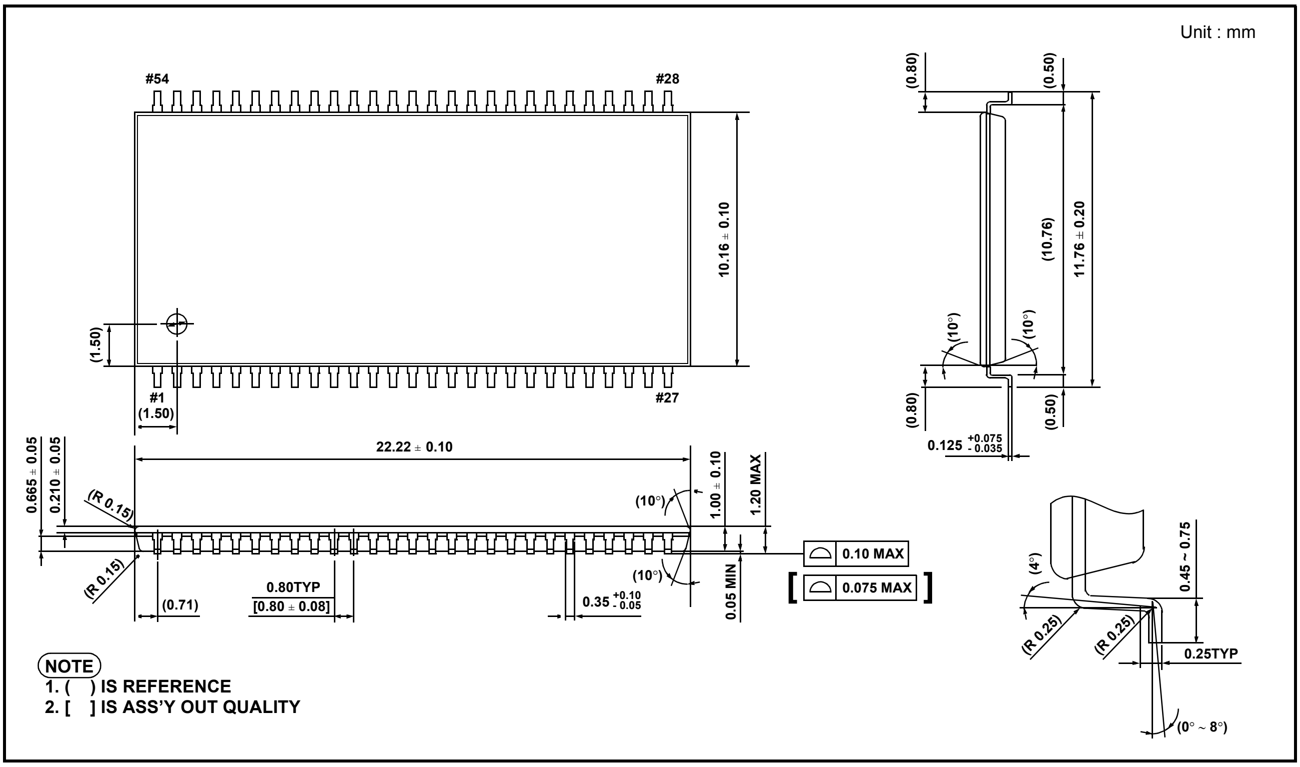
12. Speed (Default CL= 3)

7A : PC133 (133MHz CL=3/PC100 CL2)

E. SDRAM Module Product Guide

Org.	Density	Part No.	Speed	Composition	Comp. Version	Power (V)	Internal Banks	External Banks	Feature	Avail.
168pin PC133 Registered DIMM										
32Mx72	256MB	M390S3253HU1	C7A	32M x 8 * 9 pcs	256Mb H-die	3.3 V	4	1	DS, 1500mil	EOL JUN.'08
64Mx72	512MB	M390S6450HU1	C7A	64M x 4 * 18 pcs	256Mb H-die			1	DS, 1700mil	
		M390S6450HUU	C7A	64M x 4 * 18 pcs	256Mb H-die			1	DS, 1200mil	
168pin PC133 Unbuffered DIMM										
8Mx64	64MB	M366S0924IUS	C7A	8M x 16 * 4 pcs	128Mb I-die	3.3V	4	1	SS, 1000mil	EOL JUN.'08
16Mx64	128MB	M366S1723IUS	C7A	16M x 8 * 8 pcs	128Mb I-die			1	SS, 1375mil	
		M366S1654HUS	C7A	16M x 16 * 4 pcs	256Mb H-die			1	SS, 1000mil	EOL JUN.'08
		M366S1654JUS	C7A	16M x 16 * 4 pcs	256Mb J-die			1	SS, 1000mil	Now
16Mx72		M374S1723IUS	C7A	16M x 8 * 9 pcs	128Mb I-die			1	SS, 1375mil	EOL JUN.'08
32Mx64	256MB	M366S3323IUS	C7A	16M x 8 * 16 pcs	128Mb I-die			2	DS, 1375mil	
32Mx72		M374S3323IUS	C7A	16M x 8 * 18 pcs	128Mb I-die			2	DS, 1375mil	
32Mx64		M366S3253JUS	C7A	32M x 8 * 8 pcs	256Mb J-die			1	SS, 1375mil	Now
64Mx64	512MB	M366S6453HUS	C7A	32M x 8 * 16 pcs	256Mb H-die			2	DS, 1375mil	EOL JUN.'08
		M366S6453JUS	C7A	32M x 8 * 16 pcs	256Mb J-die			2	DS, 1375mil	Now
144pin PC133 SODIMM										
16Mx64	128MB	M464S1724IUS	L7A	8M x 16 * 8 pcs	128Mb I-die	3.3V	4	1	DS, 1250mil	EOL JUN.'08
		M464S1724KUS	L7A	8M x 16 * 8 pcs	128Mb K-die			1	DS, 1250mil	Now
32Mx64	256MB	M464S3254HUS	L7A	16M x 16 * 8 pcs	256Mb H-die			1	DS, 1250mil	EOL JUN.'08
		M464S3254JUS	L7A	16M x 16 * 8 pcs	256Mb J-die			1	DS, 1250mil	Now
64Mx64	512MB	M464S6453HV0	L7A	32M x 8 * 16 pcs	256Mb H-die			2	DS, 1250mil	EOL JUN.'08
		M464S6453JV0	L7A	32M x 8 * 16 pcs	256Mb J-die			2	DS, 1250mil	Now

F. Package Dimension



54Pin TSOP(II) Package Dimension

For further information,

semiconductor@samsung.com