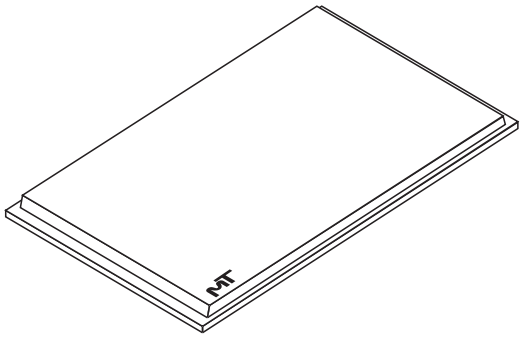
CIO RLDRAM® II

MT49H32M9 – 32 Meg x 9 x 8 Banks
MT49H16M18 – 16 Meg x 18 x 8 Banks
MT49H8M36 – 8 Meg x 36 x 8 Banks

Features

- 400 MHz DDR operation (800 Mb/s/pin data rate)
- 28.8 Gb/s peak bandwidth (x36 at 400 MHz clock frequency)
- Organization
  - 32 Meg x 9, 16 Meg x 18, and 8 Meg x 36
- 8 internal banks for concurrent operation and maximum bandwidth
- Reduced cycle time (20ns at 400 MHz)
- Nonmultiplexed addresses (address multiplexing option available)
- SRAM-type interface
- Programmable READ latency (RL), row cycle time, and burst sequence length
- Balanced READ and WRITE latencies in order to optimize data bus utilization
- Data mask for WRITE commands
- Differential input clocks (CK, CK#)
- Differential input data clocks (DK*x*, DK*x*#)
- On-die DLL generates CK edge-aligned data and output data clock signals
- Data valid signal (QVLD)
- 32ms refresh (8K refresh for each bank; 64K refresh command must be issued in total each 32ms)
- 144-ball µBGA package
- HSTL I/O (1.5V or 1.8V nominal)
- 25–60Ω matched impedance outputs
- 2.5V VEXT, 1.8V VDD, 1.5V or 1.8V VDDQ I/O
- On-die termination (ODT) RTT

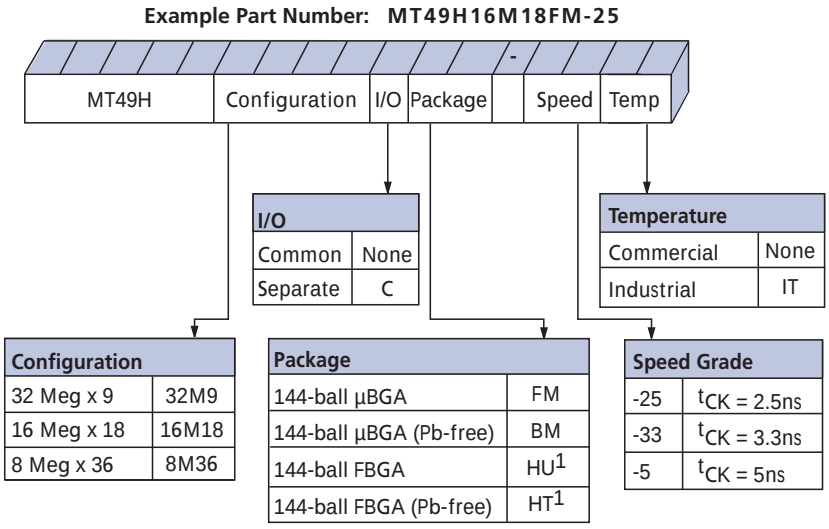
Figure 1: 144-Ball µBGA



Options	Marking
• Clock cycle timing	
– 2.5ns (400 MHz)	-25
– 3.3ns (300 MHz)	-33
– 5ns (200 MHz)	-5
• Configuration	
– 32 Meg x 9	32M9
– 16 Meg x 18	16M18
– 8 Meg x 36	8M36
• Operating temperature	
– Commercial (0° to +95°C)	None
– Industrial (T_C = –40°C to +95°C; T_A = –40°C to +85°C)	IT[1]
• Package	
– 144-ball µBGA	FM[1]
– 144-ball µBGA (Pb-free)	BM[2]
– 144-ball FBGA	HU[3]
– 144-ball FBGA (Pb-free)	HT[2, 3]

Notes: 1. Contact Micron for availability of industrial temperature products.
2. Contact Micron for availability of Pb-free products.
3. The FBGA package is being phased out.

Figure 2: 288Mb RLDRAM II CIO Part Numbers



Notes: 1. The FBGA package is being phased out.

BGA Part Marking Decoder

Due to space limitations, BGA-packaged components have an abbreviated part marking that is different from the part number. Micron's BGA Part Marking Decoder is available on Micron's Web site at micron.com.

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General Description

The Micron® reduced latency DRAM (RLDRAM®) II is a high-speed memory device designed for high bandwidth data storage—telecommunications, networking, and cache applications, etc. The chip's 8-bank architecture is optimized for sustainable high speed operation.

The DDR I/O interface transfers two data words per clock cycle at the I/O balls. Output data is referenced to the free-running output data clock.

Commands, addresses, and control signals are registered at every positive edge of the differential input clock, while input data is registered at both positive and negative edges of the input data clock(s).

Read and write accesses to the RLDRAM are burst-oriented. The burst length (BL) is programmable from 2, 4, or 8 by setting the mode register.

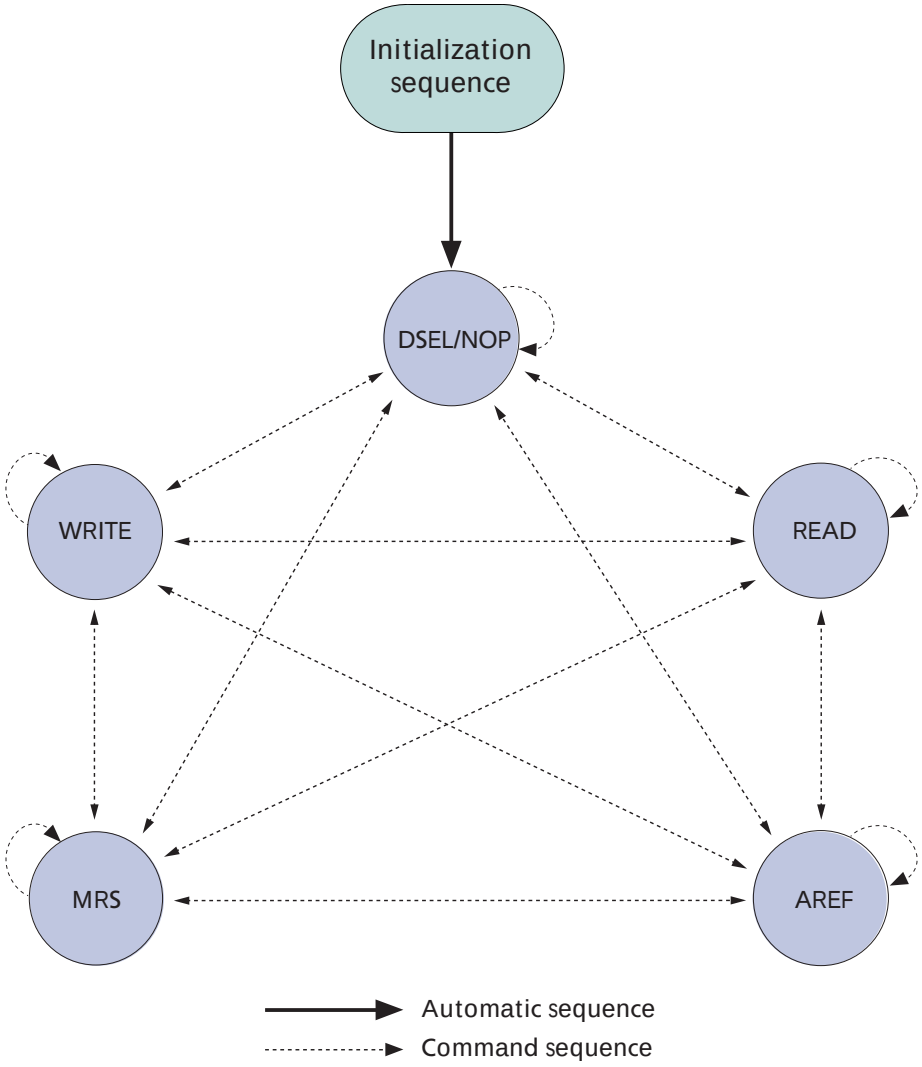
The device is supplied with 2.5V and 1.8V for the core and 1.5V or 1.8V for the output drivers.

Bank-scheduled refresh is supported with the row address generated internally.

The µBGA 144-ball package is used to enable ultra high-speed data transfer rates and a simple upgrade path from early generation devices.

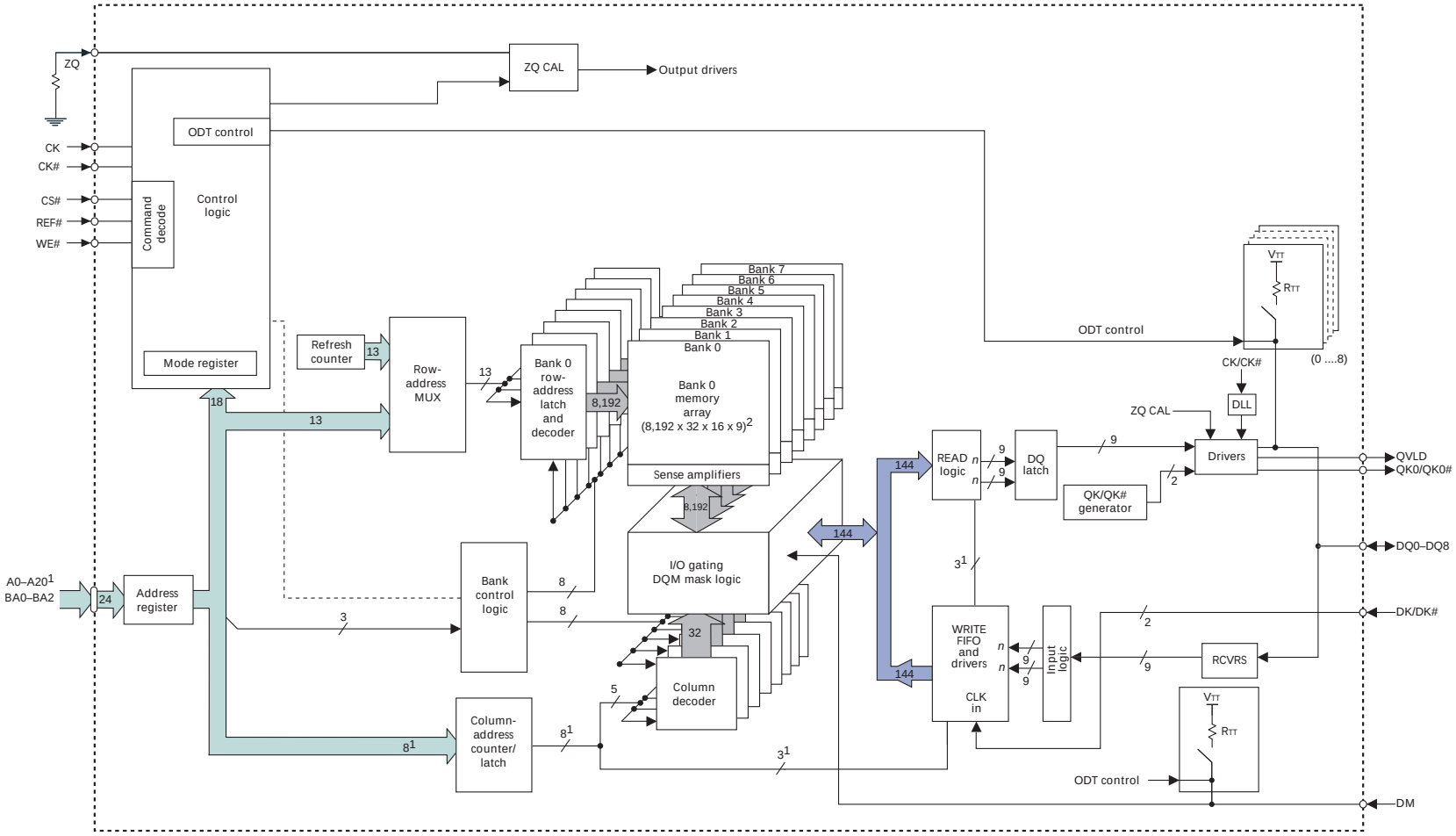
State Diagram

Figure 3: Simplified State Diagram



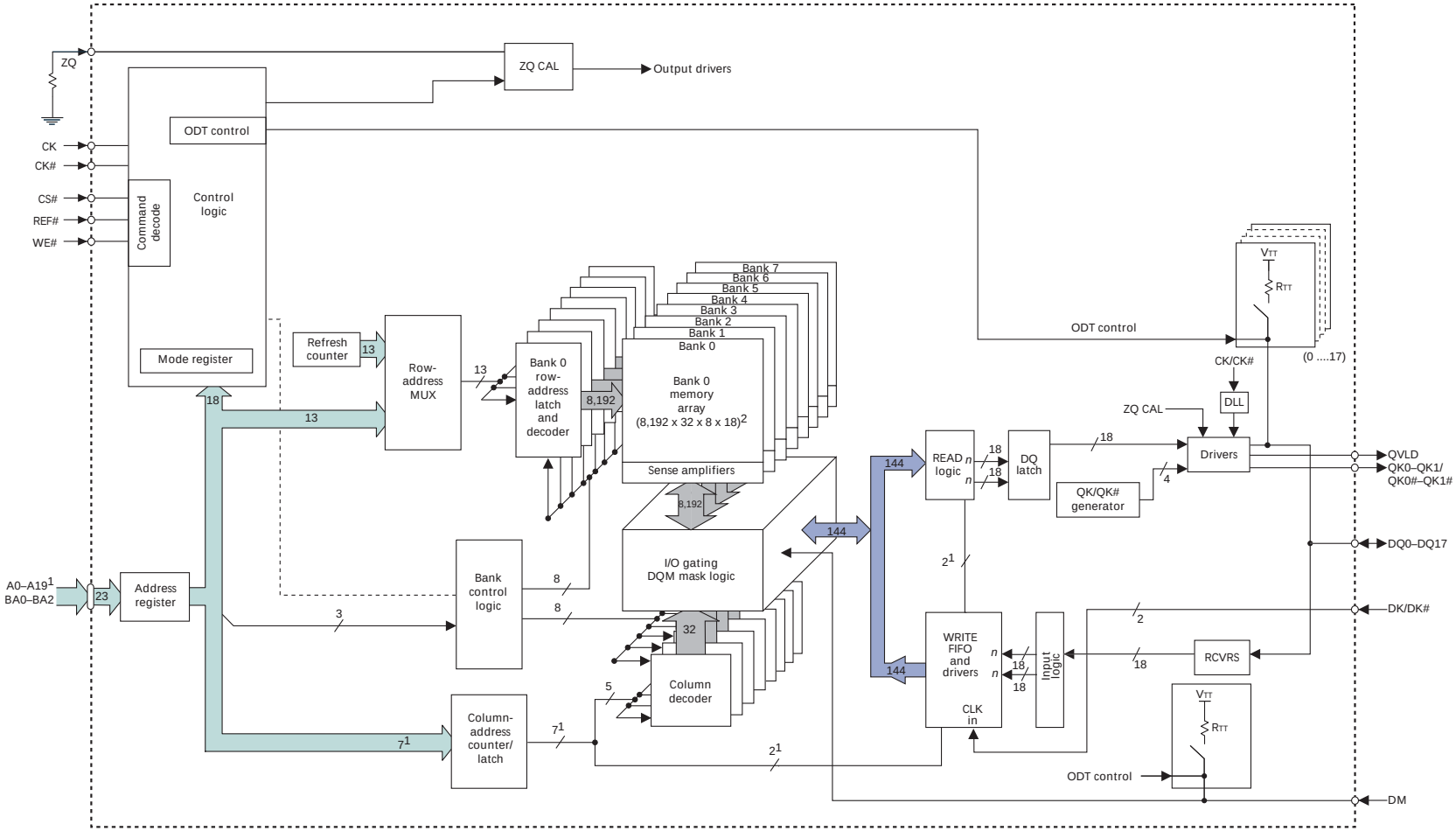
Functional Block Diagrams

Figure 4: 32 Meg x 9 Functional Block Diagram



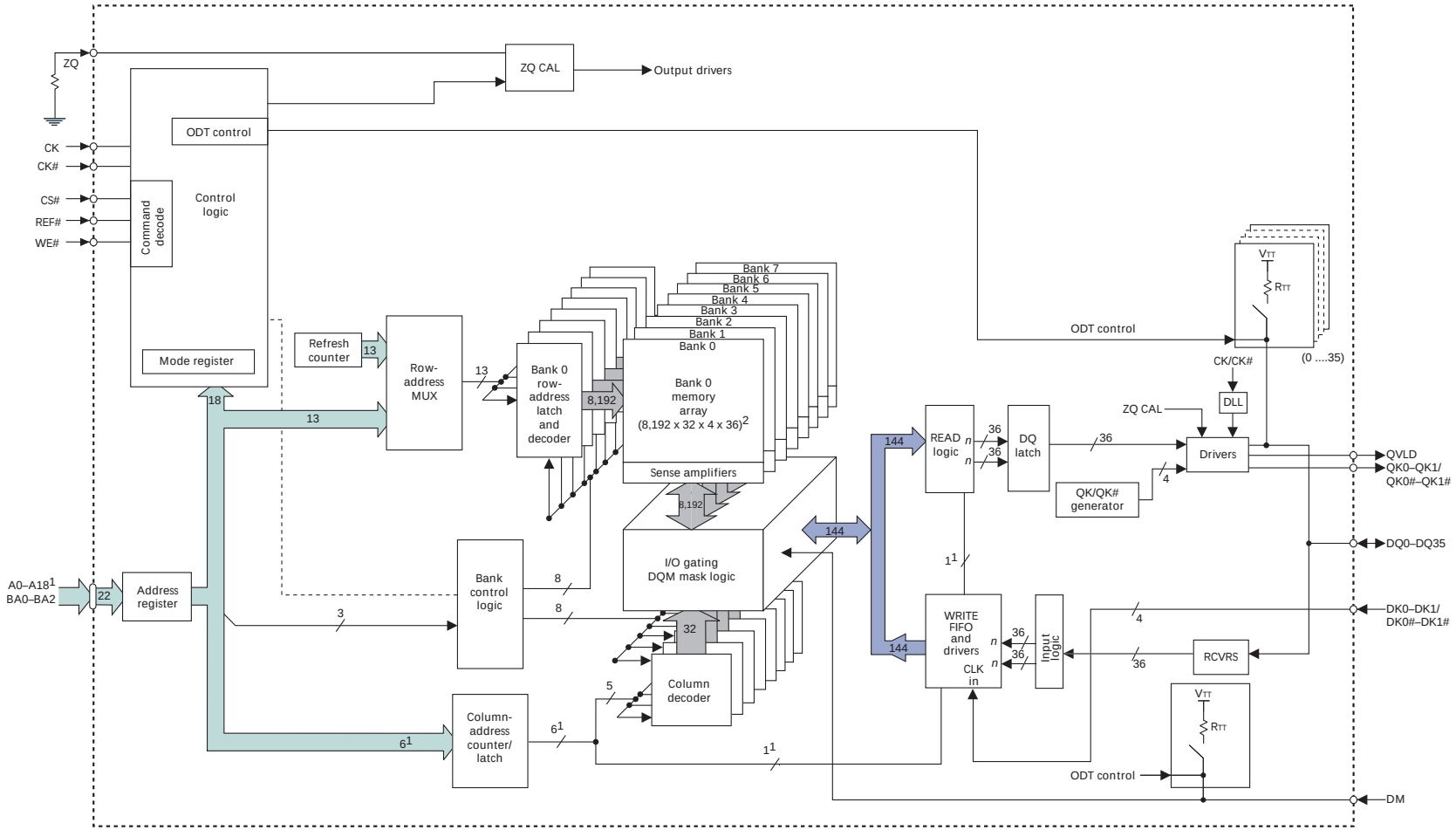
Notes: 1. Examples for BL = 2; column address will be reduced with an increase in burst length.
2. The “16” = (length of burst) x 2^(number of column addresses to WRITE FIFO and READ logic).

Figure 5: 16 Meg x 18 Functional Block Diagram



Notes:
1. Examples for BL = 2; column address will be reduced with an increase in burst length.
2. The “8” = (length of burst) x 2^(number of column addresses to WRITE FIFO and READ logic).

Figure 6: 8 Meg x 36 Functional Block Diagram



Notes:
1. Examples for BL = 2; column address will be reduced with an increase in burst length.
2. The “4” = (length of burst) x 2^(number of column addresses to WRITE FIFO and READ logic).

Ball Assignments and Descriptions

Table 1: 32 Meg x 9 Ball Assignments (Top View) 144-Ball µBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	VREF	VSS	VEXT	VSS					VSS	VEXT	TMS	TCK
B	VDD	DNU[4]	DNU[4]	VSSQ					VSSQ	DQ0	DNU[4]	VDD
C	VTT	DNU[4]	DNU[4]	VDDQ					VDDQ	DQ1	DNU[4]	VTT
D	A22[1]	DNU[4]	DNU[4]	VSSQ					VSSQ	QK0#	QK0	VSS
E	A21[2]	DNU[4]	DNU[4]	VDDQ					VDDQ	DQ2	DNU[4]	A20
F	A5	DNU[4]	DNU[4]	VSSQ					VSSQ	DQ3	DNU[4]	QVLD
G	A8	A6	A7	VDD					VDD	A2	A1	A0
H	B2	A9	VSS	VSS					VSS	VSS	A4	A3
J	NF[3]	NF[3]	VDD	VDD					VDD	VDD	B0	CK
K	DK	DK#	VDD	VDD					VDD	VDD	B1	CK#
L	REF#	CS#	VSS	VSS					VSS	VSS	A14	A13
M	WE#	A16	A17	VDD					VDD	A12	A11	A10
N	A18	DNU[4]	DNU[4]	VSSQ					VSSQ	DQ4	DNU[4]	A19
P	A15	DNU[4]	DNU[4]	VDDQ					VDDQ	DQ5	DNU[4]	DM
R	VSS	DNU[4]	DNU[4]	VSSQ					VSSQ	DQ6	DNU[4]	VSS
T	VTT	DNU[4]	DNU[4]	VDDQ					VDDQ	DQ7	DNU[4]	VTT
U	VDD	DNU[4]	DNU[4]	VSSQ					VSSQ	DQ8	DNU[4]	VDD
V	VREF	ZQ	VEXT	VSS					VSS	VEXT	TDO	TDI

Notes:
1. Reserved for future use. This signal is not connected.
2. Reserved for future use. This signal is internally connected and has parasitic characteristics of an address input signal.
3. No function. This signal is internally connected and has parasitic characteristics of a clock input signal. This may optionally be connected to GND.
4. Do not use. This signal is internally connected and has parasitic characteristics of a I/O. This may optionally be connected to GND. Note that if ODT is enabled, these pins will be connected to VTT.

Table 2: 16 Meg x 18 Ball Assignments (Top View) 144-Ball µBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	VREF	VSS	VEXT	VSS					VSS	VEXT	TMS	TCK
B	VDD	DNU[4]	DQ4	VSSQ					VSSQ	DQ0	DNU[4]	VDD
C	VTT	DNU[4]	DQ5	VDDQ					VDDQ	DQ1	DNU[4]	VTT
D	A22[1]	DNU[4]	DQ6	VSSQ					VSSQ	QK0#	QK0	VSS
E	A21[2]	DNU[4]	DQ7	VDDQ					VDDQ	DQ2	DNU[4]	A20[2]
F	A5	DNU[4]	DQ8	VSSQ					VSSQ	DQ3	DNU[4]	QVLD
G	A8	A6	A7	VDD					VDD	A2	A1	A0
H	B2	A9	VSS	VSS					VSS	VSS	A4	A3
J	NF[3]	NF[3]	VDD	VDD					VDD	VDD	B0	CK
K	DK	DK#	VDD	VDD					VDD	VDD	B1	CK#
L	REF#	CS#	VSS	VSS					VSS	VSS	A14	A13
M	WE#	A16	A17	VDD					VDD	A12	A11	A10
N	A18	DNU[4]	DQ14	VSSQ					VSSQ	DQ9	DNU[4]	A19
P	A15	DNU[4]	DQ15	VDDQ					VDDQ	DQ10	DNU[4]	DM
R	VSS	QK1	QK1#	VSSQ					VSSQ	DQ11	DNU[4]	VSS
T	VTT	DNU[4]	DQ16	VDDQ					VDDQ	DQ12	DNU[4]	VTT
U	VDD	DNU[4]	DQ17	VSSQ					VSSQ	DQ13	DNU[4]	VDD
V	VREF	ZQ	VEXT	VSS					VSS	VEXT	TDO	TDI

Notes:
1. Reserved for future use. This may optionally be connected to GND.
2. Reserved for future use. This signal is internally connected and has parasitic characteristics of an address input signal. This may optionally be connected to GND.
3. No function. This signal is internally connected and has parasitic characteristics of a clock input signal. This may optionally be connected to GND.
4. Do not use. This signal is internally connected and has parasitic characteristics of a I/O. This may optionally be connected to GND. Note that if ODT is enabled, these pins will be connected to VTT.

Table 3: 8 Meg x 36 Ball Assignments (Top View) 144-Ball µBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	VREF	VSS	VEXT	VSS					VSS	VEXT	TMS	TCK
B	VDD	DQ8	DQ9	VSSQ					VSSQ	DQ1	DQ0	VDD
C	VTT	DQ10	DQ11	VDDQ					VDDQ	DQ3	DQ2	VTT
D	A22	DQ12	DQ13	VSSQ					VSSQ	QK0#	QK0	VSS
E	A21[2]	DQ14	DQ15	VDDQ					VDDQ	DQ5	DQ4	A20[2]
F	A5	DQ16	DQ17	VSSQ					VSSQ	DQ7	DQ6	QVLD
G	A8	A6	A7	VDD					VDD	A2	A1	A0
H	B2	A9	VSS	VSS					VSS	VSS	A4	A3
J	DK0	DK0#	VDD	VDD					VDD	VDD	B0	CK
K	DK1	DK1#	VDD	VDD					VDD	VDD	B1	CK#
L	REF#	CS#	VSS	VSS					VSS	VSS	A14	A13
M	WE#	A16	A17	VDD					VDD	A12	A11	A10
N	A18	DQ24	DQ25	VSSQ					VSSQ	DQ35	DQ34	A19[2]
P	A15	DQ22	DQ23	VDDQ					VDDQ	DQ33	DQ32	DM
R	VSS	QK1	QK1#	VSSQ					VSSQ	DQ31	DQ30	VSS
T	VTT	DQ20	DQ21	VDDQ					VDDQ	DQ29	DQ28	VTT
U	VDD	DQ18	DQ19	VSSQ					VSSQ	DQ27	DQ26	VDD
V	VREF	ZQ	VEXT	VSS					VSS	VEXT	TDO	TDI

Notes:
1. Reserved for future use. This may optionally be connected to GND.
2. Reserved for future use. This signal is internally connected and has parasitic characteristics of an address input signal. This may optionally be connected to GND.

Table 4: Ball Descriptions

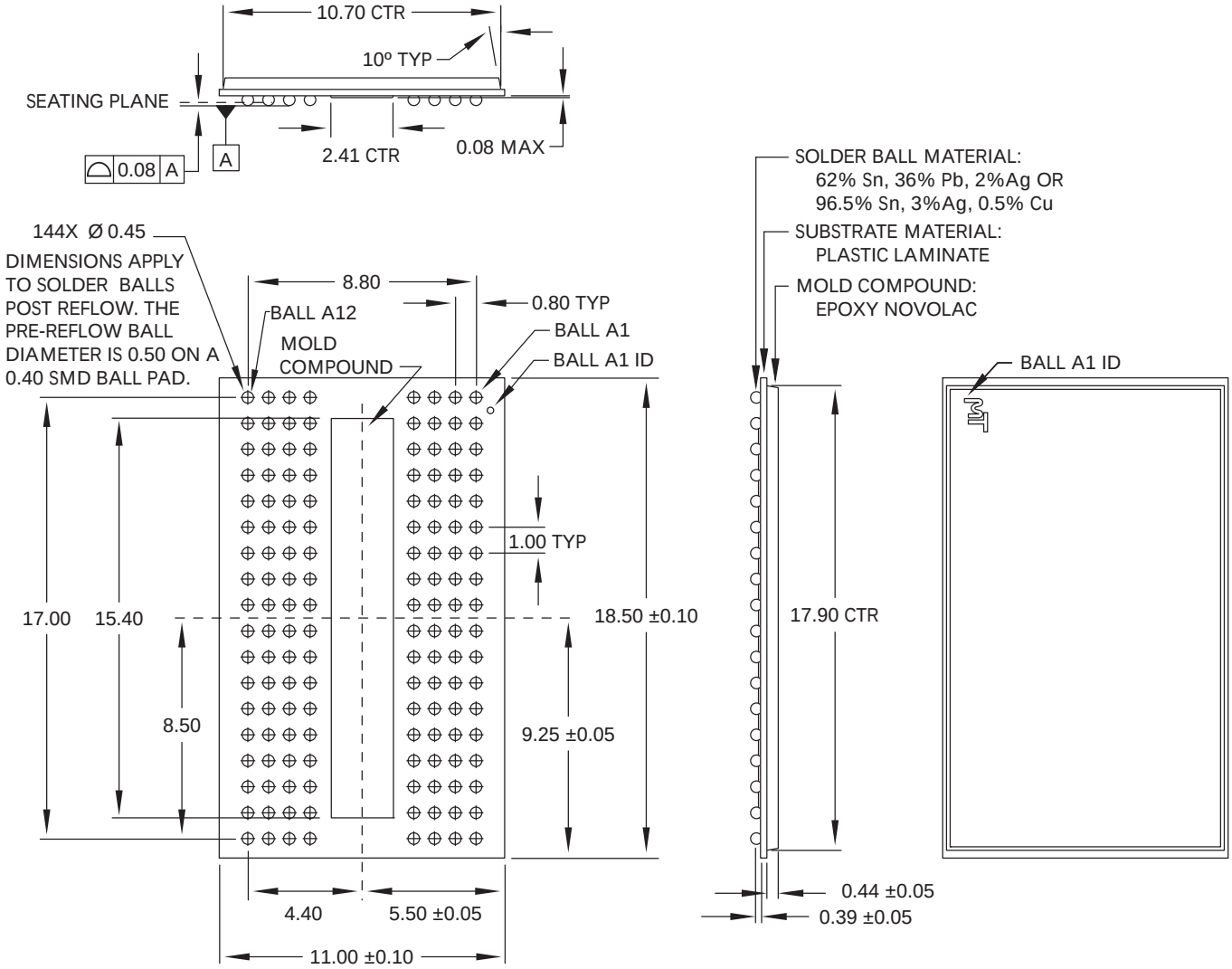
Symbol	Type	Description
A0–A20	Input	**Address inputs:** A0–A20 define the row and column addresses for READ and WRITE operations. During a MODE REGISTER SET, the address inputs define the register settings. They are sampled at the rising edge of CK.
BA0–BA2	Input	**Bank address inputs:** Select to which internal bank a command is being applied.
CK, CK#	Input	**Input clock:** CK and CK# are differential input clocks. Addresses and commands are latched on the rising edge of CK. CK# is ideally 180 degrees out of phase with CK.
CS#	Input	**Chip select:** CS# enables the command decoder when LOW and disables it when HIGH. When the command decoder is disabled, new commands are ignored, but internal operations continue.
DQ0–DQ35	Input	**Data input:** The DQ signals form the 36-bit data bus. During READ commands, the data is referenced to both edges of QK*x*. During WRITE commands, the data is sampled at both edges of DK.
DK, DK#	Input	**Input data clock:** DK and DK# are the differential input data clocks. All input data is referenced to both edges of DK. DK# is ideally 180 degrees out of phase with DK. For the x36 device, DQ0–DQ17 are referenced to DK0 and DK0# and DQ18–DQ35 are referenced to DK1 and DK1#. For the x9 and x18 devices, all DQs are referenced to DK and DK#. All DK*x* and DK*x*# pins must always be supplied to the device.
DM	Input	**Input data mask:** The DM signal is the input mask signal for WRITE data. Input data is masked when DM is sampled HIGH. DM is sampled on both edges of DK (DK1 for the x36 configuration). Tie signal to ground if not used.
TCK	Input	**IEEE 1149.1 clock input:** This ball must be tied to VSS if the JTAG function is not used.
TMS, TDI	Input	**IEEE 1149.1 test inputs:** These balls may be left as no connects if the JTAG function is not used.
WE#, REF#	Input	**Command inputs:** Sampled at the positive edge of CK, WE# and REF# define (together with CS#) the command to be executed.
VREF	Input	**Input reference voltage:** Nominally VDDQ/2. Provides a reference voltage for the input buffers.
ZQ	I/O	**External impedance (25–60Ω):** This signal is used to tune the device outputs to the system data bus impedance. DQ output impedance is set to 0.2 × RQ, where RQ is a resistor from this signal to ground. Connecting ZQ to GND invokes the minimum impedance mode. Connecting ZQ to VDD invokes the maximum impedance mode. Refer to Figure 16 on page 44 to activate this function.
QK*x*, QK*x*#	Output	**Output data clocks:** QK*x* and QK*x*# are opposite polarity, output data clocks. They are free-running, and during READs, are edge-aligned with data output from the RLDRAM. QK*x*# is ideally 180 degrees out of phase with QK*x*. For the x36 device, QK0 and QK0# are aligned with DQ0–DQ17, and QK1 and QK1# are aligned with DQ18–DQ35. For the x18 device, QK0 and QK0# are aligned with DQ0–DQ8, while QK1 and QK1# are aligned with Q9–Q17. For the x9 device, all DQs are aligned with QK0 and QK0#.
QVLD	Output	**Data valid:** The QVLD pin indicates valid output data. QVLD is edge-aligned with QK*x* and QK*x*#.
TDO	Output	**IEEE 1149.1 test output:** JTAG output. This ball may be left as no connect if the JTAG function is not used.
VDD	Supply	**Power supply:** Nominally, 1.8V. See Table 12 on page 29 for range.
VDDQ	Supply	**DQ power supply:** Nominally, 1.5V or 1.8V. Isolated on the device for improved noise immunity. See Table 12 on page 29 for range.
VEXT	Supply	**Power supply:** Nominally, 2.5V. See Table 12 on page 29 for range.
VSS	Supply	Ground.
VSSQ	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
VTT	Supply	**Power supply:** Isolated termination supply. Nominally, VDDQ/2. See Table 12 on page 29 for range.
A21	–	**Reserved for future use:** This signal is internally connected and can be treated as an address input.
A22	–	**Reserved for future use:** This signal is not connected and can be connected to ground.

Table 4: Ball Descriptions (continued)

Symbol	Type	Description
DNU	–	**Do not use:** These balls may be connected to ground. Note that if ODT is enabled, these pins will be connected to VTT.
NF	–	**No function:** These balls can be connected to ground.

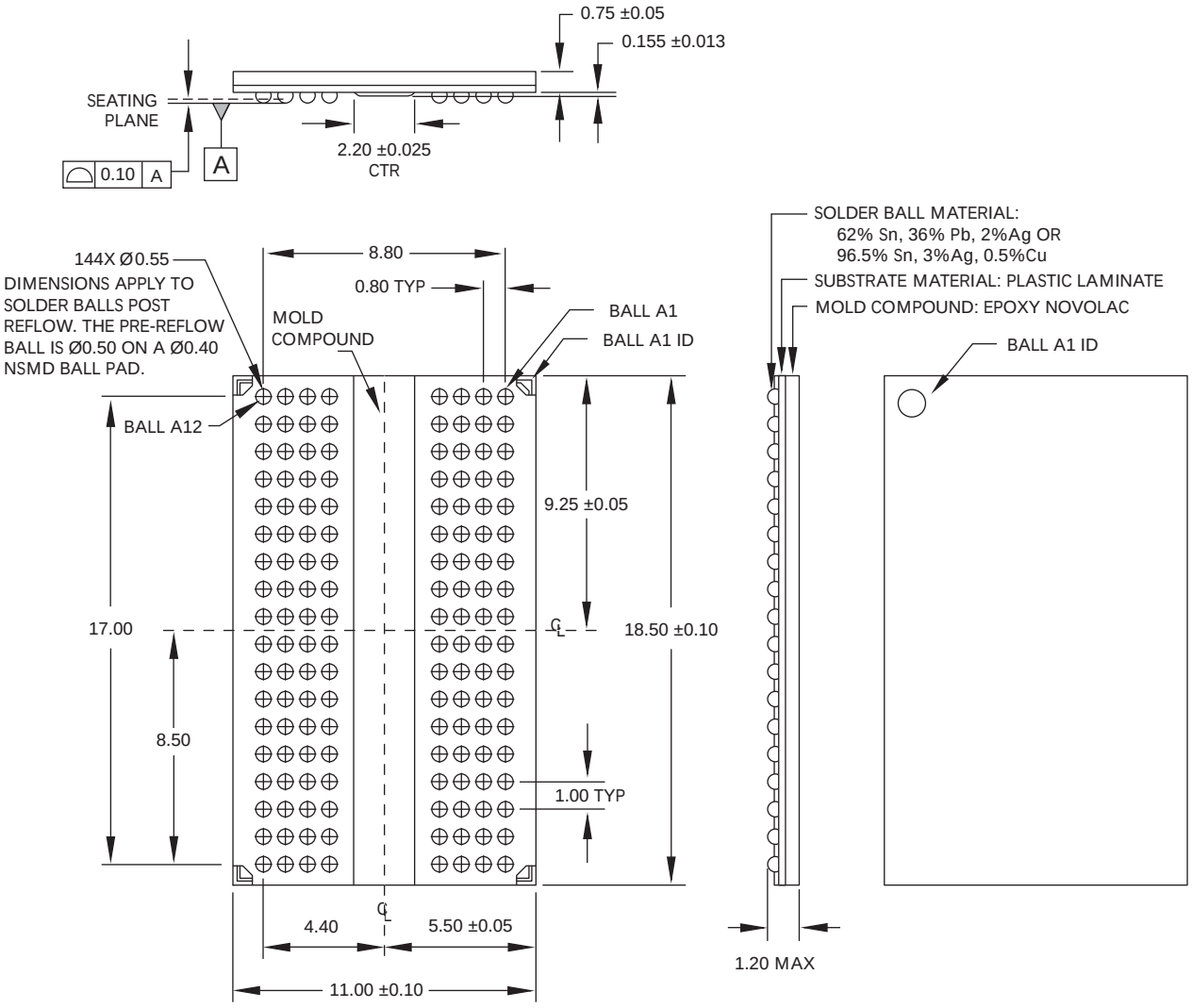
Package Dimensions

Figure 7: 144-Ball µBGA



Notes: 1. All dimensions are in millimeters.

Figure 8: 144-Ball FBGA



Notes:
1. All dimensions are in millimeters.
2. The FBGA package is being phased out.

Electrical Specifications – IDD

Table 5: IDD Operating Conditions and Maximum Limits

Description	Condition	Symbol	-25	-33	-5	Units
Standby current	tCK = idle; All banks idle; No inputs toggling	ISB1 (VDD) x9/x18	48	48	48	mA
		ISB1 (VDD) x36	48	48	48	
		ISB1 (VEXT)	26	26	26	
Active standby current	CS# = 1; No commands; Bank address incremented and half address/data change once every 4 clock cycles	ISB2 (VDD) x9/x18	288	233	189	mA
		ISB2 (VDD) x36	288	233	189	
		ISB2 (VEXT)	26	26	26	
Operational current	BL = 2; Sequential bank access; Bank transitions once every tRC; Half address transitions once every tRC; Read followed by write sequence; continuous data during WRITE commands	IDD1 (VDD) x9/x18	348	305	255	mA
		IDD1 (VDD) x36	374	343	292	
		IDD1 (VEXT)	41	36	36	
Operational current	BL = 4; Sequential bank access; Bank transitions once every tRC; Half address transitions once every tRC; Read followed by write sequence; Continuous data during WRITE commands	IDD2 (VDD) x9/x18	362	319	269	mA
		IDD2 (VDD) x36	418	389	339	
		IDD2 (VEXT)	48	42	42	
Operational current	BL = 8; Sequential bank access; Bank transitions once every tRC; half address transitions once every tRC; Read followed by write sequence; continuous data during WRITE commands	IDD3 (VDD) x9/x18	408	368	286	mA
		IDD3 (VDD) x36	n/a	n/a	n/a	
		IDD3 (VEXT)	55	48	48	
Burst refresh current	Eight-bank cyclic refresh; Continuous address/ data; Command bus remains in refresh for all eight banks	IREF1 (VDD) x9/x18	785	615	430	mA
		IREF1 (VDD) x36	785	615	430	
		IREF1 (VEXT)	133	111	105	
Distributed refresh current	Single-bank refresh; Sequential bank access; Half address transitions once every tRC, continuous data	IREF2 (VDD) x9/x18	325	267	221	mA
		IREF2 (VDD) x36	326	281	227	
		IREF2 (VEXT)	48	42	42	
Operating burst write current example	BL = 2; Cyclic bank access; Half of address bits change every clock cycle; Continuous data; measurement is taken during continuous WRITE	IDD2W (VDD) x9/x18	970	819	597	mA
		IDD2W (VDD) x36	990	914	676	
		IDD2W (VEXT)	100	90	69	
Operating burst write current example	BL = 4; Cyclic bank access; Half of address bits change every 2 clock cycles; Continuous data; Measurement is taken during continuous WRITE	IDD4W (VDD) x9/x18	779	609	439	mA
		IDD4W (VDD) x36	882	790	567	
		IDD4W (VEXT)	88	77	63	
Operating burst write current example	BL = 8; Cyclic bank access; Half of address bits change every 4 clock cycles; continuous data; Measurement is taken during continuous WRITE	IDD8W (VDD) x9/x18	668	525	364	mA
		IDD8W (VDD) x36	n/a	n/a	n/a	
		IDD8W (VEXT)	60	51	40	
Operating burst read current example	BL = 2; Cyclic bank access; Half of address bits change every clock cycle; Measurement is taken during continuous READ	IDD2R (VDD) x9/x18	860	735	525	mA
		IDD2R (VDD) x36	880	795	565	
		IDD2R (VEXT)	100	90	69	
Operating burst read current example	BL = 4; Cyclic bank access; Half of address bits change every 2 clock cycles; Measurement is taken during continuous READ	IDD4R (VDD) x9/x18	680	525	380	mA
		IDD4R (VDD) x36	730	660	455	
		IDD4R (VEXT)	88	77	63	
Operating burst read current example	BL = 8; Cyclic bank access; Half of address bits change every 4 clock cycles; Measurement is taken during continuous READ	IDD8R (VDD) x9/x18	570	450	310	mA
		IDD8R (VDD) x36	n/a	n/a	n/a	
		IDD8R (VEXT)	60	51	40	

Notes:
1. IDD specifications are tested after the device is properly initialized. +0°C ≤ T_C ≤ +95°C; +1.7V ≤ VDD ≤ +1.9V, +2.38V ≤ VEXT ≤ +2.63V, +1.4V ≤ VDDQ ≤ VDD, VREF = VDDQ/2.
2. ^{t}CK = ^{t}DK = MIN, ^{t}RC = MIN.
3. Input slew rate is specified in Table 8 on page 19.
4. Definitions for IDD conditions:
   - 4a. LOW is defined as VIN ≤ VIL(AC) MAX.
   - 4b. HIGH is defined as VIN ≥ VIH(AC) MIN.
   - 4c. Stable is defined as inputs remaining at a HIGH or LOW level.
   - 4d. Floating is defined as inputs at VREF = VDDQ/2.
   - 4e. Continuous data is defined as half the DQ signals changing between HIGH and LOW every half clock cycle (twice per clock).
   - 4f. Continuous address is defined as half the address signals changing between HIGH and LOW every clock cycle (once per clock).
   - 4g. Sequential bank access is defined as the bank address incrementing by one every ^{t}RC.
   - 4h. Cyclic bank access is defined as the bank address incrementing by one for each command access. For BL = 2 this is every clock, for BL = 4 this is every other clock, and for BL = 8 this is every fourth clock.
5. CS# is HIGH unless a READ, WRITE, AREF, or MRS command is registered. CS# never transitions more than once per clock cycle.
6. IDD parameters are specified with ODT disabled.
7. Tests for AC timing, IDD, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operations are tested for the full voltage range specified.
8. IDD tests may use a VIL-to-VIH swing of up to 1.5V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK/CK#), and parameter specifications are tested for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 2 V/ns in the range between VIL(AC) and VIH(AC).

Electrical Specifications – AC and DC

Absolute Maximum Ratings

Stresses greater than those listed in Table 6 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 6: Absolute Maximum Ratings

Parameter	Min	Max	Units
I/O voltage	–0.3	VDDQ + 0.3	V
Voltage on VEXT supply relative to VSS	–0.3	+2.8	V
Voltage on VDD supply relative to VSS	–0.3	+2.1	V
Voltage on VDDQ supply relative to VSS	–0.3	+2.1	V

AC and DC Operating Conditions

Table 7: DC Electrical Characteristics and Operating Conditions

Note 1 applies to the entire table; Unless otherwise noted: +0°C ≤ T_C ≤ +95°C; +1.7V ≤ VDD ≤ +1.9V

Description	Conditions	Symbol	Min	Max	Units	Notes
Supply voltage	–	VEXT	2.38	2.63	V	
Supply voltage	–	VDD	1.7	1.9	V	2
Isolated output buffer supply	–	VDDQ	1.4	VDD	V	2, 3
Reference voltage	–	VREF	0.49 × VDDQ	0.51 × VDDQ	V	4, 5, 6
Termination voltage	–	VTT	0.95 × VREF	1.05 × VREF	V	7, 8
Input high (logic 1) voltage	–	VIH	VREF + 0.1	VDDQ + 0.3	V	2
Input low (logic 0) voltage	–	VIL	VSSQ - 0.3	VREF - 0.1	V	2
Output high current	VOH = VDDQ/2	IOH	(VDDQ/2)/ (1.15 × RQ/5)	(VDDQ/2)/ (0.85 × RQ/5)	A	9, 10, 11
Output low current	VOL = VDDQ/2	IOL	(VDDQ/2)/ (1.15 × RQ/5)	(VDDQ/2)/ (0.85 × RQ/5)	A	9, 10, 11
Clock input leakage current	0V ≤ VIN ≤ VDD	ILC	–5	5	µA	
Input leakage current	0V ≤ VIN ≤ VDD	ILI	–5	5	µA	
Output leakage current	0V ≤ VIN ≤ VDDQ	ILO	–5	5	µA	
Reference voltage current	–	IREF	–5	5	µA	

Notes:
1. All voltages referenced to VSS (GND).
2. Overshoot: VIH(AC) ≤ VDD + 0.7V for t ≤ ^{t}CK/2. Undershoot: VIL(AC) ≥ –0.5V for t ≤ ^{t}CK/2. During normal operation, VDDQ must not exceed VDD. Control input signals may not have pulse widths less than ^{t}CK/2 or operate at frequencies exceeding ^{t}CK (MAX).
3. VDDQ can be set to a nominal 1.5V ± 0.1V or 1.8V ± 0.1V supply.
4. Typically the value of VREF is expected to be 0.5 x VDDQ of the transmitting device. VREF is expected to track variations in VDDQ.
5. Peak-to-peak AC noise on VREF must not exceed ±2 percent VREF(DC).
6. VREF is expected to equal VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on VREF may not exceed ±2 percent of the DC value. Thus, from VDDQ/2, VREF is allowed ±2 percent VDDQ/2 for DC error and an additional ±2 percent VDDQ/2 for AC noise. This measurement is to be taken at the nearest VREF bypass capacitor.

7. VTT is expected to be set equal to VREF and must track variations in the DC level of VREF.
8. On-die termination may be selected using mode register bit 9 (see Figure 11 on page 32). A resistance RTT from each data input signal to the nearest VTT can be enabled.
   RTT = 125–185Ω at 95°C T_C.
9. IOH and IOL are defined as absolute values and are measured at VDDQ/2. IOH flows from the device, IOL flows into the device.
10. If MRS bit A8 is 0, use RQ = 250Ω in the equation in lieu of presence of an external impedance matched resistor.
11. For VOL and VOH, refer to the RLDRAM II HSPICE or IBIS driver models.

Table 8: Input AC Logic Levels

Notes 1–3 apply to entire table; Unless otherwise noted: +0°C ≤ T_C ≤ +95°C; +1.7V ≤ VDD ≤ +1.9V

Description	Symbol	Min	Max	Units
Input high (logic 1) voltage	VIH	VREF + 0.2	–	V
Input low (logic 0) voltage	VIL	–	VREF - 0.2	V

Notes:
1. All voltages referenced to VSS (GND).
2. The AC and DC input level specifications are as defined in the HSTL standard (that is, the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
3. The minimum slew rate for the input signals used to test the device is 2 V/ns in the range between VIL(AC) and VIH(AC). See illustration below:

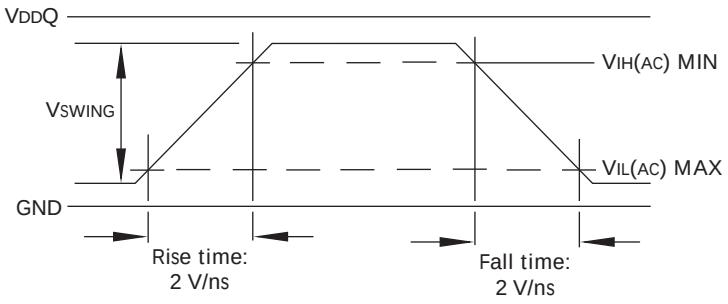


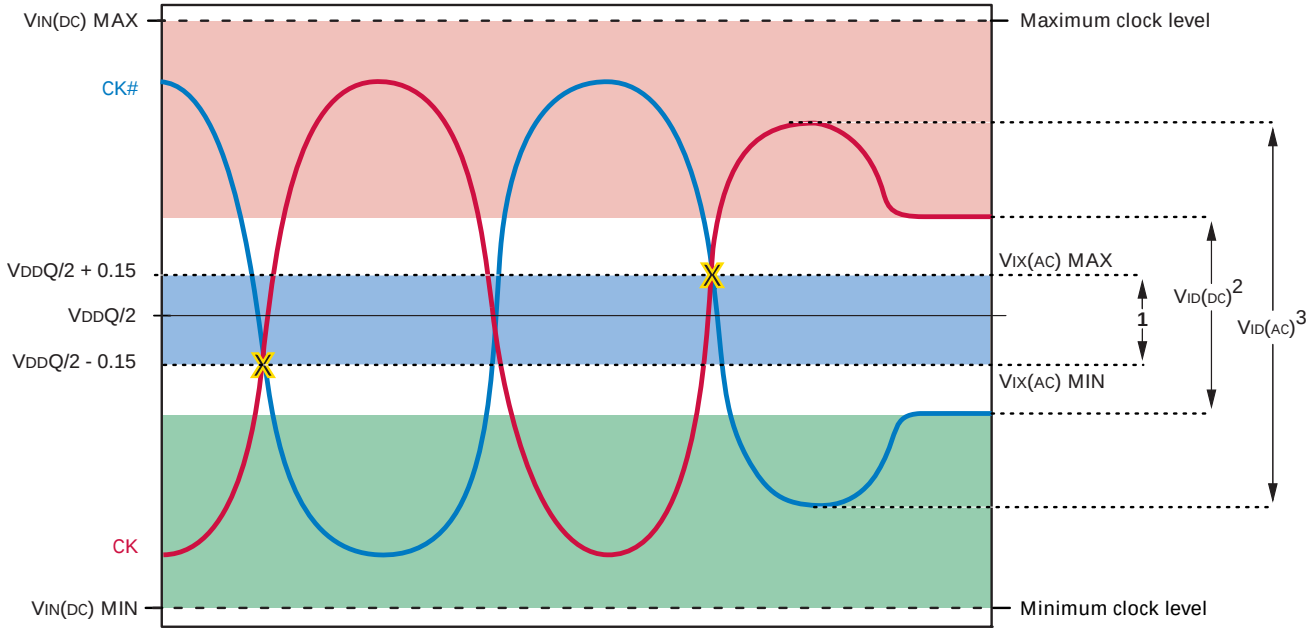
Table 9: Differential Input Clock Operating Conditions

Notes 1–4 apply to the entire table; Unless otherwise noted: +0°C ≤ T_C ≤ +95°C; +1.7V ≤ VDD ≤ +1.9V

Parameter/Condition	Symbol	Min	Max	Units	Notes
Clock input voltage level: CK and CK#	VIN(DC)	–0.3	VDDQ + 0.3	V	
Clock input differential voltage: CK and CK#	VID(DC)	0.2	VDDQ + 0.6	V	5
Clock input differential voltage: CK and CK#	VID(AC)	0.4	VDDQ + 0.6	V	5
Clock input crossing point voltage: CK and CK#	VIX(AC)	VDDQ/2 - 0.15	VDDQ/2 + 0.15	V	6

Notes:
1. DK*x* and DK*x*# have the same requirements as CK and CK#.
2. All voltages referenced to VSS (GND).
3. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross. The input reference level for signals other than CK/CK# is VREF.
4. CK and CK# input slew rate must be ≥2 V/ns (≥4 V/ns if measured differentially).
5. VID is the magnitude of the difference between the input level on CK and the input level on CK#.
6. The value of VIX is expected to equal VDDQ/2 of the transmitting device and must track variations in the DC level of the same.

Figure 9: Clock Input



Notes:
1. CK and CK# must cross within this region.
2. CK and CK# must meet at least VID(DC) MIN when static and centered around VDDQ/2.
3. Minimum peak-to-peak swing.
4. It is a violation to tristate CK and CK# after the part is initialized.

Input Slew Rate Derating

Table 10 on page 22 and Table 11 on page 23 define the address, command, and data setup and hold derating values. These values are added to the default ^{t}AS/^{t}CS/^{t}DS and ^{t}AH/^{t}CH/^{t}DH specifications when the slew rate of any of these input signals is less than the 2 V/ns the nominal setup and hold specifications are based upon.

To determine the setup and hold time needed for a given slew rate, add the ^{t}AS/^{t}CS default specification to the "^{t}AS/^{t}CS VREF to CK/CK# Crossing" and the ^{t}AH/^{t}CH default specification to the "^{t}AH/^{t}CH CK/CK# Crossing to VREF" derated values on Table 10. The derated data setup and hold values can be determined in a like manner using the "^{t}DS VREF to CK/CK# Crossing" and "^{t}DH to CK/CK# Crossing to VREF" values on Table 11. The derating values on Table 10 and Table 11 apply to all speed grades.

The setup times on Table 10 and Table 11 represent a rising signal. In this case, the time from which the rising signal crosses VIH(AC) MIN to the CK/CK# cross point is static and must be maintained across all slew rates. The derated setup timing represents the point at which the rising signal crosses VREF(DC) to the CK/CK# cross point. This derated value is calculated by determining the time needed to maintain the given slew rate and the delta between VIH(AC) MIN and the CK/CK# cross point. The setup values in Table 10 and Table 11 are also valid for falling signals (with respect to VIL[AC] MAX and the CK/CK# cross point).

The hold times in Table 10 and Table 11 represent falling signals. In this case, the time from the CK/CK# cross point to when the signal crosses VIH(DC) MIN is static and must be maintained across all slew rates. The derated hold timing represents the delta between the CK/CK# cross point to when the falling signal crosses VREF(DC). This derated value is calculated by determining the time needed to maintain the given slew rate and the delta between the CK/CK# cross point and VIH(DC). The hold values in Table 10 and Table 11 are also valid for rising signals (with respect to VIL[DC] MAX and the CK and CK# cross point).

Note: The above descriptions also pertain to data setup and hold derating when CK/CK# are replaced with DK/DK#.

Table 10: Address and Command Setup and Hold Derating Values

Command/ Address Slew Rate (V/ns)	^{t}AS/^{t}CS VREF to CK/CK# Crossing	^{t}AS/^{t}CS VIH(AC) MIN to CK/CK# Crossing	^{t}AH/^{t}CH CK/CK# Crossing to VREF	^{t}AH/^{t}CH CK/CK# Crossing to VIH(DC) MIN	Units
	CK, CK# Differential Slew Rate: 2.0 V/ns				
2.0	0	–100	0	–50	ps
1.9	5	–100	3	–50	ps
1.8	11	–100	6	–50	ps
1.7	18	–100	9	–50	ps
1.6	25	–100	13	–50	ps
1.5	33	–100	17	–50	ps
1.4	43	–100	22	–50	ps
1.3	54	–100	27	–50	ps
1.2	67	–100	34	–50	ps
1.1	82	–100	41	–50	ps
1.0	100	–100	50	–50	ps
	CK, CK# Differential Slew Rate: 1.5 V/ns				
2.0	30	–70	30	–20	ps
1.9	35	–70	33	–20	ps
1.8	41	–70	36	–20	ps
1.7	48	–70	39	–20	ps
1.6	55	–70	43	–20	ps
1.5	63	–70	47	–20	ps
1.4	73	–70	52	–20	ps
1.3	84	–70	57	–20	ps
1.2	97	–70	64	–20	ps
1.1	112	–70	71	–20	ps
1.0	130	–70	80	–20	ps
	CK, CK# Differential Slew Rate: 1.0 V/ns				
2.0	60	–40	60	10	ps
1.9	65	–40	63	10	ps
1.8	71	–40	66	10	ps
1.7	78	–40	69	10	ps
1.6	85	–40	73	10	ps
1.5	93	–40	77	10	ps
1.4	103	–40	82	10	ps
1.3	114	–40	87	10	ps
1.2	127	–40	94	10	ps
1.1	142	–40	101	10	ps
1.0	160	–40	110	10	ps

Table 11: Data Setup and Hold Derating Values

Data Slew Rate (V/ns)	^{t}DS VREF to CK/CK# Crossing	^{t}DS VIH(AC) MIN to CK/CK# Crossing	^{t}DH CK/CK# Crossing to VREF	^{t}DH CK/CK# Crossing to VIH(DC) MIN	Units
	DK, DK# Differential Slew Rate: 2.0 V/ns				
2.0	0	–100	0	–50	ps
1.9	5	–100	3	–50	ps
1.8	11	–100	6	–50	ps
1.7	18	–100	9	–50	ps
1.6	25	–100	13	–50	ps
1.5	33	–100	17	–50	ps
1.4	43	–100	22	–50	ps
1.3	54	–100	27	–50	ps
1.2	67	–100	34	–50	ps
1.1	82	–100	41	–50	ps
1.0	100	–100	50	–50	ps
	DK, DK# Differential Slew Rate: 1.5 V/ns				
2.0	30	–70	30	–20	ps
1.9	35	–70	33	–20	ps
1.8	41	–70	36	–20	ps
1.7	48	–70	39	–20	ps
1.6	55	–70	43	–20	ps
1.5	63	–70	47	–20	ps
1.4	73	–70	52	–20	ps
1.3	84	–70	57	–20	ps
1.2	97	–70	64	–20	ps
1.1	112	–70	71	–20	ps
1.0	130	–70	80	–20	ps
	DK, DK# Differential Slew Rate: 1.0 V/ns				
2.0	60	–40	60	10	ps
1.9	65	–40	63	10	ps
1.8	71	–40	66	10	ps
1.7	78	–40	69	10	ps
1.6	85	–40	73	10	ps
1.5	93	–40	77	10	ps
1.4	103	–40	82	10	ps
1.3	114	–40	87	10	ps
1.2	127	–40	94	10	ps
1.1	142	–40	101	10	ps
1.0	160	–40	110	10	ps

Figure 10: Nominal ^{t}AS/^{t}CS/^{t}DS and ^{t}AH/^{t}CH/^{t}DH Slew Rate

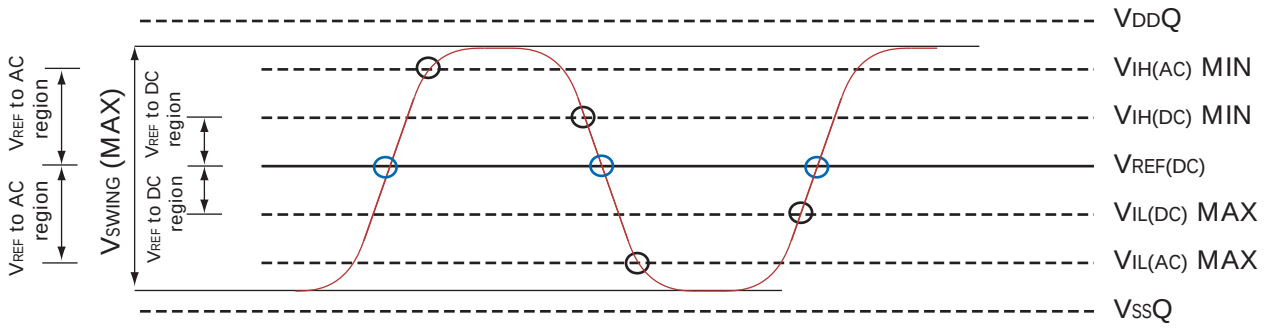


Table 12: Capacitance
Notes 1–2 apply to entire table

Description	Symbol	Conditions	Min	Max	Units
Address/control input capacitance	CI	T_A = 25°C; *f* = 100 MHz VDD = VDDQ = 1.8V	1.5	2.5	pF
Input/output capacitance (DQ, DM, and QK/QK#)	CO		3.5	5.0	pF
Clock capacitance (CK/CK#, and DK/DK#)	CCK		2.0	3.0	pF
JTAG pins	CJTAG		2.0	5.0	pF

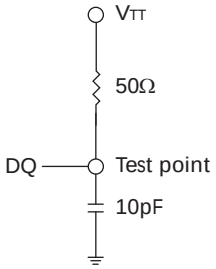
Notes: 1. Capacitance is not tested on ZQ pin.
2. JTAG pins are tested at 50 MHz.

Table 13: AC Electrical Characteristics: -25, -33, -5
Notes 1–4 (page 39) apply to the entire table

Description	Symbol	-25		-33		-5		Units	Notes
		Min	Max	Min	Max	Min	Max		
Clock									
Input clock cycle time	^{t}CK	2.5	5.7	3.3	5.7	5.0	5.7	ns	
Input data clock cycle time	^{t}DK	^{t}CK		^{t}CK		^{t}CK		ns	
Clock jitter: period	^{t}JITPER	–150	150	–200	200	–250	250	ps	5, 6
Clock jitter: cycle-to-cycle	^{t}JITCC		300		400		500	ps	
Clock HIGH time	^{t}CKH, ^{t}DKH	0.45	0.55	0.45	0.55	0.45	0.55	^{t}CK	
Clock LOW time	^{t}CKL, ^{t}DKL	0.45	0.55	0.45	0.55	0.45	0.55	^{t}CK	
Clock to input data clock	^{t}CKDK	–0.3	0.5	–0.3	1.0	–0.3	1.5	ns	
Mode register set cycle time to any command	^{t}MRSC	6	–	6	–	6	–	^{t}CK	
Setup Times									
Address/command and input setup time	^{t}AS/^{t}CS	0.4	–	0.5	–	0.8	–	ns	
Data-in and data mask to DK setup time	^{t}DS	0.25	–	0.3	–	0.4	–	ns	
Hold Times									
Address/command and input hold time	^{t}AH/^{t}CH	0.4	–	0.5	–	0.8	–	ns	
Data-in and data mask to DK hold time	^{t}DH	0.25	–	0.3	–	0.4	–	ns	
Data and Data Strobe									
Output data clock HIGH time	^{t}QKH	0.9	1.1	0.9	1.1	0.9	1.1	^{t}CKH	
Output data clock LOW time	^{t}QKL	0.9	1.1	0.9	1.1	0.9	1.1	^{t}CKL	
Half-clock period	^{t}QHP	MIN (^{t}QKH, ^{t}QKL)	–	MIN (^{t}QKH, ^{t}QKL)	–	MIN (^{t}QKH, ^{t}QKL)	–		
QK edge to clock edge skew	^{t}CKQK	–0.25	0.25	–0.3	0.3	–0.5	0.5	ns	
QK edge to output data edge	^{t}QKQ0, ^{t}QKQ1	–0.2	0.2	–0.25	0.25	–0.3	0.3	ns	7
QK edge to any output data edge	^{t}QKQ	–0.3	0.3	–0.35	0.35	–0.4	0.4	ns	8
QK edge to QVLD	^{t}QKVLD	–0.3	0.3	–0.35	0.35	–0.4	0.4	ns	
Data valid window	^{t}DVW	^{t}QHP - (^{t}QKQ*x* [MAX] + |^{t}QKQ*x* [MIN]|)	–	^{t}QHP - (^{t}QKQ*x* [MAX] + |^{t}QKQ*x* [MIN]|)	–	^{t}QHP - (^{t}QKQ*x* [MAX] + |^{t}QKQ*x* [MIN]|)	–		
Refresh									
Average periodic refresh interval	^{t}REFI	–	0.49	–	0.49	–	0.49	µs	9

Notes

1. All timing parameters are measured relative to the crossing point of CK/CK#, DK/DK# and to the crossing point with VREF of the command, address, and data signals.
2. Outputs measured with equivalent load:



3. Tests for AC timing, IDD, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operations are tested for the full voltage range specified.
4. AC timing may use a VIL-to-VIH swing of up to 1.5V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK/CK#), and parameter specifications are tested for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 2 V/ns in the range between VIL(AC) and VIH(AC).
5. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
6. Frequency drift is not allowed.
7. ^{t}QKQ0 is referenced to DQ0–DQ17 for the x36 configuration and DQ0–DQ8 for the x18 configuration. ^{t}QKQ1 is referenced to DQ18–DQ35 for the x36 configuration and DQ9–DQ17 for the x18 configuration.
8. ^{t}QKQ takes into account the skew between any QK*x* and any Q.
9. To improve efficiency, eight AREF commands (one for each bank) can be posted to the RLDRAM on consecutive cycles at periodic intervals of 3.90µs.

Temperature and Thermal Impedance

It is imperative that the RLDRAM device's temperature specifications, shown in Table 14, be maintained in order to ensure the junction temperature is in the proper operating range to meet data sheet specifications. An important step in maintaining the proper junction temperature is using the device's thermal impedances correctly. The thermal impedances are listed for the packages available.

Incorrectly using thermal impedances can produce significant errors. Read Micron technical note TN-00-08, "Thermal Applications" prior to using the thermal impedances listed in Table 14. For designs that are expected to last several years and require the flexibility to use several DRAM die shrinks, consider using final target theta values (rather than existing values) to account for increased thermal impedances from the die size reduction.

The RLDRAM device's safe junction temperature range can be maintained when the T_C specification is not exceeded. In applications where the device's ambient temperature is too high, use of forced air and/or heat sinks may be required in order to satisfy the case temperature specifications.

Table 14: Temperature Limits

Parameter		Symbol	Min	Max	Units	Notes
Storage temperature		T_{STG}	–55	+150	°C	1
Reliability junction temperature	Commercial	T_J	–	+110	°C	2
	Industrial		–	+110	°C	2
Operating junction temperature	Commercial	T_J	0	+100	°C	3
	Industrial		–40	+100	°C	3
Operating case temperature	Commercial	T_C	0	+95	°C	4, 5
	Industrial		–40	+95	°C	4, 5, 6

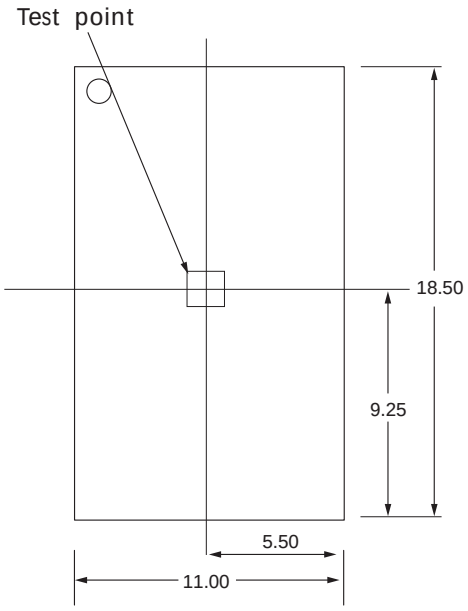
Notes:
1. MAX storage case temperature; T_{STG} is measured in the center of the package, as shown in Figure 10 on page 29. This case temperature limit is allowed to be exceeded briefly during package reflow, as noted in Micron technical note TN-00-15.
2. Temperatures greater than 110°C may cause permanent damage to the device. This is a stress rating only and functional operation of the device at or above this is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability of the part.
3. Junction temperature depends upon package type, cycle time, loading, ambient temperature, and airflow.
4. MAX operating case temperature; T_C is measured in the center of the package, as shown in Figure 10 on page 29.
5. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.
6. Both temperature specifications must be satisfied.

Table 15: Thermal Impedance

Package	Substrate	θ JA (°C/W) Airflow = 0m/s	θ JA (°C/W) Airflow = 1m/s	θ JA (°C/W) Airflow = 2m/s	θ JB (°C/W)	θ JC (°C/W)
µBGA	2-layer	41.2	29.1	25.3	14.3	2.27
	4-layer	28.2	21.9	19.9	13.6	
FBGA	2-layer	42.2	29.3	25.3	16.4	2.6
	4-layer	28.5	22.0	19.9	13.4	

Notes: Thermal impedance data is based on a number of samples from multiple lots and should be viewed as a typical number.

Figure 11: Example Temperature Test Point Location



Commands

The following table provides descriptions of the valid commands of the RLDRAM. All input states or sequences not shown are illegal or reserved. All command and address inputs must meet setup and hold times around the rising edge of CK.

Table 16: Description of Commands

Command	Description	Notes
DSEL/NOP	The NOP command is used to perform a no operation to the RLDRAM, which essentially deselects the chip. Use the NOP command to prevent unwanted commands from being registered during idle or wait states. Operations already in progress are not affected. Output values depend on command history.	1
MRS	The mode register is set via the address inputs A0–A17. See Figure 11 on page 32 for further information. The MRS command can only be issued when all banks are idle and no bursts are in progress.	
READ	The READ command is used to initiate a burst read access to a bank. The value on the BA0–BA2 inputs selects the bank, and the address provided on inputs A0–A*n* selects the data location within the bank.	2
WRITE	The WRITE command is used to initiate a burst write access to a bank. The value on the BA0–BA2 inputs selects the bank, and the address provided on inputs A0–A*n* selects the data location within the bank. Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If the DM signal is registered LOW, the corresponding data will be written to memory. If the DM signal is registered HIGH, the corresponding data inputs will be ignored (that is, this part of the data word will not be written).	2
AREF	The AREF command is used during normal operation of the RLDRAM to refresh the memory content of a bank. The command is nonpersistent, so it must be issued each time a refresh is required. The value on the BA0–BA2 inputs selects the bank. The refresh address is generated by an internal refresh controller, effectively making each address bit a "Don't Care" during the AREF command. See "AUTO REFRESH (AREF)" on page 39 for more details.	

Notes: 1. When the chip is deselected, internal NOP commands are generated and no commands are accepted.
2. *n* = 20.

Table 17: Command Table
Notes 1–2 apply to the entire table

Operation	Code	CS#	WE#	REF#	A0–A*n*[2]	BA0–BA2	Notes
Device DESELECT/no operation	DSEL/NOP	H	X	X	X	X	
MRS	MRS	L	L	L	OPCODE	X	3
READ	READ	L	H	H	A	BA	4
WRITE	WRITE	L	L	H	A	BA	4
AUTO REFRESH	AREF	L	H	L	X	BA	

Notes: 1. X = "Don't Care;" H = logic HIGH; L = logic LOW; A = valid address; BA = valid bank address.
2. *n* = 20.
3. Only A0–A17 are used for the MRS command.
4. Address width varies with burst length; see Table 19 on page 35 for details.

MODE REGISTER SET (MRS)

The mode register set stores the data for controlling the operating modes of the memory. It programs the RLDRAM configuration, burst length, test mode, and I/O options. During an MRS command, the address inputs A0–A17 are sampled and stored in the mode register. After issuing a valid MRS command, ^{t}MRSC must be met before any command can be issued to the RLDRAM. This statement does not apply to the consecutive MRS commands needed for internal logic reset during the initialization routine. The MRS command can only be issued when all banks are idle and no bursts are in progress.

Note: The data written by the prior burst length is not guaranteed to be accurate when the burst length of the device is changed.

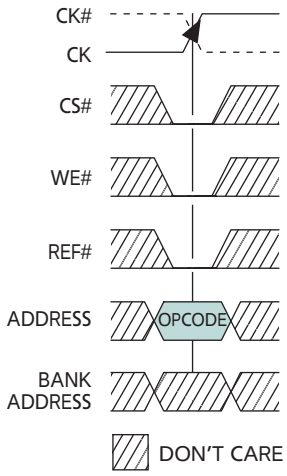
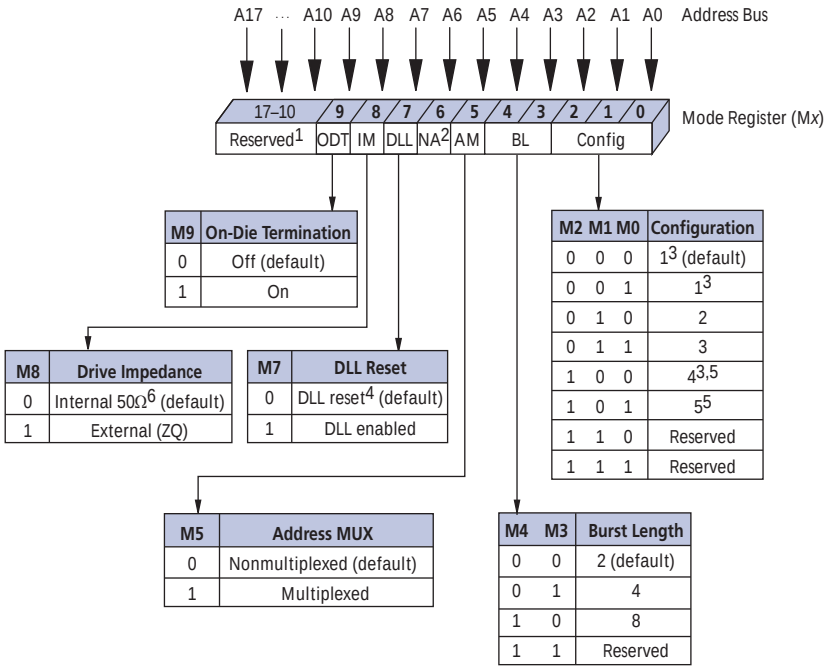


Figure 11: Mode Register Definition in Nonmultiplexed Address Mode



Notes:
1. A10–A17 must be set to zero; A18–A*n* = "Don't Care."
2. A6 not used in MRS.
3. BL = 8 is not available.
4. DLL RESET turns the DLL off.
5. Available in 576Mb part only.
6. ±30 percent temperature variation.

Configuration Tables

Table 18 shows the different configurations that can be programmed into the mode register. The WRITE latency is equal to the READ latency plus one in each configuration in order to maximize data bus utilization. Bits M0, M1, and M2 are used to select the configuration during the MRS command.

Table 18: Cycle Time and READ/WRITE Latency Configuration Table

Parameter	Configuration			Units
	1[1]	2	3	
^{t}RC	4	6	8	^{t}CK
^{t}RL	4	6	8	^{t}CK
^{t}WL	5	7	9	^{t}CK
Valid frequency range	200–175	300–175	400–175	MHz

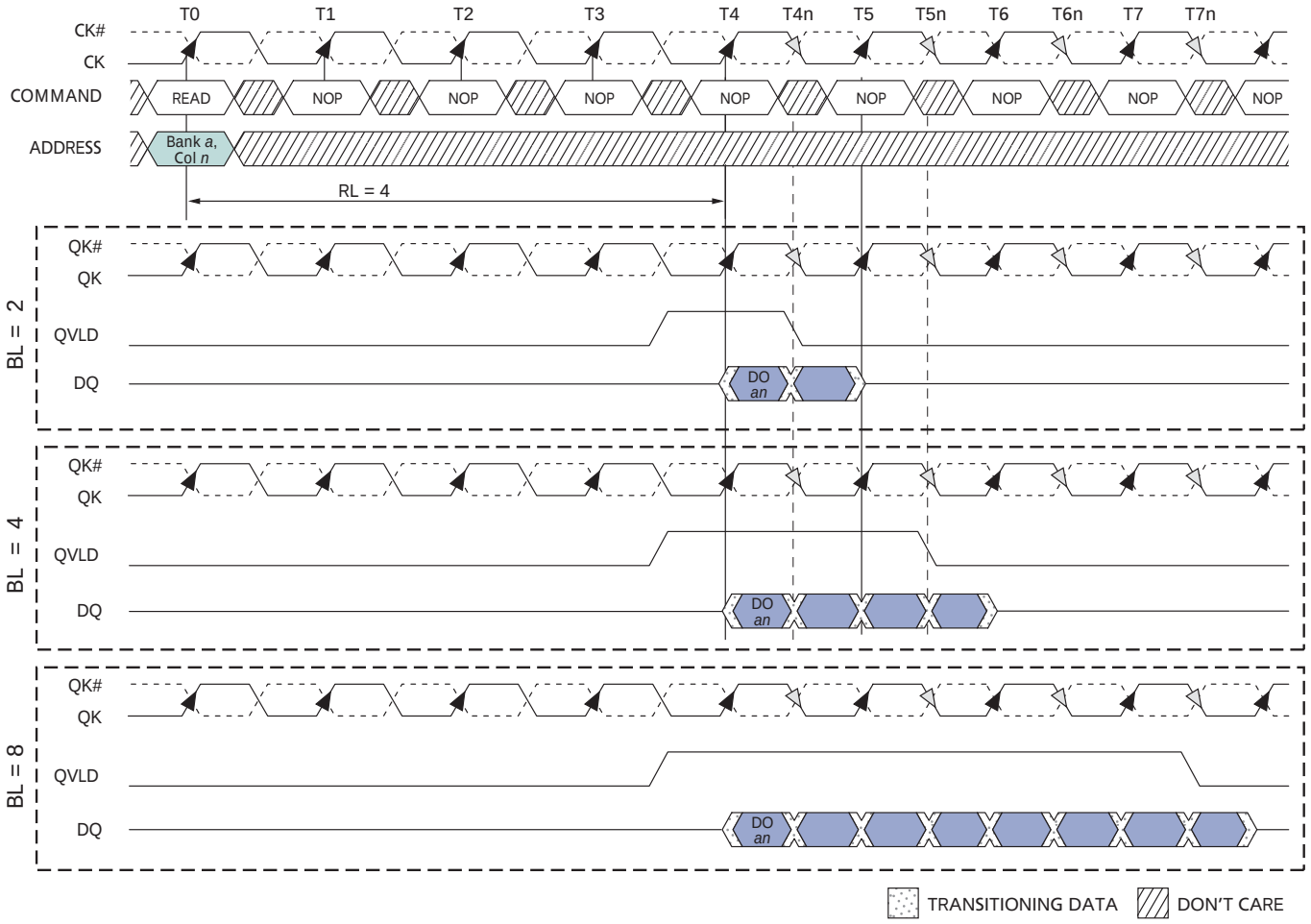
Notes: 1. BL = 8 is not available.

Burst Length (BL)

Burst length is defined by M3 and M4 of the mode register. Read and write accesses to the RLDRAM are burst-oriented, with the burst length being programmable to 2, 4, or 8. Figure 12 on page 34 illustrates the different burst lengths with respect to a READ command. Changes in the burst length affect the width of the address bus (see Table 19 on page 35 for details).

Note: The data written by the prior burst length is not guaranteed to be accurate when the burst length of the device is changed.

Figure 12: Read Burst Lengths



Notes:
1. DO a*n* = data-out from bank *a* and address *an*.
2. Subsequent elements of data-out appear after DO *n*.
3. Shown with nominal ^{t}CKQK.

Table 19: Address Widths at Different Burst Lengths

Burst Length	x9	x18	x36
2	A0–A20	A0–A19	A0–A18
4	A0–A19	A0–A18	A0–A17
8	A0–A18	A0–A17	n/a

Address Multiplexing

Although the RLDRAM has the ability to operate with an SRAM interface by accepting the entire address in one clock, an option in the mode register can be set so that it functions with multiplexed addresses, similar to a traditional DRAM. In multiplexed address mode, the address can be provided to the RLDRAM in two parts that are latched into the memory with two consecutive rising clock edges. This provides the advantage of only needing a maximum of 11 address balls to control the RLDRAM, reducing the number of

signals on the controller side. The data bus efficiency in continuous burst mode is only affected when using the BL = 2 setting since the device requires two clocks to read and write the data. The bank addresses are delivered to the RLDRAM at the same time as the WRITE and READ command and the first address part, A*x*. Table 21 on page 61 and Table 22 on page 62 show the addresses needed for both the first and second rising clock edges (A*x* and A*y*, respectively). The AREF command does not require an address on the second rising clock edge, as only the bank address is needed during this command. Because of this, AREF commands may be issued on consecutive clocks.

The multiplexed address option is available by setting bit M5 to "1" in the mode register. Once this bit is set, the READ, WRITE, and MRS commands follow the format described in Figure 35 on page 57. Further information on operation with multiplexed addresses can be seen in "Multiplexed Address Mode" on page 57.

DLL RESET

DLL RESET is selected with bit M7 of the mode register as is shown in Figure 11 on page 32. The default setting for this option is LOW, whereby the DLL is disabled. Once M7 is set HIGH, 1,024 cycles (5µs at 200 MHz) are needed before a READ command can be issued. This time allows the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the ^{t}CKQK parameter. A reset of the DLL is necessary if ^{t}CK or VDD is changed after the DLL has already been enabled. To reset the DLL, an MRS command must be issued where M7 is set LOW. After waiting ^{t}MRSC, a subsequent MRS command should be issued whereby M7 goes HIGH. 1,024 clock cycles are then needed before a READ command is issued.

Drive Impedance Matching

The RLDRAM II is equipped with programmable impedance output buffers. This option is selected by setting bit M8 HIGH during the MRS command. The purpose of the programmable impedance output buffers is to allow the user to match the driver impedance to the system. To adjust the impedance, an external precision resistor (RQ) is connected between the ZQ ball and VSS. The value of the resistor must be five times the desired impedance. For example, a 300Ω resistor is required for an output impedance of 60Ω. The range of RQ is 125–300Ω, which guarantees output impedance in the range of 25–60Ω (within 15 percent).

Output impedance updates may be required because over time variations may occur in supply voltage and temperature. When the external drive impedance is enabled in the MRS, the device will periodically sample the value of RQ. An impedance update is transparent to the system and does not affect device operation. All data sheet timing and current specifications are met during an update.

When bit M8 is set LOW during the MRS command, the RLDRAM provides an internal impedance at the output buffer of 50Ω (±30 percent with temperature variation). This impedance is also periodically sampled and adjusted to compensate for variation in supply voltage and temperature.

On-Die Termination (ODT)

ODT is enabled by setting M9 to "1" during an MRS command. With ODT on, the DQs and DM are terminated to VTT with a resistance RTT. The command, address, QVLD, and clock signals are not terminated. Figure 13 on page 36 shows the equivalent circuit of a DQ receiver with ODT. The ODT function is dynamically switched off when a DQ begins

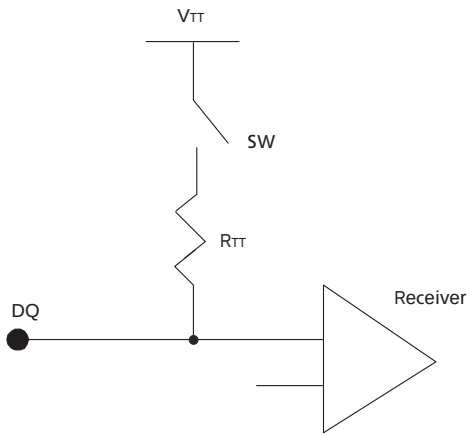
to drive after a READ command is issued. Similarly, ODT is designed to switch on at the DQs after the RLDRAM has issued the last piece of data. The DM pin will always be terminated. See section entitled “Operations” on page 40 for relevant timing diagrams.

Table 20: On-Die Termination DC Parameters

Description	Symbol	Min	Max	Units	Notes
Termination voltage	VTT	0.95 × VREF	1.05 × VREF	V	1, 2
On-die termination	RTT	125	185	Ω	3

Notes:
1. All voltages referenced to VSS (GND).
2. VTT is expected to be set equal to VREF and must track variations in the DC level of VREF.
3. The RTT value is measured at 95°C T_C.

Figure 13: On-Die Termination-Equivalent Circuit



WRITE

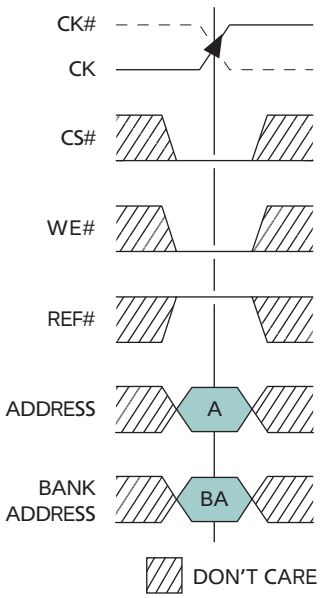
Write accesses are initiated with a WRITE command, as shown in Figure 14. The address needs to be provided during the WRITE command.

During WRITE commands, data will be registered at both edges of DK according to the programmed burst length (BL). The RLDRAM operates with a WRITE latency (WL) that is one cycle longer than the programmed READ latency (RL + 1), with the first valid data registered at the first rising DK edge WL cycles after the WRITE command.

Any WRITE burst may be followed by a subsequent READ command (assuming ^{t}RC is met). To avoid external data bus contention, at least one NOP command is needed between the WRITE and READ commands. Figure 21 on page 45 and Figure 22 on page 46 illustrate the timing requirements for a WRITE followed by a READ where one and two intermediary NOPs are required, respectively.

Setup and hold times for incoming DQ relative to the DK edges are specified as ^{t}DS and ^{t}DH. The input data is masked if the corresponding DM signal is HIGH. The setup and hold times for the DM signal are also ^{t}DS and ^{t}DH.

Figure 14: WRITE Command



READ

Read accesses are initiated with a READ command, as shown in Figure 15. Addresses are provided with the READ command.

During READ bursts, the memory device drives the read data so it is edge-aligned with the QK*x* signals. After a programmable READ latency, data is available at the outputs. One half clock cycle prior to valid data on the read bus, the data valid signal, QVLD, transitions from LOW to HIGH. QVLD is also edge-aligned with the QK*x* signals.

The skew between QK and the crossing point of CK is specified as ^{t}CKQK. ^{t}QKQ0 is the skew between QK0 and the last valid data edge generated at the DQ signals associated with QK0 (^{t}QKQ0 is referenced to DQ0–DQ17 for the x36 configuration and DQ0–DQ8 for the x18 configuration). ^{t}QKQ1 is the skew between QK1 and the last valid data edge generated at the DQ signals associated with QK1 (^{t}QKQ1 is referenced to DQ18–DQ35 for the x36 and DQ9–DQ17 for the x18 configuration). ^{t}QKQ*x* is derived at each QK*x* clock edge and is not cumulative over time. ^{t}QKQ is defined as the skew between either QK differential pair and any output data edge.

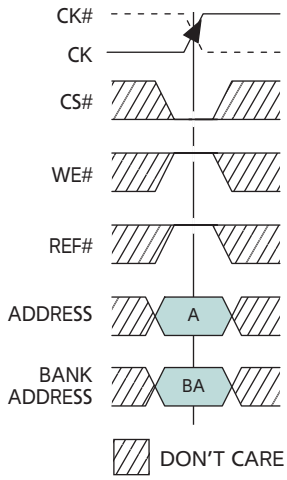
After completion of a burst, assuming no other commands have been initiated, output data (DQ) will go High-Z. The QVLD signal transitions LOW on the last bit of the READ burst. Note that if CK/CK# violates the VID(DC) specification while a READ burst is occurring, QVLD will remain HIGH until a dummy READ command is issued. The QK clocks are free-running and will continue to cycle after the read burst is complete. Back-to-back READ commands are possible, producing a continuous flow of output data.

The data valid window is derived from each QK transition and is defined as:

^{t}QHP - (^{t}QKQ [MAX] + |^{t}QKQ [MIN]|). See Figures 28–30 for illustration.

Any READ burst may be followed by a subsequent WRITE command. Figure 27 on page 50 illustrate the timing requirements for a READ followed by a WRITE. Some systems having long line lengths or severe skews may need additional idle cycles inserted between READ and WRITE commands to prevent data bus contention.

Figure 15: READ Command

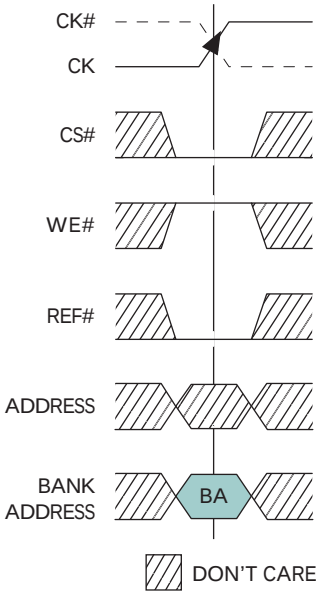


AUTO REFRESH (AREF)

AREF is used to perform a REFRESH cycle on one row in a specific bank. Because the row addresses are generated by an internal refresh counter for each bank, the external address balls are "Don't Care." The bank addresses must be provided during the AREF command. The bank address is needed during the AREF command so refreshing of the part can effectively be hidden behind commands to other banks. The delay between the AREF command and a subsequent command to the same bank must be at least ^{t}RC.

Within a period of 32ms (^{t}REF), the entire device must be refreshed. For the 288Mb device, the RLDRAM requires 64K cycles at an average periodic interval of 0.49µs MAX (actual periodic refresh interval is 32ms/8K rows/8 banks = 0.488µs). To improve efficiency, eight AREF commands (one for each bank) can be posted to the RLDRAM at periodic intervals of 3.9µs (32ms/8K rows = 3.90µs). Figure 31 on page 54 illustrates an example of a refresh sequence.

Figure 16: AUTO REFRESH Command



Operations

INITIALIZATION

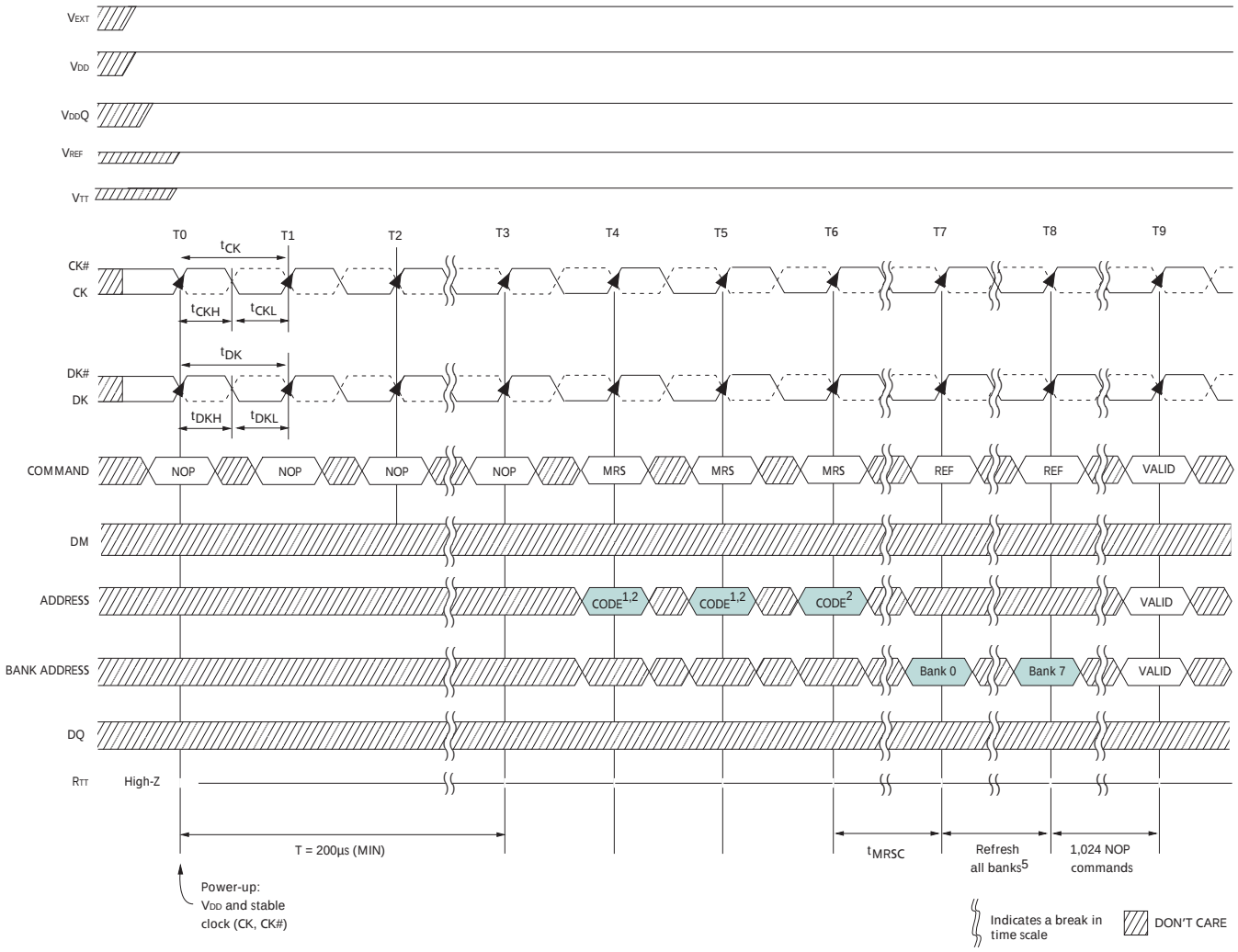
The RLDRAM must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operations or permanent damage to the device.

The following sequence is used for power-up:

1. Apply power (VEXT, VDD, VDDQ, VREF, VTT) and start clock as soon as the supply voltages are stable. Apply VDD and VEXT before or at the same time as VDDQ.[1] Apply VDDQ before or at the same time as VREF and VTT. Although there is no timing relation between VEXT and VDD, the chip starts the power-up sequence only after both voltages approach their nominal levels. CK/CK# must meet VID(DC) prior to being applied.[2] Apply NOP conditions to command pins. Ensuring CK/CK# meet VID(DC) while applying NOP conditions to the command pins guarantees that the RLDRAM will not receive unwanted commands during initialization.
2. Maintain stable conditions for 200µs (MIN).
3. Issue at least three consecutive MRS commands: two or more dummies plus one valid MRS. The purpose of these consecutive MRS commands is to internally reset the logic of the RLDRAM. Note that ^{t}MRSC does not need to be met between these consecutive commands. It is recommended that all address pins are held LOW during the dummy MRS commands.
4. ^{t}MRSC after the valid MRS, an AUTO REFRESH command to all 8 banks (along with 1,024 NOP commands) must be issued prior to normal operation. The sequence of the eight AUTO REFRESH commands (with respect to the 1,024 NOP commands) does not matter. As is required for any operation, ^{t}RC must be met between an AUTO REFRESH command and a subsequent VALID command to the same bank. Note that older versions of the data sheet required each of these AUTO REFRESH commands be separated by 2,048 NOP commands. This properly initializes the RLDRAM but is no longer required.

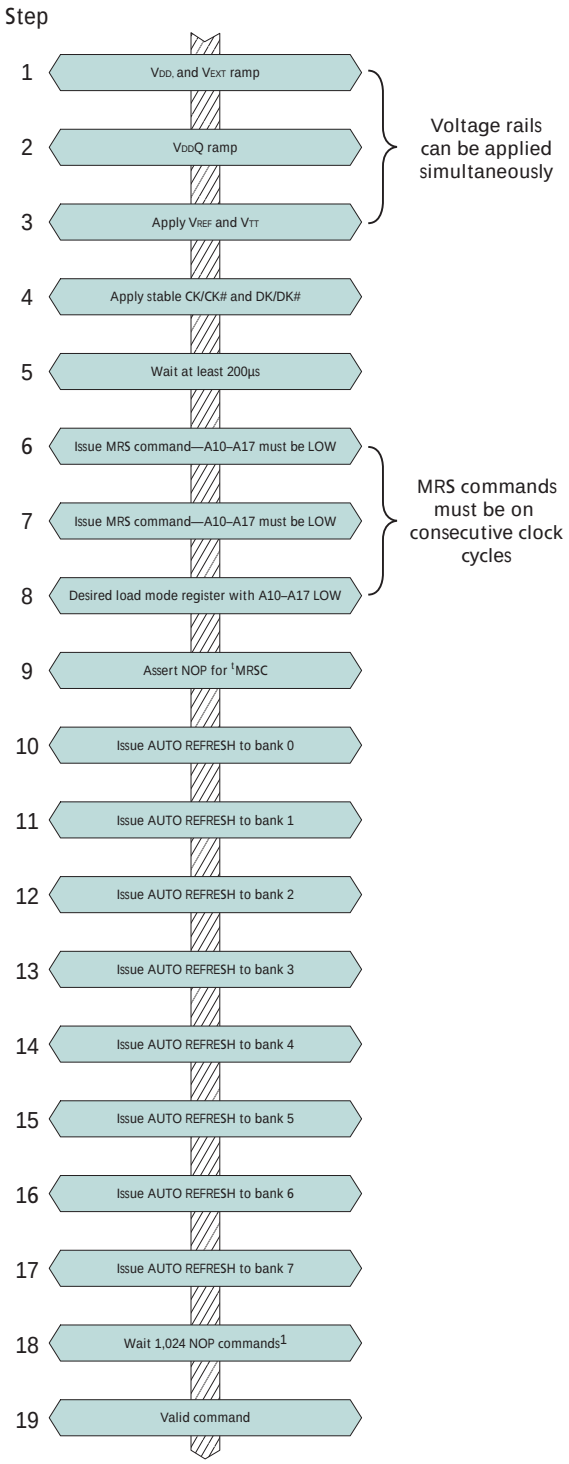
Notes:
1. It is possible to apply VDDQ before VDD. However, when doing this, the DQs, DM, and all other pins with an output driver, will go HIGH instead of tri-stating. These pins will remain HIGH until VDD is at the same level as VDDQ. Care should be taken to avoid bus conflicts during this period.
2. If VID(DC) on CK/CK# can not be met prior to being applied to the RLDRAM, placing a large external resistor from CS# to VDD is a viable option for ensuring the command bus does not receive unwanted commands during this unspecified state.

Figure 17: Power-Up/Initialization Sequence



Notes:
1. Recommend all address pins held LOW during dummy MRS commands.
2. A10–A17 must be LOW.
3. DLL must be reset if ^{t}CK or VDD are changed.
4. CK and CK# must be separated at all times to prevent bogus commands from being issued.
5. The sequence of the eight AUTO REFRESH commands (with respect to the 1,024 NOP commands) does not matter. As is required for any operation, ^{t}RC must be met between an AUTO REFRESH command and a subsequent VALID command to the same bank.

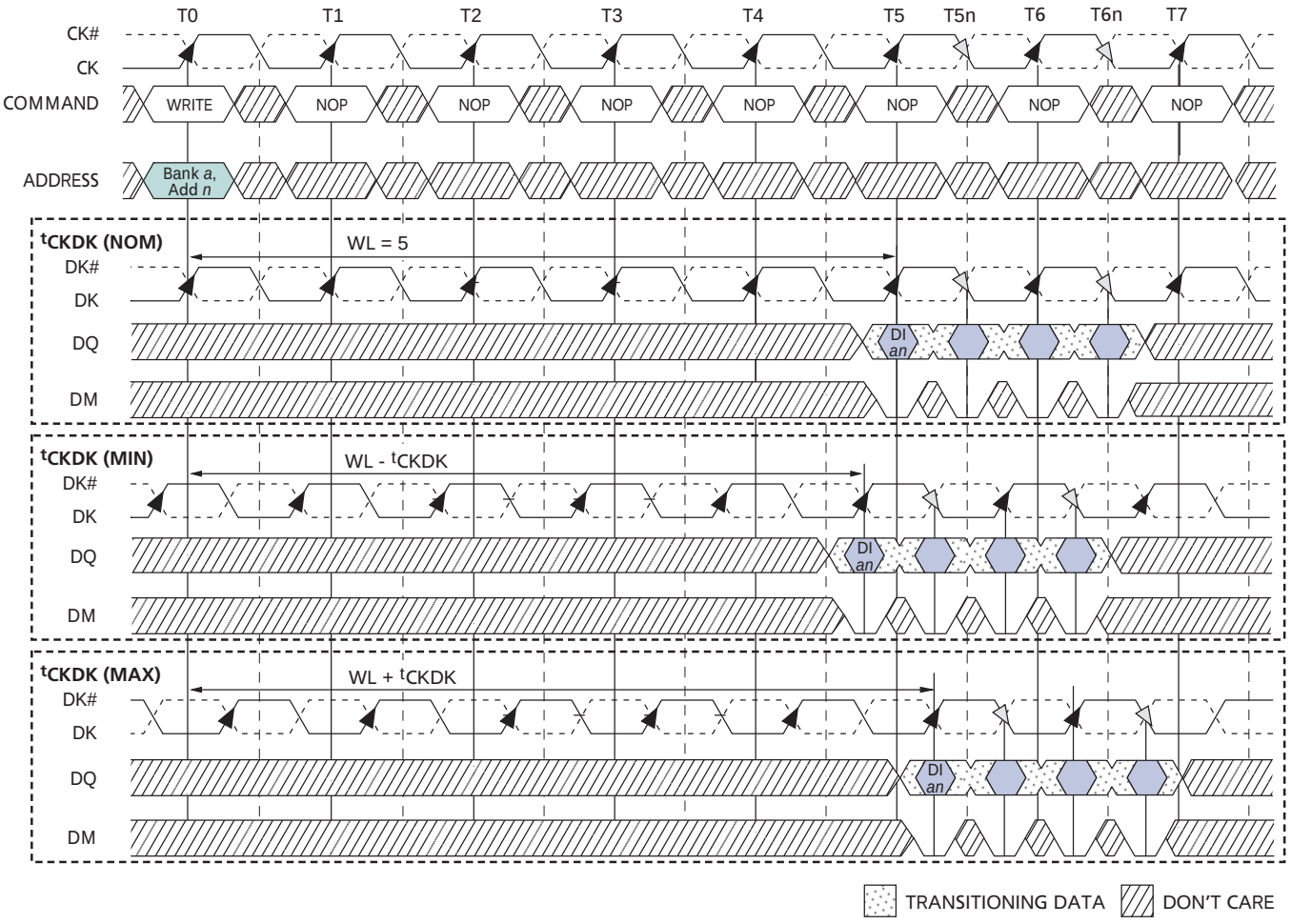
Figure 18: Power-Up/Initialization Flow Chart



Notes: 1. The sequence of the eight AUTO REFRESH commands (with respect to the 1,024 NOP commands) does not matter. As is required for any operation, ^{t}RC must be met between an AUTO REFRESH command and a subsequent VALID command to the same bank.

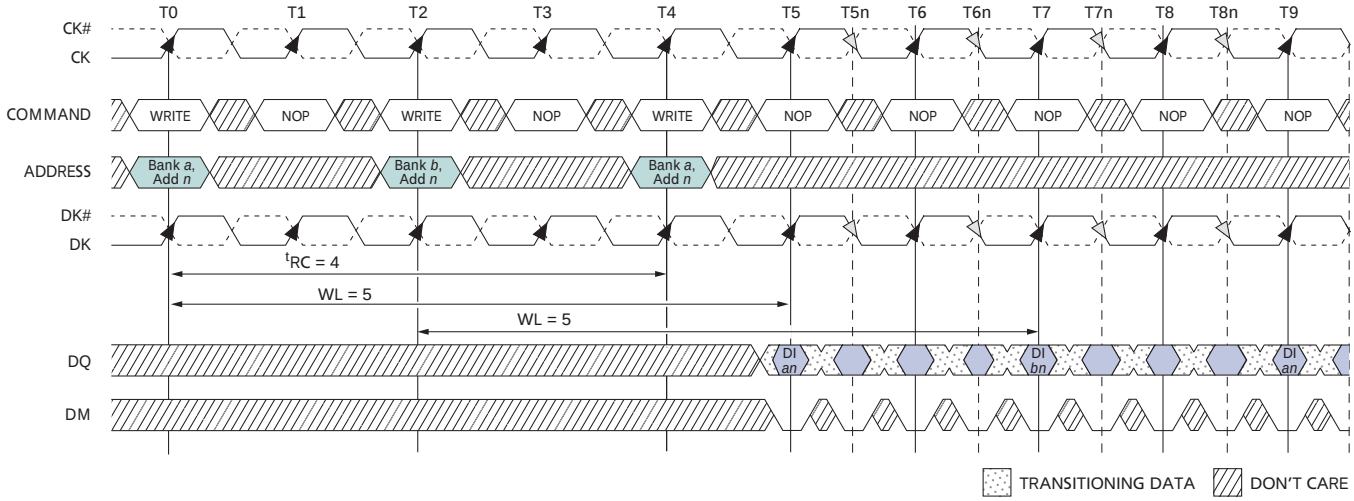
WRITE

Figure 19: WRITE Burst



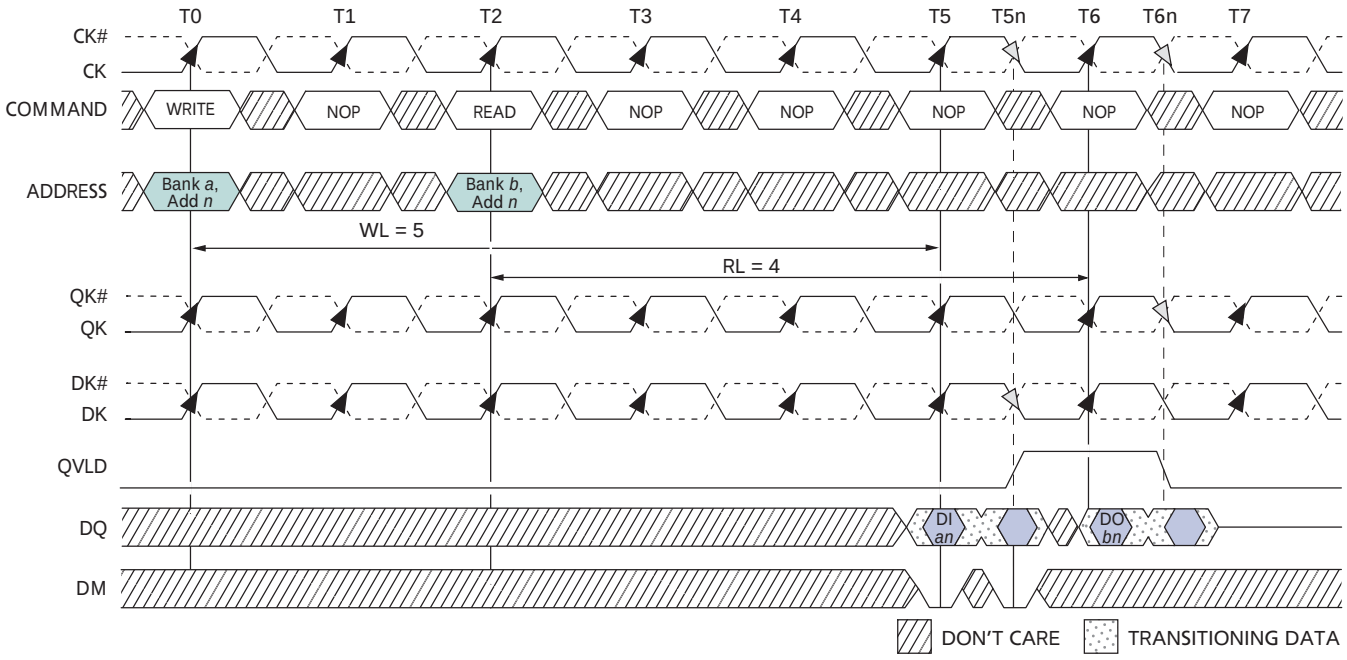
Notes: 1. DI *an* = data-in for bank *a* and address *n*; subsequent elements of burst are applied following DI *an*.
2. BL = 4.

Figure 20: Consecutive WRITE-to-WRITE



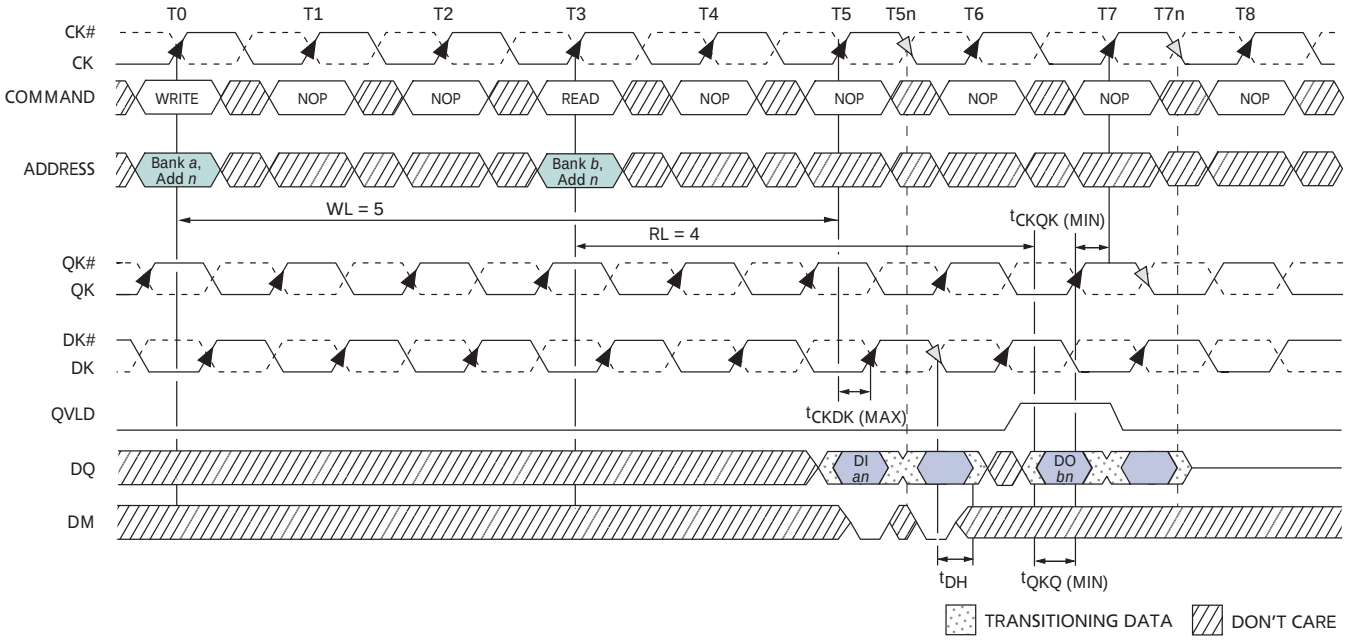
Notes:
1. DI *an* (or *bn)* = data-in for bank *a* (or *b*) and address *n*.
2. Three subsequent elements of the burst are applied following DI for each bank.
3. BL = 4.
4. Each WRITE command may be to any bank; if the second WRITE is to the same bank, ^{t}RC must be met.
5. Nominal conditions are assumed for specifications not defined.

Figure 21: WRITE-to-READ



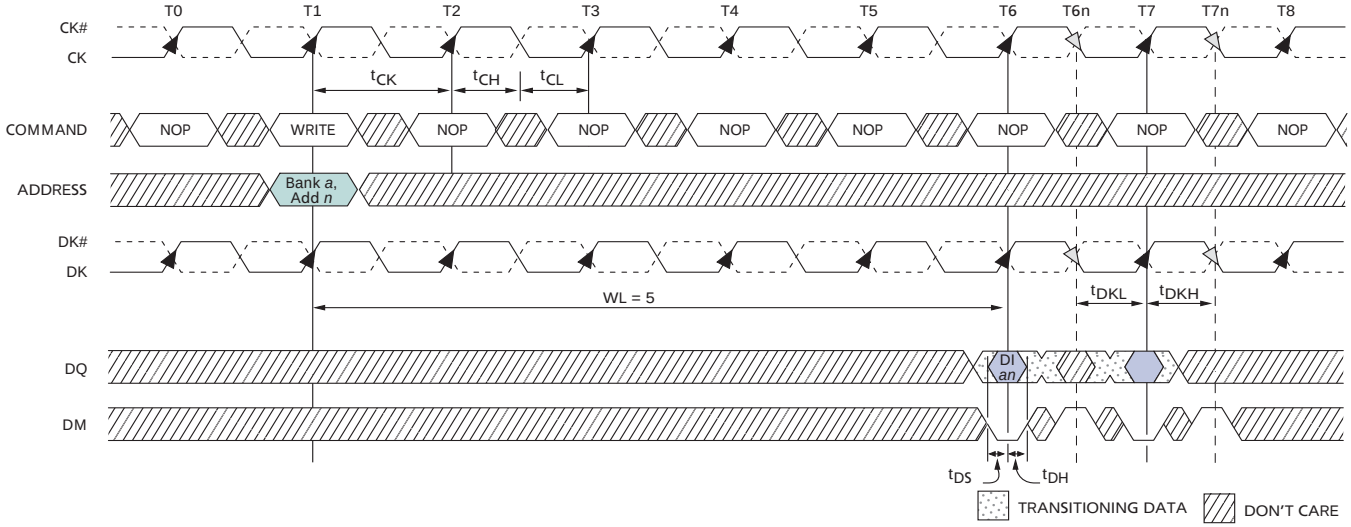
Notes:
1. DI *an* = data-in for bank *a* and address *n*.
2. DO *bn* = data-out from bank *b* and address *n*.
3. Two subsequent elements of each burst follow DI *an* and DO *bn*.
4. BL = 2.
5. Nominal conditions are assumed for specifications not defined.

Figure 22: WRITE-to-READ (Separated by Two NOPs)



Notes:
1. DI *an* = data-in for bank *a* and address *n*.
2. DO *bn* = data-out from bank *b* and address *n*.
3. One subsequent element of each burst follow both DI *an* and DO *bn*.
4. BL = 2.
5. Only one NOP separating the WRITE and READ would have led to contention on the data bus because of the input and output data timing conditions being used.
6. Nominal conditions are assumed for specifications not defined.

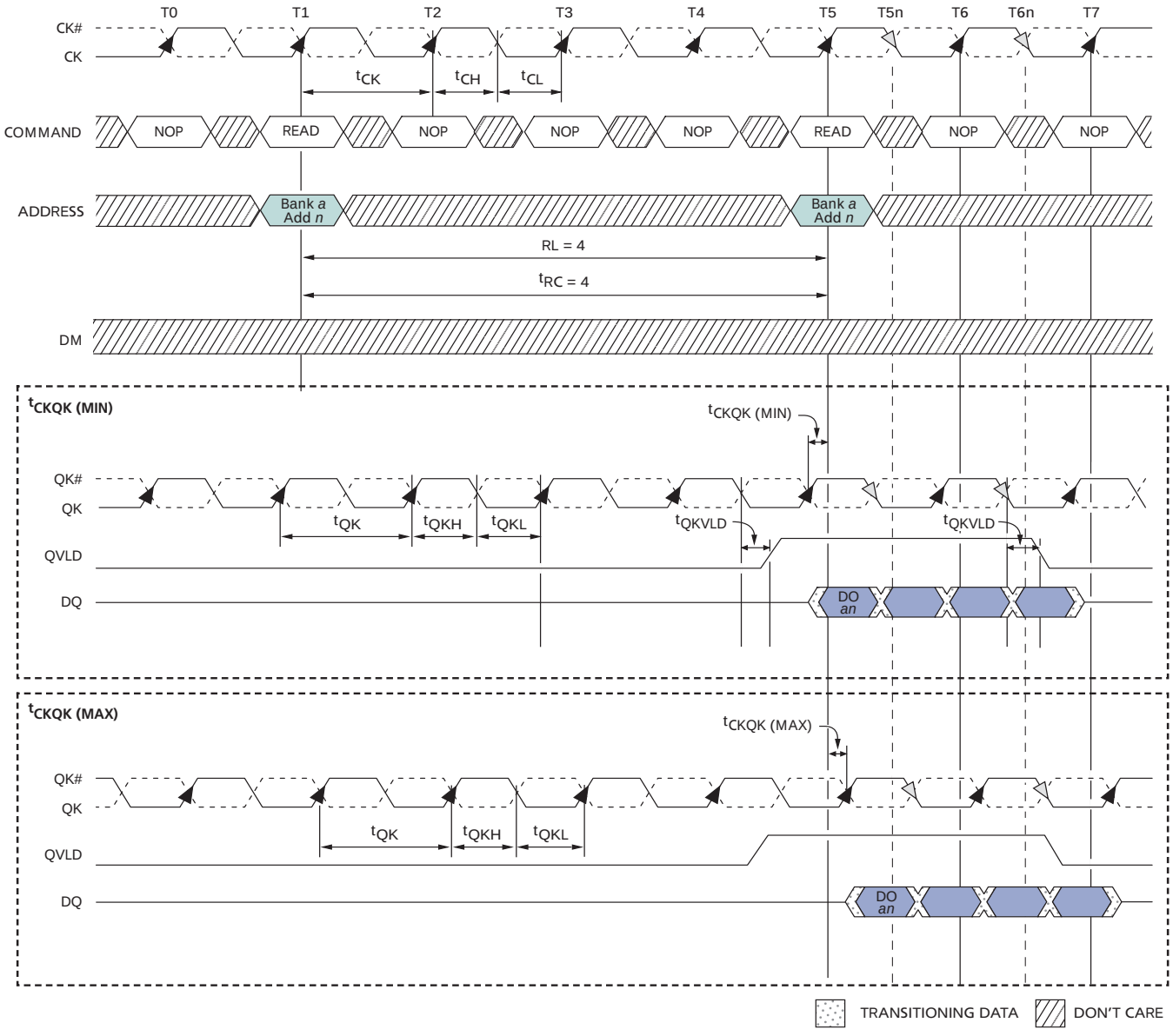
Figure 23: WRITE – DM Operation



Notes:
1. DI *an* = data-in for bank *a* and address *n*.
2. Subsequent elements of burst are provided on following clock edges.
3. BL = 4.
4. Nominal conditions are assumed for specifications not defined.

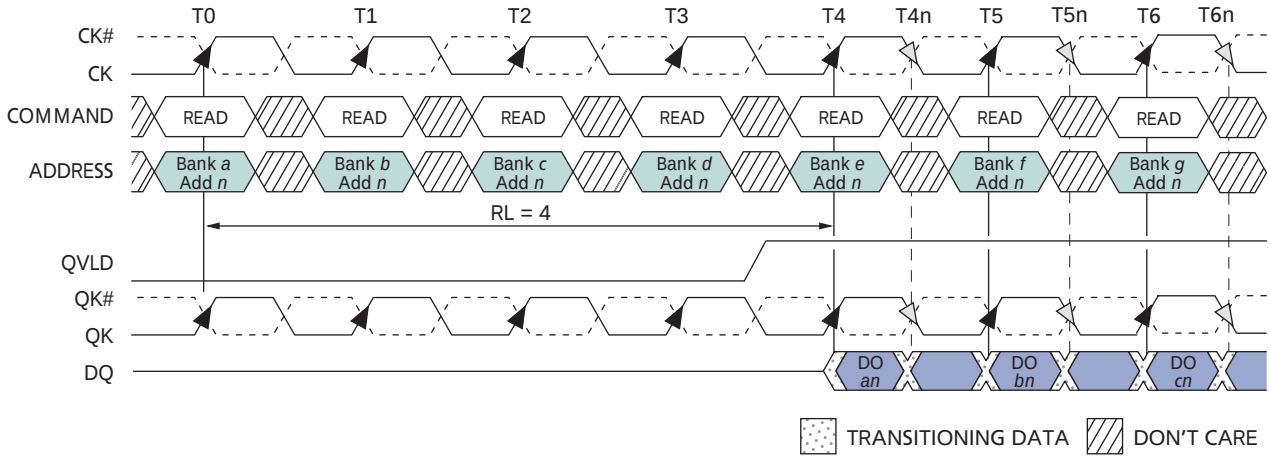
READ

Figure 24: Basic READ Burst Timing



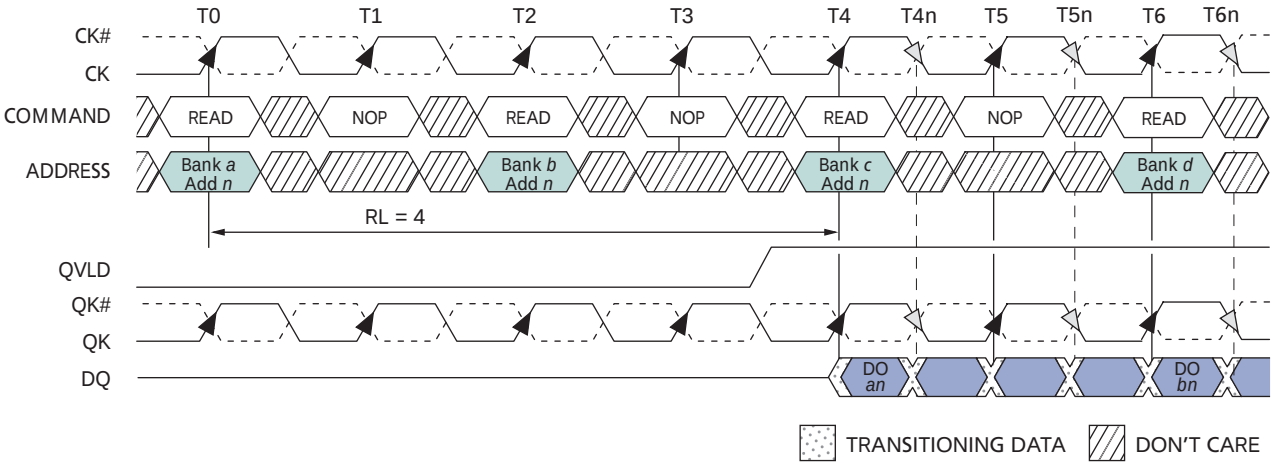
Notes:
1. DO *an* = data-out from bank *a* and address *an*.
2. Three subsequent elements of the burst are applied following DO *an*.
3. BL = 4.
4. Nominal conditions are assumed for specifications not defined.

Figure 25: Consecutive READ Bursts (BL = 2)



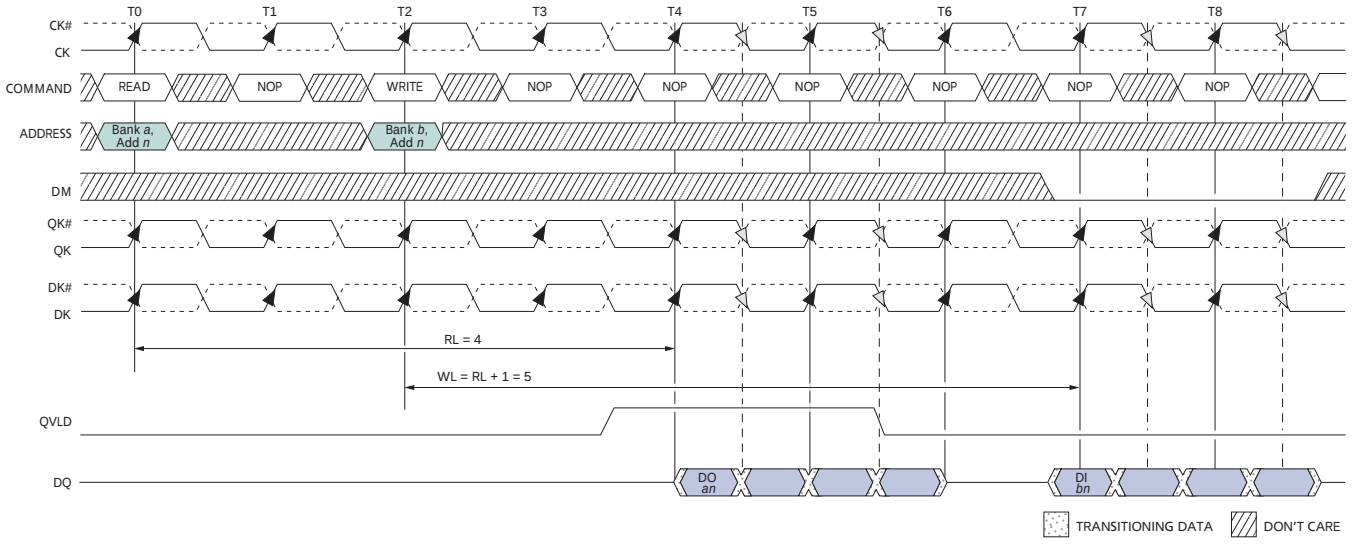
Notes:
1. DO *an* (or *bn* or *cn*) = data-out from bank *a* (or bank *b* or bank *c*) and address *n*.
2. One subsequent element of the burst from each bank appears after each DO *x*.
3. Nominal conditions are assumed for specifications not defined.
4. Example applies only when READ commands are issued to same device.
5. Bank address can be to any bank, but the subsequent READ can only be to the same bank if ^{t}RC has been met.
6. Data from the READ commands to bank *d* through bank *g* will appear on subsequent clock cycles that are not shown.

Figure 26: Consecutive READ Bursts (BL = 4)



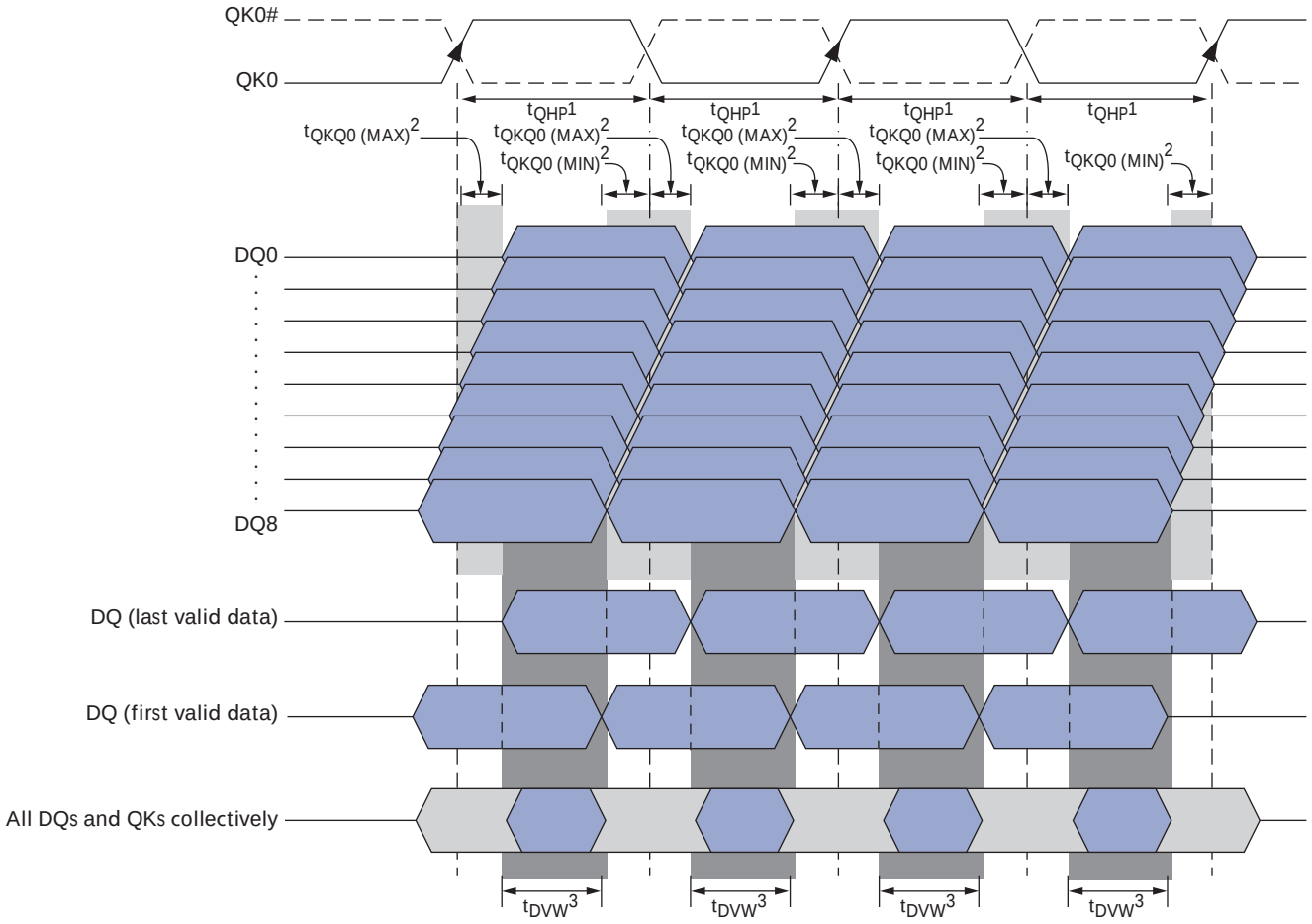
Notes:
1. DO *an* (or *bn*) = data-out from bank *a* (or bank *b*) and address *n*.
2. Three subsequent elements of the burst from each bank appears after each DO *x*.
3. Nominal conditions are assumed for specifications not defined.
4. Example applies only when READ commands are issued to same device.
5. Bank address can be to any bank, but the subsequent READ can only be to the same bank if ^{t}RC has been met.
6. Data from the READ commands to banks *c* and *d* will appear on subsequent clock cycles that are not shown.

Figure 27: READ-to-WRITE



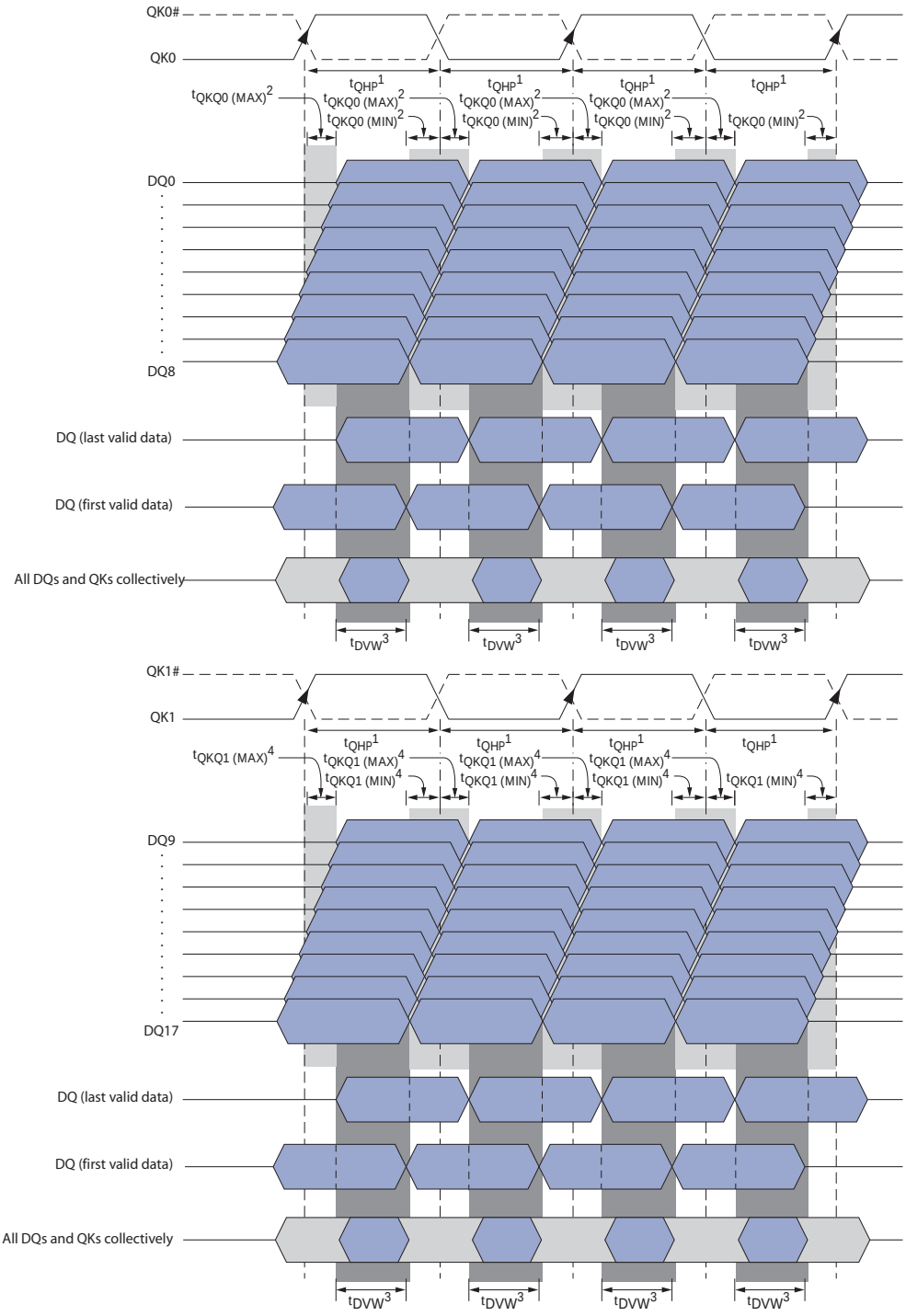
Notes:
1. DO *an* = data-out from bank *a* and address *n*.
2. DI *bn* = data-in for bank *b* and address *n*.
3. Three subsequent elements of each burst follow DI *bn* and each DO *an*.
4. BL = 4.
5. Nominal conditions are assumed for specifications not defined.

Figure 28: Read Data Valid Window for x9 Device



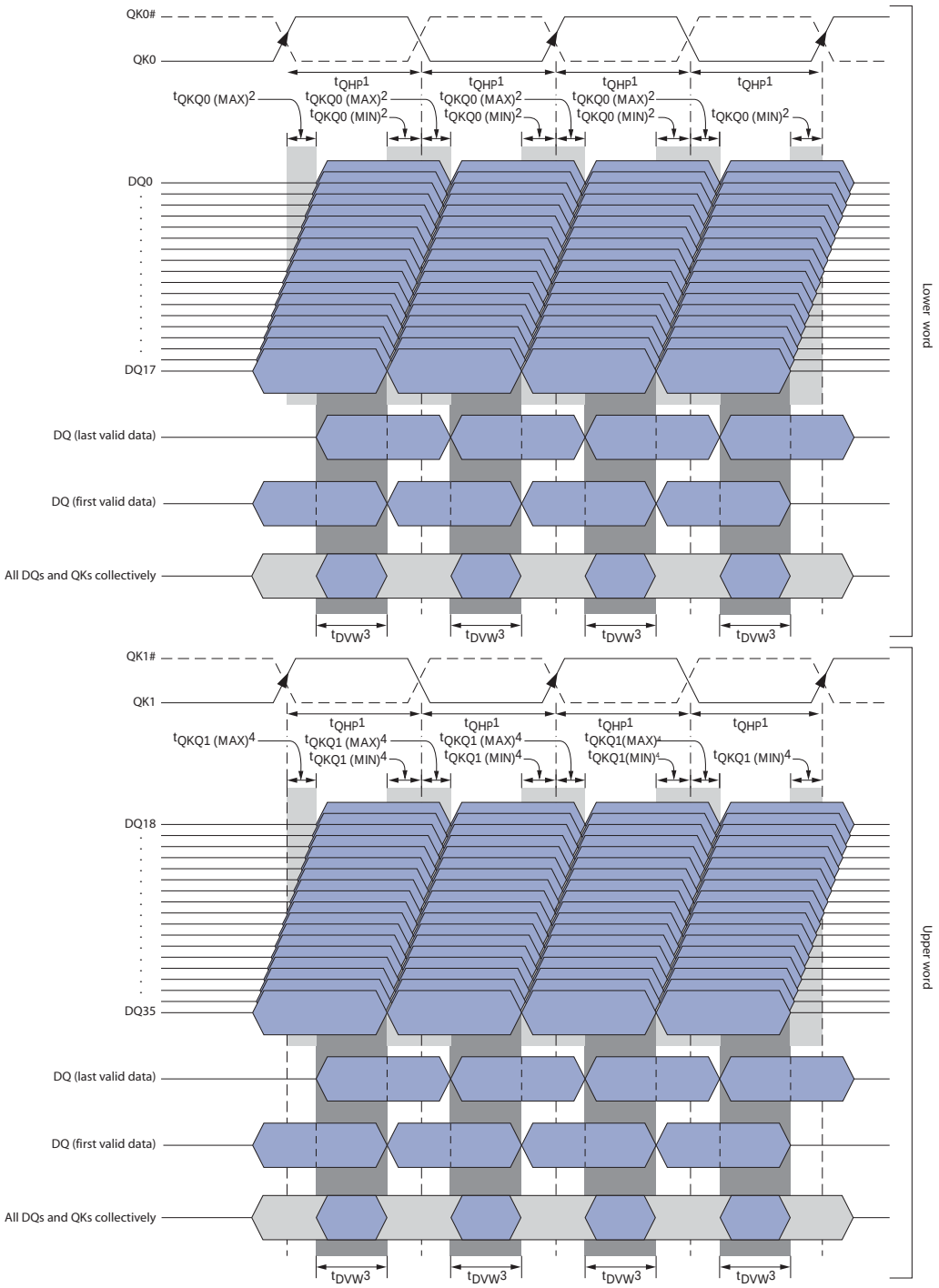
Notes:
1. ^{t}QHP is defined as the lesser of ^{t}QKH or ^{t}QKL.
2. ^{t}QKQ0 is referenced to DQ0–DQ8.
3. Minimum data valid window (^{t}DVW) can be expressed as ^{t}QHP - (^{t}QKQ*x* [MAX] + |^{t}QKQ*x* [MIN]|).

Figure 29: Read Data Valid Window for x18 Device



Notes:
1. tQHP is defined as the lesser of tQKH or tQKL.
2. tQKQ0 is referenced to DQ0–DQ8.
3. Minimum data valid window (tDVW) can be expressed as tQHP - (tQKQ*x* [MAX] + |tQKQ*x* [MIN]|).
4. tQKQ1 is referenced to DQ9–DQ17.
5. tQKQ takes into account the skew between any QK*x* and any DQ.

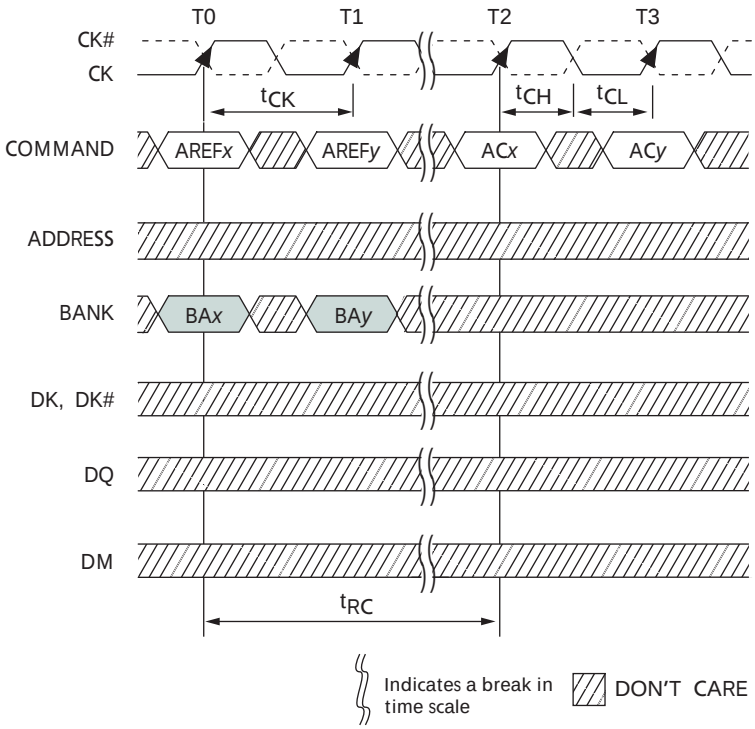
Figure 30: Read Data Valid Window for x36 Device



Notes:
1. tQHP is defined as the lesser of tQKH or tQKL.
2. tQKQ0 is referenced to DQ0–DQ17.
3. Minimum data valid window, tDVW, can be expressed as tQHP - (tQKQ*x* [MAX] + |tQKQ*x* [MIN]|).
4. tQKQ1 is referenced to DQ18–DQ35.
5. tQKQ takes into account the skew between any QK*x* and any DQ.

AUTO REFRESH

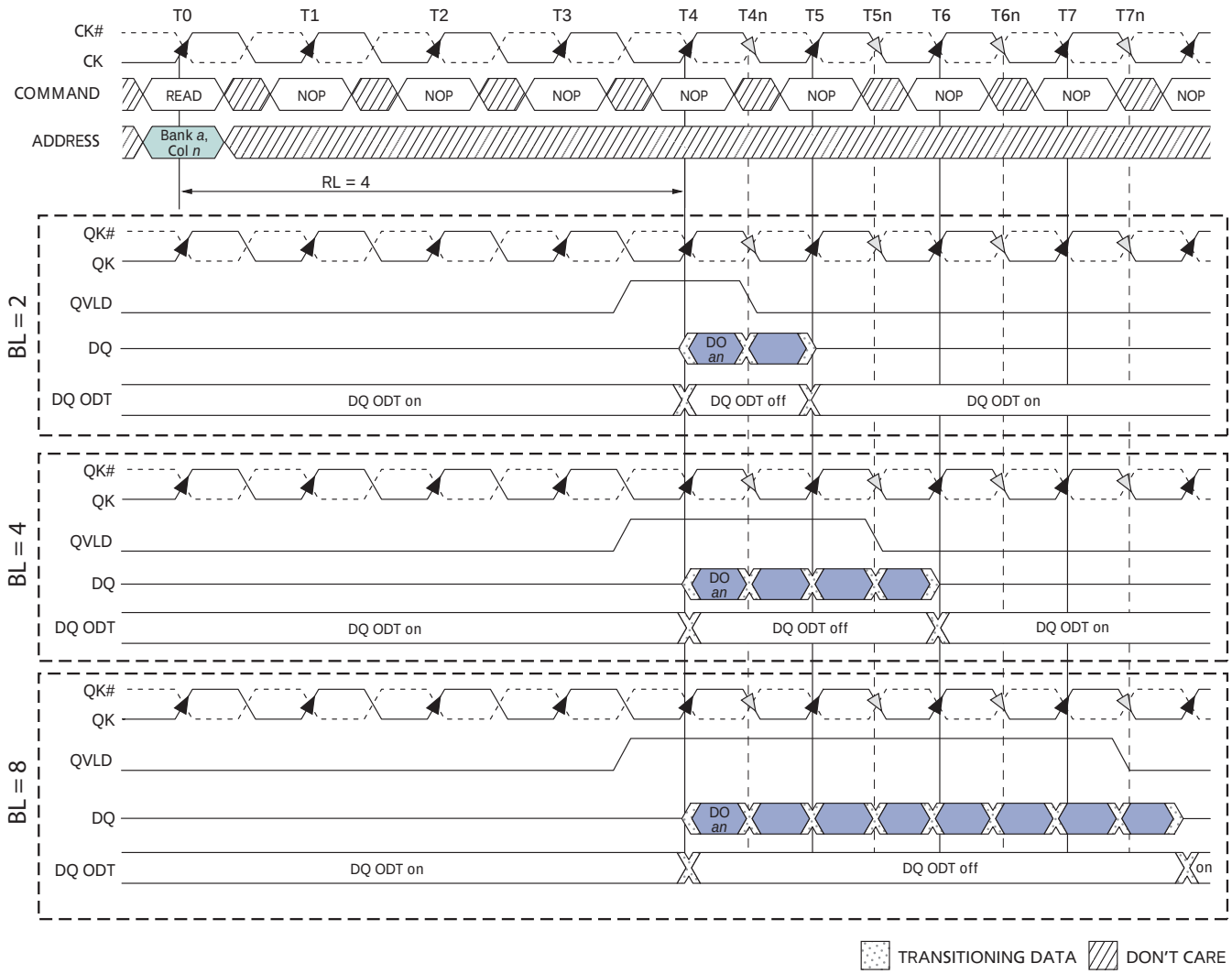
Figure 31: AUTO REFRESH Cycle



Notes:
1. AREF*x* = AUTO REFRESH command to bank *x*.
2. AC*x* = any command to bank *x*; AC*y* = any command to bank *y*.
3. BA*x* = bank address to bank *x*; BA*y* = bank address to bank *y*.

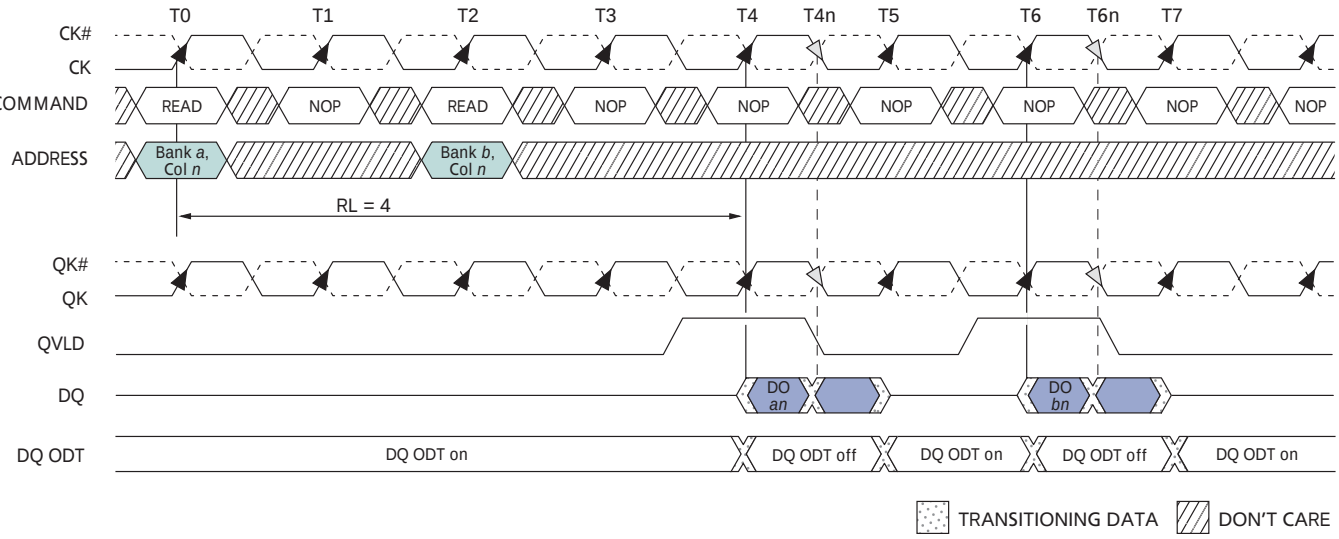
On-Die Termination

Figure 32: READ Burst with ODT



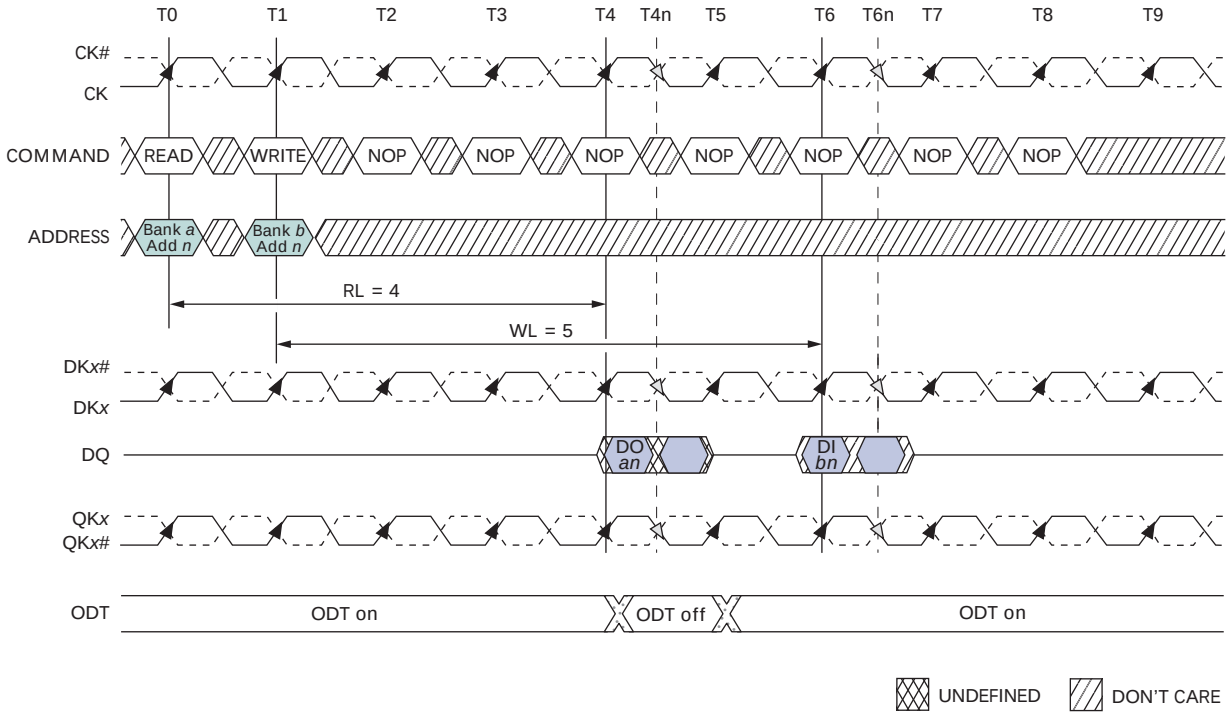
Notes:
1. DO *an* = data out from bank *a* and address *n*.
2. DO *an* is followed by the remaining bits of the burst.
3. Nominal conditions are assumed for specifications not defined.

Figure 33: READ-NOP-READ with ODT



Notes:
1. DO *an* (or *bn*) = data-out from bank *a* (or bank *b*) and address *n*.
2. BL = 2.
3. One subsequent element of the burst appear after DO *an* and DO *bn*.
4. Nominal conditions are assumed for specifications not defined.

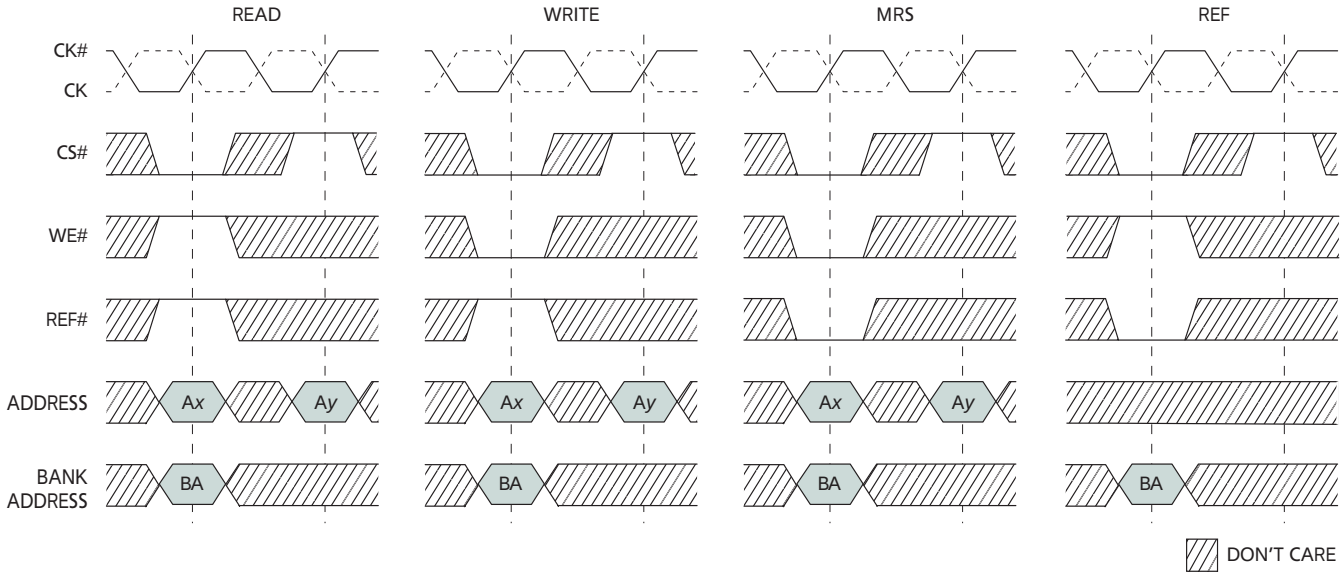
Figure 34: READ-to-WRITE with ODT



Notes:
1. DO *an* = data-out from bank *a* and address *n*; DI *bn* = data-in for bank *b* and address *n*.
2. BL = 2.
3. One subsequent element of each burst appears after each DO *an* and DI *bn*.
4. Nominal conditions are assumed for specifications not defined.

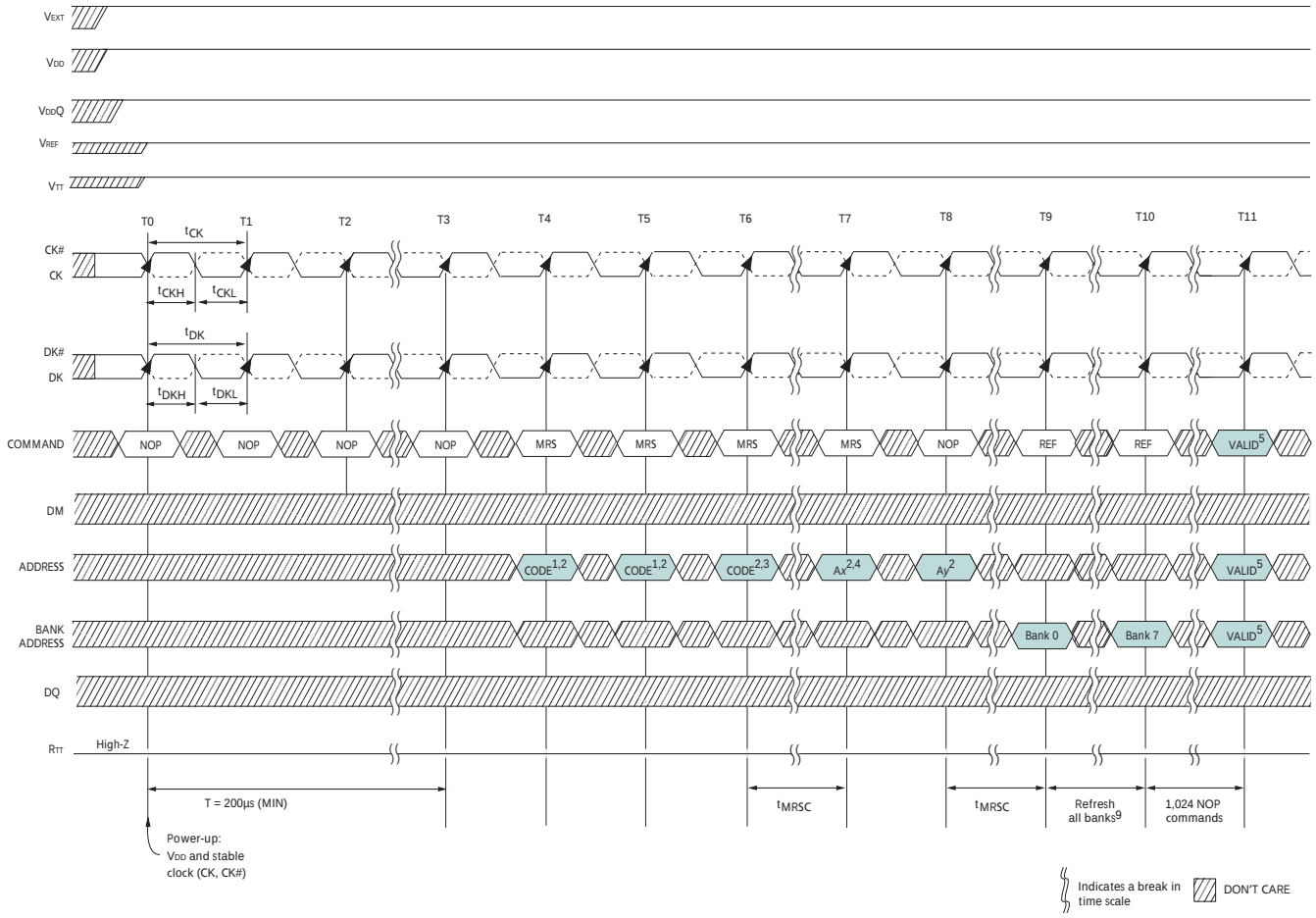
Multiplexed Address Mode

Figure 35: Command Description in Multiplexed Address Mode



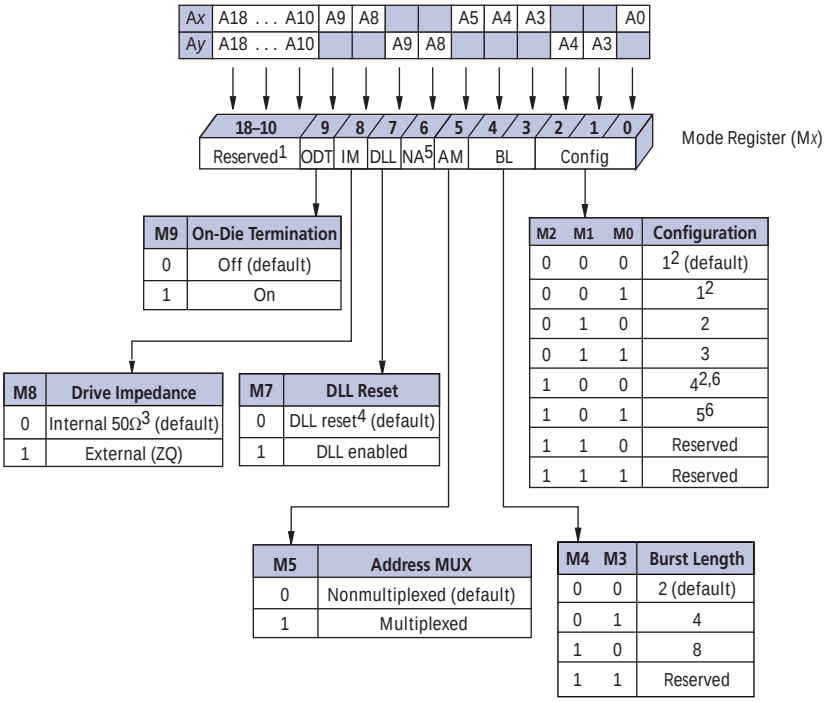
Notes: 1. The minimum setup and hold times of the two address parts are defined ^{t}AS and ^{t}AH.

Figure 36: Power-Up/Initialization Sequence in Multiplexed Address Mode



Notes:
1. Recommended that all address pins held LOW during dummy MRS commands.
2. A10–A18 must be LOW.
3. Set address A5 HIGH. This enbles the part to enter multiplexed address mode when in non-multiplexed mode operation. Multiplexed address mode can also be entered at some later time by issuing an MRS command with A5 HIGH. Once address bit A5 is set HIGH, ^{t}MRSC must be satisfied before the two-cycle multiplexed mode MRS command is issued.
4. Address A5 must be set HIGH. This and the following step set the desired mode register once the RLDRAM is in multiplexed address mode.
5. Any command or address.
6. The above sequence must be followed in order to power up the RLDRAM in the multiplexed address mode.
7. DLL must be reset if ^{t}CK or VDD are changed.
8. CK and CK# must separated at all times to prevent bogus commands from being issued.
9. The sequence of the eight AUTO REFRESH commands (with respect to the 1,024 NOP commands) does not matter. As is required for any operation, ^{t}RC must be met between an AUTO REFRESH command and a subsequent VALID command to the same bank.

Figure 37: Mode Register Definition in Multiplexed Address Mode



Notes:
1. Bits A10–A18 must be set to zero.
2. BL = 8 is not available.
3. ±30 percent temperature variation.
4. DLL RESET turns the DLL off.
5. Ay8 not used in MRS.
6. Available only in 576Mb device.
7. BA0–BA2 are "Don't Care."
8. Addresses A0, A3, A4, A5, A8, and A9 must be set as shown in order to activate the mode register in the multiplexed address mode.

Address Mapping in Multiplexed Address Mode

Table 21: 288Mb Address Mapping in Multiplexed Address Mode

Data Width	Burst Length	Ball	Address										
			A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
x36	2	A*x*	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		A*y*	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
	4	A*x*	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	X
		A*y*	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
x18	2	A*x*	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		A*y*	X	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	4	A*x*	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		A*y*	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
	8	A*x*	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	X
		A*y*	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
x9	2	A*x*	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		A*y*	A20	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	4	A*x*	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		A*y*	X	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	8	A*x*	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		A*y*	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15

Notes: 1. X = “Don’t Care.”

Configuration Tables in Multiplexed Address Mode

In multiplexed address mode, the read and write latencies are increased by one clock cycle. However, the RLDRAM cycle time remains the same as when in non-multiplexed address mode.

Table 22: Cycle Time and READ/WRITE Latency Configuration Table in Multiplexed Mode

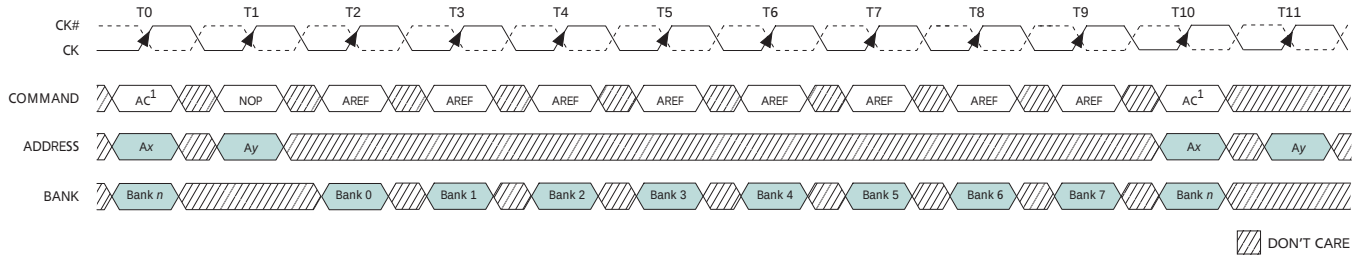
Parameter	Configuration			Units
	1[1]	2	3	
^{t}RC	4	6	8	^{t}CK
^{t}RL	5	7	9	^{t}CK
^{t}WL	6	8	10	^{t}CK
Valid frequency range	200–175	300–175	400–175	MHz

Notes: 1. BL = 8 is not available.

REFRESH Command in Multiplexed Address Mode

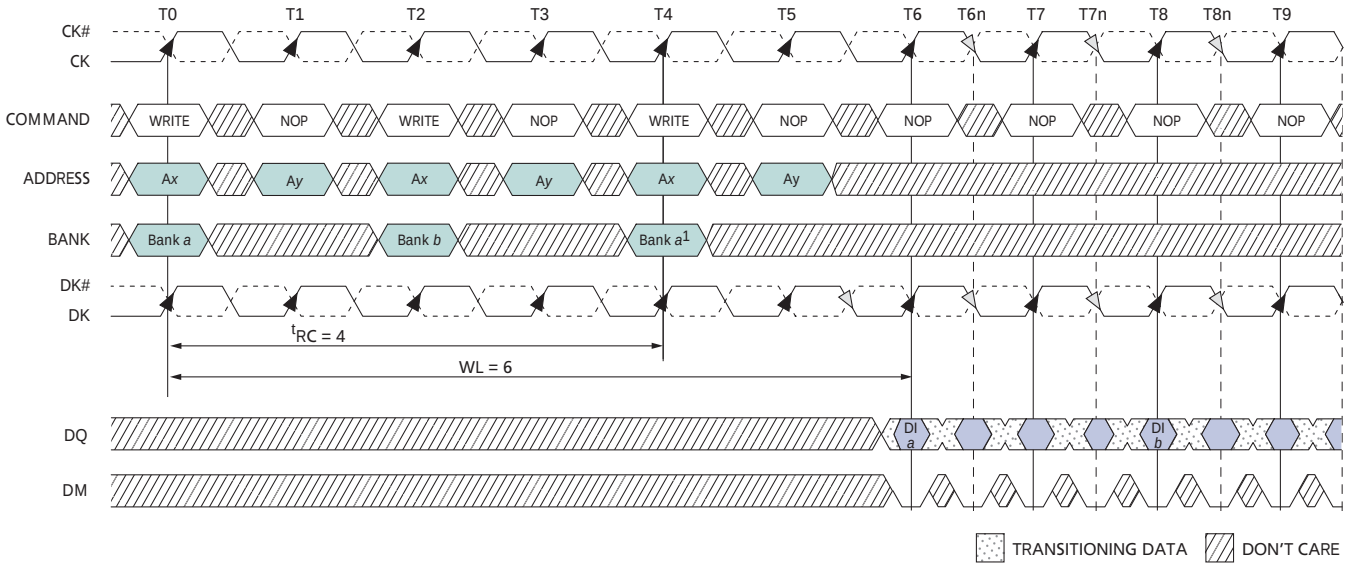
Similar to other commands when in multiplexed address mode, AREF is executed on the rising clock edge following the one on which the command is issued. However, since only the bank address is required for AREF, the next command can be applied on the following clock. The operation of the AREF command and any other command is represented in Figure 38 on page 61.

Figure 38: BURST REFRESH Operation with Multiplexed Addressing



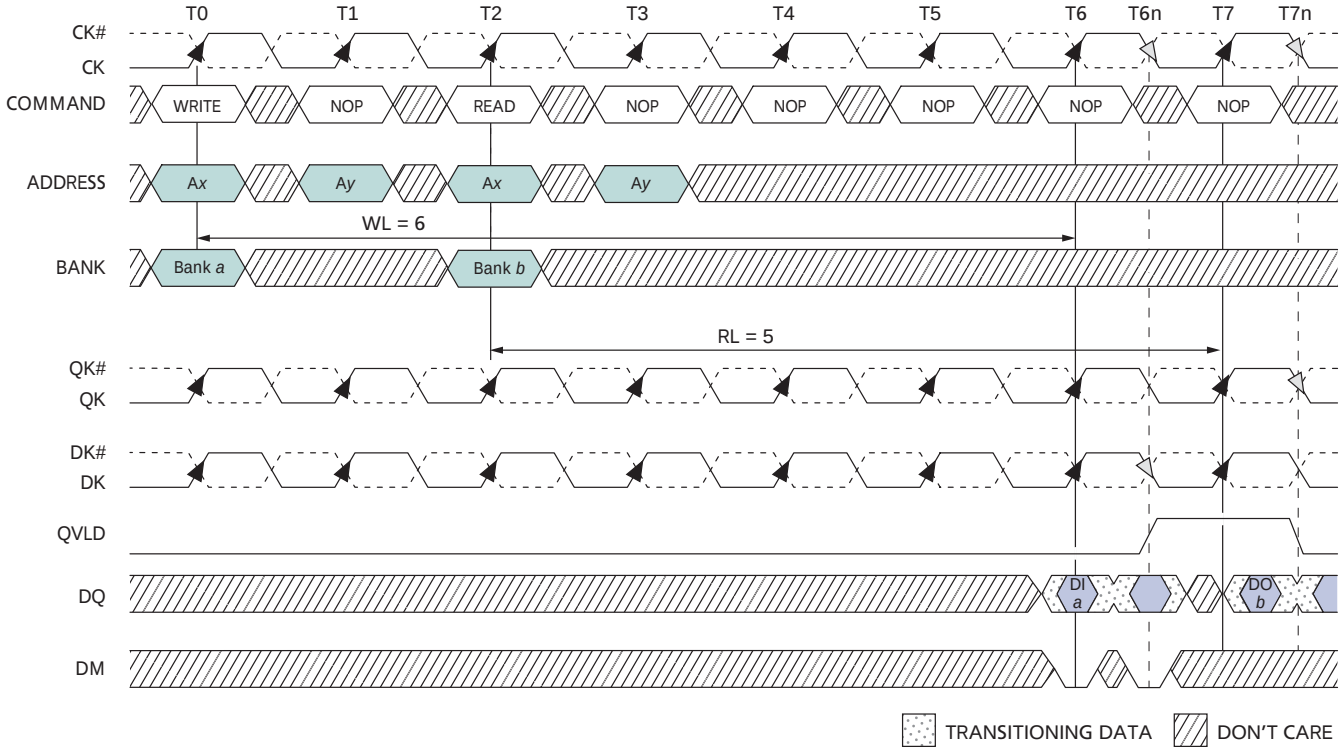
Notes: 1. Any command.
2. Bank *n* is chosen so that ^{t}RC is met.

Figure 39: Consecutive WRITE Bursts with Multiplexed Addressing



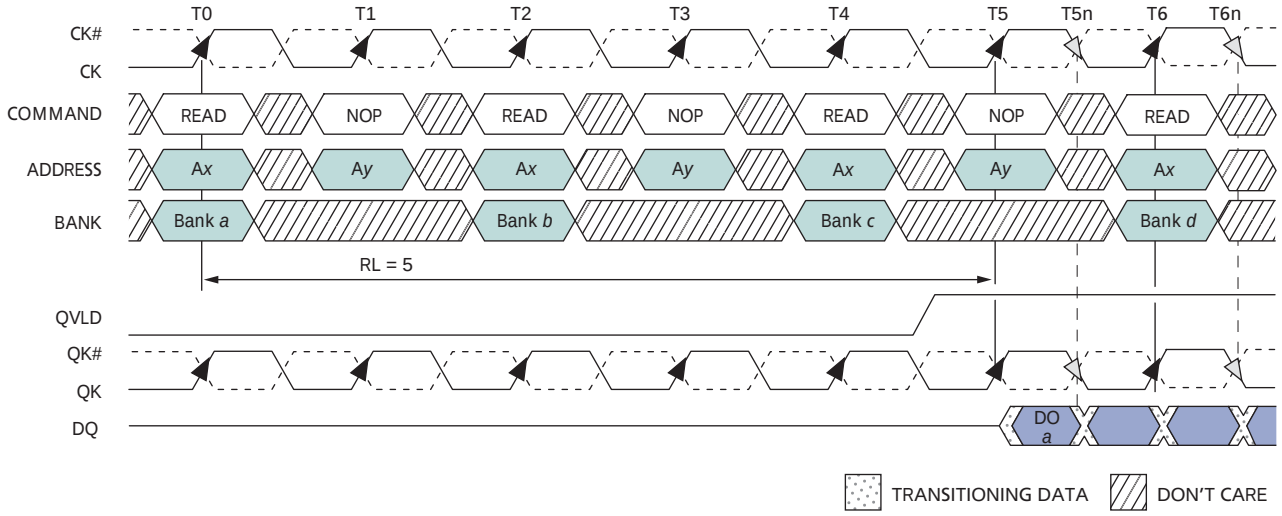
Notes:
1. Data from the second WRITE command to bank *a* will appear on subsequent clock cycles that are not shown.
2. DI *a* = data-in for bank *a*; DI *b* = data-in for bank *b*.
3. Three subsequent elements of the burst are applied following DI for each bank.
4. Each WRITE command may be to any bank; if the second WRITE is to the same bank, ^{t}RC must be met.

Figure 40: WRITE-to-READ with Multiplexed Addressing



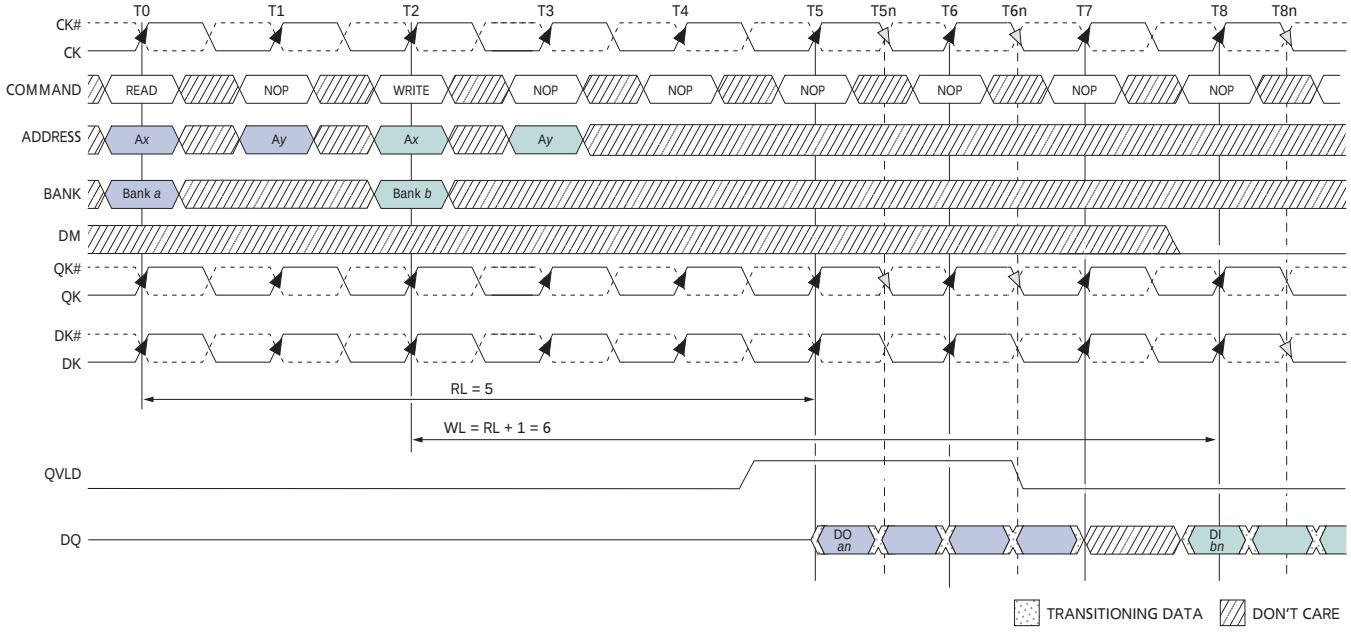
Notes:
1. DI *a* = data-in for bank *a*.
2. DO *b* = data-out from bank *b*.
3. One subsequent element of each burst follows DI *a* and DO *b*.
4. BL = 2.
5. Nominal conditions are assumed for specifications not defined.
6. Bank address can be to any bank, but the subsequent READ can only be to the same bank if ^{t}RC has been met.

Figure 41: Consecutive READ Bursts with Multiplexed Addressing



Notes:
1. DO *a* = data-out from bank *a*.
2. Nominal conditions are assumed for specifications not defined.
3. BL = 4.
4. Three subsequent elements of the burst appear following DO *a*.
5. Example applies only when READ commands are issued to same device.
6. Bank address can be to any bank, but the subsequent READ can only be to the same bank if ^{t}RC has been met.
7. Data from the READ commands to banks *b* through bank *d* will appear on subsequent clock cycles that are not shown.

Figure 42: READ-to-WRITE with Multiplexed Addressing



Notes:
1. DO *an* = data-out from bank *a*.
2. DI *bn* = data-in for bank *b*.
3. Nominal conditions are assumed for specifications not defined.
4. BL = 4.
5. Three subsequent elements of the burst are applied following DO *an*.
6. Three subsequent elements of the burst which appear following DI *bn* are not all shown.
7. Bank address can be to any bank, but the WRITE command can only be to the same bank if ^{t}RC has been met.

IEEE 1149.1 Serial Boundary Scan (JTAG)

RLDRAM incorporates a serial boundary-scan test access port (TAP) for the purpose of testing the connectivity of the device once it has been mounted on a printed circuit board (PCB). As the complexity of PCB high-density surface mounting techniques increases, the boundary-scan architecture is a valuable resource for interconnectivity debug. This port operates in accordance with IEEE Standard 1149.1-2001 (JTAG) with the exception of the ZQ pin. To ensure proper boundary-scan testing of the ZQ pin, MRS bit M8 needs to be set to 0 until the JTAG testing of the pin is complete. Note that upon power up, the default state of MRS bit M8 is low.

The input signals of the test access port (TDI, TMS, and TCK) use VDD as a supply, while the output signal of the TAP (TDO) uses VDDQ.

The JTAG test access port utilizes the TAP controller on the RLDRAM, from which the instruction register, boundary scan register, bypass register, and ID register can be selected. Each of these functions of the TAP controller is described in detail below.

Disabling the JTAG Feature

It is possible to operate RLDRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (VSS) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to VDD through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state, which will not interfere with the operation of the device.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK.

All of the states in Figure 43: “TAP Controller State Diagram,” on page 68 are entered through the serial input of the TMS pin. A “0” in the diagram represents a LOW on the TMS pin during the rising edge of TCK while a “1” represents a HIGH on TMS.

Test Data-In (TDI)

The TDI ball is used to serially input test instructions and data into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see Figure 43 on page 68. TDI is connected to the most significant bit (MSB) of any register (see Figure 44 on page 68).

Test Data-Out (TDO)

The TDO output ball is used to serially clock test instructions and data out from the registers. The TDO output driver is only active during the Shift-IR and Shift-DR TAP controller states. In all other states, the TDO pin is in a High-Z state. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register (see Figure 44 on page 68).

TAP Controller

The TAP controller is a finite state machine that uses the state of the TMS pin at the rising edge of TCK to navigate through its various modes of operation. The TAP controller state diagram can be seen in Figure 43 on page 68. Each state is described in detail below.

Test-Logic-Reset

The test-logic-reset controller state is entered when TMS is held HIGH for at least five consecutive rising edges of TCK. As long as TMS remains HIGH, the TAP controller will remain in the test-logic-reset state. The test logic is inactive during this state.

Run-Test/Idle

The run-test/idle is a controller state in between scan operations. This state can be maintained by holding TMS LOW. From here either the data register scan, or subsequently, the instruction register scan can be selected.

Select-DR-Scan

Select-DR-scan is a temporary controller state. All test data registers retain their previous state while here.

Capture-DR

The capture-DR state is where the data is parallel-loaded into the test data registers. If the boundary scan register is the currently selected register, then the data currently on the pins is latched into the test data registers.

Shift-DR

Data is shifted serially through the data register while in this state. As new data is input through the TDI pin, data is shifted out of the TDO pin.

Exit1-DR, Pause-DR, and Exit2-DR

The purpose of exit1-DR is used to provide a path to return back to the run-test/idle state (through the update-DR state). The pause-DR state is entered when the shifting of data through the test registers needs to be suspended. When shifting is to reconvene, the controller enters the exit2-DR state and then can re-enter the shift-DR state.

Update-DR

When the EXTEST instruction is selected, there are latched parallel outputs of the boundary-scan shift register that only change state during the update-DR controller state.

Instruction Register States

The instruction register states of the TAP controller are similar to the data register states. The desired instruction is serially shifted into the instruction register during the shift-IR state and is loaded during the update-IR state.

Figure 43: TAP Controller State Diagram

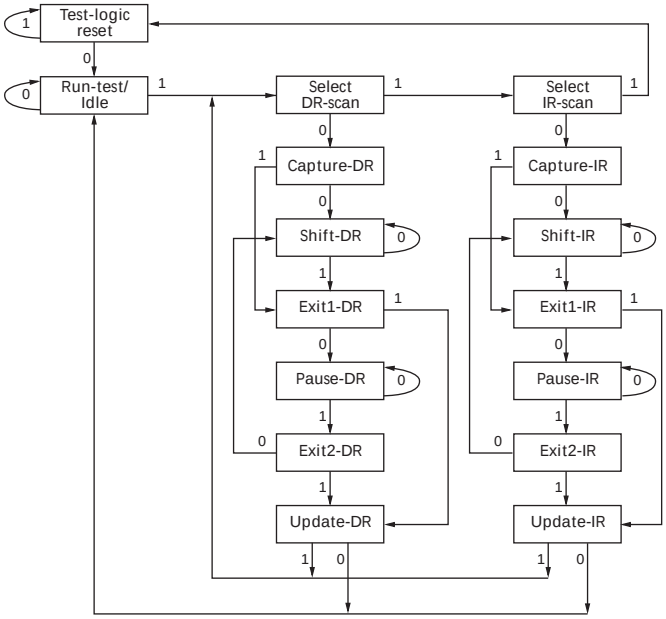
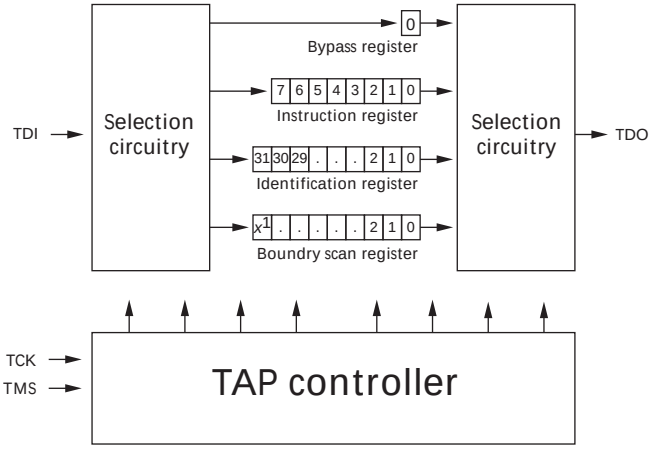


Figure 44: TAP Controller Block Diagram



Notes: 1. *x* = 112 for all configurations.

Performing a TAP RESET

A reset is performed by forcing TMS HIGH (VDDQ) for five rising edges of TCK. This RESET does not affect the operation of the RLDRAM and may be performed while the RLDRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the RLDRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Eight-bit instructions can be serially loaded into the instruction register. This register is loaded during the update-IR state of the TAP controller. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the capture-IR state, the two LSBs are loaded with a binary "01" pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the RLDRAM with minimal delay. The bypass register is set LOW (VSS) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the RLDRAM. Several balls are also included in the scan register to reserved balls. The RLDRAM has a 113-bit register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the shift-DR state.

Table 29 on page 74 shows the order in which the bits are connected. Each bit corresponds to one of the balls on the RLDRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the RLDRAM and can be shifted out when the TAP controller is in the shift-DR state. The ID register has a vendor code and other information described in Table 26 on page 73.

TAP Instruction Set

Overview

Many different instructions (2^8) are possible with the 8-bit instruction register. All combinations used are listed in Table 28 on page 74. These six instructions are described in detail below. The remaining instructions are reserved and should not be used.

The TAP controller used in this RLDRAM is fully compliant to the 1149.1 convention.

Instructions are loaded into the TAP controller during the shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the update-IR state.

EXTEST

The EXTEST instruction allows circuitry external to the component package to be tested. Boundary-scan register cells at output balls are used to apply a test vector, while those at input balls capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the update-IR state of EXTEST, the output driver is turned on, and the PRELOAD data is driven onto the output balls.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

High-Z

The High-Z instruction causes the boundary scan register to be connected between the TDI and TDO. This places all RLDRAM outputs into a High-Z state.

CLAMP

When the CLAMP instruction is loaded into the instruction register, the data driven by the output balls are determined from the values held in the boundary scan register.

SAMPLE/PRELOAD

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the capture-DR state, a snapshot of data on the inputs and bidirectional balls is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 50 MHz, while the RLDRAM clock operates significantly faster. Because there is a large difference between the clock frequencies, it is possible that during the capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To ensure that the boundary scan register will capture the correct value of a signal, the RLDRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (^tCS plus ^tCH). The RLDRAM clock input might not be captured

correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the shift-DR state. This places the boundary scan register between the TDI and TDO balls.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved for Future Use

The remaining instructions are not implemented but are reserved for future use. Do not use these instructions.

Figure 45: JTAG Operation – Loading Instruction Code and Shifting Out Data

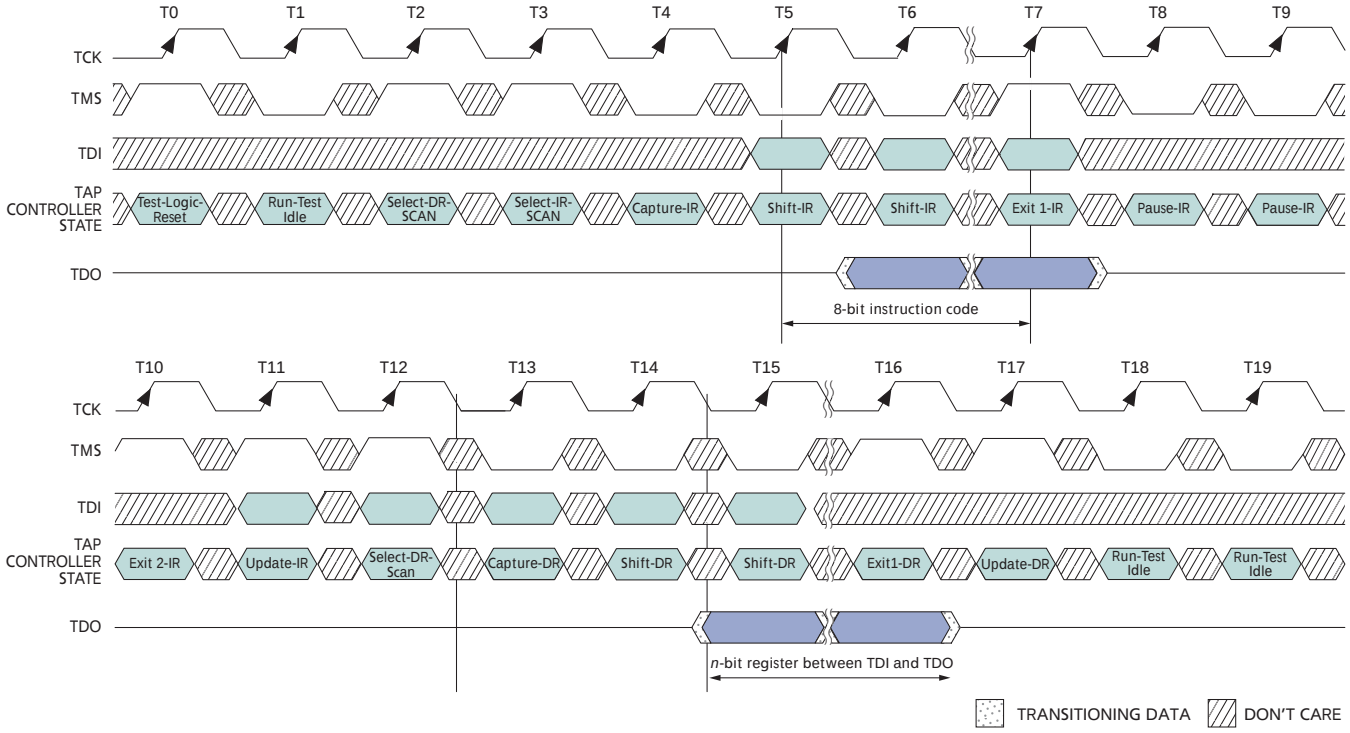


Figure 46: TAP Timing

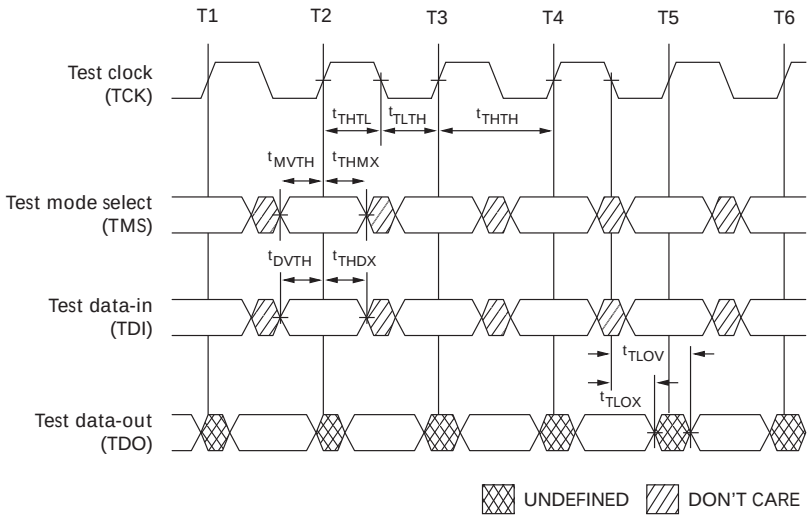


Table 23: TAP Input AC Logic Levels

+0°C ≤ T_C ≤ +95°C; +1.7V ≤ V_{DD} ≤ +1.9V, unless otherwise noted

Description	Symbol	Min	Max	Units
Input high (logic 1) voltage	V_{IH}	V_{REF} + 0.3	–	V
Input low (logic 0) voltage	V_{IL}	–	V_{REF} - 0.3	V

Notes: 1. All voltages referenced to V_{SS} (GND).

Table 24: TAP AC Electrical Characteristics

+0°C ≤ T_C ≤ +95°C; +1.7V ≤ V_{DD} ≤ +1.9V

Description	Symbol	Min	Max	Units
Clock				
Clock cycle time	^{t}THTH	20		ns
Clock frequency	^{f}TF		50	MHz
Clock HIGH time	^{t}THTL	10		ns
Clock LOW time	^{t}TLTH	10		ns
TDI/TDO times				
TCK LOW to TDO unknown	^{t}TLOX	0		ns
TCK LOW to TDO valid	^{t}TLOV		10	ns
TDI valid to TCK HIGH	^{t}DVTH	5		ns
TCK HIGH to TDI invalid	^{t}THDX	5		ns
Setup times				
TMS setup	^{t}MVTH	5		ns
Capture setup	^{t}CS	5		ns
Hold times				
TMS hold	^{t}THMX	5		ns
Capture hold	^{t}CH	5		ns

Notes: 1. ^{t}CS and ^{t}CH refer to the setup and hold time requirements of latching data from the boundary scan register.

Table 25: TAP DC Electrical Characteristics and Operating Conditions

+0°C ≤ T_C ≤ +95°C; +1.7V ≤ VDD ≤ +1.9V, unless otherwise noted

Description	Condition	Symbol	Min	Max	Units	Notes
Input high (logic 1) voltage		VIH	VREF + 0.15	VDD + 0.3	V	1, 2
Input low (logic 0) voltage		VIL	VSSQ - 0.3	VREF - 0.15	V	1, 2
Input leakage current	0V ≤ VIN ≤ VDD	ILI	–5.0	5.0	µA	
Output leakage current	Output disabled, 0V ≤ VIN ≤ VDDQ	ILO	–5.0	5.0	µA	
Output low voltage	IOLC = 100µA	VOL1		0.2	V	1
Output low voltage	IOLT = 2mA	VOL2		0.4	V	1
Output high voltage	|IOHC| = 100µA	VOH1	VDDQ - 0.2		V	1
Output high voltage	|IOHT| = 2mA	VOH2	VDDQ - 0.4		V	1

Notes:
1. All voltages referenced to VSS (GND).
2. Overshoot = VIH(AC) ≤ VDD + 0.7V for t ≤ ^{t}CK/2; undershoot = VIL(AC) ≥ –0.5V for t ≤ ^{t}CK/2; during normal operation, VDDQ must not exceed VDD.

Table 26: Identification Register Definitions

Instruction Field	All Devices	Description
Revision number (31:28)	abcd	ab = die revision cd = 00 for x9, 01 for x18, 10 for x36
Device ID (27:12)	00jkidef10100111	def = 000 for 288Mb, 001 for 576Mb i = 0 for common I/O, 1 for separate I/O jk = 01 for RLDRAM II, 00 for RLDRAM
Micron JEDEC ID code (11:1)	00000101100	Allows unique identification of RLDRAM vendor
ID register presence indicator (0)	1	Indicates the presence of an ID register

Table 27: Scan Register Sizes

Register Name	Bit Size
Instruction	8
Bypass	1
ID	32
Boundary scan	113

Table 28: Instruction Codes

Instruction	Code	Description
Extest	0000 0000	Captures I/O ring contents; Places the boundary scan register between TDI and TDO; This operation does not affect RLDRAM operations
ID code	0010 0001	Loads the ID register with the vendor ID code and places the register between TDI and TDO; This operation does not affect RLDRAM operations
Sample/preload	0000 0101	Captures I/O ring contents; Places the boundary scan register between TDI and TDO
Clamp	0000 0111	Selects the bypass register to be connected between TDI and TDO; Data driven by output balls are determined from values held in the boundary scan register
High-Z	0000 0011	Selects the bypass register to be connected between TDI and TDO; All outputs are forced into High-Z
Bypass	1111 1111	Places the bypass register between TDI and TDO; This operation does not affect RLDRAM operations

Table 29: Boundary Scan (Exit) Order

Bit#	Ball	Bit#	Ball	Bit#	Ball
1	K1	39	R11	77	C11
2	K2	40	R11	78	C11
3	L2	41	P11	79	C10
4	L1	42	P11	80	C10
5	M1	43	P10	81	B11
6	M3	44	P10	82	B11
7	M2	45	N11	83	B10
8	N1	46	N11	84	B10
9	P1	47	N10	85	B3
10	N3	48	N10	86	B3
11	N3	49	P12	87	B2
12	N2	50	N12	88	B2
13	N2	51	M11	89	C3
14	P3	52	M10	90	C3
15	P3	53	M12	91	C2
16	P2	54	L12	92	C2
17	P2	55	L11	93	D3
18	R2	56	K11	94	D3
19	R3	57	K12	95	D2
20	T2	58	J12	96	D2
21	T2	59	J11	97	E2
22	T3	60	H11	98	E2
23	T3	61	H12	99	E3
24	U2	62	G12	100	E3
25	U2	63	G10	101	F2
26	U3	64	G11	102	F2
27	U3	65	E12	103	F3
28	V2	66	F12	104	F3
29	U10	67	F10	105	E1
30	U10	68	F10	106	F1
31	U11	69	F11	107	G2
32	U11	70	F11	108	G3

Table 29: Boundary Scan (Exit) Order (continued)

Bit#	Ball	Bit#	Ball	Bit#	Ball
33	T10	71	E10	109	G1
34	T10	72	E10	110	H1
35	T11	73	E11	111	H2
36	T11	74	E11	112	J2
37	R10	75	D11	113	J1
38	R10	76	D10	–	–

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