CSD13306W 12 V N Channel NexFET™ Power MOSFET

1 Features

- Ultra Low on Resistance
- Low Q_g and Q_{gd}
- Small Footprint 1 × 1.5 mm
- Low Profile 0.62 mm Height
- Pb Free
- RoHS Compliant
- Halogen Free

2 Applications

- Battery Management
- Load Switch
- Battery Protection

3 Description

This 8.8 mΩ, 12 V, N-Channel device is designed to deliver the lowest on resistance and gate charge in a small 1 x 1.5 mm outline with excellent thermal characteristics and an ultra low profile.

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	12		V
Q_g	Gate Charge Total (4.5 V)	8.6		nC
Q_{gd}	Gate Charge Gate-to-Drain	3.0		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 2.5 V	12.9	mΩ
		V_{GS} = 4.5 V	8.8	mΩ
$V_{GS(th)}$	Voltage Threshold	1.0		V

Ordering Information(1)

Device	Qty	Media	Package	Ship
CSD13306W	3000	7-Inch Reel	1.0 mm × 1.5 mm Wafer Level Package	Tape and Reel
CSD13306WT	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

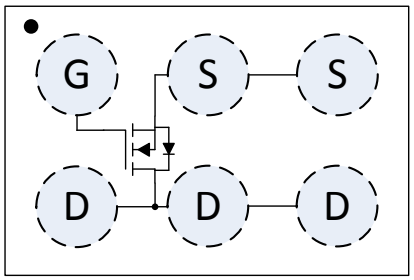
T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	12	V
V_{GS}	Gate-to-Source Voltage	±10	V
I_D	Continuous Drain Current(1)	3.5	A
I_{DM}	Pulsed Drain Current (2)	44	A
P_D	Power Dissipation(3)	1.9	W
T_{stg}	Storage Temperature Range	–55 to 150	°C
T_J	Operating Junction Temperature Range		

(1) Device Operating at a temperature of 105ºC

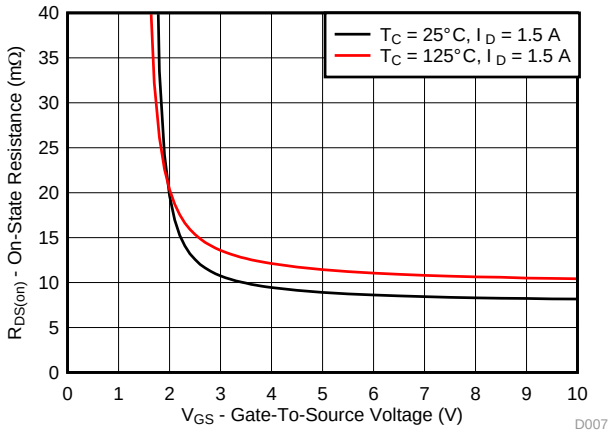
(2) Min Cu Typ $R_{\theta JA}$ = 230ºC/W, Pulse width ≤100 µs, duty cycle ≤1%

(3) Max Cu Typ $R_{\theta JA}$ = 65ºC/W

Top View



$R_{DS(on)}$ vs V_{GS}



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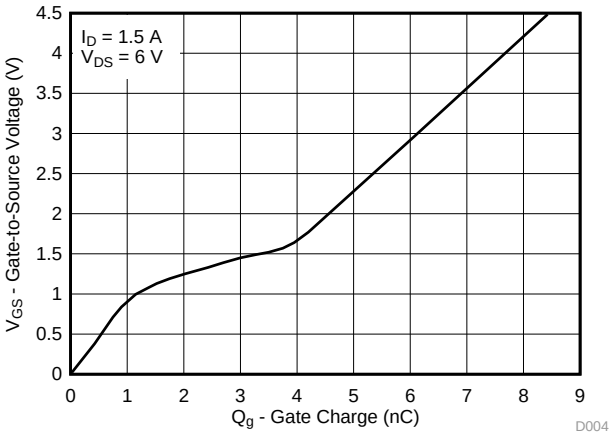
Gate Charge



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4 Revision History

DATE	REVISION	NOTES
March 2015	*	Initial release.

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

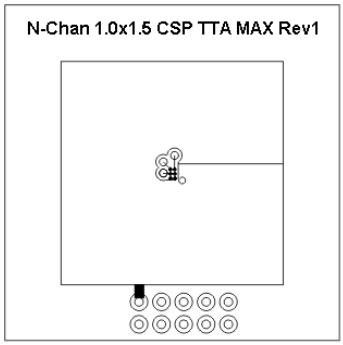
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 250 µA	12			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 9.6 V			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 10 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.7	1.0	1.3	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 2.5 V, I_D = 1.5 A		12.9	15.5	mΩ
		V_{GS} = 4.5 V, I_D = 1.5 A		8.8	10.2	mΩ
g_{fs}	Transconductance	V_{DS} = 1.2 V, I_D =1.5 A		15		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 6 V, f = 1 MHz		1050	1370	pF
C_{OSS}	Output Capacitance			324	421	pF
C_{RSS}	Reverse Transfer Capacitance			226	294	pF
R_g				4.2	8.4	Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 6 V, I_D = 1.5 A		8.6	11.2	nC
Q_{gd}	Gate Charge Gate-to-Drain			3.0		nC
Q_{gs}	Gate Charge Gate-to-Source			1.1		nC
$Q_{g(th)}$	Gate Charge at Vth			1.2		nC
Q_{OSS}	Output Charge	V_{DS} = 6 V, V_{GS} = 0 V		3.3		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 6 V, V_{GS} = 4.5 V, I_D = 1.5 A R_G = 4 Ω		7		ns
t_r	Rise Time			11		ns
$t_{d(off)}$	Turn Off Delay Time			20		ns
t_f	Fall Time			8		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_S = 1.5 A, V_{GS} = 0 V		0.7	1.0	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 6 V, I_F = 1.5 A, di/dt = 200 A/µs		14.8		nC
t_{rr}	Reverse Recovery Time			23		ns

5.2 Thermal Information

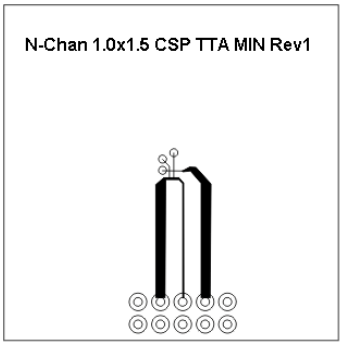
T_A = 25°C unless otherwise stated

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance (1)		230		°C/W
	Junction-to-Ambient Thermal Resistance (2)		65		

(1) Device mounted on FR4 material with minimum Cu mounting area
(2) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu.



Typ $R_{\theta JA}$ = 65°C/W when mounted on 1 inch^2 of 2 oz. Cu.



Typ $R_{\theta JA}$ = 230°C/W when mounted on minimum pad area of 2 oz. Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

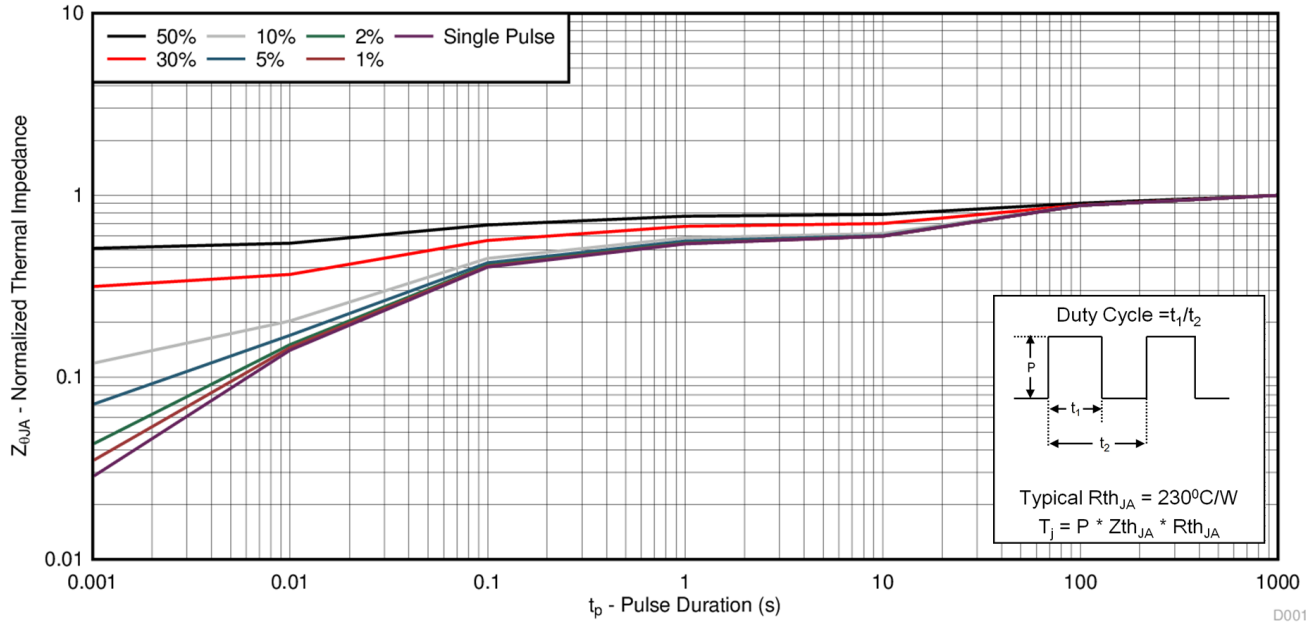


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

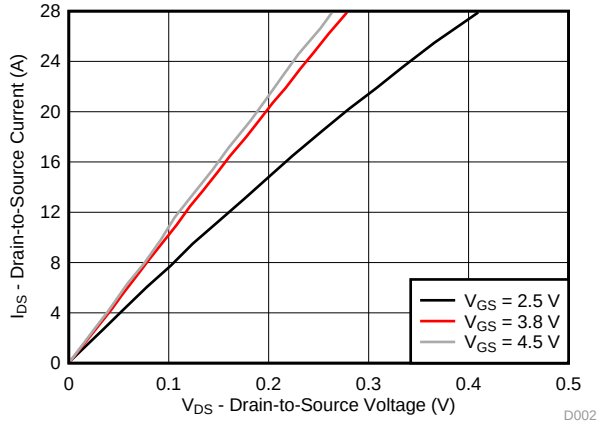


Figure 2. Saturation Characteristics

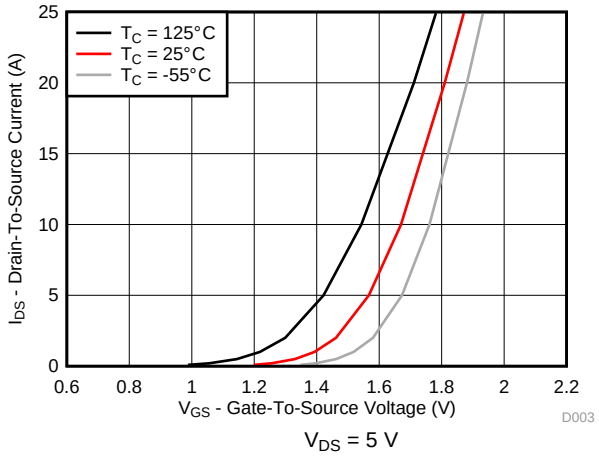


Figure 3. Transfer Characteristics

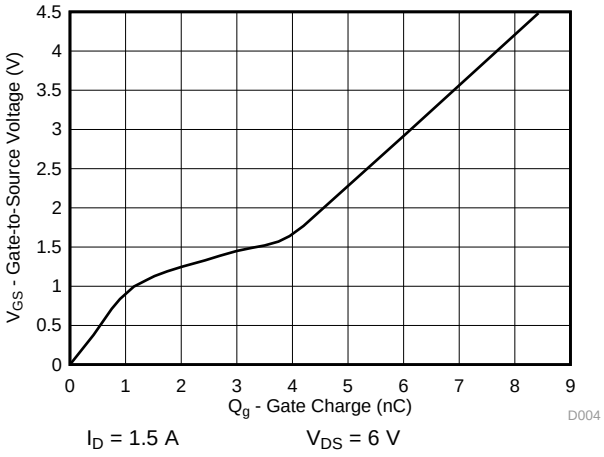


Figure 4. Gate Charge

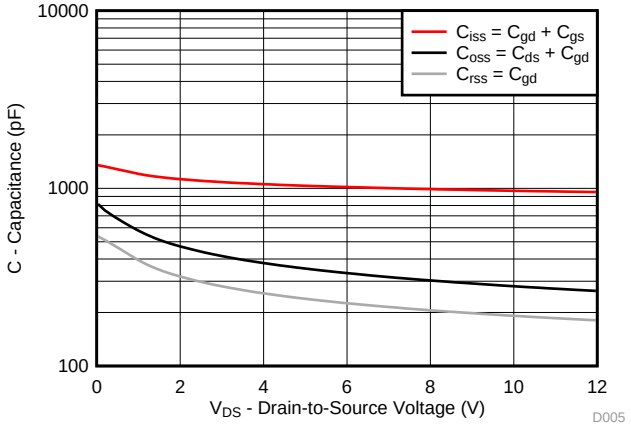


Figure 5. Capacitance

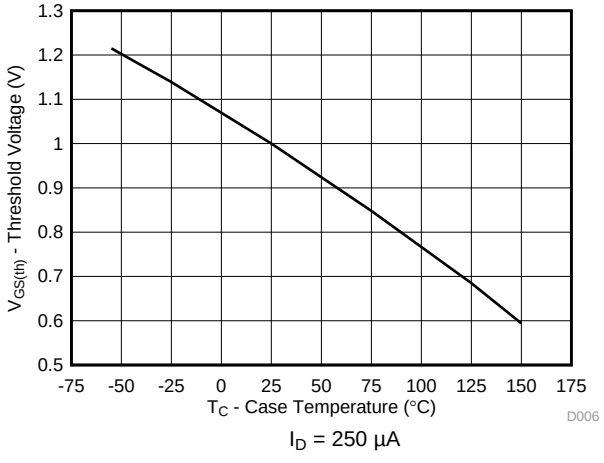


Figure 6. Threshold Voltage vs Temperature

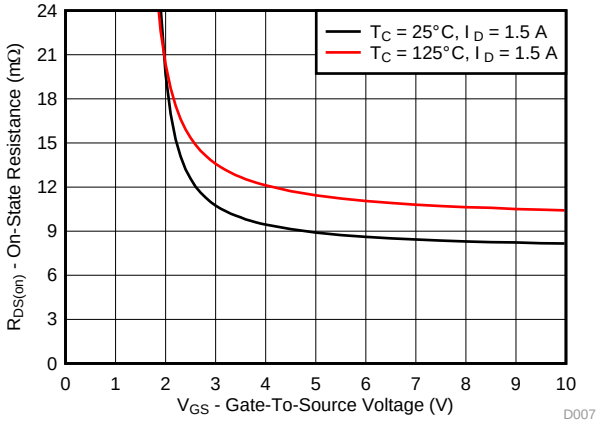


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

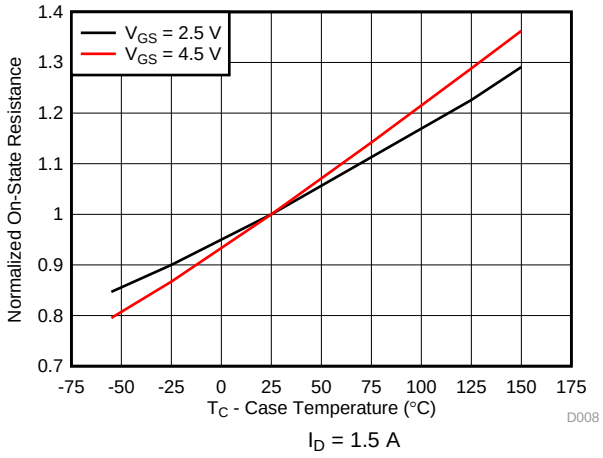


Figure 8. Normalized On-State Resistance vs Temperature

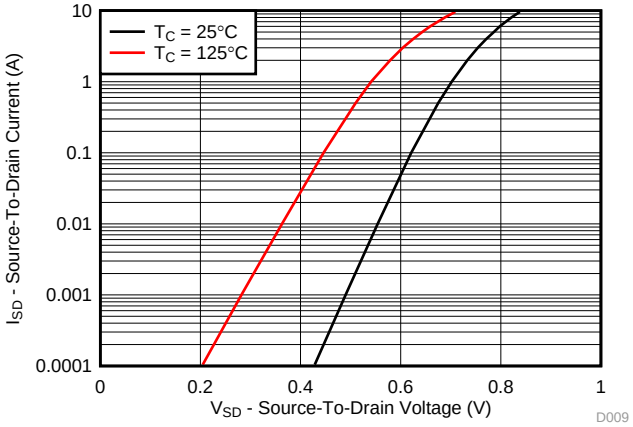


Figure 9. Typical Diode Forward Voltage

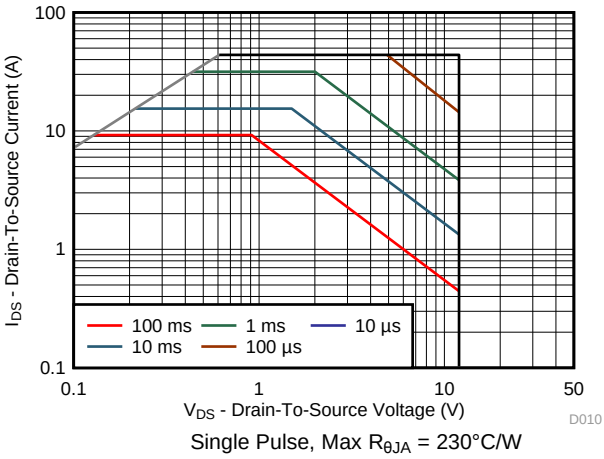


Figure 10. Maximum Safe Operating Area

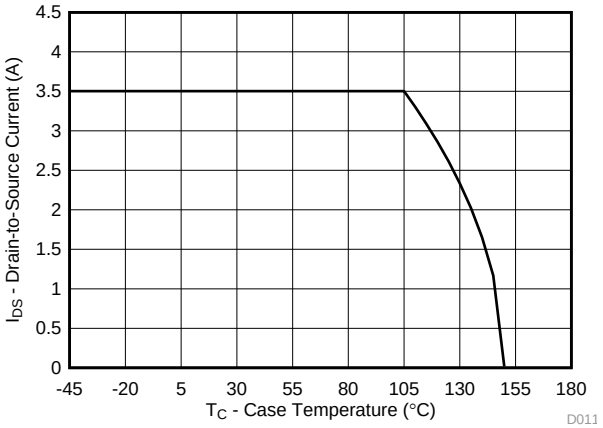


Figure 11. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

6.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

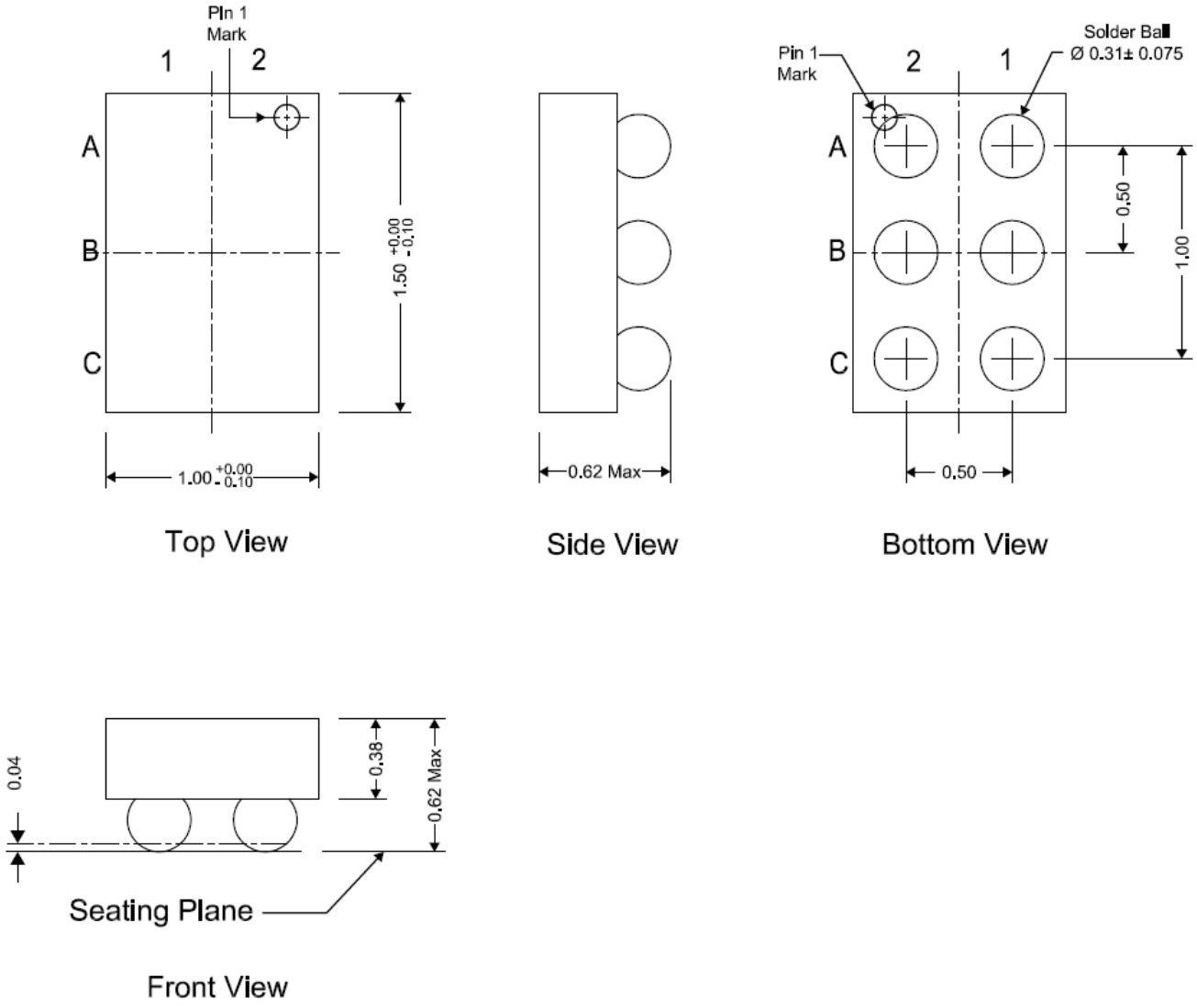
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 CSD13306W Package Dimensions

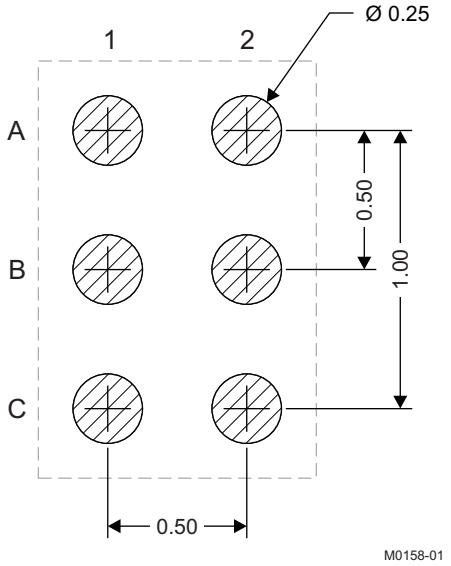


NOTE: All dimensions are in mm (unless otherwise specified)

Pinout

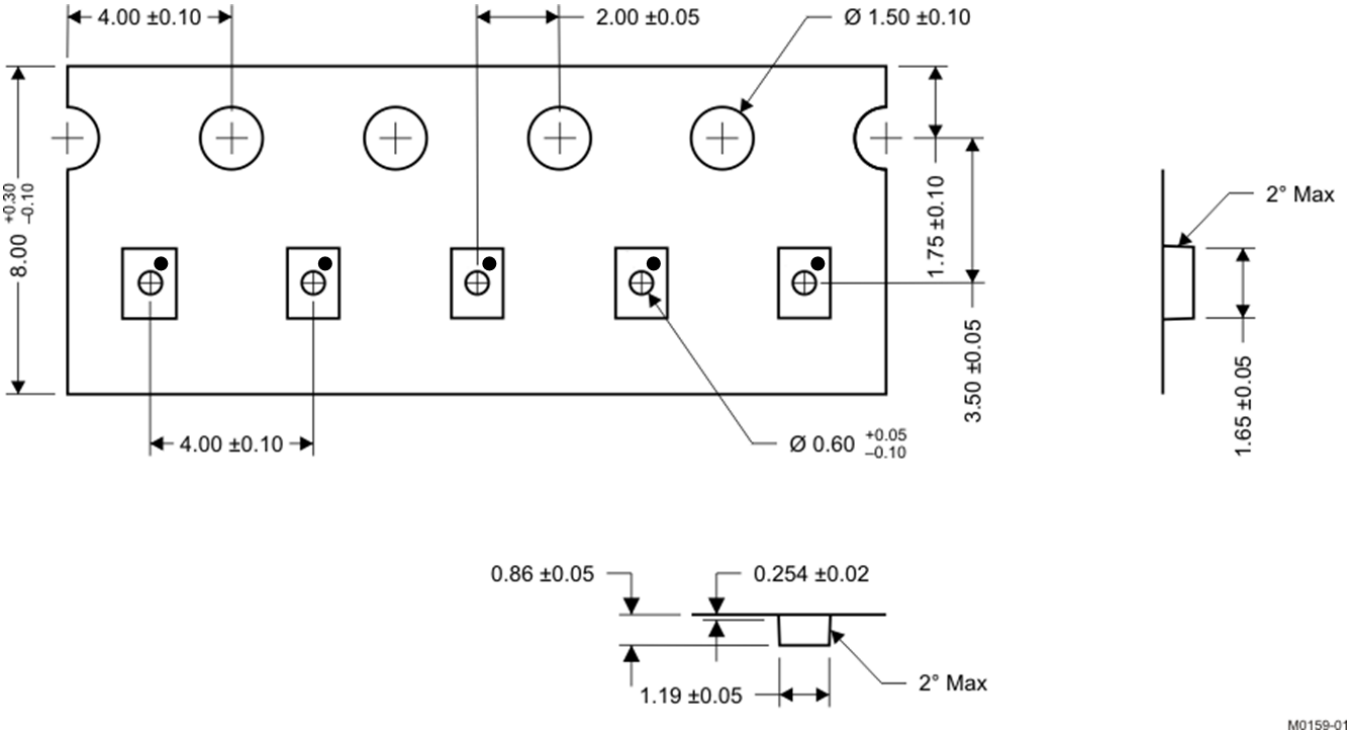
POSITION	DESIGNATION
C2, B2	Source
A2	Gate
A1, B1, C1	Drain

Land Pattern Recommendation



NOTE: All dimensions are in mm (unless otherwise specified)

7.2 Tape and Reel Information



NOTE: All dimensions are in mm (unless otherwise specified)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD13306W	ACTIVE	DSBGA	YZC	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		13306	Samples
CSD13306WT	ACTIVE	DSBGA	YZC	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		13306	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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