



**GD25Q64B  
DATASHEET**



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## 1. FEATURES

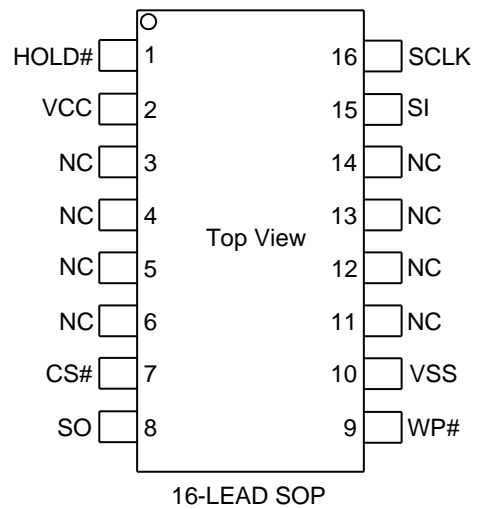
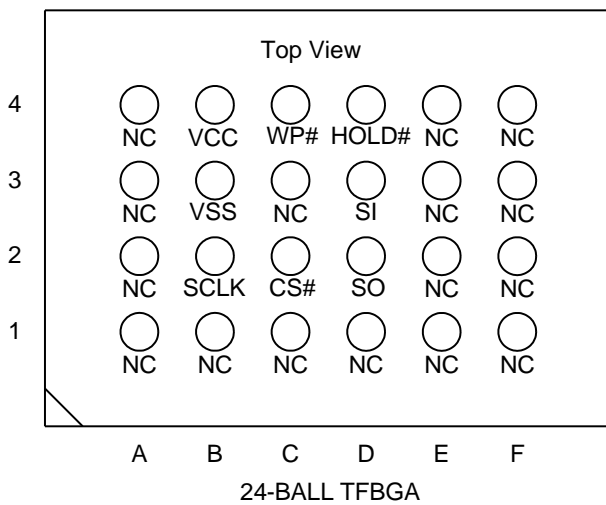
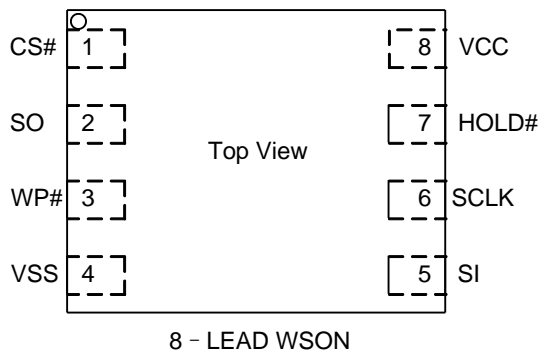
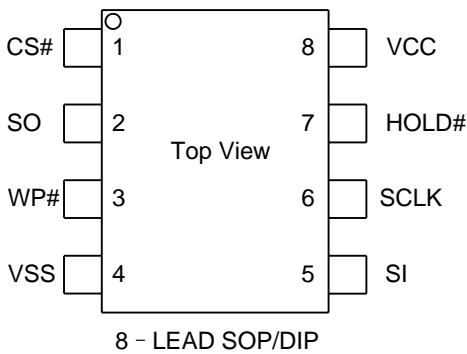
- ◆ 64M-bit Serial Flash
  - 8192K-byte
  - 256 bytes per programmable page
- ◆ Standard, Dual, Quad SPI
  - Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
  - Dual SPI: SCLK, CS#, IO0, IO1, WP#, HOLD#
  - Quad SPI: SCLK, CS#, IO0, IO1, IO2, IO3
- ◆ High Speed Clock Frequency
  - 120MHz for fast read with 30PF load
  - Dual I/O Data transfer up to 240Mbits/s
  - Quad I/O Data transfer up to 480Mbits/s
- ◆ Software/Hardware Write Protection
  - Write protect all/portion of memory via software
  - Enable/Disable protection with WP# Pin
  - Top or Bottom, Sector or Block selection
- ◆ Minimum 100,000 Program/Erase Cycles
- ◆ Program/Erase Speed
  - Page Program time: 0.4ms typical
  - Sector Erase time: 40ms typical
  - Block Erase time: 0.2/0.4s typical
  - Chip Erase time: 30s typical
- ◆ Flexible Architecture
  - Sector of 4K-byte
  - Block of 32/64k-byte
- ◆ Low Power Consumption
  - 20mA maximum active current
  - 5uA maximum power down current
- ◆ Advanced security Features<sup>(1)</sup>
  - 4\*256-Byte Security Registers With OTP Lock
- ◆ Single Power Supply Voltage
  - Full voltage range:2.7~3.6V

Note: 1.Please contact GigaDevice for details.

## 2. GENERAL DESCRIPTION

The GD25Q64B (64M-bit) Serial flash supports the standard Serial Peripheral Interface (SPI), and supports the Dual/Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2 (WP#), and I/O3 (HOLD#). The Dual I/O data is transferred with speed of 240Mbits/s and the Quad I/O & Quad output data is transferred with speed of 480Mbits/s.

### CONNECTION DIAGRAM

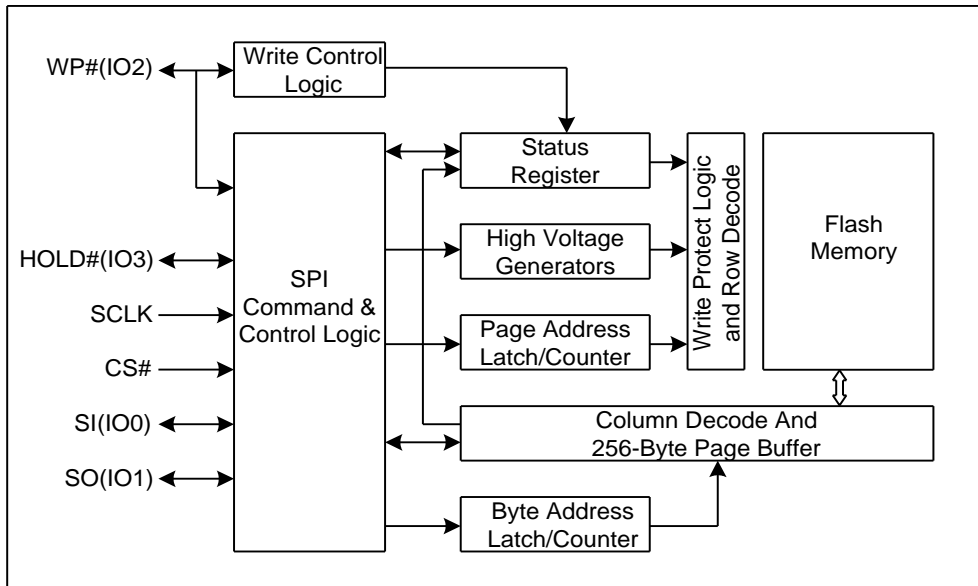


### PIN DESCRIPTION

Pin Name	I/O	Description
CS#	I	Chip Select Input
SO (IO1)	I/O	Data Output (Data Input Output 1)
WP# (IO2)	I/O	Write Protect Input (Data Input Output 2)
VSS		Ground
SI (IO0)	I/O	Data Input (Data Input Output 0)
SCLK	I	Serial Clock Input
HOLD# (IO3)	I/O	Hold Input (Data Input Output 3)
VCC		Power Supply



BLOCK DIAGRAM





### 3. MEMORY ORGANIZATION

#### GD25Q64B

Each device has	Each block has	Each sector has	Each page has	
8M	64/32K	4K	256	bytes
32K	256/128	16	-	pages
2048	16/8	-	-	sectors
128/256	-	-	-	blocks

#### UNIFORM BLOCK SECTOR ARCHITECTURE

##### GD25Q64B 64K Bytes Block Sector Architecture

Block	Sector	Address range	
127	2047	7FF000H	7FFFFFFH
	.....	.....	.....
	2032	7F0000H	7F0FFFFH
126	2031	7EF000H	7EFFFFFFH
	.....	.....	.....
	2016	7E0000H	7E0FFFFH
.....	.....	.....	.....
	.....	.....	.....
	.....	.....	.....
.....	.....	.....	.....
	.....	.....	.....
	.....	.....	.....
2	47	02F000H	02FFFFFFH
	.....	.....	.....
	32	020000H	020FFFFH
1	31	01F000H	01FFFFFFH
	.....	.....	.....
	16	010000H	010FFFFH
0	15	00F000H	00FFFFFFH
	.....	.....	.....
	0	000000H	000FFFFH

## 4. DEVICE OPERATION

### SPI Mode

#### Standard SPI

The GD25Q64B features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

#### Dual SPI

The GD25Q64B supports Dual SPI operation when using the “Dual Output Fast Read” and “Dual I/O Fast Read” (3BH and BBH) commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

#### Quad SPI

The GD25Q64B supports Quad SPI operation when using the “Quad Output Fast Read”, “Quad I/O Fast Read”, “Quad I/O Word Fast Read” (6BH, EBH, E7H) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and WP# and HOLD# pins become IO2 and IO3. Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register to be set.

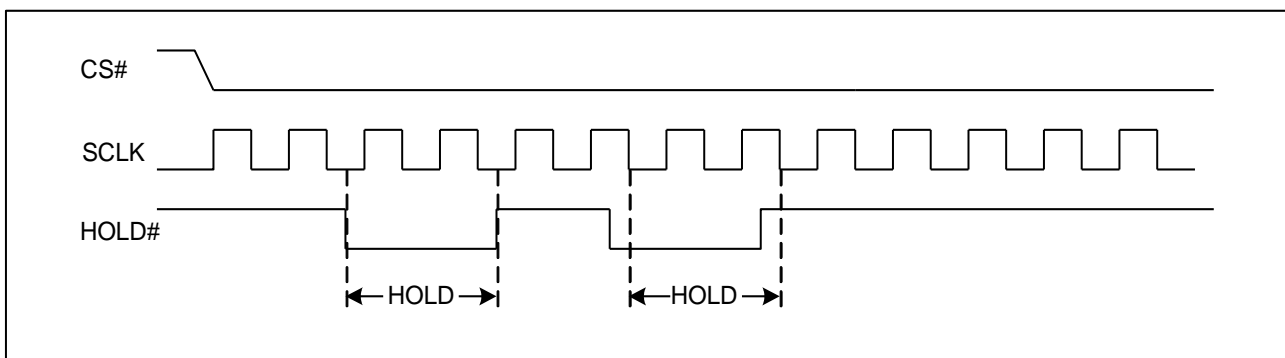
### Hold

The HOLD# signal goes low to stop any serial communications with the device, but doesn't stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD, need CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of HOLD# signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

The SO is high impedance, both SI and SCLK don't care during the HOLD operation, if CS# drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and then CS# must be at low.

**Figure1. Hold Condition**





## 5. DATA PROTECTION

The GD25Q64B provide the following data protection methods:

- ◆ Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
  - Power-Up
  - Write Disable (WRDI)
  - Write Status Register (WRSR)
  - Page Program (PP)
  - Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)
- ◆ Software Protection Mode: The Block Protect (BP4, BP3, BP2, BP1, BP0) bits define the section of the memory array that can be read but not change.
- ◆ Hardware Protection Mode: WP# going low to protected the BP0~BP4 bits and SRP bit.
- ◆ Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command.

**Table1.0 GD25Q64B Protected area size (CMP=0)**

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	126 to 127	7E0000H-7FFFFFFH	128KB	Upper 1/64
0	0	0	1	0	124 to 127	7C0000H-7FFFFFFH	256KB	Upper 1/32
0	0	0	1	1	120 to 127	780000H-7FFFFFFH	512KB	Upper 1/16
0	0	1	0	0	112 to 127	700000H-7FFFFFFH	1MB	Upper 1/8
0	0	1	0	1	96 to 127	600000H-7FFFFFFH	2MB	Upper 1/4
0	0	1	1	0	64 to 127	400000H-7FFFFFFH	4MB	Upper 1/2
0	1	0	0	1	0 to 1	000000H-01FFFFH	128KB	Lower 1/64
0	1	0	1	0	0 to 3	000000H-03FFFFH	256KB	Lower 1/32
0	1	0	1	1	0 to 7	000000H-07FFFFH	512KB	Lower 1/16
0	1	1	0	0	0 to 15	000000H-0FFFFFFH	1MB	Lower 1/8
0	1	1	0	1	0 to 31	000000H-1FFFFFFH	2MB	Lower 1/4
0	1	1	1	0	0 to 63	000000H-3FFFFFFH	4MB	Lower 1/2
X	X	1	1	1	0 to 127	000000H-7FFFFFFH	8MB	ALL
1	0	0	0	1	127	7FF000H-7FFFFFFH	4KB	Top Block
1	0	0	1	0	127	7FE000H-7FFFFFFH	8KB	Top Block
1	0	0	1	1	127	7FC000H-7FFFFFFH	16KB	Top Block
1	0	1	0	X	127	7F8000H-7FFFFFFH	32KB	Top Block
1	0	1	1	0	127	7F8000H-7FFFFFFH	32KB	Top Block
1	1	0	0	1	0	000000H-000FFFH	4KB	Bottom Block
1	1	0	1	0	0	000000H-001FFFH	8KB	Bottom Block
1	1	0	1	1	0	000000H-003FFFH	16KB	Bottom Block
1	1	1	0	X	0	000000H-007FFFH	32KB	Bottom Block
1	1	1	1	0	0	000000H-007FFFH	32KB	Bottom Block

Table1.1 GD25Q64B Protected area size (CMP=1)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	ALL	000000H-7FFFFFFH	ALL	ALL
0	0	0	0	1	0 to 125	000000H-7DFFFFFFH	8064KB	Lower 63/64
0	0	0	1	0	0 to 123	000000H-7BFFFFFFH	7936KB	Lower 31/32
0	0	0	1	1	0 to 119	000000H-77FFFFFFH	7680KB	Lower 15/16
0	0	1	0	0	0 to 111	000000H-6FFFFFFH	7MB	Lower 7/8
0	0	1	0	1	0 to 95	000000H-5FFFFFFH	6MB	Lower 3/4
0	0	1	1	0	0 to 63	000000H-3FFFFFFH	4MB	Lower 1/2
0	1	0	0	1	2 to 127	020000H-7FFFFFFH	8064KB	Upper 63/64
0	1	0	1	0	4 to 127	040000H-7FFFFFFH	7936KB	Upper 31/32
0	1	0	1	1	8 to 127	080000H-7FFFFFFH	7680KB	Upper 15/16
0	1	1	0	0	16 to 127	100000H-7FFFFFFH	7MB	Upper 7/8
0	1	1	0	1	32 to 127	200000H-7FFFFFFH	6MB	Upper 3/4
0	1	1	1	0	64 to 127	400000H-7FFFFFFH	4MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 to 127	000000H-7FEFFFFH	8188KB	L-2047/2048
1	0	0	1	0	0 to 127	000000H-7FDFFFFH	8184KB	L-1023/1024
1	0	0	1	1	0 to 127	000000H-7FBFFFFH	8176KB	L-511/512
1	0	1	0	X	0 to 127	000000H-7F7FFFFH	8160KB	L-255/256
1	0	1	1	0	0 to 127	000000H-7F7FFFFH	8160KB	L-255/256
1	1	0	0	1	0 to 127	001000H-7FFFFFFH	8188KB	U-2047/2048
1	1	0	1	0	0 to 127	002000H-7FFFFFFH	8184KB	U-1023/1024
1	1	0	1	1	0 to 127	004000H-7FFFFFFH	8176KB	U-511/512
1	1	1	0	X	0 to 127	008000H-7FFFFFFH	8160KB	U-255/256
1	1	1	1	0	0 to 127	008000H-7FFFFFFH	8160KB	U-255/256

## 6. STATUS REGISTER

<b>S15</b>	<b>S14</b>	<b>S13</b>	<b>S12</b>	<b>S11</b>	<b>S10</b>	<b>S9</b>	<b>S8</b>
<b>SUS</b>	<b>CMP</b>	Reserved	Reserved	Reserved	<b>LB</b>	<b>QE</b>	Reserved

<b>S7</b>	<b>S6</b>	<b>S5</b>	<b>S4</b>	<b>S3</b>	<b>S2</b>	<b>S1</b>	<b>S0</b>
<b>SRP</b>	<b>BP4</b>	<b>BP3</b>	<b>BP2</b>	<b>BP1</b>	<b>BP0</b>	<b>WEL</b>	<b>WIP</b>

The status and control bits of the Status Register are as follows:

### WIP bit.

The Write In Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

### WEL bit.

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

### BP4, BP3, BP2, BP1, BP0 bits.

The Block Protect (BP4, BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table1).becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP4, BP3, BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed, if the Block Protect (BP2, BP1, BP0) bits and CMP are all 0 or all 1.

### SRP bit.

The Status Register Protect (SRP) bit is non-volatile Read/Write bits in the status register. The SRP bit controls the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

<b>SRP</b>	<b>#WP</b>	<b>Status Register</b>	<b>Description</b>
0	X	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1.(Default)
1	0	Hardware Protected	WP#=0, the Status Register locked and can not be written to.
1	1	Hardware Unprotected	WP#=1, the Status Register is unlocked and can be written to after a Write Enable command, WEL=1.

### QE bit.

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is set to 0 (Default) the WP# pin and HOLD# pin are enable. When the QE pin is set to 1, the Quad IO2 and IO3 pins are enabled. (The QE bit should never be set to 1 during standard SPI or Dual SPI operation if the WP# or HOLD# pins are tied directly to the power supply or ground)

### LB bit.

The LB bit is a non-volatile One Time Program (OTP) bit in Status Register (S10) that provide the write protect control



and status to the Security Registers. The default state of LB is 0, the security registers are unlocked. LB can be set to 1 individually using the Write Register instruction. LB is One Time Programmable, once it's set to 1, the Security Registers will become read-only permanently.

**CMP bit**

The CMP bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction the BP4-BP0 bits to provide more flexibility for the array protection. Please see the Status registers Memory Protection table for details. The default setting is CMP=0.

**SUS bit**

The SUS bit is a read only bit in the status register (S15 ) that is set to 1 after executing an Erase/Program Suspend (75H) command. The SUS bit is cleared to 0 by Erase/Program Resume (7AH) command as well as a power-down, power-up cycle.

## 7. COMMANDS DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See Table2, every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been shifted in. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. CS# can be driven high after any bit of the data-out sequence is being shifted out.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That is CS# must driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

**Table2. Commands**

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Write Enable	06H						
Write Disable	04H						
Read Status Register	05H	(S7-S0)					(continuous)
Read Status Register-1	35H	(S15-S8)					(continuous)
Write Status Register	01H	(S7-S0)	(S15-S8)				
Read Data	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	(continuous)
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(continuous)
Dual Output Fast Read	3BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0) <sup>(1)</sup>	(continuous)
Dual I/O Fast Read	BBH	A23-A8 <sup>(2)</sup>	A7-A0 M7-M0 <sup>(2)</sup>	(D7-D0) <sup>(1)</sup>			(continuous)
Quad Output Fast Read	6BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0) <sup>(3)</sup>	(continuous)
Quad I/O Fast Read	EBH	A23-A0 M7-M0 <sup>(4)</sup>	dummy <sup>(5)</sup>	(D7-D0) <sup>(3)</sup>			(continuous)
Quad I/O Word Fast Read <sup>(7)</sup>	E7H	A23-A0 M7-M0 <sup>(4)</sup>	dummy <sup>(6)</sup>	(D7-D0) <sup>(3)</sup>			(continuous)
Continuous Read Reset	FFH						
Page Program	02 H	A23-A16	A15-A8	A7-A0	(D7-D0)	Next byte	
Quad Page Program	32H	A23-A16	A15-A8	A7-A0	(D7-D0) <sup>(3)</sup>		
Sector Erase	20H	A23-A16	A15-A8	A7-A0			
Block Erase(32K)	52H	A23-A16	A15-A8	A7-A0			
Block Erase(64K)	D8H	A23-A16	A15-A8	A7-A0			
Chip Erase	C7/60 H						
Program/Erase Suspend	75H						
Program/Erase Resume	7AH						
Deep Power-Down	B9H						
Release From Deep Power-Down, And Read Device ID	ABH	dummy	dummy	dummy	(DID7- DID0)		(continuous)
Release From Deep Power-Down	ABH						



Manufacturer/ Device ID	90H	dummy	dummy	00H	(MID7- MID0)	(DID7- DID0)	(continuous)
High Performance Mode	A3H	dummy	dummy	dummy			
Read Identification	9FH	(MID7- M0)	(JDID15- JDID8)	(JDID7- JDID0)			(continuous)
Erase Security Registers <sup>(8)</sup>	44H	A23-A16	A15-A8	A7-A0			
Program Security Registers <sup>(8)</sup>	42H	A23-A16	A15-A8	A7-A0	(D7-D0)	(D7-D0)	
Read Security Registers <sup>(8)</sup>	48H	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	

**NOTE:**

1. Dual Output data

IO0 = (D6, D4, D2, D0)

IO1 = (D7, D5, D3, D1)

2. Dual Input Address

IO0 = A22, A20, A18, A16, A14, A12, A10, A8      A6, A4, A2, A0, M6, M4, M2, M0

IO1 = A23, A21, A19, A17, A15, A13, A11, A9      A7, A5, A3, A1, M7, M5, M3, M1

3. Quad Output Data

IO0 = (D4, D0, .....)

IO1 = (D5, D1, .....)

IO2 = (D6, D2, .....)

IO3 = (D7, D3,.....)

4. Quad Input Address

IO0 = A20, A16, A12, A8,    A4, A0, M4, M0

IO1 = A21, A17, A13, A9,    A5, A1, M5, M1

IO2 = A22, A18, A14, A10, A6, A2, M6, M2

IO3 = A23, A19, A15, A11, A7, A3, M7, M3

5. Fast Read Quad I/O Data

IO0 = (x, x, x, x, D4, D0,...)

IO1 = (x, x, x, x, D5, D1,...)

IO2 = (x, x, x, x, D6, D2,...)

IO3 = (x, x, x, x, D7, D3,...)

6. Fast Word Read Quad I/O Data

IO0 = (x, x, D4, D0,...)

IO1 = (x, x, D5, D1,...)

IO2 = (x, x, D6, D2,...)

IO3 = (x, x, D7, D3,...)

7. Fast Word Read Quad I/O Data: the lowest address bit must be 0.

8. Security Registers Address:

Security Register0: A23-A16=00H, A15-A8=00H, A7-A0= Byte Address;

Security Register1: A23-A16=00H, A15-A8=01H, A7-A0= Byte Address;

Security Register2: A23-A16=00H, A15-A8=02H, A7-A0= Byte Address;

Security Register3: A23-A16=00H, A15-A8=03H, A7-A0= Byte Address.



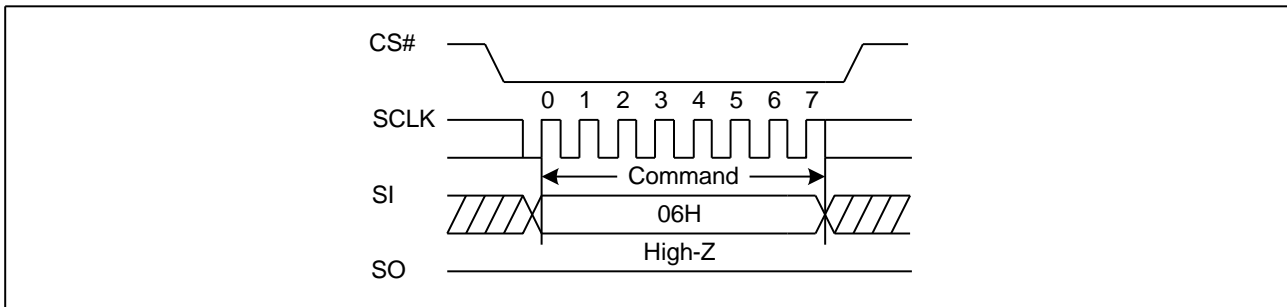
**Table of ID Definitions:**  
**GD25Q64B**

<b>Operation Code</b>	<b>M7-M0</b>	<b>ID15-ID8</b>	<b>ID7-ID0</b>
9FH	C8	40	17
90H	C8		16
ABH			16

### 7.1. Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE) and Write Status Register (WRSR) command. The Write Enable (WREN) command sequence: CS# goes low → sending the Write Enable command → CS# goes high.

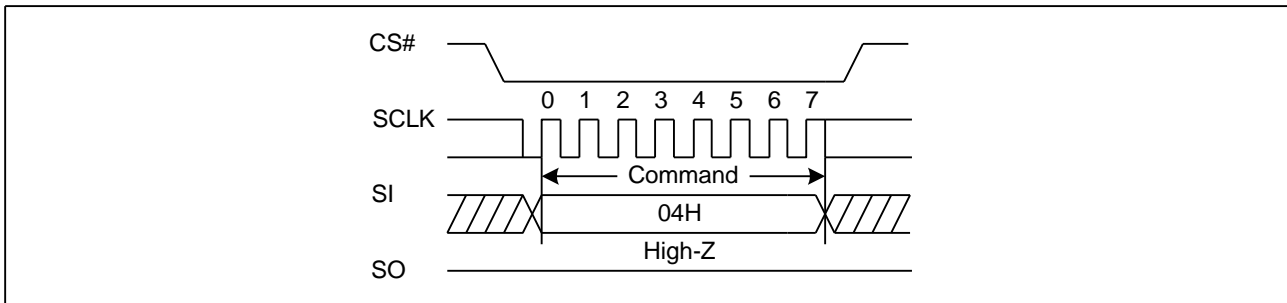
**Figure2. Write Enable Sequence Diagram**



### 7.2. Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Disable command sequence: CS# goes low → Sending the Write Disable command → CS# goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase commands.

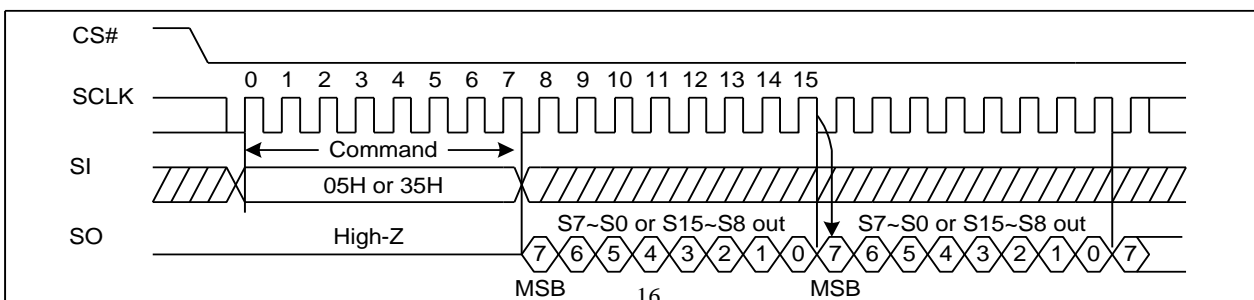
**Figure3. Write Disable Sequence Diagram**



### 7.3. Read Status Register (RDSR) (05H or 35H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code "05H", the SO will output Status Register bits S7~S0. The command code "35H", the SO will output Status Register bits S15~S8.

**Figure4. Read Status Register Sequence Diagram**





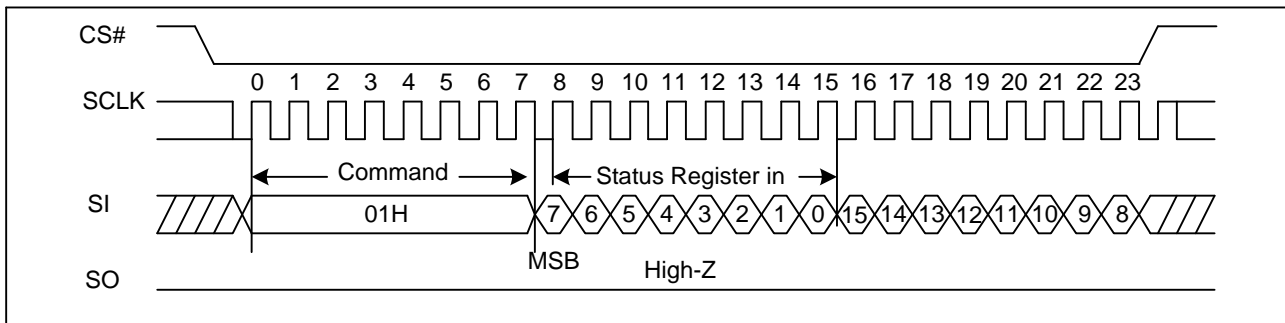
### 7.4. Write Status Register (WRSR) (01H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on S15, S1 and S0 of the Status Register. CS# must be driven high after the eighth or sixteen bit of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. If CS# is driven high after eighth bit of the data byte, the CMP and QE bit will be cleared to 0. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is  $t_w$ ) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table1. The Write Status Register (WRSR) command also allows the user to set or reset the Status Register Protect (SRP) bit in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register (WRSR) command is not executed once the Hardware Protected Mode is entered.

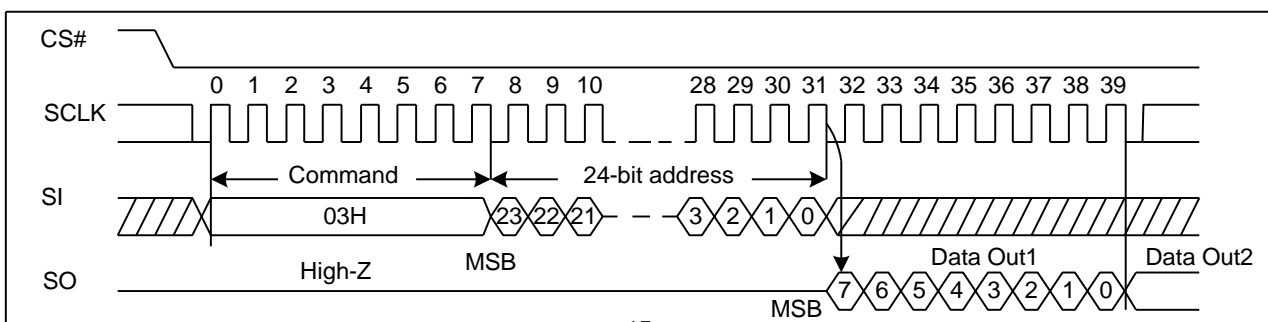
**Figure5. Write Status Register Sequence Diagram**



### 7.5. Read Data Bytes (READ) (03H)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency  $f_R$ , during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

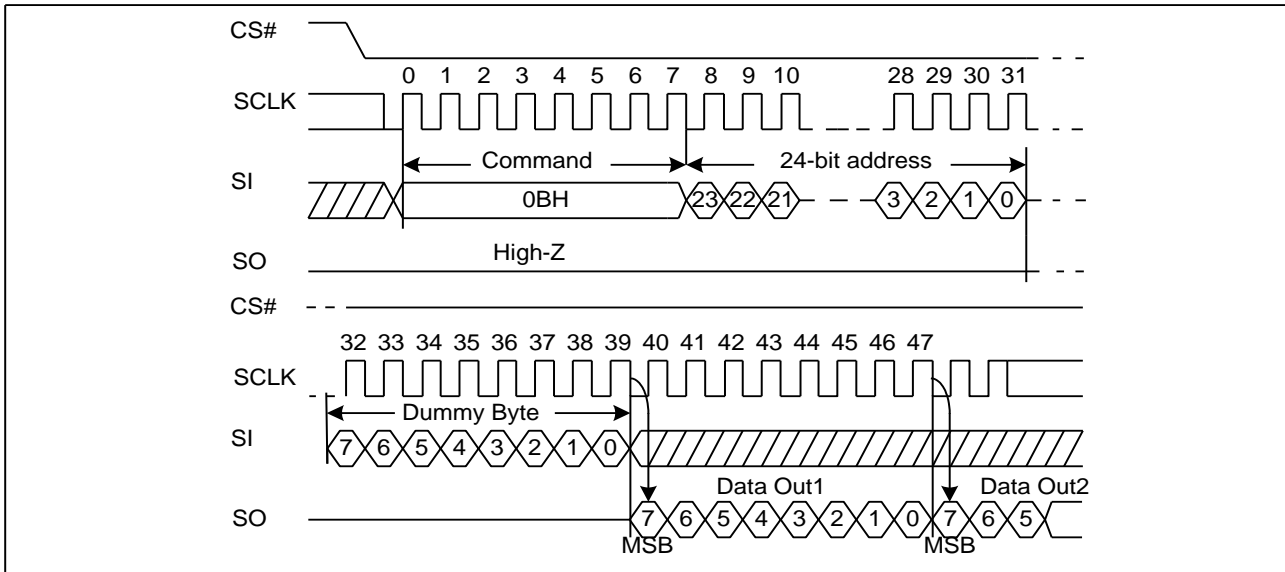
**Figure6. Read Data Bytes Sequence Diagram**



### 7.6. Read Data Bytes At Higher Speed (Fast Read) (0BH)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency  $f_c$ , during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

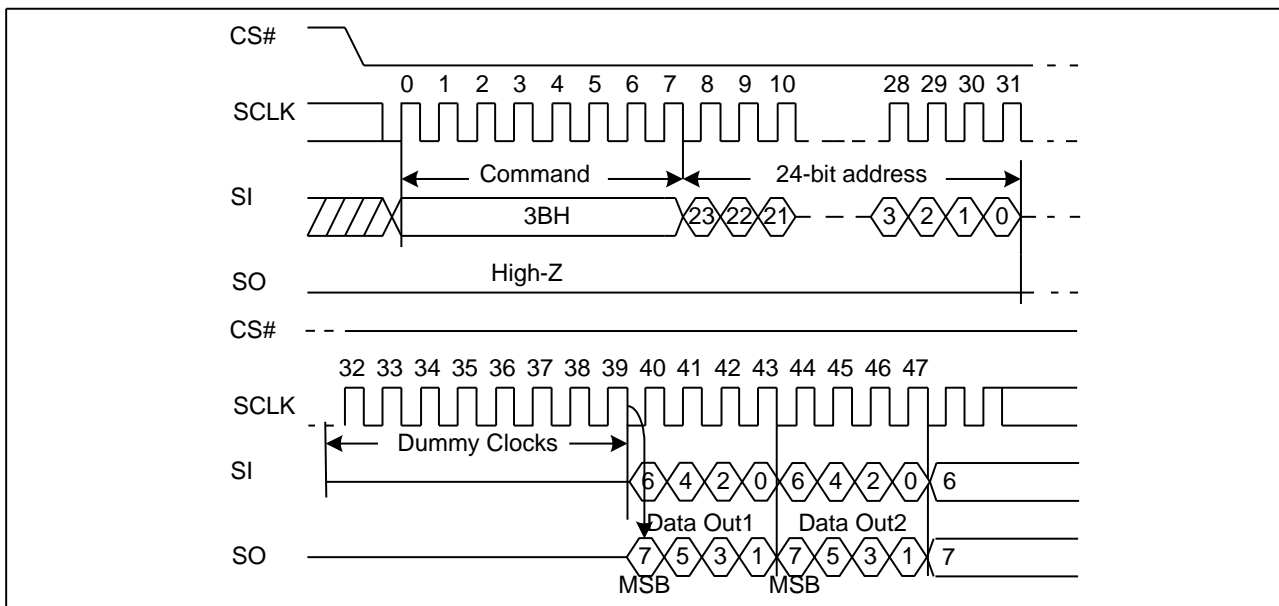
**Figure7. Read Data Bytes at Higher Speed Sequence Diagram**



### 7.7. Dual Output Fast Read (3BH)

The Dual Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in followed Figure8. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

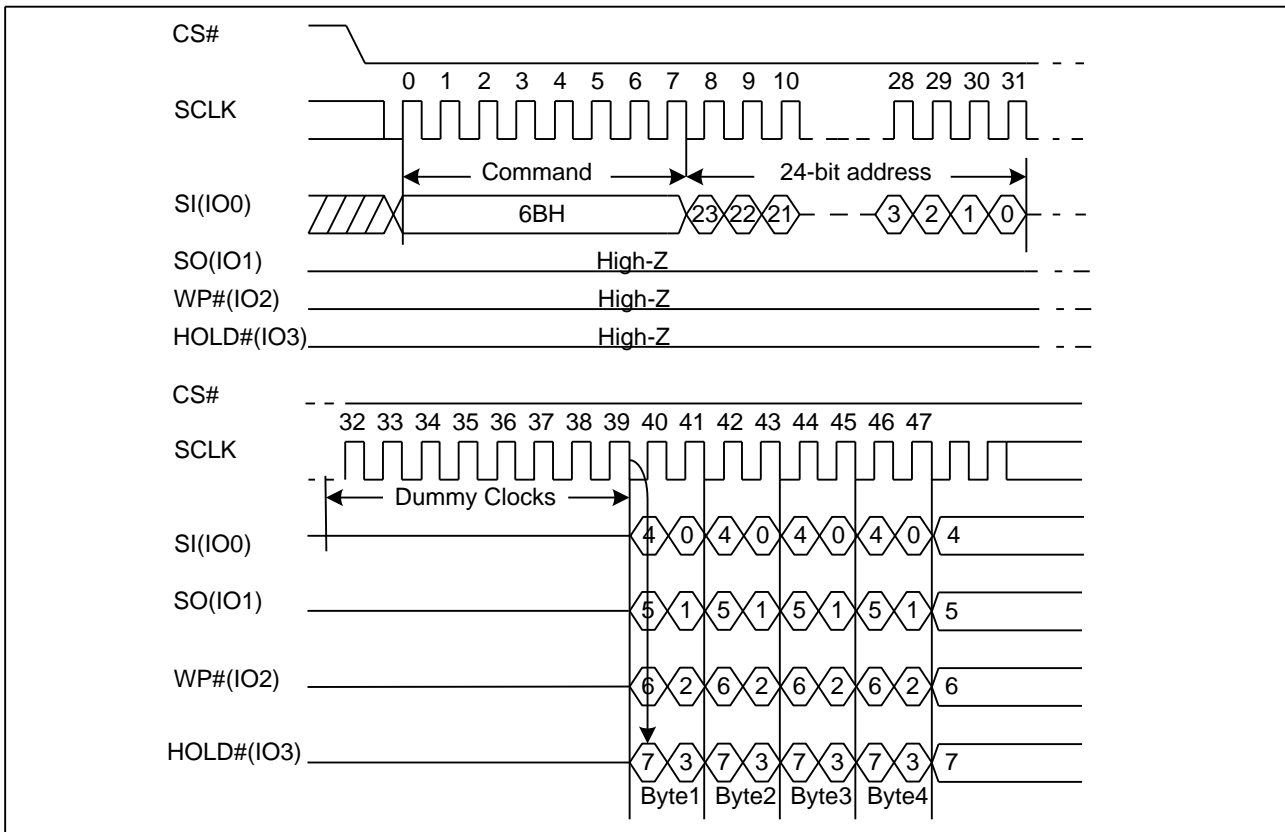
**Figure8. Dual Output Fast Read Sequence Diagram**



### 7.8. Quad Output Fast Read (6BH)

The Quad Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The command sequence is shown in followed Figure9. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Figure9. Quad Output Fast Read Sequence Diagram



### 7.9. Dual I/O Fast Read (BBH)

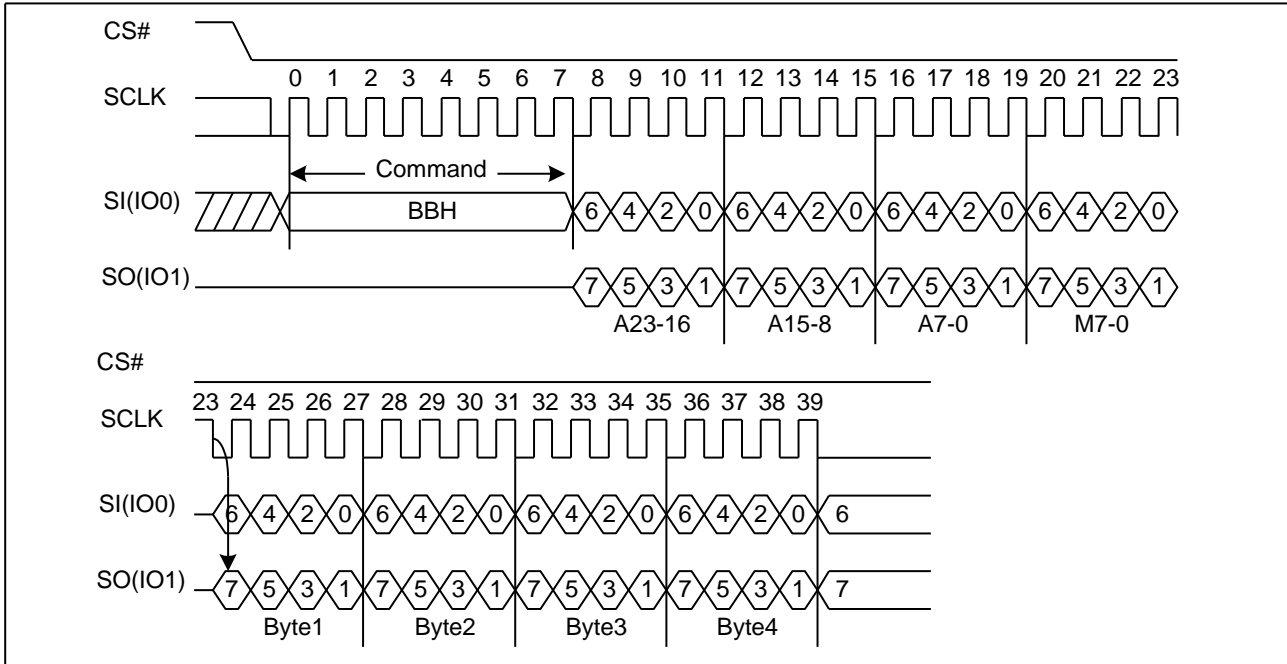
The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte 2-bit per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in followed Figure10. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. To ensure optimum performance the High Performance Mode (HPM) command (A3H) must be executed once, prior to the Dual I/O Fast Read command.

#### Dual I/O Fast Read with “Continuous Read Mode”

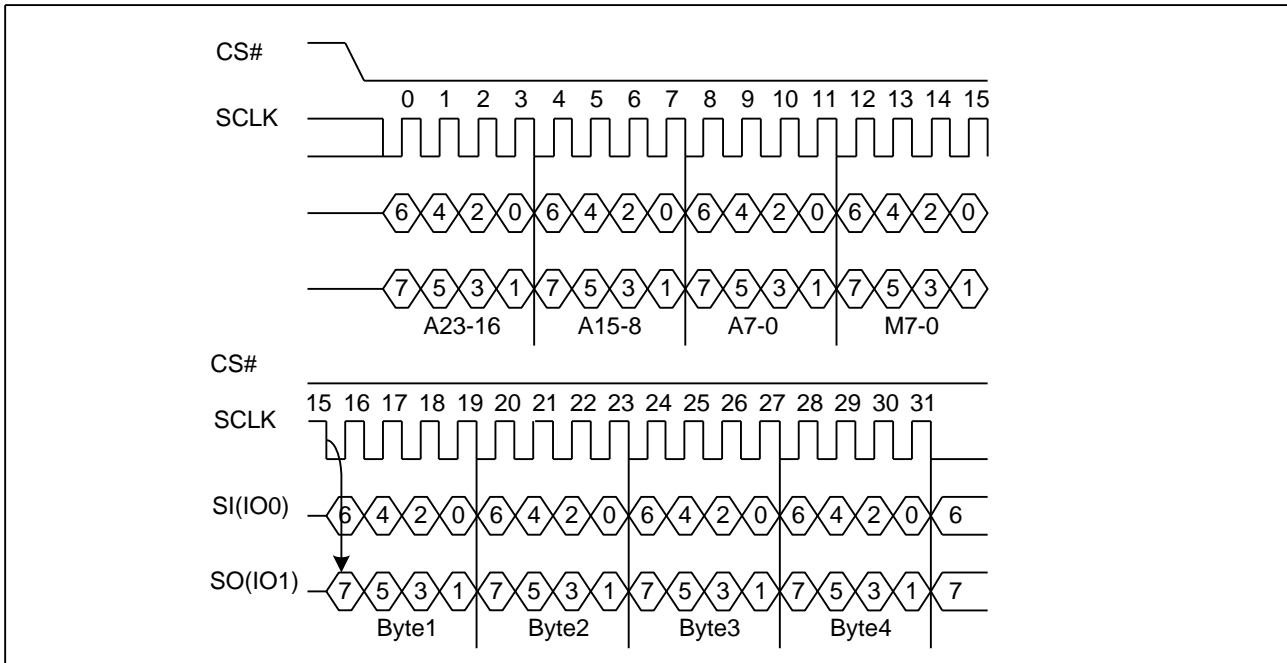
The Dual I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M7-0) = AXH, then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. The command sequence is shown in followed Figure11. If the “Continuous Read Mode” bits (M7-0) are any value other than AXH, the next command requires the first BBH command code, thus returning to normal operation. A “Continuous Read

Mode<sup>®</sup> Reset command can be used to reset (M7-0) before issuing normal command.

**Figure10. Dual I/O Fast Read Sequence Diagram (M7-0= 0XH or not AXH)**



**Figure11. Dual I/O Fast Read Sequence Diagram (M7-0= AXH)**



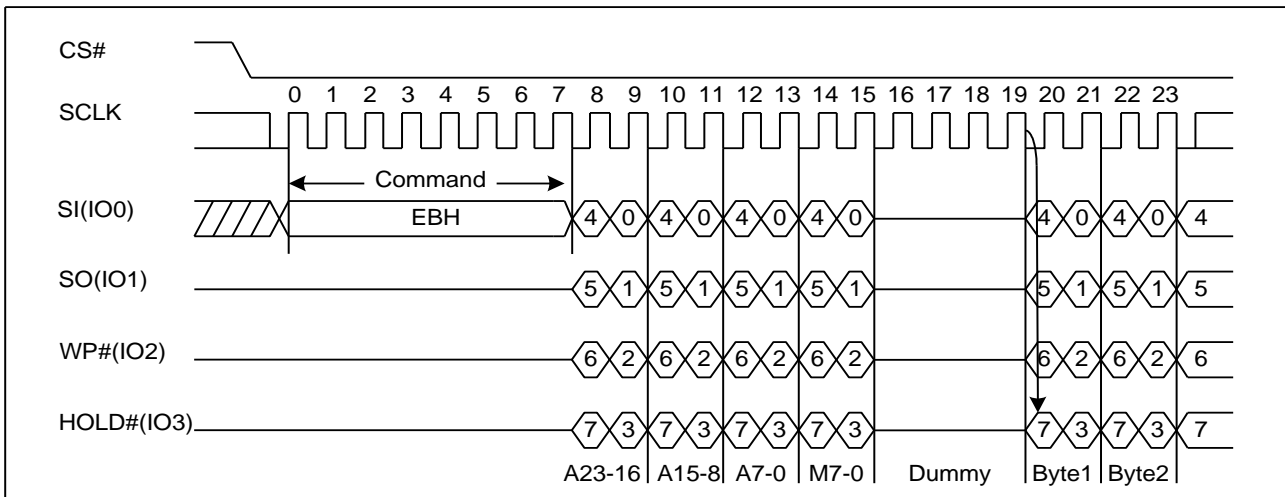
### 7.10. Quad I/O Fast Read (EBH)

The Quad I/O Fast Read command is similar to the Dual I/O Fast Read command but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte and 4-dummy clock 4-bit per clock by IO0, IO1, IO3, IO4, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The command sequence is shown in followed Figure12. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Fast read command. To ensure optimum performance the High Performance Mode (HPM) command (A3H) must be executed once, prior to the Quad I/O Fast Read command.

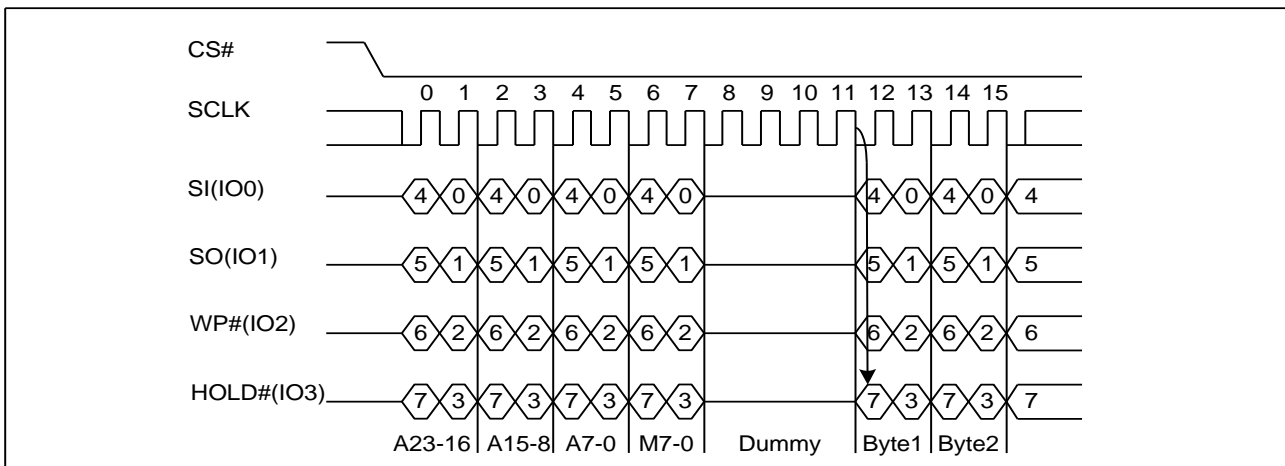
#### Quad I/O Fast Read with “Continuous Read Mode”

The Quad I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M7-0) = AXH, then the next Quad I/O Fast Read command (after CS# is raised and then lowered) does not require the EBH command code. The command sequence is shown in followed Figure13. If the “Continuous Read Mode” bits (M7-0) are any value other than AXH, the next command requires the first EBH command code, thus returning to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M7-0) before issuing normal command.

**Figure12. Quad I/O Fast Read Sequence Diagram (M7-0= 0XH or not AXH)**



**Figure13. Quad I/O Fast Read Sequence Diagram (M7-0= AXH)**



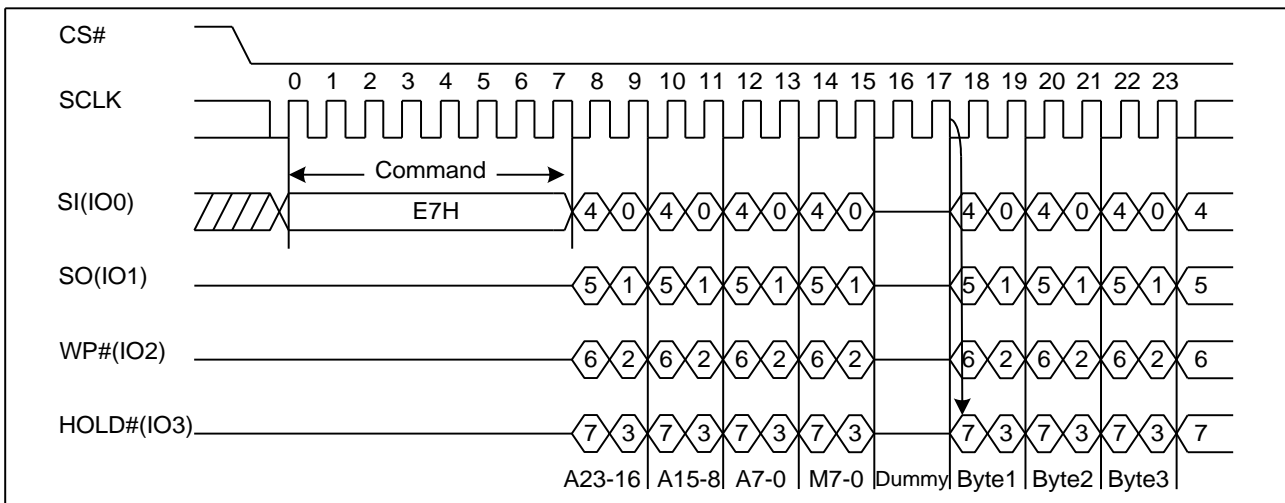
### 7.11. Quad I/O Word Fast Read (E7H)

The Quad I/O Word Fast Read command is similar to the Quad I/O Fast Read command except that the lowest address bit (A0) must equal 0 and only 2-dummy clock. The command sequence is shown in followed Figure14. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Word Fast read command. To ensure optimum performance the High Performance Mode (HPM) command (A3h) must be executed once, prior to the Quad I/O Word Fast Read command.

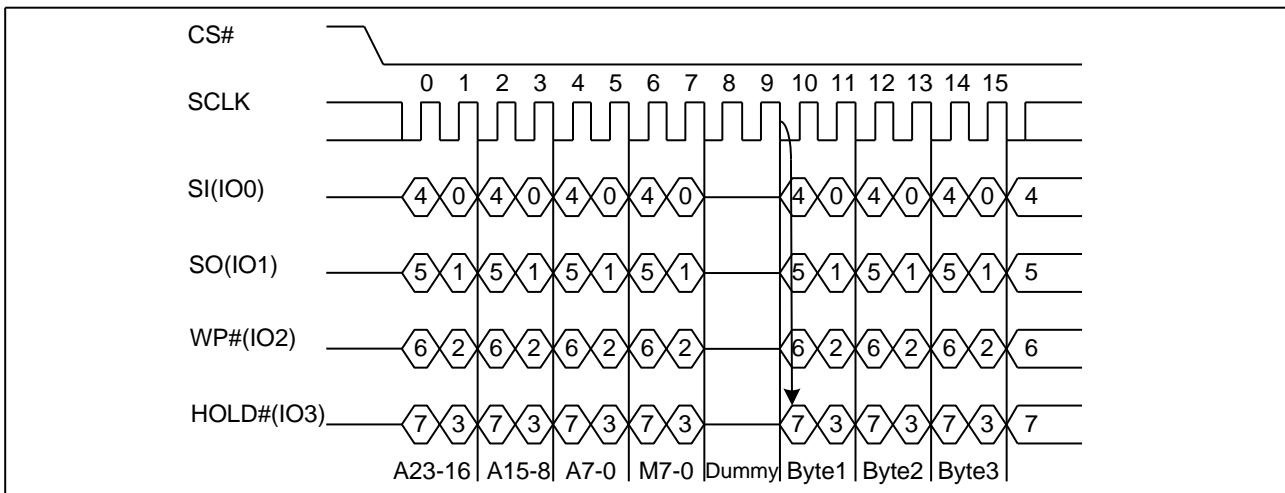
#### Quad I/O Word Fast Read with “Continuous Read Mode”

The Quad I/O Word Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M7-0) = AXH, then the next Quad I/O Word Fast Read command (after CS# is raised and then lowered) does not require the E7H command code. The command sequence is shown in followed Figure15. If the “Continuous Read Mode” bits (M7-0) are any value other than AXH, the next command requires the first E7H command code, thus returning to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M7-0) before issuing normal command.

**Figure14. Quad I/O Word Fast Read Sequence Diagram (M7-0= 0XH or not AXH)**



**Figure15. Quad I/O Word Fast Read Sequence Diagram (M7-0= AXH)**



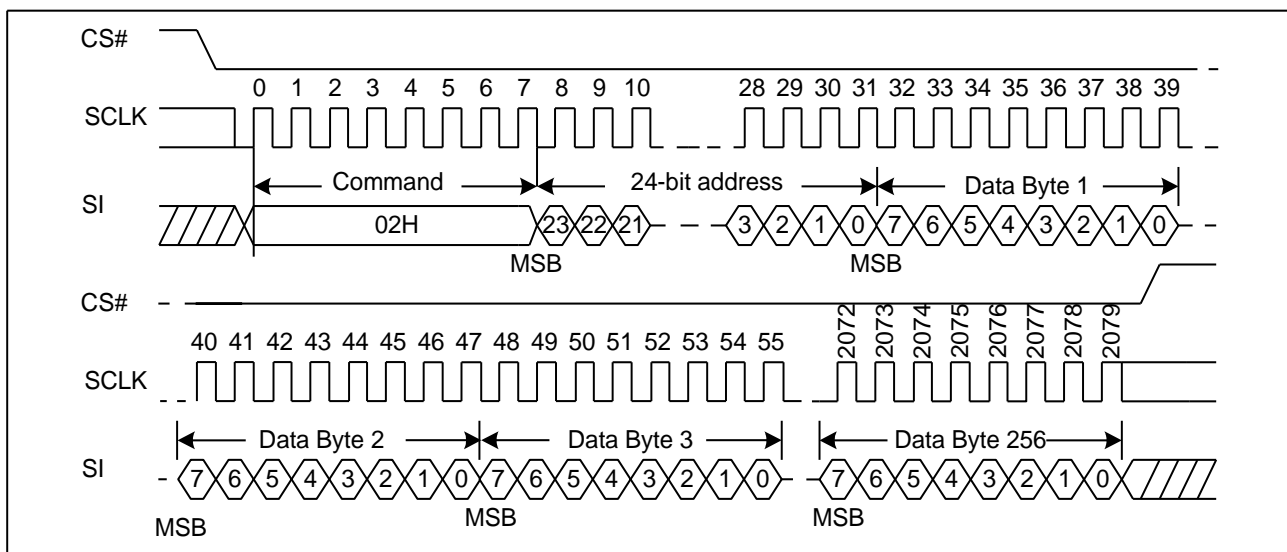
### 7.12. Page Program (PP) (02H)

The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low → sending Page Program command → 3-byte address on SI → at least 1 byte data on SI → CS# goes high. The command sequence is shown in Figure 16. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is  $t_{PP}$ ) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) is not executed.



**Figure 16. Page Program Sequence Diagram**

### 7.13. Quad Page Program (32H)

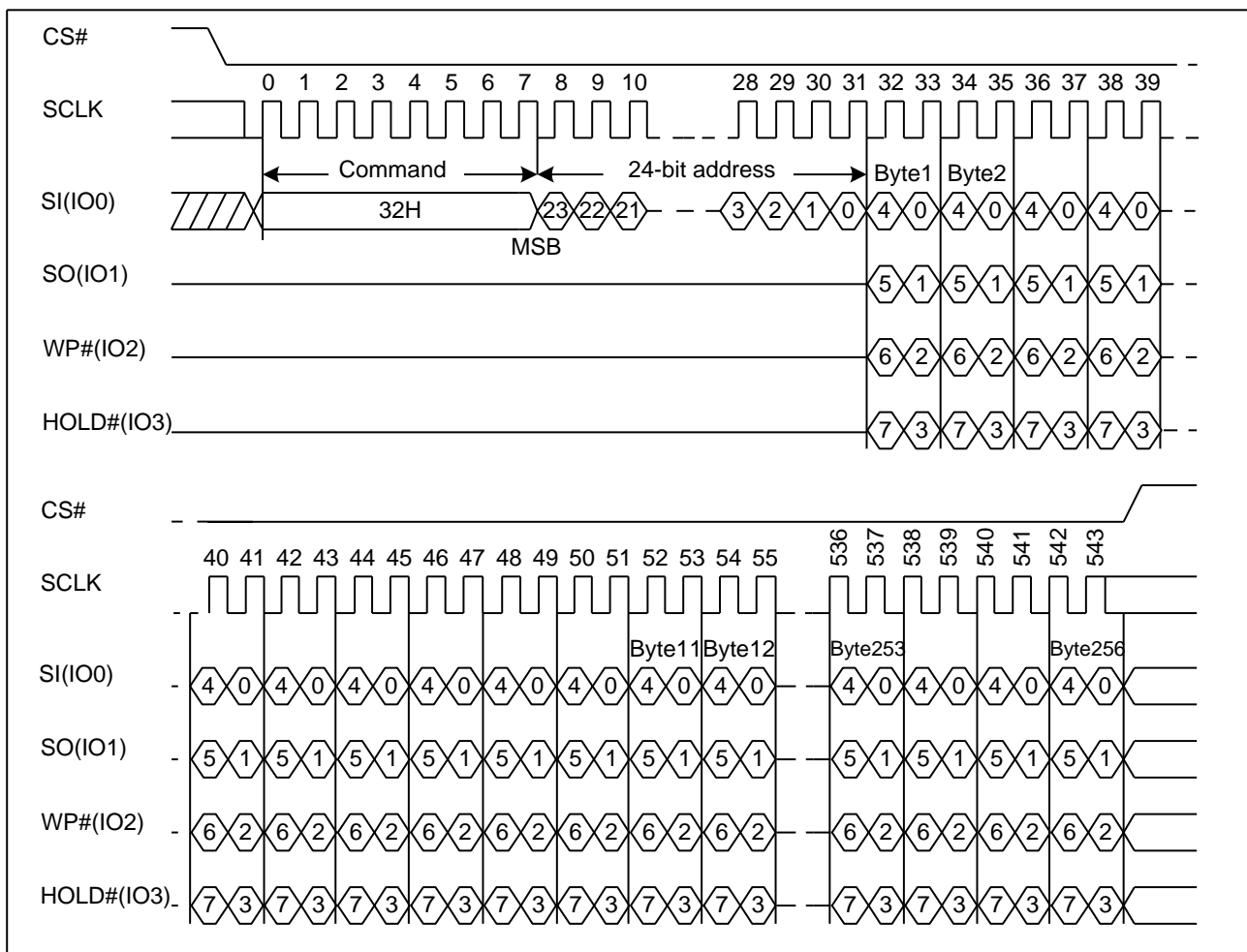
The Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. To use Quad Page Program the Quad enable in status register Bit9 must be set (QE=1). A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The Quad Page Program command is entered by driving CS# Low, followed by the command code (32H), three address bytes and at least one data byte on IO pins.

The command sequence is shown in Figure17. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Quad Page Program command is not executed.

As soon as CS# is driven high, the self-timed Quad Page Program cycle (whose duration is  $t_{PP}$ ) is initiated. While the Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Quad Page Program command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) is not executed.

**Figure17. Quad Page Program Sequence Diagram**



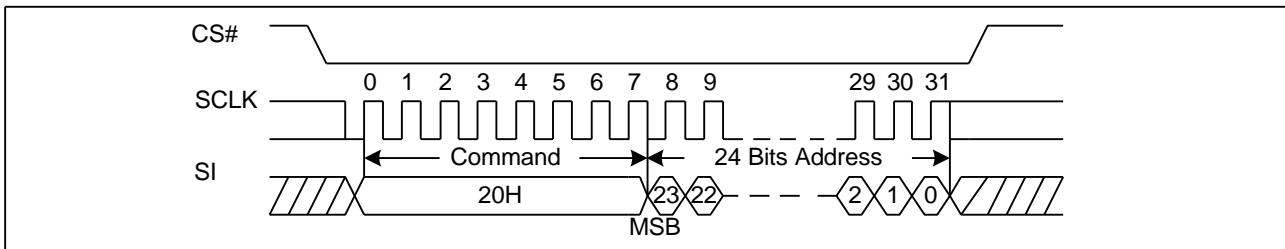


### 7.14. Sector Erase (SE) (20H)

The Sector Erase (SE) command is for erasing the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: CS# goes low → sending Sector Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in Figure18. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is  $t_{SE}$ ) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bit (see Table1.0&1.1) is not executed.

**Figure18. Sector Erase Sequence Diagram**

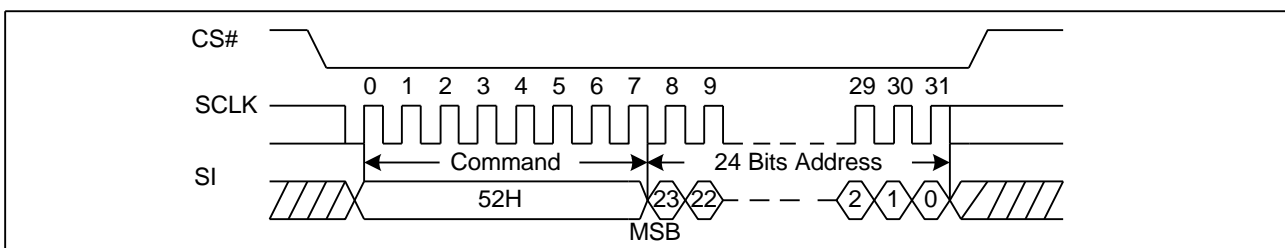


### 7.15. 32KB Block Erase (BE) (52H)

The 32KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 32KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 32KB Block Erase command sequence: CS# goes low → sending 32KB Block Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in Figure19. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is  $t_{BE}$ ) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see Table1.0&1.1) is not executed.

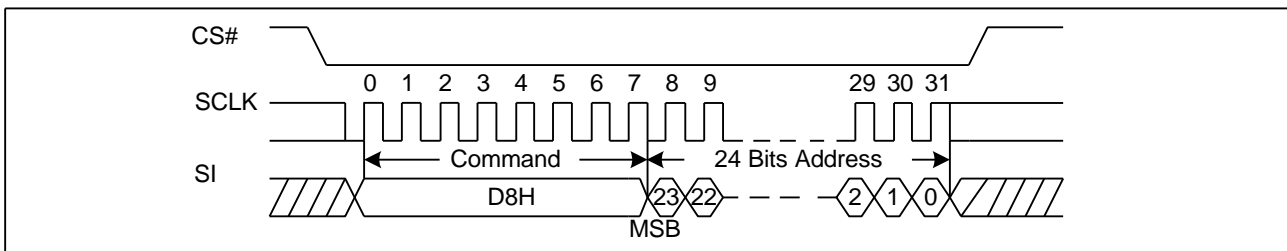
**Figure19. 32KB Block Erase Sequence Diagram**



### 7.16. 64KB Block Erase (BE) (D8H)

The 64KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 64KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 64KB Block Erase command sequence: CS# goes low → sending 64KB Block Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in Figure20. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is  $t_{BE}$ ) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see Table1.0&1.1) is not executed.



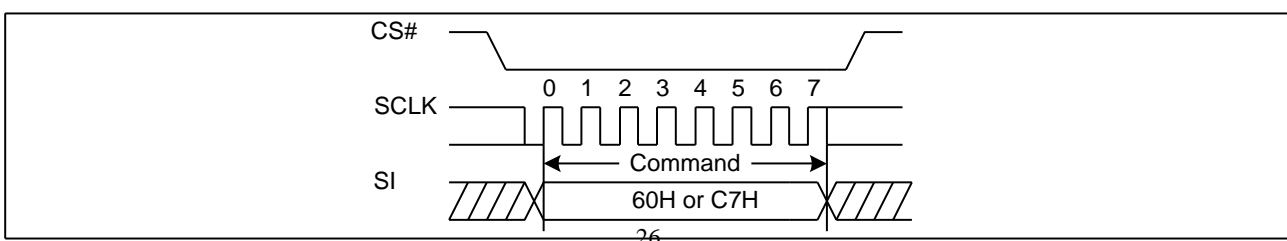
**Figure20. 64KB Block Erase Sequence Diagram**

### 7.17. Chip Erase (CE) (60/C7H)

The Chip Erase (CE) command is for erasing the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low → sending Chip Erase command → CS# goes high. The command sequence is shown in Figure21. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Chip Erase command is not executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is  $t_{CE}$ ) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is executed if the Block Protect (BP2, BP1, BP0) bits and CMP are all 0 or all 1. The Chip Erase (CE) command is ignored if one or more sectors are protected.

**Figure21. Chip Erase Sequence Diagram**



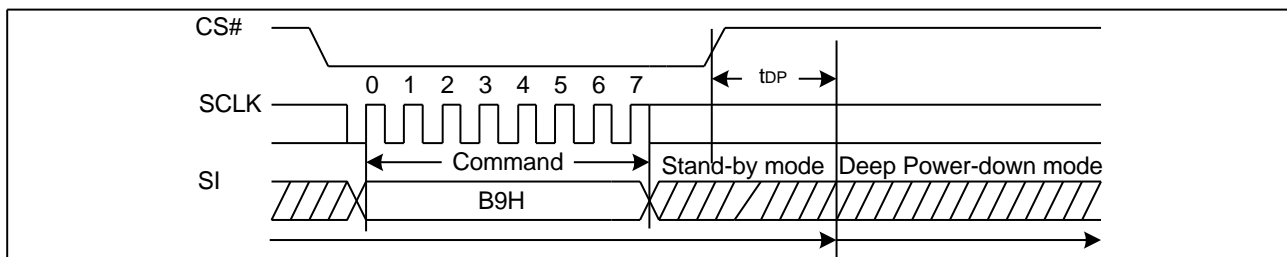
### 7.18. Deep Power-Down (DP) (B9H)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID (RDI) command. This releases the device from this mode. The Release from Deep Power-Down and Read Device ID (RDI) command also allows the Device ID of the device to be output on SO.

The Deep Power-Down Mode automatically stops at Power-Down, and the device always Power-Up in the Standby Mode. The Deep Power-Down (DP) command is entered by driving CS# low, followed by the command code on SI. CS# must be driven low for the entire duration of the sequence.

The Deep Power-Down command sequence: CS# goes low → sending Deep Power-Down command → CS# goes high. The command sequence is shown in Figure22. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of  $t_{DP}$  before the supply current is reduced to  $I_{CC2}$  and the Deep Power-Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

**Figure22. Deep Power-Down Sequence Diagram**



### 7.19. Release from Deep Power-Down Or High Performance Mode And Read Device ID (RDI) (ABH)

The Release from Power-Down or High Performance Mode / Device ID command is a multi-purpose command. It can be used to release the device from the Power-Down state or High Performance Mode or obtain the devices electronic identification (ID) number.

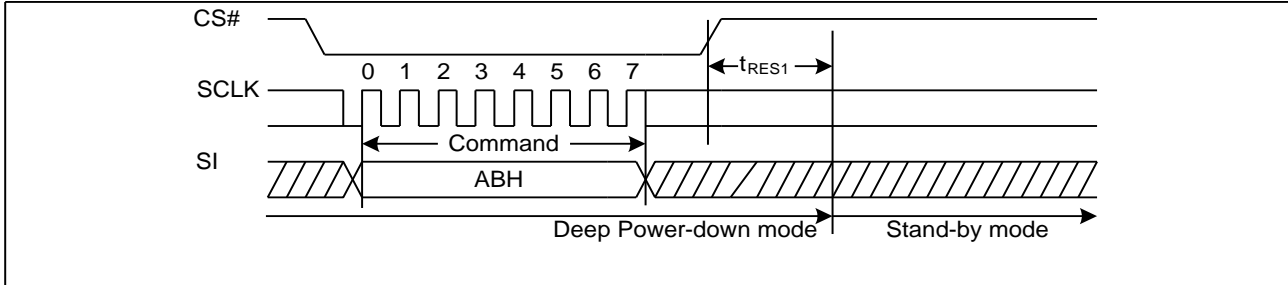
To release the device from the Power-Down state or High Performance Mode, the command is issued by driving the CS# pin low, shifting the instruction code “ABH” and driving CS# high as shown in Figure23. Release from Power-Down will take the time duration of  $t_{RES1}$  (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the  $t_{RES1}$  time duration.

When used only to obtain the Device ID while not in the Power-Down state, the command is initiated by driving the CS# pin low and shifting the instruction code “ABH” followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure23. The Device ID value for the GD25Q64B is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

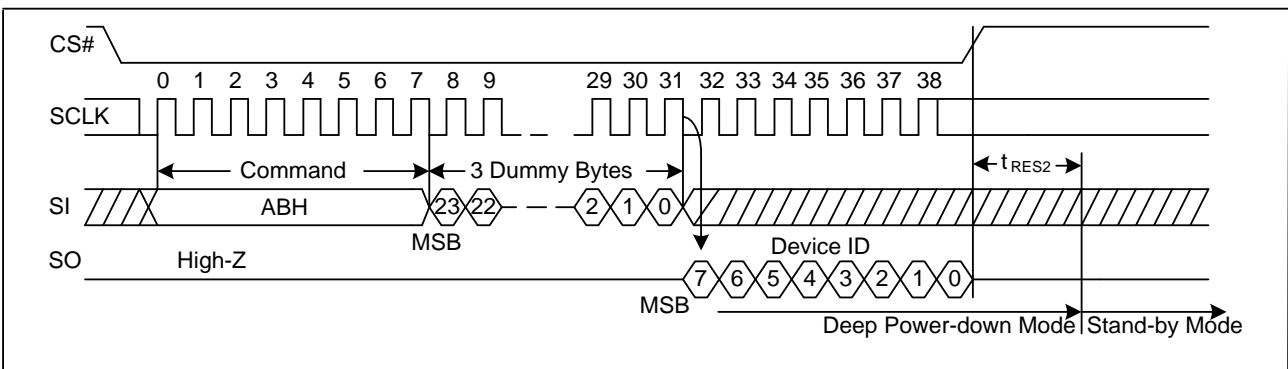
When used to release the device from the Power-Down state and obtain the Device ID, the command is the same as previously described, and shown in Figure23, except that after CS# is driven high it must remain high for a time

duration of  $t_{RES2}$  (See AC Characteristics). After this time duration the device will resume normal operation and other command will be accepted. If the Release from Power-Down / Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the command is ignored and will not have any effects on the current cycle.

**Figure23. Release Power-Down or High Performance Mode Sequence Diagram**



**Figure24. Release Power-Down/Read Device ID Sequence Diagram**

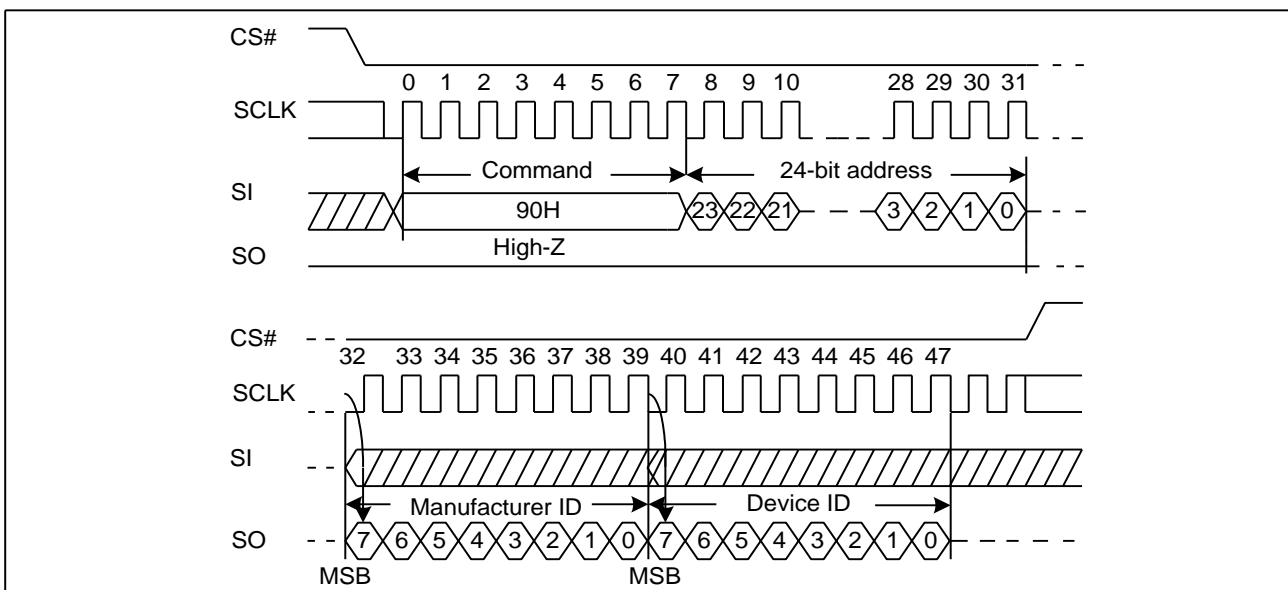


## 7.20. Read Manufacture ID/ Device ID (REMS) (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code “90H” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure25. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

**Figure25. Read Manufacture ID/ Device ID Sequence Diagram**

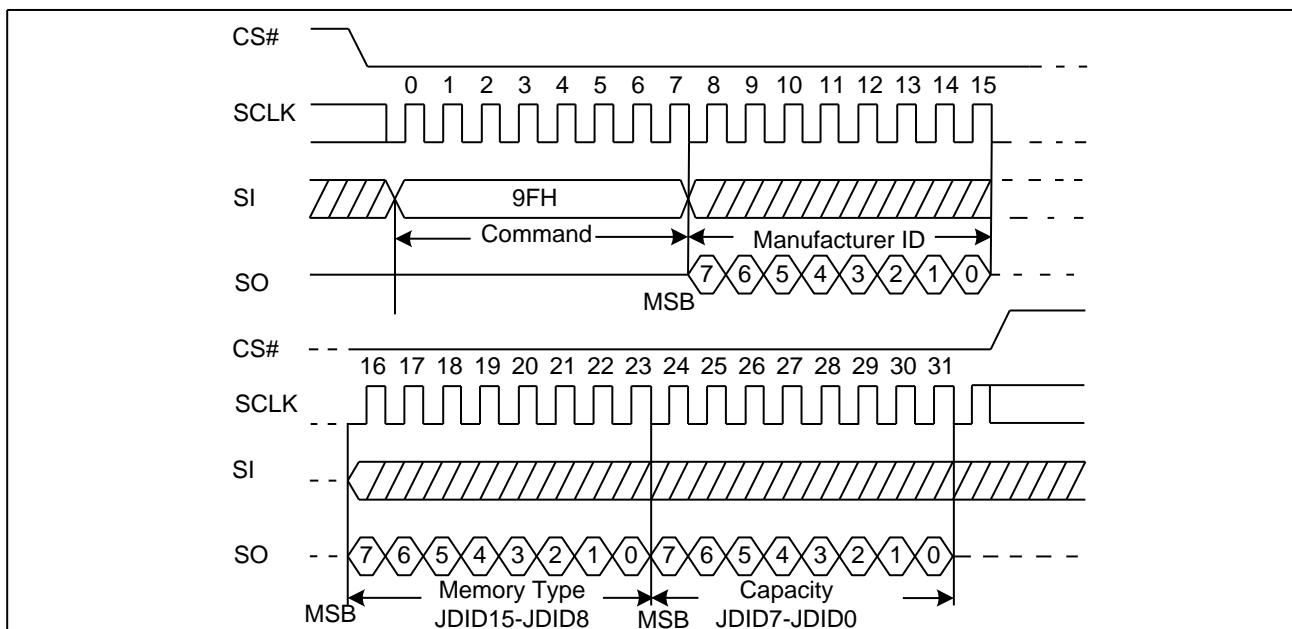


## 7.21. Read Identification (RDID) (9FH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. Any Read Identification (RDID) command while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# to low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The command sequence is shown in Figure26. The Read Identification (RDID) command is terminated by driving CS# to high at any time during data output. When CS# is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

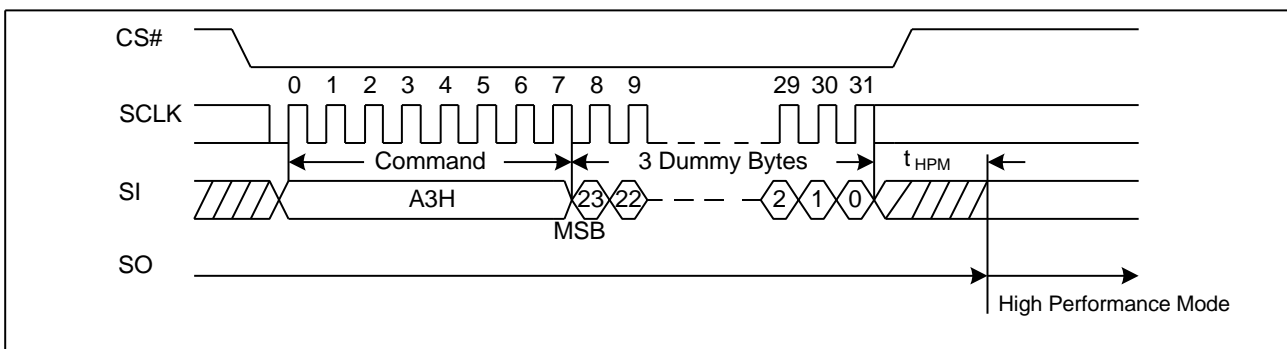
Figure26. Read Identification ID Sequence Diagram



### 7.22. High Performance Mode (HPM) (A3H)

The High Performance Mode (HPM) command must be executed prior to Dual or Quad I/O commands when operating at high frequencies (see  $f_R$  and  $f_{C1}$  in AC Electrical Characteristics). This command allows pre-charging of internal charge pumps so the voltages required for accessing the flash memory array are readily available. The command sequence: CS# goes low → Sending A3H command → Sending 3-dummy byte → CS# goes high. See Figure27. After the HPM command is executed, the device will maintain a slightly higher standby current ( $I_{cc8}$ ) than standard SPI operation. The Release from Power-Down or HPM command (ABH) can be used to return to standard SPI standby current ( $I_{cc1}$ ). In addition, Write Enable command (06H) and Power-Down command (B9H) will also release the device from HPM mode back to standard SPI standby state.

**Figure27. High Performance Mode Sequence Diagram**

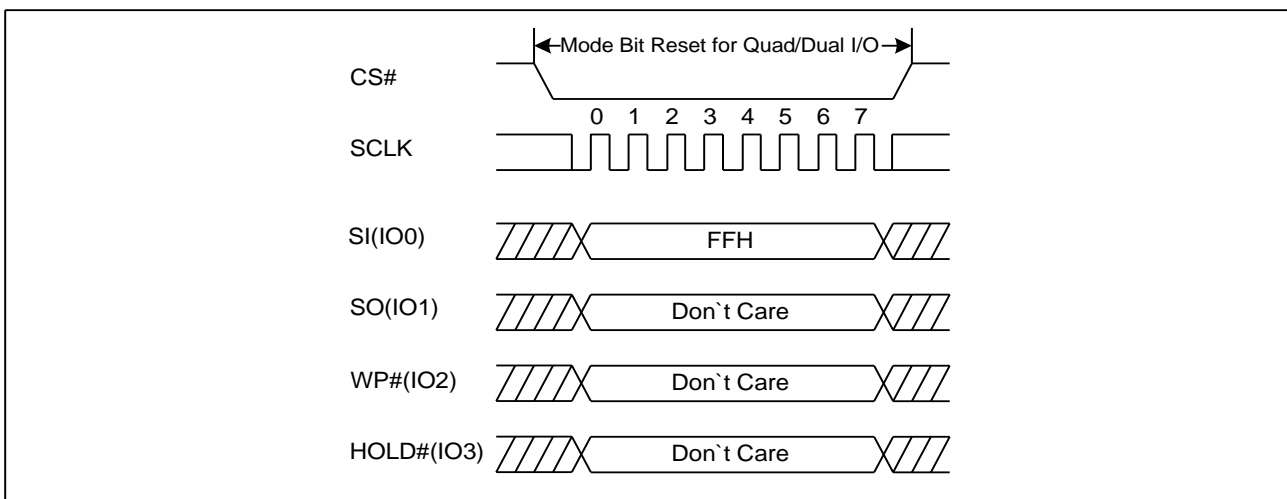


### 7.23. Continuous Read Mode Reset (CRMR) (FFH)

The Dual/Quad I/O Fast Read operations, “Continuous Read Mode” bits (M7-0) are implemented to further reduce command overhead. By setting the (M7-0) to AXH, the next Dual/Quad I/O Fast Read operations do not require the BBH/EBH/E7H command code.

Because the GD25Q64B has no hardware reset pin, so if Continuous Read Mode bits are set to “AXH”, the GD25Q64B will not recognize any standard SPI commands. So Continuous Read Mode Reset command will release the Continuous Read Mode from the “AXH” state and allow standard SPI command to be recognized. The command sequence is show in Figure28.

**Figure28. Continuous Read Mode Reset Sequence Diagram**

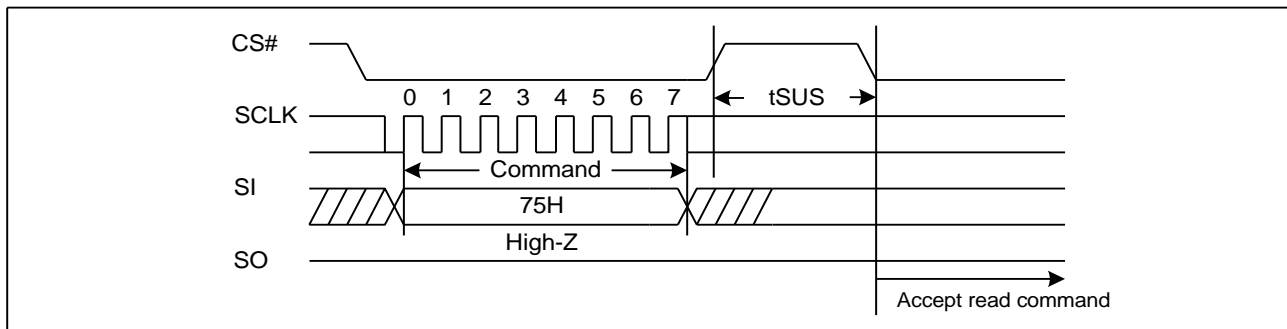


### 7.24. Program/Erase Suspend (PES) (75H)

The Program/Erase Suspend command “75H”, allows the system to interrupt a page program or sector/block erase operation and then read data from any other sector or block. The Write Status Register command (01H) and Erase Security Registers (44H, 42H) and Erase commands (20H, 52H, D8H, C7H, 60H) and Page Program command are not allowed during Program/Erase suspend. Program/Erase Suspend is valid only during the page program or sector/block erase operation. A maximum of time of “tsus” (See AC Characteristics) is required to suspend the program/erase operation.

The Program/Erase Suspend command will be accepted by the device only if the SUS bit in the Status Register equal to 0 and WIP bit equal to 1 while a Page Program or a Sector or Block Erase operation is on-going. If the SUS bit equal to 1 or WIP bit equal to 0, the Suspend command will be ignored by the device. The WIP bit will be cleared from 1 to 0 within “tsus” and the SUS bit will be set from 0 to 1 immediately after Program/Erase Suspend. A power-off during the suspend period will reset the device and release the suspend state. The command sequence is show in Figure29.

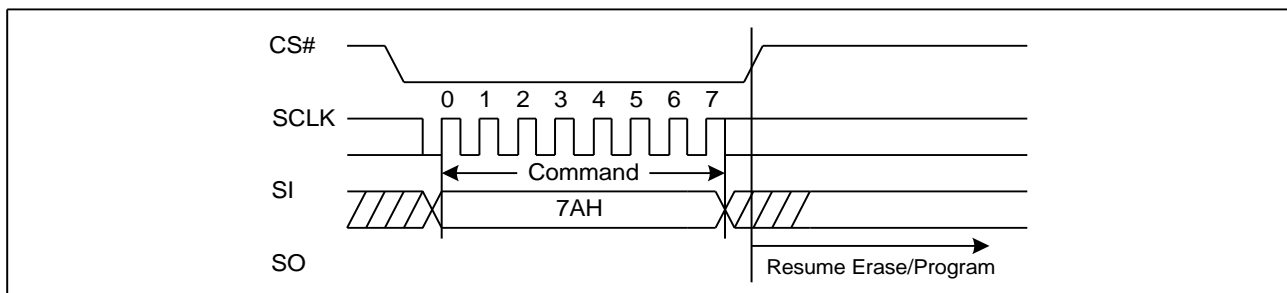
**Figure29. Program/Erase Suspend Sequence Diagram**



### 7.25. Program/Erase Resume (PER) (7AH)

The Program/Erase Resume command must be written to resume the program or sector/block erase operation after a Program/Erase Suspend command. The Program/Erase command will be accepted by the device only if the SUS bit equal to 1 and the WIP bit equal to 0. After issued the SUS bit in the status register will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. The Program/Erase Resume command will be ignored unless a Program/Erase Suspend is active. The command sequence is show in Figure30.

**Figure30. Program/Erase Resume Sequence Diagram**



## 7.26. Erase Security Registers (44H)

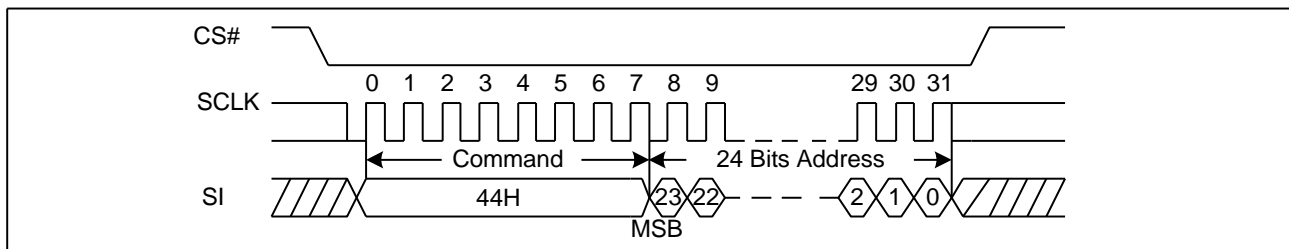
The GD25Q64B provides four 256-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low → sending Erase Security Registers command → CS# goes high. The command sequence is shown in Figure31. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is  $t_{SE}$ ) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock Bit (LB) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers command will be ignored.

Address	A23-A16	A15-A10	A9-A0
Security Registers	00000000	000000	Don't Care

**Figure31. Erase Security Registers command Sequence Diagram**





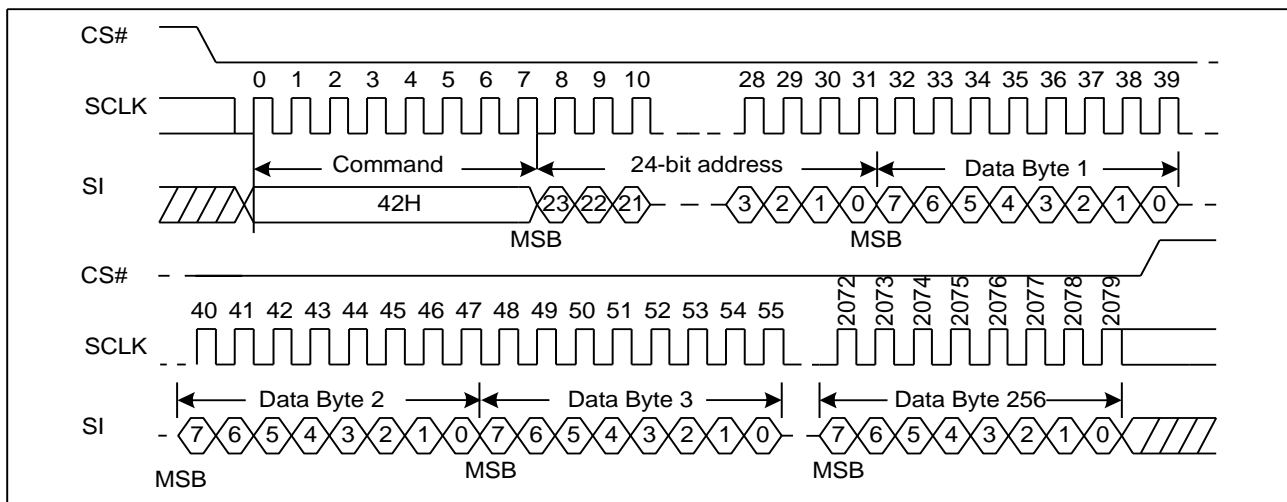
### 7.27. Program Security Registers (42H)

The Program Security Registers command is similar to the Page Program command. It allows from 1 to 256 bytes Security Registers data to be programmed. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving CS# Low, followed by the command code (42H), three address bytes and at least one data byte on SI. As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is  $t_{PP}$ ) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the Security Registers Lock Bit (LB) is set to 1, the Security Registers will be permanently locked. Program Security Registers command will be ignored.

Address	A23-A16	A15-A8	A7-A0
Security Registers 0	00H	00H	Byte Address
Security Registers 1	00H	01H	Byte Address
Security Registers 2	00H	02H	Byte Address
Security Registers 3	00H	03H	Byte Address

Figure32. Program Security Registers command Sequence Diagram

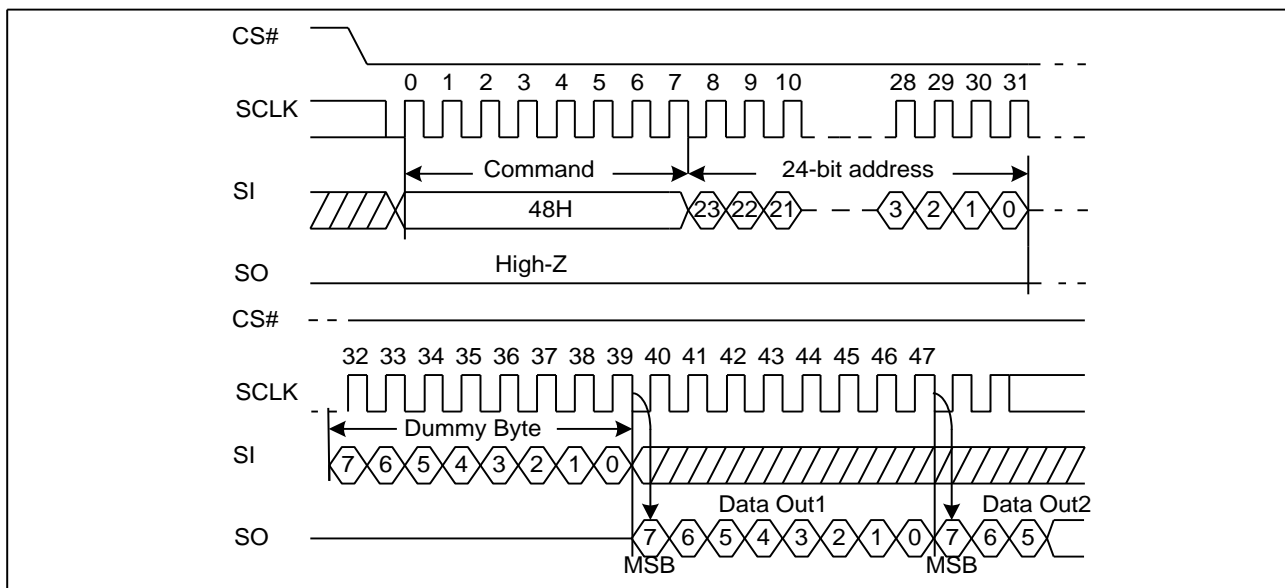


## 7.28. Read Security Registers (48H)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency  $f_c$ , during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Once the A9-A0 address reaches the last byte of the register (Byte 3FFH), it will reset to 000H, the command is completed by driving CS# high.

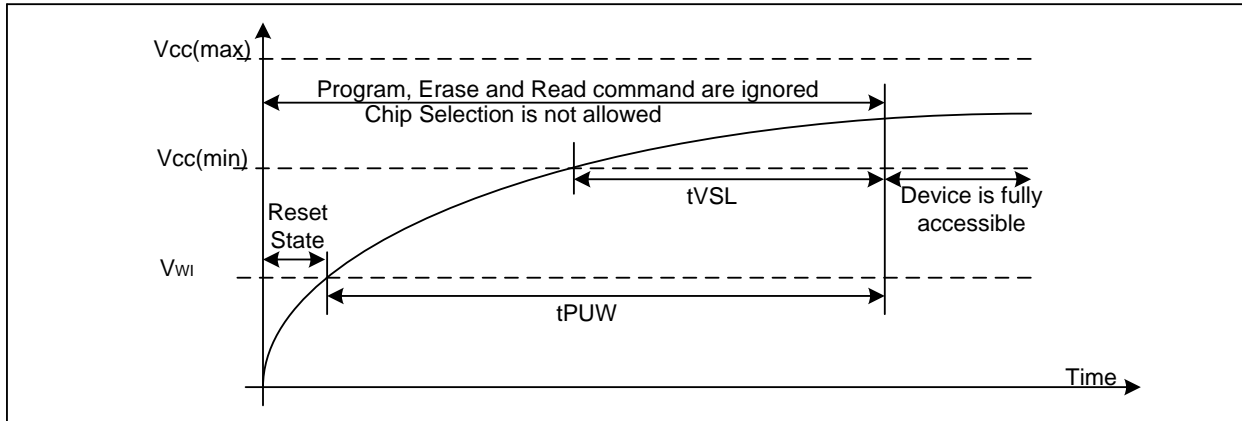
Address	A23-A16	A15-A10	A9-A0
Security Registers	00000000	000000	Address

Figure33. Read Security Registers command Sequence Diagram



## 8. ELECTRICAL CHARACTERISTICS

### 8.1. POWER-ON TIMING



**Table3. Power-Up Timing and Write Inhibit Threshold**

Symbol	Parameter	Min	Max	Unit
tVSL	VCC(min) To CS# Low	5		ms
tPUW	Time Delay Before Write Instruction	5	10	ms
VWI	Write Inhibit Voltage	1	2.5	V

### 8.2. INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFH). The Status Register contains 00H (all Status Register bits are 0).

### 8.3. DATA RETENTION AND ENDURANCE

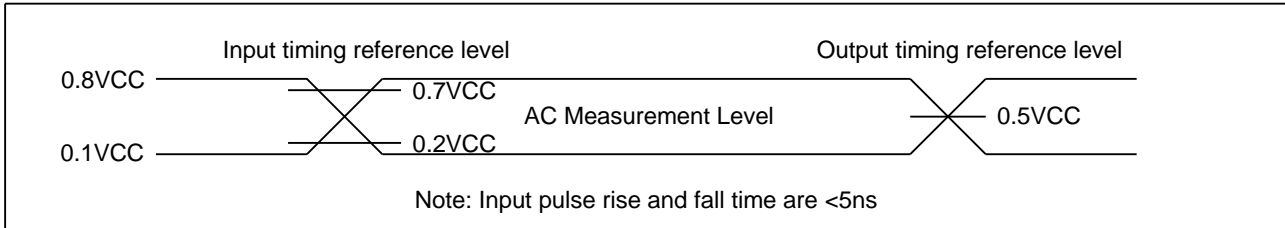
Parameter	Test Condition	Min	Units
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years
Erase/Program Endurance	-40 to 85°C	100K	Cycles

### 8.4. LATCH UP CHARACTERISTICS

Parameter	Min	Max
Input Voltage Respect To VSS On I/O Pins	-1.0V	VCC+1.0V
VCC Current	-100mA	100mA

**8.5. ABSOLUTE MAXIMUM RATINGS**

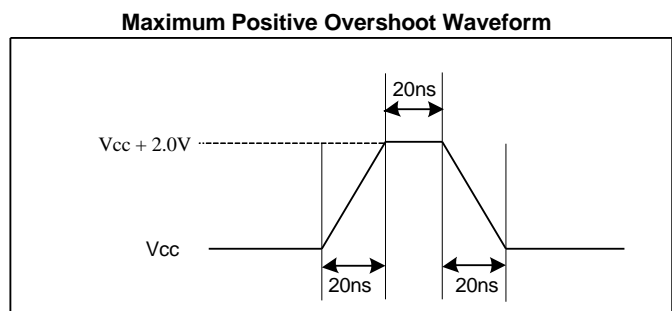
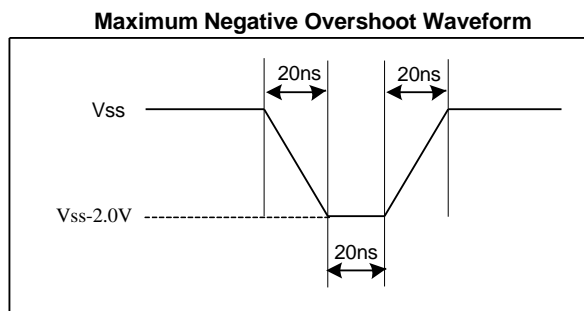
Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	°C
Storage Temperature	-65 to 150	°C
Output Short Circuit Current	200	mA
Applied Input/Output Voltage	-0.5 to 4.0	V
VCC	-0.5 to 4.0	V



**8.6. CAPACITANCE MEASUREMENT CONDITIONS**

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
CL	Load Capacitance	30			pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.1VCC to 0.8VCC			V	
	Input Timing Reference Voltage	0.2VCC to 0.7VCC			V	
	Output Timing Reference Voltage	0.5VCC			V	

**Figure34. Input Test Waveform and Measurement Level**





**8.7. DC CHARACTERISTICS**

(T= -40°C~85°C, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ	Max.	Unit.
I <sub>LI</sub>	Input Leakage Current				±2	μA
I <sub>LO</sub>	Output Leakage Current				±2	μA
I <sub>CC1</sub>	Standby Current	CS#=VCC, V <sub>IN</sub> =VCC or VSS		1	5	μA
I <sub>CC2</sub>	Deep Power-Down Current	CS#=VCC, V <sub>IN</sub> =VCC or VSS		1	5	μA
I <sub>CC3</sub>	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 120MHz, Q=Open(*1 I/O)		15	20	mA
		CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(*1,*2,*4 I/O)		13	18	mA
I <sub>CC4</sub>	Operating Current (PP)	CS#=VCC			10	mA
I <sub>CC5</sub>	Operating Current(WRSR)	CS#=VCC			10	mA
I <sub>CC6</sub>	Operating Current (SE)	CS#=VCC			10	mA
I <sub>CC7</sub>	Operating Current (BE)	CS#=VCC			10	mA
I <sub>CC8</sub>	High Performance Current			600	800	uA
V <sub>IL</sub>	Input Low Voltage		-0.5		0.2VCC	V
V <sub>IH</sub>	Input High Voltage		0.7VCC		VCC+0.4	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> =1.6mA			0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> =-100μA	VCC-0.2			V



**8.8. AC CHARACTERISTICS**

(T= -40°C~85°C, VCC=2.7~3.6V, CL=30pf)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
f <sub>c</sub>	Serial Clock Frequency For: FAST_READ(0BH), Dual Output(3BH)	DC.		120	MHz
f <sub>c1</sub>	Serial Clock Frequency For: Dual I/O(BBH), Quad I/O(EBH), Quad Output(6BH) (Dual I/O & Quad I/O With High Performance Mode)	DC.	80	120	MHz
f <sub>c2</sub>	Serial Clock Frequency For: Dual I/O(BBH), Quad I/O(EBH) (Dual I/O & Quad I/O Without High Performance Mode), on 3.0V~3.6V power supply	DC.		104	MHz
f <sub>c3</sub>	Serial Clock Frequency For: Fast Read(0BH) (with/without High Performance Mode), on 2.7V-3.6V power supply	DC.		120	MHz
f <sub>R</sub>	Serial Clock Frequency For: Read(03H), Read Status Register (05H, 15H, 35H) Read Device ID (ABH, 90H, 92H, 94H, 9FH)	DC.		80	MHz
t <sub>CLH</sub>	Serial Clock High Time	4			ns
t <sub>CLL</sub>	Serial Clock Low Time	4			ns
t <sub>CLCH</sub>	Serial Clock Rise Time (Slew Rate)	0.1			V/ns
t <sub>CHCL</sub>	Serial Clock Fall Time (Slew Rate)	0.1			V/ns
t <sub>SLCH</sub>	CS# Active Setup Time	5			ns
t <sub>CHSH</sub>	CS# Active Hold Time	5			ns
t <sub>SHCH</sub>	CS# Not Active Setup Time	5			ns
t <sub>CHSL</sub>	CS# Not Active Hold Time	5			ns
t <sub>SHSL</sub>	CS# High Time (read/write)	20			ns
t <sub>SHQZ</sub>	Output Disable Time			6	ns
t <sub>CLQX</sub>	Output Hold Time	1.0			ns
t <sub>DVCH</sub>	Data In Setup Time	2			ns
t <sub>CHDX</sub>	Data In Hold Time	2			ns
t <sub>HLCH</sub>	Hold# Low Setup Time (relative to Clock)	5			ns
t <sub>HHCH</sub>	Hold# High Setup Time (relative to Clock)	5			ns
t <sub>CHHL</sub>	Hold# High Hold Time (relative to Clock)	5			ns
t <sub>CHHH</sub>	Hold# Low Hold Time (relative to Clock)	5			ns
t <sub>HLQZ</sub>	Hold# Low To High-Z Output			6	ns
t <sub>HHQX</sub>	Hold# Low To Low-Z Output			6	ns
t <sub>CLQV</sub>	Clock Low To Output Valid			6.5	ns
t <sub>WHSL</sub>	Write Protect Setup Time Before CS# Low	20			ns
t <sub>SHWL</sub>	Write Protect Hold Time After CS# High	100			ns
t <sub>DP</sub>	CS# High To Deep Power-Down Mode			0.1	μs
t <sub>RES1</sub>	CS# High To Standby Mode Without Electronic Signature Read			0.1	μs
t <sub>RES2</sub>	CS# High To Standby Mode With Electronic Signature			0.1	μs



**Uniform Sector  
Dual and Quad Serial Flash**

**GD25Q64B**

	Read				
t <sub>HPM</sub>	CS# High To High Performance Mode			0.2	us
t <sub>SUS</sub>	CS# High To Next Command After Suspend			2	us
t <sub>w</sub>	Write Status Register Cycle Time		2	15	ms
t <sub>PP</sub>	Page Programming Time		0.4	2.4	ms
t <sub>SE</sub>	Sector Erase Time		40	300/500(1)	ms
t <sub>BE</sub>	Block Erase Time(32K Bytes)		200	500/700(2)	ms
t <sub>BE</sub>	Block Erase Time(64K Bytes)		400	600/800(3)	ms
t <sub>CE</sub>	Chip Erase Time(GD25Q64B)		30	60	s
t <sub>RST_R</sub>	CS# High To Next Command After Reset (from read)			20	μs
t <sub>RST_P</sub>	CS# High To Next Command After Reset (from program)			20	μs
t <sub>RST_E</sub>	CS# High To Next Command After Reset (from erase)			12	ms

**Note:**

1. Max Value t<sub>SE</sub> with <50K cycles is 300ms and >50K & <100k cycles is 500ms.
2. Max Value 32KB t<sub>BE</sub> with <50K cycles is 500ms and >50K & <100k cycles is 700ms.
3. Max Value 64KB t<sub>BE</sub> with <50K cycles is 600ms and >50K & <100k cycles is 800ms.

Figure35. Serial Input Timing

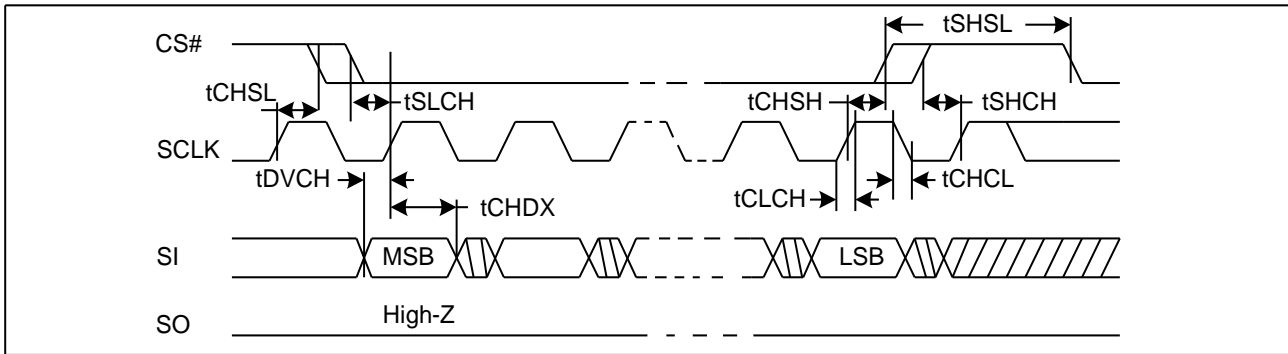


Figure36. Output Timing

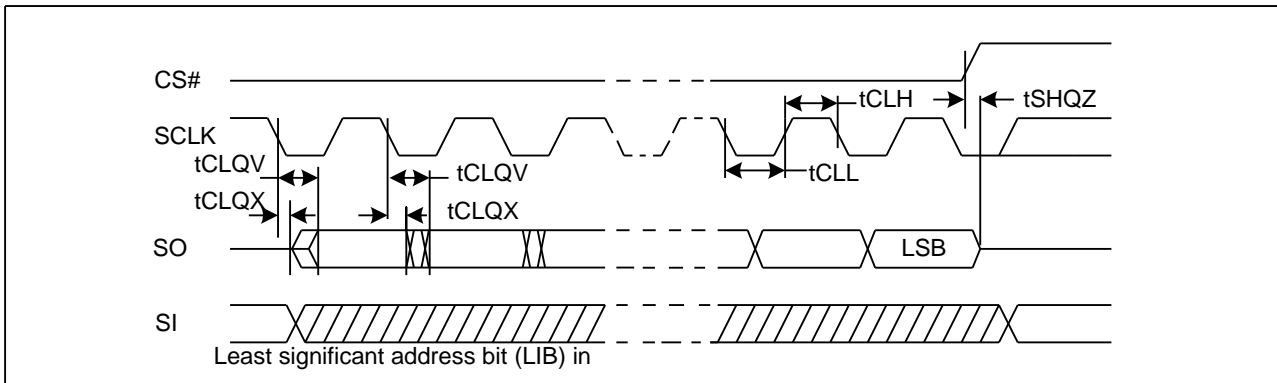
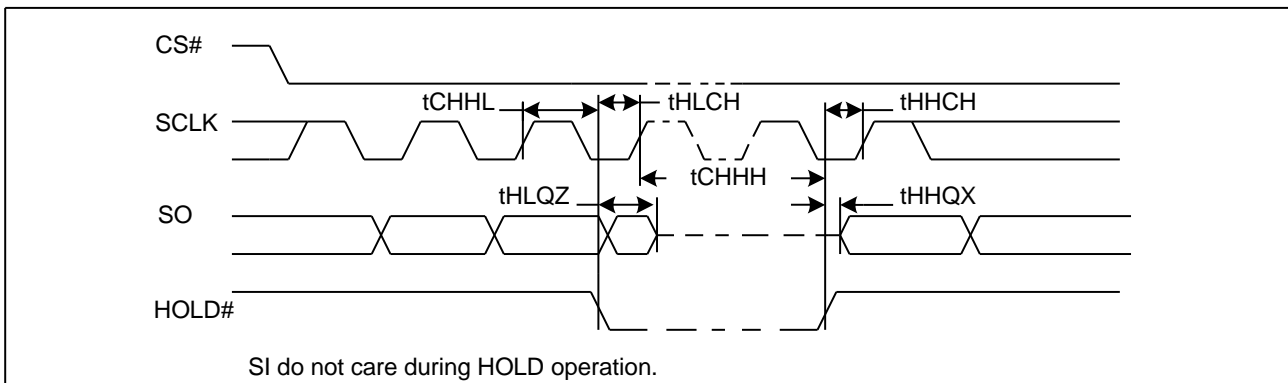


Figure37. Hold Timing

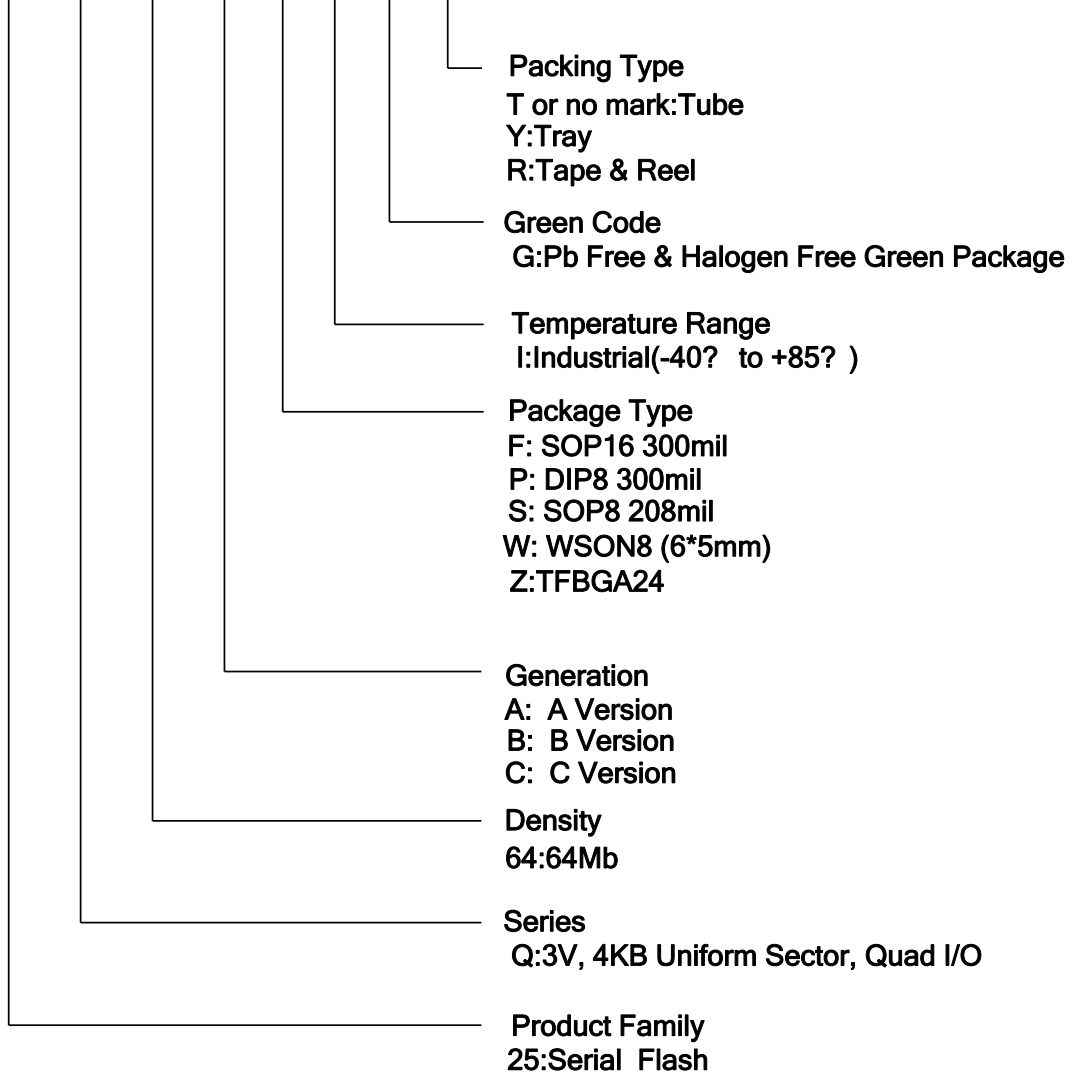






**9. ORDERING INFORMATION**

**GD XX X XX X X X X X**

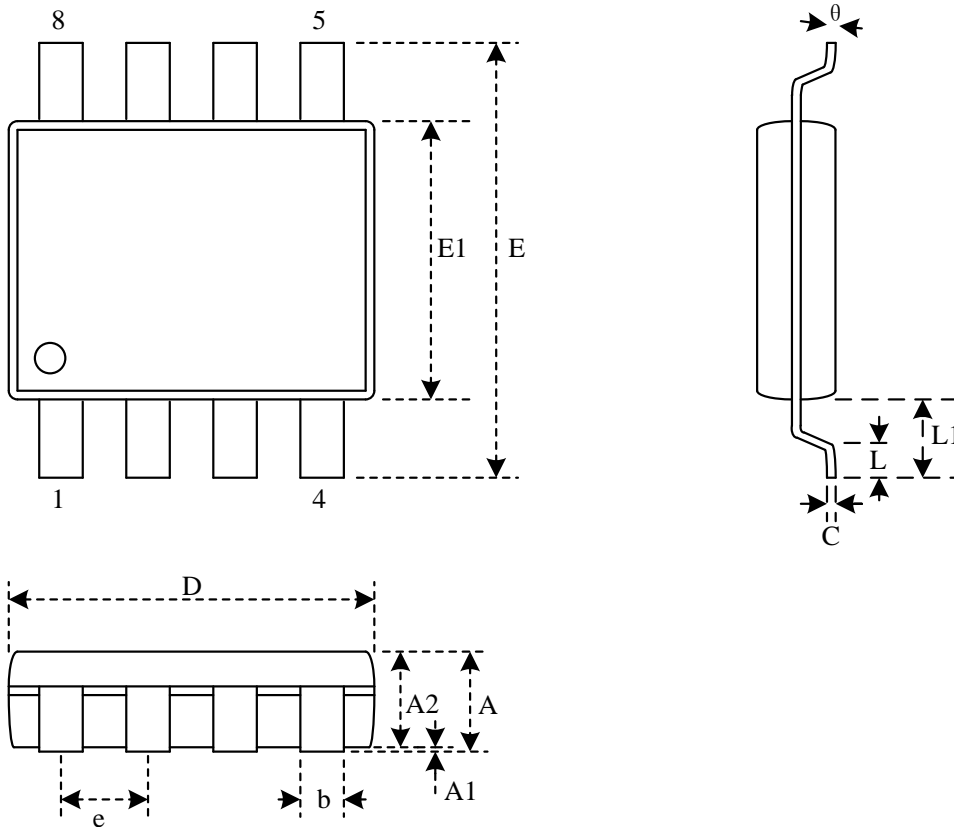


**NOTE:**

1. Standard bulk shipment is in Tube. Any alternation of packing method (for Tape, Reel and Tray etc.), please advise in advance.

## 10. PACKAGE INFORMATION

### 10.1. Package SOP8 208MIL

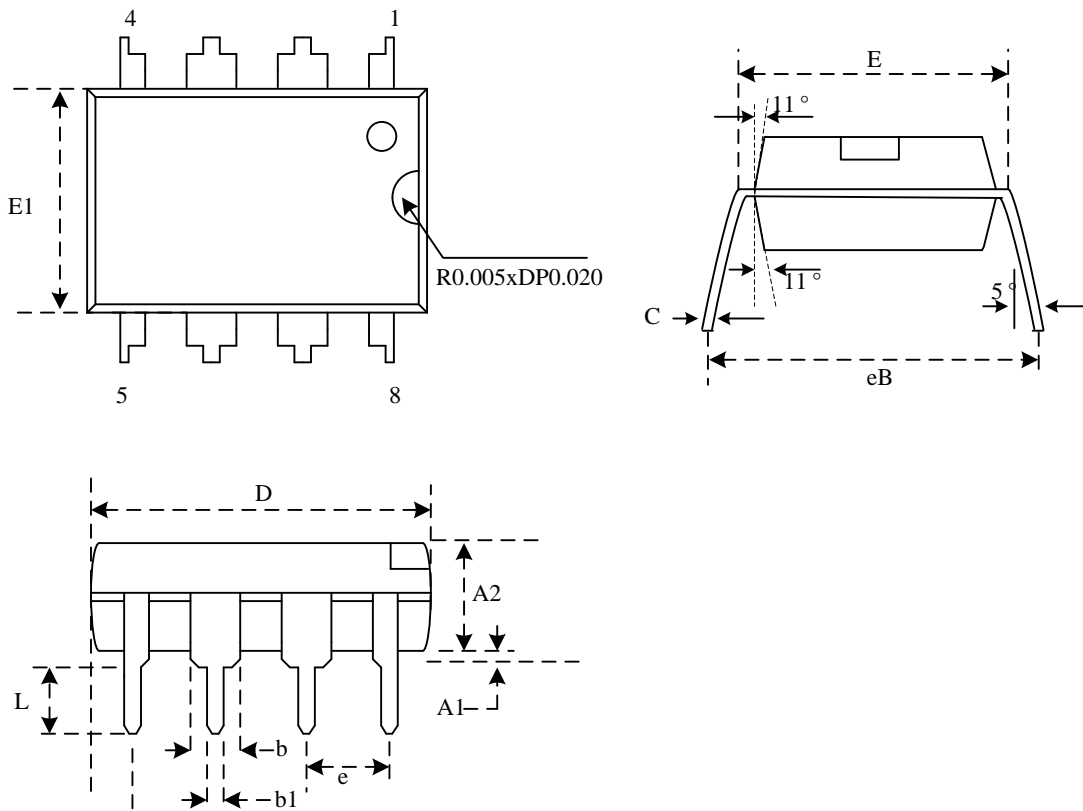


### Dimensions

Symbol		A	A1	A2	b	C	D	E	E1	e	L	L1	$\theta$
Unit													
mm	Min		0.05	1.70	0.31	0.18	5.13	7.70	5.18		0.50	1.21	0
	Nom		0.15	1.80	0.41	0.21	5.23	7.90	5.28	1.27	0.67	1.31	5
	Max	2.16	0.25	1.91	0.51	0.25	5.33	8.10	5.38		0.85	1.41	8
Inch	Min		0.002	0.067	0.012	0.007	0.202	0.303	0.204		0.020	0.048	0
	Nom		0.006	0.071	0.016	0.008	0.206	0.311	0.208	0.050	0.026	0.052	5
	Max	0.085	0.010	0.075	0.020	0.010	0.210	0.319	0.212		0.033	0.056	8

Note: Both package length and width do not include mold flash.

10.2. Package DIP8 300MIL

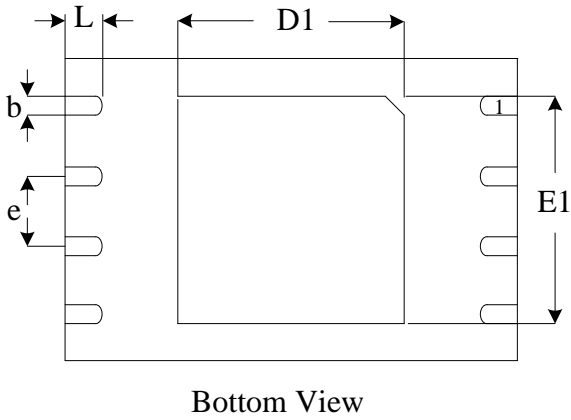
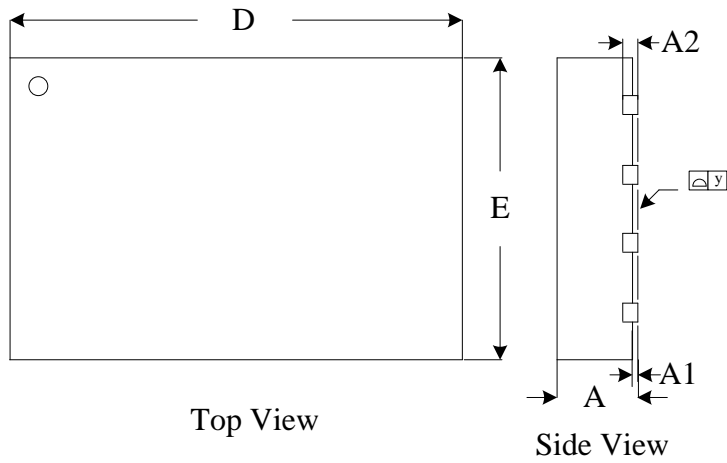


Dimensions

Symbol		A1	A2	b	b1	C	D	E	E1	e	eB	L
Unit												
mm	Min	0.38	3.00	1.27	0.38	0.20	9.05	7.62	6.12		7.62	3.04
	Nom	0.72	3.25	1.46	0.46	0.28	9.32	7.94	6.38	2.54	8.49	3.30
	Max	1.05	3.50	1.65	0.54	0.34	9.59	8.26	6.64		9.35	3.56
Inch	Min	0.015	0.118	0.05	0.015	0.008	0.356	0.300	0.242		0.333	0.12
	Nom	0.028	0.128	0.058	0.018	0.011	0.367	0.313	0.252	0.1	0.345	0.13
	Max	0.041	0.138	0.065	0.021	0.014	0.378	0.326	0.262		0.357	0.14

Note: Both package length and width do not include mold flash.

**10.3. Package WSON8 (6\*5mm)**

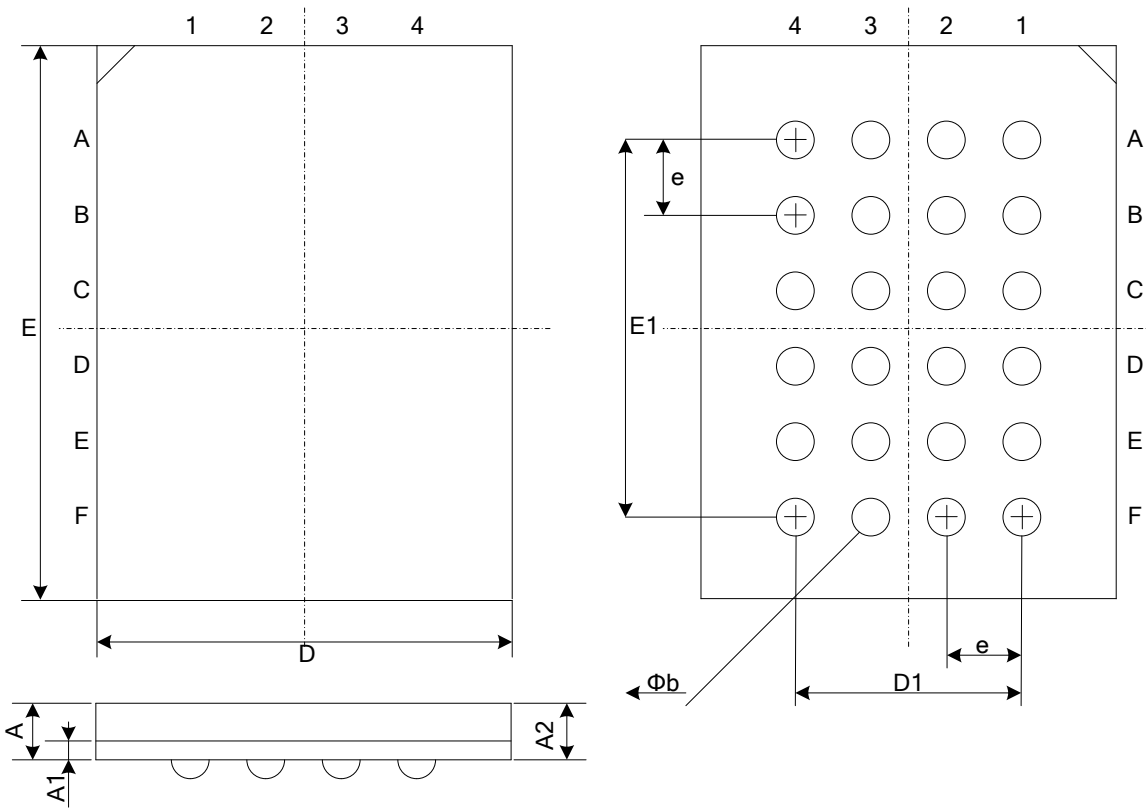


**Dimensions**

Symbol		A	A1	A2	b	D	D1	E	E1	e	y	L
Unit												
mm	Min	0.70		0.19	0.35	5.90	3.25	4.90	3.85		0.00	0.50
	Nom	0.75		0.22	0.42	6.00	3.37	5.00	3.97	1.27	0.04	0.60
	Max	0.80	0.05	0.25	0.48	6.10	3.50	5.10	4.10		0.08	0.75
Inch	Min	0.028		0.007	0.014	0.232	0.128	0.193	0.151		0.000	0.020
	Nom	0.030		0.009	0.016	0.236	0.133	0.197	0.156	0.05	0.001	0.024
	Max	0.032	0.002	0.010	0.019	0.240	0.138	0.201	0.161		0.003	0.030

Note: Both package length and width do not include mold flash.

**10.4. Package TFBGA-24BALL (6\*4 ball array)**

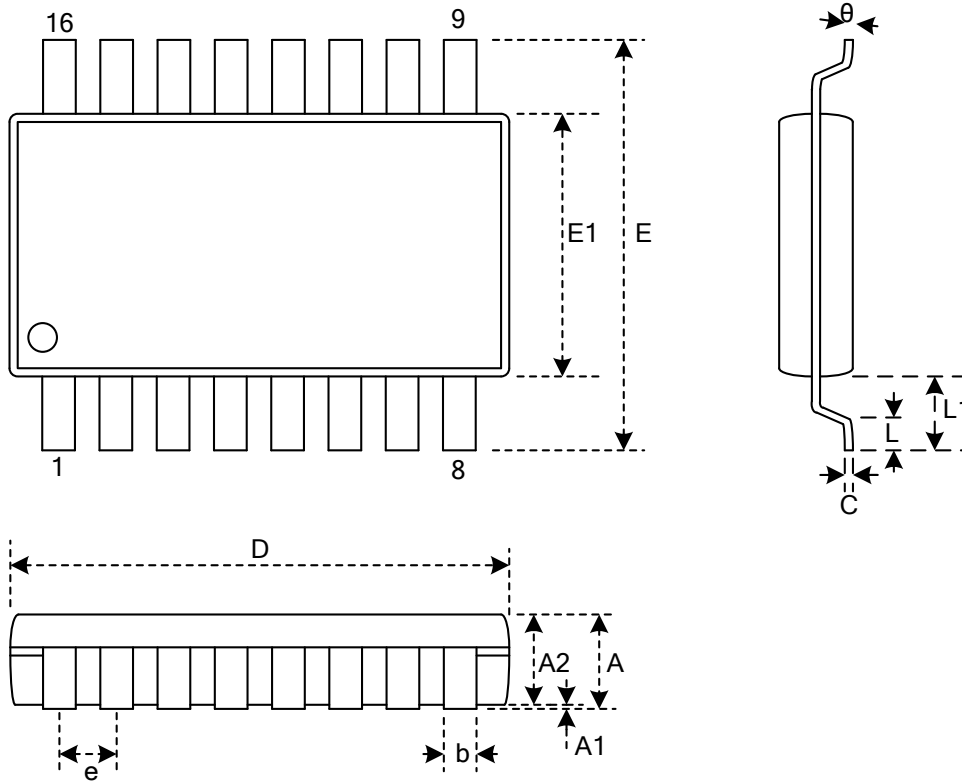


**Dimensions**

Symbol		A	A1	A2	b	D	D1	E	E1	e
Unit										
mm	Min		0.25		0.35	5.90		7.90		
	Nom		0.30	0.85	0.40	6.00	3.00	8.00	5.00	1.00
	Max	1.20	0.35		0.45	6.10		8.10		
Inch	Min		0.010		0.014	0.232		0.311		
	Nom		0.012	0.033	0.016	0.236	0.120	0.315	0.200	0.039
	Max	0.047	0.014		0.018	0.240		0.319		

Note: Both package length and width do not include mold flash.

10.5. Package SOP16 300MIL



Dimensions

Symbol		A	A1	A2	b	C	D	E	E1	e	L	L1	$\theta$
Unit													
mm	Min	2.36	0.10	2.24	0.36	0.20	10.10	10.10	7.42		0.40	1.31	0
	Nom	2.55	0.20	2.34	0.41	0.25	10.30	10.35	7.52	1.27	0.84	1.44	5
	Max	2.75	0.30	2.44	0.51	0.30	10.50	10.60	7.60		1.27	1.57	8
Inch	Min	0.093	0.004	0.088	0.014	0.008	0.397	0.397	0.292		0.016	0.052	0
	Nom	0.100	0.008	0.092	0.016	0.010	0.405	0.407	0.296	0.050	0.033	0.057	5
	Max	0.108	0.012	0.096	0.020	0.012	0.413	0.417	0.299		0.050	0.062	8

Note: Both package length and width do not include mold flash.

## 11. REVISION HISTORY

Version No	Description	Date
1.0	Release Version1.0	Aug.03,2011
1.1	Add Package TFBGA24 BALL	Aug.10,2011
1.2	Add Package SOP16	Sep.07,2011
1.3	Update Package Information	Nov.02,2011
	Update Maximum Erase time information	Aug.06,2012
1.4	Update Program and Erase time information	Oct.08,2012
1.5	Update Package Information	Oct.22,2012
1.6	Update Status Register	Mar. 05, 2013
	Update Ordering Information	
1.7	Update POWER-ON TIMING Description	Mar. 25, 2013
	Update Storage Temperature: -55~125 change to -65~150	
	Add Package TSOP8 208mil	
	Add Package WSON8 8*6mm	
1.8	Update CAPACITANCE MEASUREMENT CONDITIONS: Input Pulse Voltage "0.2VCC to 0.8VCC" change to "0.1VCC to 0.8VCC"	Jul. 8,2013
	Input Timing Reference Voltage "0.3VCC to 0.7VCC" change to "0.2VCC to 0.7VCC"	
	Update the format and add content	
1.9	Modify AC CHARACTERISTICS: t <sub>CLQV</sub> 7.0ns max change to 6.5ns max	Sep. 25,2013
	Modify AC CHARACTERISTICS: t <sub>CLQX</sub> 0ns min change to 1.0ns min	
2.0	Delete Package VSOP8 208mil	Feb. 21, 2014
	Delete Package WSON8 8*6mm	
2.1	Modify AC CHARACTERISTICS: t <sub>SE</sub> 70ms typ change to 40ms typ	Jun. 5, 2014
2.2	Modify Package WSON8 (6*5mm)	Jun. 11, 2015
	Modify Package TFBGA-24BALL (6*4 ball array)	
2.3	Modify Package SOP16 300MIL	July.20,2015
2.4	Modify Package TFBGA-24BALL (6*4 ball array)	July.23,2015
2.5	Modify AC CHARACTERISTICS: t <sub>CHCL</sub> Min.0.2 V/ns Change to 0.1 V/ns	Nov.12,2015
	t <sub>CLCH</sub> Min.0.2 V/ns Change to 0.1 V/ns; modify fc3/fr's Parameter and Max. Modify Figure 40. Power-on Timing Sequence Diagram	
2.6	Modify AC CHARACTERISTICS: add t <sub>RST_R</sub> & t <sub>RST_P</sub> & t <sub>RST_E</sub>	Dec.23,2015
	Modify POWER-ON TIMING: T <sub>VSL</sub> Min 10us Change to 5ms	
	Modify POWER-ON TIMING: T <sub>puw</sub> Min 1ms Change to 5ms	