Data Sheet

BCM43341

Single-Chip, Dual-Band (2.4 GHz/5 GHz) IEEE 802.11 a/b/g/n MAC/Baseband/Radio with Integrated Bluetooth 4.0, FM Receiver, and NFC Controller

GENERAL DESCRIPTION

The Broadcom® BCM43341 single–chip quad–radio device provides the highest level of integration for a mobile or handheld wireless system, with integrated dual band (2.4 GHz / 5 GHz) IEEE 802.11 a/b/g and single–stream IEEE 802.11n MAC/baseband/radio, Bluetooth 4.0, and FM radio receiver. It also integrates a low power NFC controller based on the BCM2079X, an NFC standards–compliant standalone solution. The BCM43341 includes integrated power amplifiers and LNAs for the 2.4 GHz and 5 GHz WLAN bands, and an integrated 2.4 GHz T/R switch. This greatly reduces the external part count, PCB footprint, and cost of the solution.

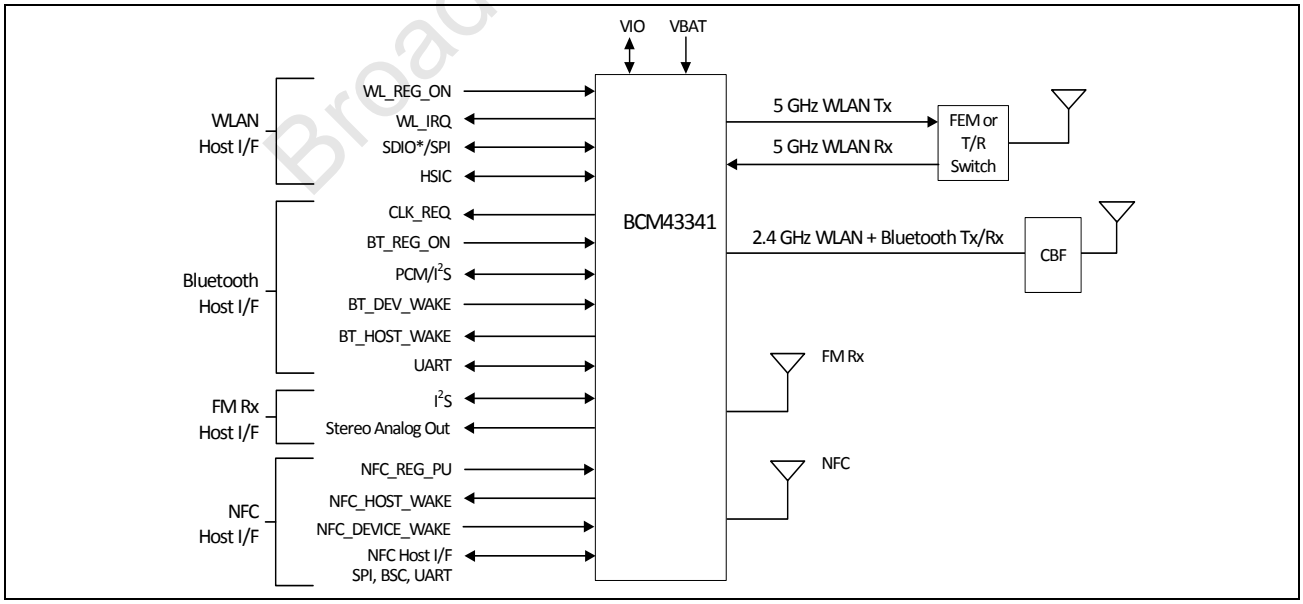
Using advanced design techniques and process technology to reduce active and idle power, the BCM43341 is designed to address the needs of mobile devices that require minimal power consumption and compact size. It includes a power management unit which simplifies the system power topology and allows for operation directly from a mobile platform battery while maximizing battery life.

FEATURES

The BCM43341 implements the highly sophisticated Enhanced Collaborative Coexistence algorithms and hardware mechanisms, allowing for an extremely collaborative Bluetooth coexistence scheme along with coexistence support for external radios (such as cellular and LTE, GPS, WiMAX, and Ultra–Wideband) and a single shared 2.4 GHz antenna for Bluetooth and WLAN. As a result, enhanced overall quality for simultaneous voice, video, and data transmission on a handheld system is achieved.

For the WLAN section, two host interface options are included: an SDIO v2.0 interface (including gSPI) and a High-Speed Inter-Chip (HSIC) interface (a USB 2.0 derivative for short-distance on-board connections). An independent, high-speed UART is provided for the Bluetooth host interface. Separate independent interfaces (I^2C-compatible Broadcom Serial Control [BSC], SPI, and UART) for NFC are also provided.

Figure 1: Functional Block Diagram



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FEATURES

IEEE 802.11x Key Features

- Dual–band 2.4 GHz and 5 GHz IEEE 802.11 a/b/g/n
- Single–stream IEEE 802.11n support for 20 MHz and 40 MHz channels provides PHY layer rates up to 150 Mbps for typical upper–layer throughput in excess of 90 Mbps.
- Supports the IEEE 802.11n STBC (space–time block coding) RX and LDPC (low–density parity check) TX options for improved range and power efficiency.
- Supports a single 2.4 GHz antenna shared between WLAN and Bluetooth.
- Shared Bluetooth and 2.4 GHz WLAN receive signal path eliminates the need for an external power splitter while maintaining excellent sensitivity for both Bluetooth and WLAN.
- Internal fractional nPLL allows support for a wide range of reference clock frequencies
- Supports IEEE 802.15.2 external coexistence interface to optimize bandwidth utilization with other co–located wireless technologies such as GPS, WiMAX, or UWB
- Supports standard SDIO v2.0 and gSPI (48 MHz) host interfaces.
- Alternative host interface supports HSIC v1.0 (short–distance USB device)
- Integrated ARM® Cortex™–M3 processor and on-chip memory for complete WLAN subsystem functionality, minimizing the need to wake up the applications processor for standard WLAN functions. This allows for further minimization of power consumption, while maintaining the ability to field upgrade with future features. On-chip memory includes 512 KB SRAM and 640 KB ROM.
- OneDriver™ software architecture for easy migration from existing embedded WLAN and Bluetooth devices as well as future devices.

FEATURES

NFC Key Features

- Support for the ISO/IEC 18092, ISO/IEC 21481, ISO/IEC 14443 Types A, B and B', Japanese Industrial Standard (JIS) (X) 6319–4, and ISO/IEC 15693 standards
- No active components requirement for antenna or field–power conditioning
- Individual byte framing
- Hardware–based collision detection and modulation controls
- Reader/Writer (R/W) mode
- Active and Passive Peer–to–Peer (P2P) mode
- Tag/Card Emulation mode:
  - Support for host switched off card emulation mode
  - Support for completely powered from the field (battery-off) card emulation mode
- Dual Single Wire Protocol (SWP) interfaces:
  - SWP_0 with platform PMU power switching to UICC SIM card
  - SWP_1 for embedded secure element
- Supports AID routing between host and secure element(s)
- Supports application tunnelling to secure
- elements over SWP
- Internal low–power oscillator for periodic wake–up and mode switch operation
- Low–power target detection mode for extremely low average current consumption "sniff mode"
- NFC Forum NFC Controller Interface (NCI) for host interface
- Multiple low–power modes for flexible power management

FEATURES

Bluetooth and FM Key Features

- Complies with Bluetooth Core Specification Version 4.0 with provisions for supporting future specifications.
- Bluetooth Class 1 or Class 2 transmitter operation
- Supports extended Synchronous Connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive Frequency Hopping (AFH) for reducing radio frequency interference
- Interface support—Host Controller Interface (HCI) using a high–speed UART interface and PCM for audio data
- The FM receiver unit supports HCI for communication.
- Low power consumption improves battery life of handheld devices.
- FM receiver: 76 MHz to 108 MHz FM bands; supports the European Radio Data Systems (RDS) and the North American Radio Broadcast Data System (RBDS) standards
- Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound.
- Automatic frequency detection for standard crystal and TCXO values

FEATURES

General Features

- Supports battery voltage range from 2.9V to 4.8V supplies with internal switching regulator.
- Programmable dynamic power management
- 3072–bit OTP for storing board parameters
- Routable on low–cost 1–x–1 PCB stack–ups
- 141-ball WLBGA package(5.67 mm × 4.47 mm, 0.4 mm pitch)
- Security:
  - WPA™ and WPA2™ (Personal) support for powerful encryption and authentication
  - AES in WLAN hardware for faster data encryption and IEEE 802.11i compatibility
  - Reference WLAN subsystem provides Cisco® Compatible Extensions (CCX, CCX 2.0, CCX 3.0, CCX 4.0, CCX 5.0)
  - Reference WLAN subsystem provides Wi–Fi Protected Setup (WPS)
- Worldwide regulatory support: Global products supported with worldwide homologated design

Revision History

Revision	*Date*	*Change Description*
MMP43341-DS103-R	09/10/15	**Updated:** • Figure 25: “WLBGA Signal Descriptions,” on page 111
MMP43341-DS102-R	01/28/15	**Updated:** • Figure 25: “WLBGA Signal Descriptions,” on page 111
MMP43341-DS101-R	07/07/14	**Updated:** • Figure 65: “WLBGA Keep-Out Areas for PCB Layout — Bottom View,” on page 175
MMP43341-DS100-R	04/07/14	• Initial release

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About This Document

Purpose and Audience

This document provides details of the functional, operational, and electrical characteristics of the Broadcom® BCM43341. It is intended for hardware design, application, and OEM engineers.

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use. Acronyms and abbreviations in this document are also defined in Appendix A: “Acronyms and Abbreviations,” on page 178

For a comprehensive list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

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References

The references in this section may be used in conjunction with this document.

Note: Broadcom provides customer access to technical documentation and software through its Customer Support Portal (CSP) and Downloads & Support site (see Technical Support).

For Broadcom documents, replace the "x" in the document number with the largest number available in the repository to ensure that you have the most current version of the document.

Document (or Item) Name	Number	Source
Broadcom Items		
[1] Current Consumption While Polling	20791–AN1xx–R	Broadcom CSP
Other Items		
[2] Identification cards – Contactless integrated circuit cards – Proximity cards– Part 2: Radio frequency power and signal interface	ISO/IEC 14443–2:2010	www.iso.org/
[3] Identification cards – Contactless integrated circuit(s) cards – Proximity cards – Part 3: Initialization and anticollision	ISO/IEC 14443–3:2001	www.iso.org/
[4] Identification cards – Contactless integrated circuit cards– Proximity cards — Part 4: Transmission protocol	ISO/IEC 14443–4:2008 (2nd Edition)	www.iso.org/
[5] Identification cards – Contactless integrated circuit cards – Vicinity cards – Part 2: Air interface and initialization	ISO/IEC 15693–2:2006	www.iso.org/
[6] Identification cards – Contactless integrated circuit cards – Vicinity cards – Part 3: Anticollision and transmission protocol	ISO/IEC 15693–3:2009	www.iso.org/
[7] Information technology – Telecommunications and information exchange between systems – Near Field Communication – Interface and Protocol (NFCIP–1)	ISO/IEC 18092:2004	www.iso.org/
[8] Information technology – Telecommunications and information exchange between systems – Near Field Communication Interface and Protocol –2 (NFCIP–2)	ISO/IEC 21481:2005	www.iso.org/
[9] Specification of implementation for integrated circuit(s) cards – Part 4: High Speed proximity cards	JIS (X) 6319–4	http:// www.jisc.go.jp

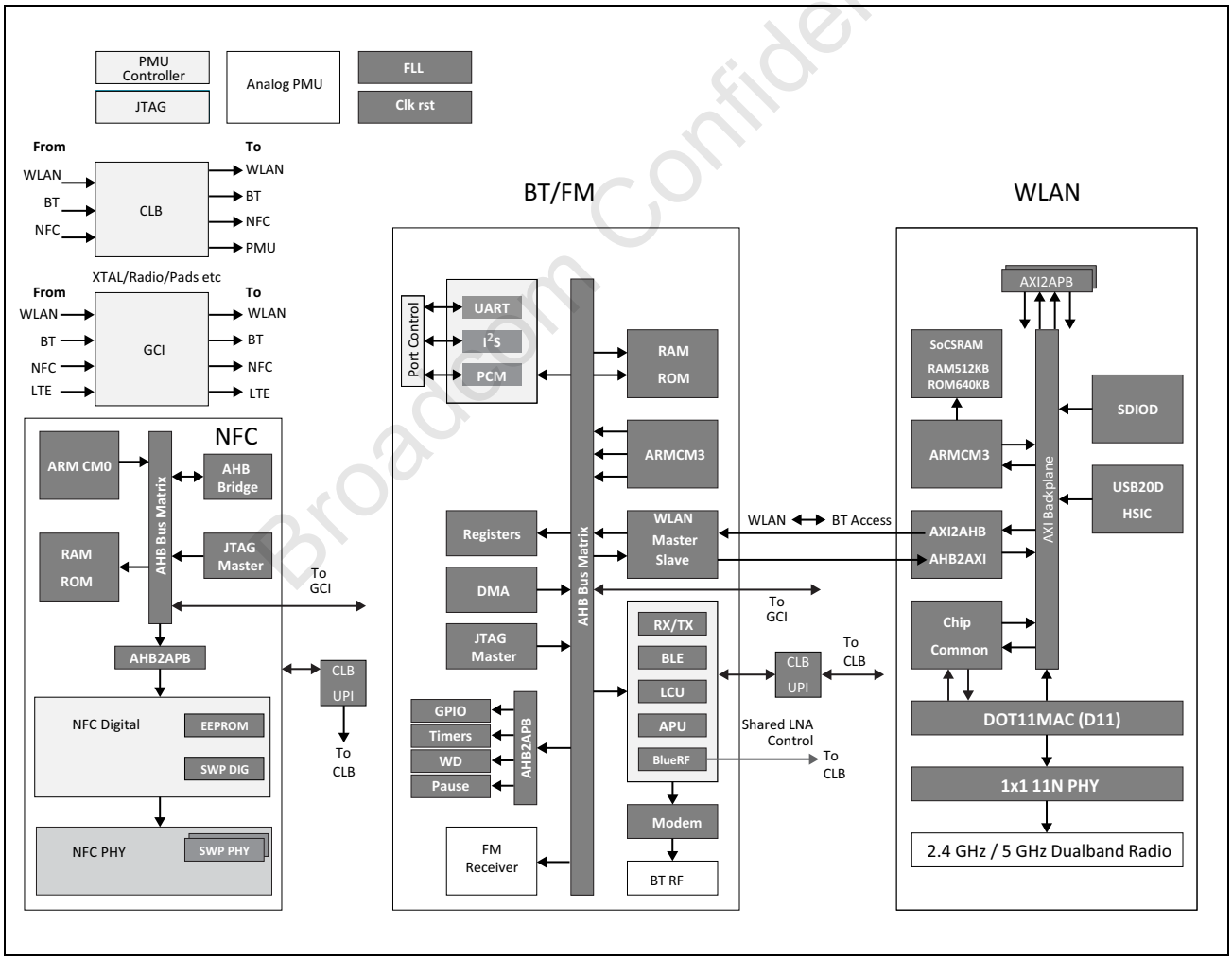
Section 1: Introduction

Overview

The Broadcom® BCM43341 single-chip device provides the highest level of integration for a mobile or handheld wireless system, with integrated IEEE 802.1 a/b/g/n MAC/baseband/radio, Bluetooth 4.0, FM RX, and NFC controller. It provides a small form-factor solution with minimal external components to drive down cost for mass volumes and allows for handheld device flexibility in size, form, and function. Comprehensive power management circuitry and software ensure the system can meet the needs of highly mobile devices that require minimal power consumption and reliable operation.

Figure 2 shows the interconnect of all the major physical blocks in the BCM43341 and their associated external interfaces, which are described in greater detail in the following sections.

Figure 2: BCM43341 Block Diagram



Features

The BCM43341 supports the following WLAN, Bluetooth, and FM features:

- IEEE 802.11a/b/g/n dual-band radio with internal Power Amplifiers, LNAs, and T/R switches
- Bluetooth v4.0 with integrated Class 1 PA
- Concurrent Bluetooth, FM (RX) RDS/RBDS, NFC, and WLAN operation
- On-chip WLAN driver execution capable of supporting IEEE 802.11 functionality
- Single- and dual-antenna support
  - Single antenna with shared LNA
  - Simultaneous BT/WLAN receive with single antenna
- WLAN host interface options:
  - SDIO v2.0, including default and high-speed timing.
  - gSPI—up to 48 MHz clock rate
  - HSIC (USB device interface for short distance on-board applications)
- BT host digital interface (can be used concurrently with above interfaces):
  - UART (up to 4 Mbps)
- ECI—enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives
- I^2S/PCM for FM/BT audio, HCI for FM block control
- HCI high-speed UART (H4, H5) transport support
- Wideband speech support (16 bits linear data, MSB first, left justified at 4K samples/s for transparent air coding, both through I^2S and PCM interface)
- Bluetooth SmartAudio® technology improves voice and music quality to headsets
- Bluetooth low power inquiry and page scan
- Bluetooth Low Energy (BLE) support
- Bluetooth Packet Loss Concealment (PLC)
- Bluetooth Wideband Speech (WBS)
- FM advanced internal antenna support
- FM auto search/tuning functions
- FM multiple audio routing options: I^2S, PCM, eSCO, A2DP
- FM mono-stereo blend and switch, and soft mute support
- FM audio pause detect support
- Audio rate-matching algorithms
- Multiple simultaneous A2DP audio stream
- FM over Bluetooth operation and on-chip stereo headset emulation

The BCM43341 supports the following NFC features:

- Support for the ISO/IEC 18092, ISO/IEC 21481, ISO/IEC 14443 Types A, B, and B', Japanese Industrial Standard (JIS) (X) 6319-4, and ISO/IEC 15693 standards
- No active components required for antenna or field-power conditioning
- Individual byte framing
- Hardware-based collision detection and modulation controls
- Reader/Writer (R/W) mode
- Active and Passive Peer-to-Peer (P2P) mode
- Tag/Card Emulation mode:
  - Support for host-switched-off card emulation mode
  - Support for completely powered from the field (battery-off) card emulation mode
- Dual Single Wire Protocol (SWP) interfaces:
  - SWP_0 with platform PMU power switching to UICC SIM card.
  - SWP_1 for embedded secure element or secondary UICC SIM cards
  - Supports application tunnelling to secure elements over SWP
- Supports Application ID (AID) routing between a reader and secure element(s)
- Ability to recover card emulation personality data
- Internal low-power oscillator for periodic wake-up and mode switch operation
- Low-Power Target Detection mode for extremely low average current consumption ("sniff mode")
- NFC Forum NFC Controller Interface (NCI) for the host interface

Standards Compliance

The BCM43341 supports the following standards:

- Bluetooth 4.0 (including Bluetooth Low Energy)
- 76 MHz to 108 MHz FM bands (US, Europe, and Japan)
- IEEE 802.11n—Handheld Device Class (Section 11)
- IEEE 802.11a
- IEEE 802.11b
- IEEE 802.11g
- IEEE 802.11d
- IEEE 802.11h
- IEEE 802.11i

The BCM43341 will support the following future drafts/standards:

- IEEE 802.11r—Fast Roaming (between APs)
- IEEE 802.11k—Resource Management
- IEEE 802.11w—Secure Management Frames
- IEEE 802.11 Extensions:
  - IEEE 802.11e QoS Enhancements (as per the WMM® specification is already supported)
  - IEEE 802.11h 5 GHz Extensions
  - IEEE 802.11i MAC Enhancements
  - IEEE 802.11r Fast Roaming Support
  - IEEE 802.11k Radio Resource Measurement

The BCM43341 supports the following security features and proprietary protocols:

- Security:
  - WEP
  - WPA™ Personal
  - WPA2™ Personal
  - WMM
  - WMM-PS (U-APSD)
  - WMM-SA
  - WAPI
  - AES (Hardware Accelerator)
  - TKIP (host-computed)
  - CKIP (SW Support)

- Proprietary Protocols:
  - CCXv2
  - CCXv3
  - CCXv4
  - CCXv5
- IEEE 802.15.2 Coexistence Compliance—on silicon solution compliant with IEEE 3 wire requirements

See Table 20 on page 96 for details on supported NFC standards.

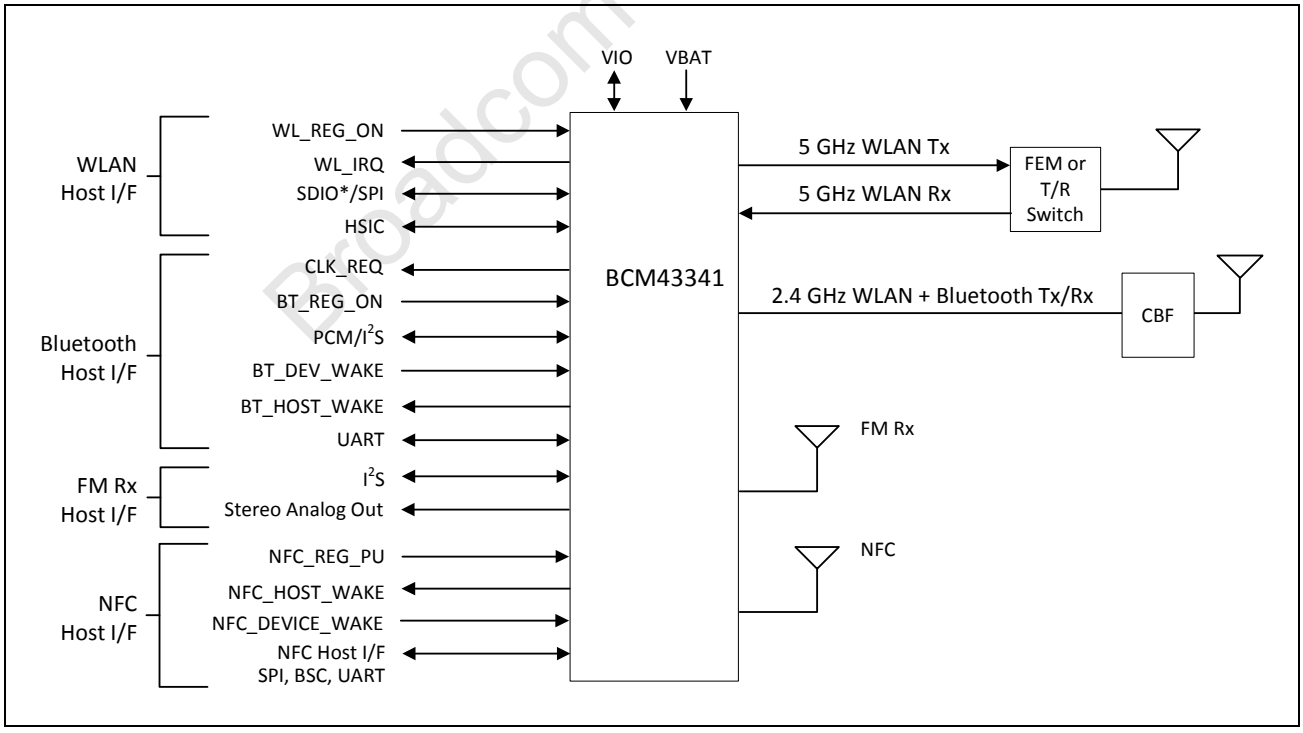
Mobile Phone Usage Model

The BCM43341 incorporates a number of unique features to simplify integration into mobile phone platforms. Its flexible PCM and UART interfaces enable it to transparently connect with the existing circuits. In addition, the TCXO and LPO inputs allow the use of existing handset features to further minimize the size, power, and cost of the complete system.

- The PCM interface provides multiple modes of operation to support both master and slave as well as hybrid interfacing to single or multiple external codec devices.
- The UART interface supports hardware flow control with tight integration to power control sideband signaling to support the lowest power operation.
- The TCXO interface accommodates any of the typical reference frequencies used by cell phones.
- FM digital interfaces can use either I^2S, PCM, or stereo analog output (an analog FM receiver interface is available for legacy systems.)
- The highly linear design of the radio transceiver ensures that the device has the lowest spurious emissions output regardless of the state of operation. It has been fully characterized in the global cellular bands.
- The transceiver design has excellent blocking (eliminating desensitization of the Bluetooth receiver) and intermodulation performance (distortion of the transmitted signal caused by the mixing of the cellular and Bluetooth transmissions) in the presence of a any cellular transmission (GSM®, GPRS, CDMA, WCDMA, or iDEN). Minimal external filtering is required for integration inside the handset.

The BCM43341 is designed to provide direct interface with new and existing handset designs as shown in Figure 3.

Figure 3: Mobile Phone System Block Diagram



Section 2: Power Supplies and Power Management

Power Supply Topology

One Buck regulator, multiple LDO regulators, and a Power Management Unit (PMU) are integrated into the BCM43341. All regulators are programmable via the PMU. These blocks simplify power supply design for Bluetooth, WLAN, FM, and NFC functions in embedded designs.

A single VBAT (2.9–4.8V) and VIO supply (1.8V to 3.3V) can be used, with all additional voltages being provided by the regulators in the BCM43341.

Two control signals, BT_REG_ON and WL_REG_ON, are used to power-up the regulators and take the respective section out of reset. The CBUCK CLDO and LNLDO power up when any of the reset signals are deasserted. All regulators are powered down only when both BT_REG_ON and WL_REG_ON are deasserted. The CLDO and LNLDO may be turned off/on based on the dynamic demands of the digital baseband.

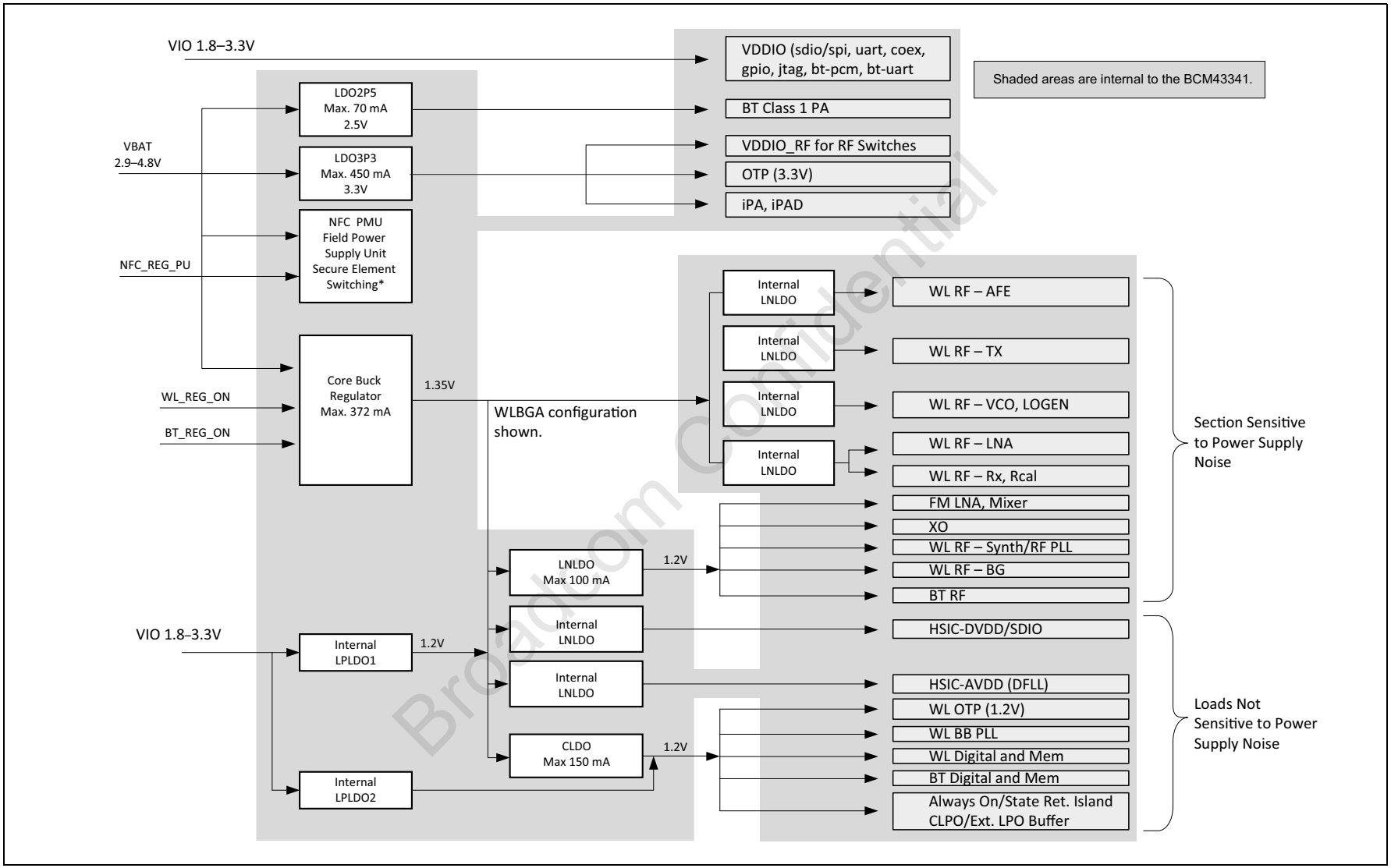
The BCM43341 allows for an extremely low power-consumption mode by completely shutting down the CBUCK, CLDO, and LNDLO regulators. When in this state, LPLDO1 and LPLDO2 (which are low-power linear regulators that are supplied by the system VIO supply) provide the BCM43341 with all the voltages it requires, further reducing leakage currents.

BCM43341 PMU Features

- VBAT to 1.35Vout (372 mA maximum) Core-Buck (CBUCK) switching regulator
- VBAT to 3.3Vout (450 mA maximum) LDO3P3 (external-capacitor)
- VBAT to 2.5Vout (70 mA maximum) LDO2P5 (external-capacitor)
- 1.35V to 1.2Vout (100 mA maximum) LNLDO (external-capacitor)
- 1.35V to 1.2Vout (150 mA maximum) CLDO (external-capacitor)
- 1.35V to 1.2Vout (80 mA maximum) HSICDVDD LDO (external-capacitor)
- Additional internal LDOs (not externally accessible)

Figure 4 on page 25 shows the regulators and a typical power topology.

Figure 4: Typical Power Topology



NFC PMU

The NFC portion of the BCM43341 has its own PMU including multiple LDO regulators. All regulators are programmable through the PMU. These blocks simplify power supply design for NFC functionality in embedded designs. Main digital and analog regulator outputs are brought out to pins for decoupling. A single VBAT (2.9–4.8V) and VDDIO (1.8–3.3V) can be used to supply power, with all additional voltages being provided by the regulators in the BCM43341. A control signal (NFC_REG_PU, regulator power-up) is used to power up the regulators and take the respective section out of reset. This signal provides a method for the host to override the operational control of the internal LDOs. NFC_REG_PU operates on the VDDIO domain. Even with NFC_REG_PU deasserted, there is a low current always-on digital LDO that is used to keep alive the state of important register settings within the front-end system. This uses residual power from the host battery to maintain the Card Emulation personality and persistence data.

NFC Power Management

The BCM43341 NFC core has been designed with the stringent power consumption requirements of mobile devices in mind. All areas of the chip design are optimized to minimize power consumption. The PMU, in conjunction with the local microcontroller (MCU) and firmware, enables and disables internal regulators and circuit blocks depending on the requirements of the operating modes selected. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

The NFC core main power states are described as follows:

- Full Power mode—All required regulators are enabled and the necessary circuit blocks are energized as required for the NFC operation mode. The BCM43341 NFC core and the host device operate in all NFC operating modes (that is, Peer, Reader/Writer, and Card Emulation). There are various submodes within this level as required to optimize the transient power operation of the BCM43341 host interfaces, the MCU, and NFC subsystems.
- Snooze Standby mode—During operation of the NFC Forum Mode Switch, in between the polling events, the BCM43341 NFC core enters Snooze Standby mode, where the analog LDO is off and all main clocks (PLL and crystal oscillator) are shut down to reduce active power to the minimum. Only the LPO clock is running and available for the PMU sequencer. This is used to allow the PMU sequencer to wake up the chip and transition to Full Power mode for the next poll event. In Snooze Standby mode, all firmware patches and configuration data is retained to restart the MCU; the primary power consumed is due to leakage current. The carrier detector block is also running from the always-on LDO power domain to detect an external reader during the listen time in between polling events. When an external reader carrier field is detected, the IC wakes up and enters Card Emulation and Peer Target modes.

NFC Card Emulation Power Modes

The BCM43341 has flexibility in its power modes to optimize NFC availability in card emulation (CE) mode to the user as the host battery capacity discharges and voltage level declines with time. As an option, this can extend to full Battery-off operation when the battery is deemed to be exhausted or even no longer present. The BCM43341 can move from one power mode to the next under host control. Alternatively, the BCM43341 can be configured with a built-in V_{BATT} monitor circuit that can be pre-programmed by the host to have various pre-set voltage thresholds, such that when the battery voltage drops, the BCM43341 can automatically select and transition between the power level modes after the host is no longer available.

The BCM43341 can operate in CE mode with up to three sequential levels of battery power:

- CE Level 4 Power State
- CE Level 3 Power State
- CE Level 1 Power State

CE Level 4 Power State

In the CE Level 4 power state, the device operates in card emulation mode only. The BCM43341 can be put into a very low power standby state, but still have the ability to alert the host for any CE transactions. It is lower current than the snooze standby state because the SoC is powered down, but boot time is a little slower compared to the snooze standby state, so the hardware must handle the initial part of the CE transaction.

CE Level 3 Power State

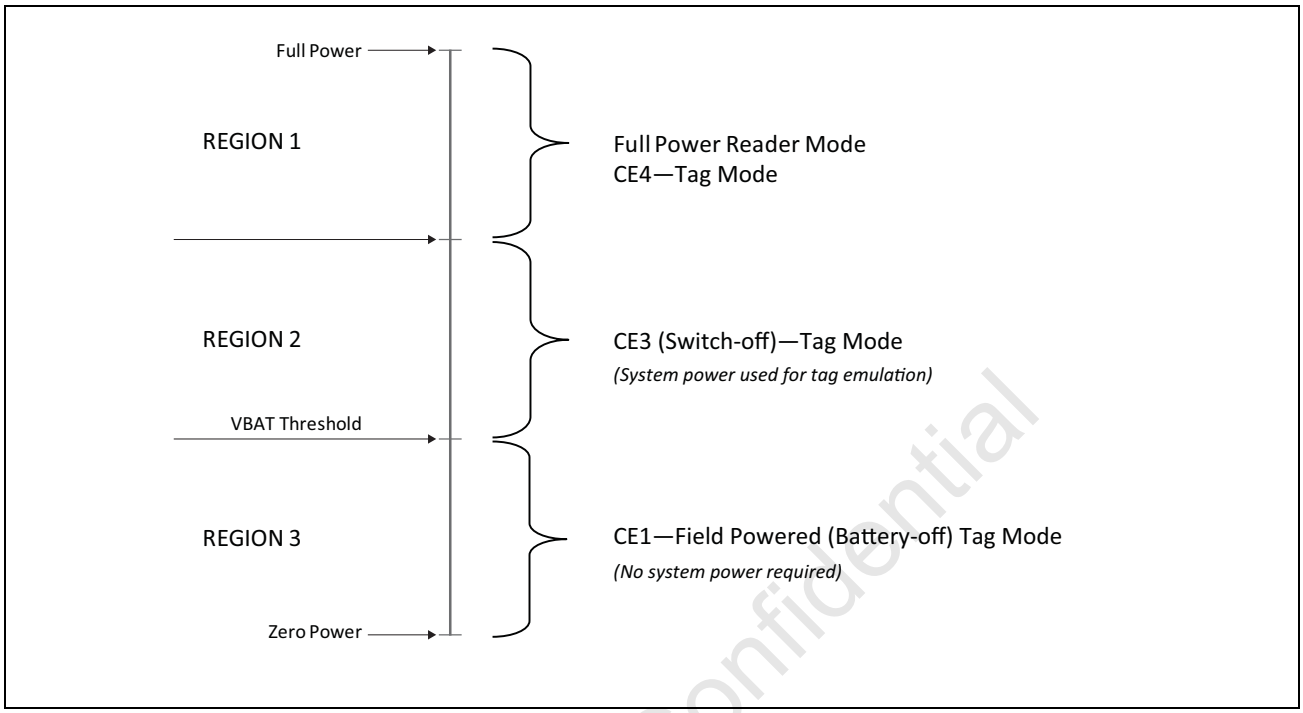
Level 3 is the host-switched-off mode in which the device operates in card emulation mode only. The operating power for the BCM43341 and Secure Element(s) is derived from the battery supply. The preset tag personality and persistence data is retained in the NFC front-end registers, ready for immediate use.

CE Level 1 Power State

Level 1 is the fully field-powered mode where the device operates in card emulation mode only. When the device is illuminated by a field and the BCM43341 harvests sufficient energy, the BCM43341 can retrieve the necessary personality and persistence data from the local nonvolatile memory (NVM), ready to respond to the reader/writer. The predesignated Secure Element is then supplied with power from the BCM43341, and the transaction can proceed to completion.

Figure 5 shows how CE levels are mapped onto GSMA-recommended handset battery power regions.

Figure 5: Mapping CE Levels



Power Levels

Full Power Mode (R/W, P2P, and CE)

- System power is available and maintains NFC IP registers.
- The host devices and host interface transport are active.
- The Secure Element (UICC) connected on the SWP-0 interface is powered by the host platform, which provides SIM power on VDDSWP_IN through the BCM43341 internal power switch.
- The eSE connected to the SWP-1 interface is powered from internal power.

Snooze Standby Mode

- System power is available and maintains NFC IP registers.
- The host has issued the SLEEP command.
- The low-power oscillator wakes up the chip periodically for mode switch polling and LPTD.
- The carrier detector wakes up in CE mode when a reader is detected.

CE Level 4 (CE Only)

- System power is available, but only used to maintain NFC registers.
- The host has issued the SLEEP command and the host interface transport is inactive.
- The carrier detector wakes up the chip in CE mode when a reader is detected.
- To allow time for the device to boot up, the transactions begin using hardware for time-critical elements until the firmware is up.
- The Secure Element (UICC) connected on the SWP-0 interface is powered by the host platform, which provides SIM power on VDDSWP_IN through the BCM43341 internal power switch.
- The eSE connected to the SWP-1 interface is powered from internal power.

CE Level 3, Switch-Off Mode (CE Only)

- The host device is inactive.
- System power is available at a reduced current for CE functionality.
- The Secure Element (UICC) or eSE operates in low power mode, as defined in TS 102 613.

CE Level 1, Battery Off/Field Power Harvesting Mode (CE Only)

- No system power is available, registers are dead.
- Persistence data registers are restored from NVM.
- Power is harvested from the field for everything.

Entering/Exiting CE3 (Switch-Off Mode)

Entering CE3

The sequence of events required to set the BCM43341 into CE3 mode is defined below.

1. The host sends SET_POWER_LEVEL_CMD to the BCM43341.
2. The host sets NFC_WAKE high.
3. The host waits for 1.5s, then sets REG_PU low.
4. The host waits for 200 ms, then sets VDDIO low.

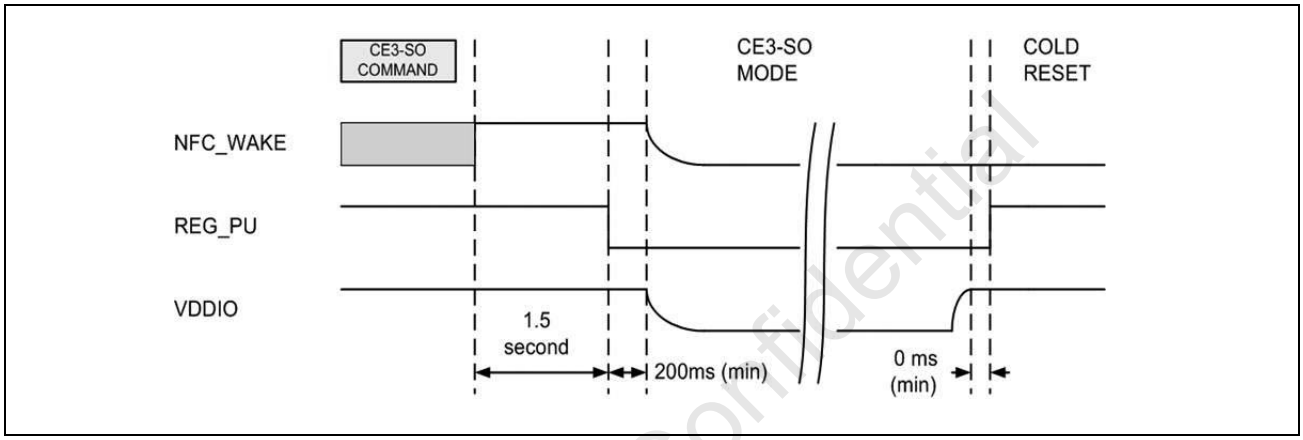
Exiting CE3

The BCM43341 can be moved out of CE3 by two different events:

- REG_PU goes high (the phone switches to Full Power mode again)
- VBAT falls below a preset threshold (battery voltage falls and the BCM43341 automatically switches to CE1 mode)

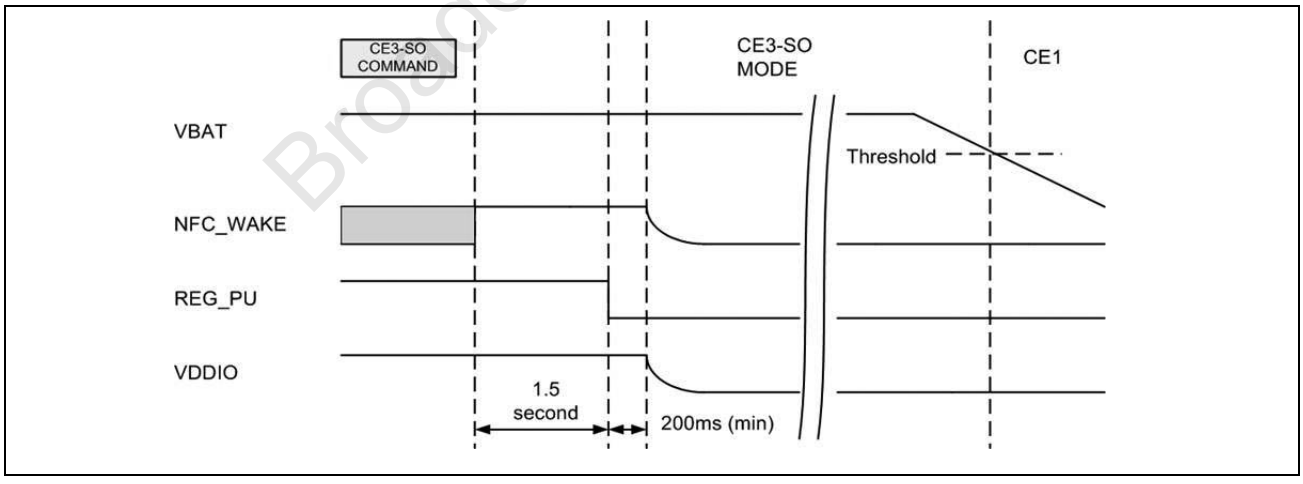
Any low-to-high transition on REG_PU resets the BCM43341 to a cold boot-up. This means that REG_PU must be held low while the system is switched off in order to keep the BCM43341 in CE3 (see Figure 6).

Figure 6: Transitioning from CE3 Mode into Full Power Mode (REG_PU Goes High)



As shown in Figure 7, if a pre-set VBAT monitor threshold has been sent to the BCM43341 when it was last in full power mode, and VBAT voltage is detected as having fallen below the pre-set threshold, the BCM43341 automatically goes to CE1.

Figure 7: Transitioning from CE3 Mode into CE1 Mode (VBAT Falls below the Pre-Set Threshold)



VBAT monitor threshold values are defined in Table 1.

Table 1: VBAT Threshold Settings

Threshold Setting	*VBAT Threshold Voltage*
111	3.2
110	3.1
101	3.0
100	2.9
011	2.8
010	2.7
001	2.2
000	2.0

Power Transitions

Power transitions controlled by the host, or automated by the pre-programmed VBAT monitor, are defined in Table 2.

Table 2: Power Transitions

Power State Name	VDDIO Present?	REG_PU State	Entry	Host Condition	Host Involvement	Description	NFC Modes Available	NFC Power	UICC-0 Power	Register Power
Full Power	Yes	REG_PU = 1	Boot-up	Handset Active **Note:** Depending on requirements, can also be in Idle (screen off) with LPTD running.	Yes, by HOST_WAKE	Full Power mode—All required regulators are enabled and the necessary circuit blocks are energized as required for the NFC operation mode. The BCM43341 and the host device operate in all NFC operating modes (that is, Peer, Reader/Writer, and Card Emulation). There are various submodes within this level as required to optimize the transient power operation of the BCM43341 host interfaces, the MCU, and NFC subsystems.	R/W, P2P, and CE	VBAT	Host SIM power on VDDSWP_IN	VBAT
Snooze Standby	Yes	REG_PU = 1	Host command	Handset Active **Note:** Depending on requirements, can also be in Idle (screen OFF) with LPTD running.	Yes, by HOST_WAKE	Snooze Standby mode—During operation of the NFC Forum Mode Switch and LPTD, in between the polling/sniffing events, the BCM43341 enters snooze standby mode, where the analog LDO is off and all main clocks (PLL and crystal oscillator) are shut down to reduce active power to the minimum. Only the LPO clock is running and available for the PMU sequencer. This is used to allow the PMU sequencer to wake up the chip and transition to Full-power mode for the next poll event. In Snooze mode, all firmware patches and configuration data is retained ready to restart the MCU and the power consumed is primarily due to leakage current. The carrier detector block is also running from the always-on LDO power domain to detect an external reader during the listen time in between polling events. When an external reader carrier field is detected, then the IC wakes up and enters Card Emulation and Peer Target modes.	R/W, P2P, and CE	VBAT	Host SIM power on VDDSWP_IN	VBAT
CE4	Yes	REG_PU=1	Host command	Handset Idle (screen OFF)	Yes by HOST_WAKE	When CE Level 4 is in effect the device operates in card emulation mode only. The BCM43341 can be put into a very low-power standby state, but still have the ability to alert the host for any CE transactions. Current is lower than in the Snooze Standby state because the SoC is powered down, but boot time is a little slower compared to the Snooze Standby state, so the hardware must handle the initial part of the CE transaction.	CE only	VBAT	Host SIM power on VDDSWP_IN	VBAT

Table 2: Power Transitions (Cont.)

Power State Name	VDDIO Present?	REG_PU State	Entry	Host Condition	Host Involvement	Description	NFC Modes Available	NFC Power	UICC-0 Power	Register Power
CE3	No	REG_PU = 0	Host Command	Handset switched off	No	When CE Level 3 (Switch-off) mode is in effect, the device operates in card emulation mode only. The operating power for the BCM43341 and Secure Element(s) is derived from the battery supply. The preset tag personality and persistence data is retained in the NFC front-end registers, ready for immediate use.	CE only	VBAT	Internal LDO power	VBAT
CE1	No	REG_PU = 0	By VBAT falling below threshold	VBAT below threshold or battery removed	No	Level 1 is the fully field-powered mode where the device operates in card emulation mode only. When the device is illuminated by a field and the BCM43341 harvests sufficient energy, the BCM43341 can retrieve the necessary personality and persistence data from NVM, ready to respond to the reader/ writer. The predesignated Secure Element is supplied with power from the BCM43341 and the transaction can proceed to completion.	CE only	Field	Internal LDO power	–

WLAN Power Management

The BCM43341 has been designed with the stringent power consumption requirements of mobile devices in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the BCM43341 integrated RAM is a high Vt memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only. Additionally, the BCM43341 includes an advanced WLAN power management unit (PMU) sequencer. The PMU sequencer provides significant power savings by putting the BCM43341 into various power management states appropriate to the current environment and activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power up sequences are fully programmable. Configurable, free-running counters (running at 32.768 kHz LPO clock) in the PMU sequencer are used to turn on/turn off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

The BCM43341 WLAN power states are described as follows:

- Active mode—All WLAN blocks in the BCM43341 are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- Doze mode—The radio, analog domains, and most of the linear regulators are powered down. The rest of the BCM43341 remains powered up in an IDLE state. All main clocks (PLL, crystal oscillator or TCXO) are shut down to reduce active power to the minimum. The 32.768 kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake up the chip and transition to Active mode. In Doze mode, the primary power consumed is due to leakage current.
- Deep-sleep mode—Most of the chip including both analog and digital domains and most of the regulators are powered off. Logic states in the digital core are saved and preserved into a retention memory in the always-ON domain before the digital core is powered off. Upon a wake-up event triggered by the PMU timers, an external interrupt or a host resume through the HSIC or SDIO bus, logic states in the digital core are restored to their pre-deep-sleep settings to avoid lengthy HW re-initialization.
- Power-down mode—The BCM43341 is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators.

PMU Sequencing

The PMU sequencer is responsible for minimizing system power consumption. It enables and disables various system resources based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them.

Resource requests may come from several sources: clock requests from cores, the minimum resources defined in the ResourceMin register, and the resources requested by any active resource request timers. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of four states: enabled, disabled, transition_on, and transition_off and has a timer that contains 0 when the resource is enabled or disabled and a non-zero value in the transition states. The timer is loaded with the time_on or time_off value of the resource when the PMU determines that the resource must be enabled or disabled. That timer decrements on each 32.768 kHz PMU clock. When it reaches 0, the state changes from transition_off to disabled or transition_on to enabled. If the time_on value is 0, the resource can go immediately from disabled to enabled. Similarly, a time_off value of 0 indicates that the resource can go immediately from enabled to disabled. The terms enable sequence and disable sequence refer to either the immediate transition or the timer load-decrement sequence.

During each clock cycle, the PMU sequencer performs the following actions:

1. Computes the required resource set based on requests and the resource dependency table.
2. Decrements all timers whose values are non zero. If a timer reaches 0, the PMU clears the ResourcePending bit for the resource and inverts the ResourceState bit.
3. Compares the request with the current resource status and determines which resources must be enabled or disabled.
4. Initiates a disable sequence for each resource that is enabled, no longer being requested, and has no powered up dependents.
5. Initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.

Power-Off Shutdown

The BCM43341 provides a low-power shutdown feature that allows the device to be turned off while the host, and any other devices in the system, remain operational. When the BCM43341 is not needed in the system, VDDIO_RF and VDDC are shut down while VDDIO remains powered. This allows the BCM43341 to be effectively off while keeping the I/O pins powered so that they do not draw extra current from any other devices connected to the I/O.

During a low-power shut-down state, provided VDDIO remains applied to the BCM43341, all outputs are tristated, and most inputs signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system, and enables the BCM43341 to be fully integrated in an embedded device and take full advantage of the lowest power-savings modes.

Two signals on the BCM43341, the frequency reference input (WRF_XTAL_CAB_OP) and the LPO_IN input, are designed to be high-impedance inputs that do not load down the driving signal even if the chip does not have VDDIO power applied to it.

When the BCM43341 is powered on from this state, it is the same as a normal power-up and the device does not retain any information about its state from before it was powered down.

Power-Up/Power-Down/Reset Circuits

The BCM43341 has two signals (see Table 3) that enable or disable the Bluetooth and WLAN circuits and the internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences, see Section 22: “Power-Up Sequence and Timing,” on page 170.

Table 3: Power-Up/Power-Down/Reset Control Signals

Signal	Description
WL_REG_ON	This signal is used by the PMU (with BT_REG_ON) to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal BCM43341 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If BT_REG_ON and WL_REG_ON are both low, the regulators are disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
BT_REG_ON	This signal is used by the PMU (with WL_REG_ON) to decide whether or not to power down the internal BCM43341 regulators. If BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.

Section 3: Frequency References

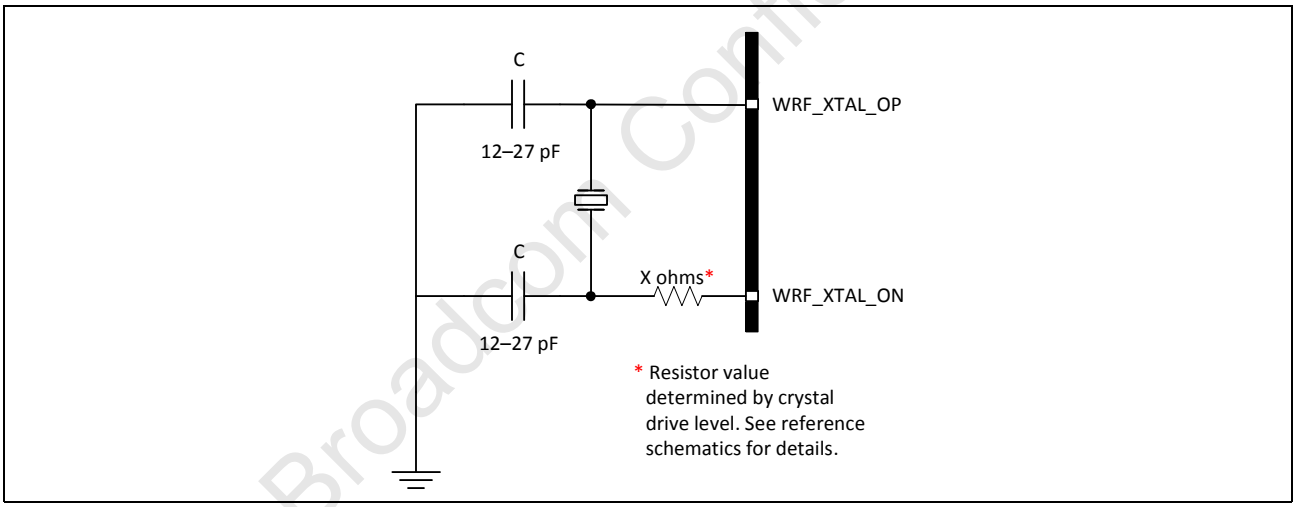
An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal may be used. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

Note: The crystal and TCXO implementations have different power supplies (WRF_XTAL_VDD1P2 for crystal, WRF_TCXO_VDD for TCXO).

Crystal Interface and Clock Generation

The BCM43341 can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in Figure 8. Consult the reference schematics for the latest configuration.

Figure 8: Recommended Oscillator Configuration



A fractional-N synthesizer in the BCM43341 generates the radio frequencies, clocks, and data/packet timing, enabling it to operate using a wide selection of frequency references.

For SDIO and HSIC applications the default frequency reference is a 37.4 MHz crystal or TCXO. The signal characteristics for the crystal interface are listed in Table 4 on page 39.

Note: Although the fractional-N synthesizer can support alternative reference frequencies, frequencies other than the default require support to be added in the driver, plus additional extensive system testing. Contact Broadcom for further details.

TCXO

As an alternative to a crystal, an external precision TCXO can be used as the frequency reference, provided that it meets the Phase Noise requirements listed in Table 4. When the clock is provided by an external TCXO, there are two possible connection methods, as shown in Figure 9 and Figure 10:

1. If the TCXO is dedicated to driving the BCM43341, it should be connected to the WRF_XTAL_OP pin through an external 1000 pF coupling capacitor, as shown in Figure 9. The internal clock buffer connected to this pin will be turned OFF when the BCM43341 goes into sleep mode. When the clock buffer turns ON and OFF there will be a small impedance variation. If the TCXO is to be shared with another device, such as a GPS receiver, and impedance variation is not allowed, a dedicated external clock buffer will be needed. Power must be supplied to the WRF_XTAL_VDD1P2 pin.
2. For 2.4 GHz operation only, an alternative is to DC-couple the TCXO to the WRF_TCXO_CK pin, as shown in Figure 10. Use this method when the same TCXO is shared with other devices and a change in the input impedance is not acceptable because it may cause a frequency shift that cannot be tolerated by the other device sharing the TCXO. This pin is connected to a clock buffer powered from WRF_TCXO_VDD. If the power supply to this buffer is always on (even in sleep mode), the clock buffer is always on, thereby ensuring a constant input impedance in all states of the device. The maximum current drawn from WRF_TCXO_VDD is approximately 500 µA.

Figure 9: Recommended Circuit to Use with an External Dedicated TCXO

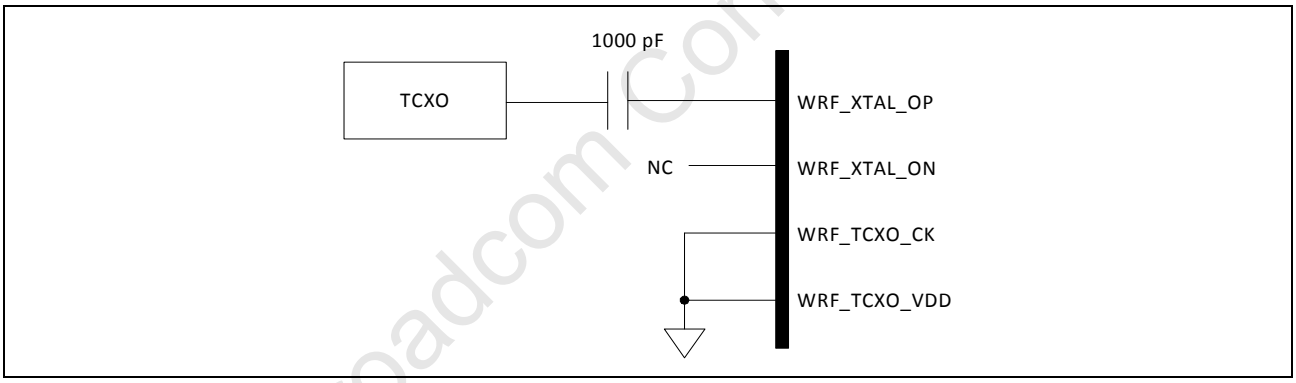


Figure 10: Recommended Circuit to Use with an External Shared TCXO

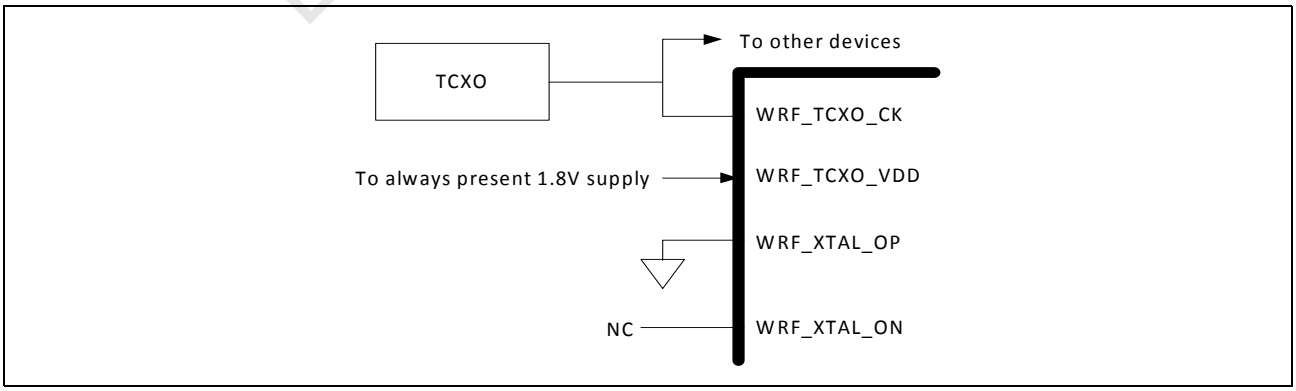


Table 4: Crystal Oscillator and External Clock – Requirements and Performance

		Crystal[a]			External Frequency Reference[b,c]			
Parameter	**Conditions/Notes**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Frequency	–	Between 19.2 MHz and 52 MHz[d,e]						
Crystal load capacitance	–	–	12	–	–	–	–	pF
ESR	–	–	–	60	–	–	–	Ω
Drive level	External crystal requirement	200[f]	–	–	–	–	–	µW
Input impedance (WRF_XTAL_OP)	Resistive	30k	100k	–	30k	100k	–	Ω
	Capacitive	–	–	7.5	–	–	7.5	pF
Input impedance (WRF_TCXO_IN)	Resistive	–	–	–	30k	100k	–	Ω
	Capacitive	–	–	–	–	–	4	pF
WRF_XTAL_OP Input low level	DC-coupled digital signal	–	–	–	0	–	0.2	V
WRF_XTAL_OP Input high level	DC-coupled digital signal	–	–	–	1.0	–	1.26	V
WRF_XTAL_OP input voltage	AC-coupled analog signal (see Figure 9)	–	–	–	400	–	1200	mV_{p-p}
WRF_TCXO_IN Input voltage	DC-coupled analog signal (see Figure 10)	–	–	–	400	–	1980	mV_{p-p}
Frequency tolerance over the lifetime of the equipment, including temperature	Without trimming	–20	–	20	–20	–	20	ppm
Duty cycle	37.4 MHz clock	–	–	–	40	50	60	%
Phase Noise (802.11b/g)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–131	dBc/Hz
	37.4 MHz clock at 100 kHz or greater offset	–	–	–	–	–	–138	dBc/Hz
Phase Noise (802.11a)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–139	dBc/Hz
	37.4 MHz clock at 100 kHz or greater offset	–	–	–	–	–	–146	dBc/Hz
Phase Noise (802.11n, 2.4 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–136	dBc/Hz
	37.4 MHz clock at 100 kHz or greater offset	–	–	–	–	–	–143	dBc/Hz
Phase Noise (802.11n, 5 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–144	dBc/Hz
	37.4 MHz clock at 100 kHz or greater offset	–	–	–	–	–	–151	dBc/Hz

a. (Crystal) Use WRF_XTAL_OP and WRF_XTAL_ON, internal power to pin WRF_XTAL_VDD1P2.
b. (TCXO) See "TCXO" on page 38 for alternative connection methods.
c. For a clock reference other than 37.4 MHz, 20 × log10(f/ 37.4) dB should be added to the limits, where f = the reference clock frequency in MHz.
d. BT_TM6 should be tied low for a 52 MHz clock reference. For other frequencies, BT_TM6 should be tied high. Note that 52 MHz is not an auto-detected frequency using the LPO clock.
e. The frequency step size is approximately 80 Hz resolution.
f. The crystal should be capable of handling a 200uW drive level from the BCM43341.

Frequency Selection

Any frequency within the ranges specified for the crystal and TCXO reference may be used. These include not only the standard handset reference frequencies of 19.2, 19.44, 19.68, 19.8, 20, 26, 37.4, and 52 MHz, but also other frequencies in this range, with approximately 80 Hz resolution. The BCM43341 must have the reference frequency set correctly in order for any of the UART or PCM interfaces to function correctly, since all bit timing is derived from the reference frequency.

Note: The fractional-N synthesizer can support many reference frequencies. However, frequencies other than the default require support to be added in the driver plus additional, extensive system testing. Contact Broadcom for further details.

The reference frequency for the BCM43341 may be set in the following ways:

- Set the *xtalfreq=xxxxx* parameter in the nvram.txt file (used to load the driver) to correctly match the crystal frequency.
- Auto-detect any of the standard handset reference frequencies using an external LPO clock.

For applications such as handsets and portable smart communication devices, where the reference frequency is one of the standard frequencies commonly used, the BCM43341 automatically detects the reference frequency and programs itself to the correct reference frequency. In order for auto frequency detection to work correctly, the BCM43341 must have a valid and stable 32.768 kHz LPO clock that meets the requirements listed in Table 5 on page 41 and is present during power-on reset.

External 32.768 kHz Low-Power Oscillator

The BCM43341 uses a secondary low frequency clock for low-power-mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz ± 30% over process, voltage, and temperature, which is adequate for some applications. However, a trade-off caused by this wide LPO tolerance is a small current consumption increase during WLAN power save mode that is incurred by the need to wake up earlier to avoid missing beacons. Whenever possible, the preferred approach for WLAN is to use a precision external 32.768 kHz clock that meets the requirements listed in Table 5.

Note: BTFM operations require the use of an external LPO that meets the requirements listed in Table 5.

Table 5: External 32.768 kHz Sleep Clock Specifications

Parameter	*LPO Clock*	*Units*
Nominal input frequency	32.768	kHz
Frequency accuracy	±200	ppm
Duty cycle	30–70	%
Input signal amplitude	200–1800	mV, p-p
Signal type	Square-wave or sine-wave	–
Input impedance[a]	>100k <5	Ω pF
Clock jitter (during initial start-up)	<10,000	ppm

a. When power is applied or switched off.

Section 4: Bluetooth + FM Subsystem Overview

The Broadcom BCM43341 is a Bluetooth 4.0-compliant, baseband processor/2.4 GHz transceiver with an integrated FM/RDS/RBDS receiver. It features the highest level of integration and eliminates all critical external components, thus minimizing the footprint, power consumption, and system cost of a Bluetooth plus FM radio solution.

The BCM43341 is the optimal solution for any Bluetooth voice and/or data application that also requires an FM radio receiver. The Bluetooth subsystem presents a standard Host Controller Interface (HCI) via a high speed UART and PCM for audio. The FM subsystem supports the HCI control interface as well as I^2S, PCM, and stereo analog interfaces. The BCM43341 incorporates all Bluetooth 4.0 features including BR/EDR and LE.

The BCM43341 Bluetooth radio transceiver provides enhanced radio performance to meet the most stringent mobile phone temperature applications and the tightest integration into mobile handsets and portable devices. It is fully compatible with any of the standard TCXO frequencies and provides full radio compatibility to operate simultaneously with GPS, WLAN, NFC, and cellular radios.

The Bluetooth transmitter also features a Class 1 power amplifier with Class 2 capability.

Features

Major Bluetooth features of the BCM43341 include:

- Supports key features of upcoming Bluetooth standards
- Fully supports Bluetooth Core Specification version 4.0 features
- UART baud rates up to 4 Mbps
- Supports all Bluetooth 4.0 packet types
- Supports maximum Bluetooth data rates over HCI UART
- Multipoint operation with up to seven active slaves
  - Maximum of seven simultaneous active ACL links
  - Maximum of three simultaneous active SCO and eSCO connections with scatternet support
- Trigger Broadcom fast connect (TBFC)
- Narrowband and wideband packet loss concealment
- Scatternet operation with up to four active piconets with background scan and support for scatter mode
- High-speed HCI UART transport support with low-power out-of-band BT_DEV_WAKE and BT_HOST_WAKE signaling (see “Host Controller Power Management” on page 48)
- Channel quality driven data rate and packet type selection
- Standard Bluetooth test modes
- Extended radio and production test mode features

- Full support for power savings modes
  - Bluetooth clock request
  - Bluetooth standard sniff
  - Deep-sleep modes and software regulator shutdown
- TCXO input and auto-detection of all standard handset clock frequencies. Also supports a low-power crystal, which can be used during power save mode for better timing accuracy.

Major FM Radio features include:

- 76 MHz to 108 MHz FM bands supported (US, Europe, and Japan)
- FM subsystem control using the Bluetooth HCI interface
- FM subsystem operates from reference clock inputs.
- Improved audio interface capabilities with full-featured bidirectional PCM, I^2S, and stereo analog output.
- I^2S can be master or slave.

FM Receiver-Specific Features Include:

- Excellent FM radio performance with 1 µV sensitivity for 26 dB (S+N)/N
- Signal-dependent stereo/mono blending
- Signal dependent soft mute
- Auto search and tuning modes
- Audio silence detection
- RSSI, IF frequency, status indicators
- RDS and RBDS demodulator and decoder with filter and buffering functions
- Automatic frequency jump

Bluetooth Radio

The BCM43341 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with the Bluetooth Radio Specification and EDR specification and meets or exceeds the requirements to provide the highest communication link quality of service.

Transmit

The BCM43341 features a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q upconversion, output power amplifier, and RF filtering. The transmitter path also incorporates $\pi/4$–DQPSK for 2 Mbps and 8–DPSK for 3 Mbps to support EDR. The transmitter section is compatible to the Bluetooth Low Energy specification. The transmitter PA bias can also be adjusted to provide Bluetooth class 1 or class 2 operation.

Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK, $\pi/4$–DQPSK, and 8–DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit-synchronization algorithm.

Power Amplifier

The fully integrated PA supports Class 1 or Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. Due to the linear nature of the PA combined with some integrated filtering, external filtering is required to meet the Bluetooth and regulatory harmonic and spurious requirements. For integrated mobile handset applications in which Bluetooth is integrated next to the cellular radio, external filtering can be applied to achieve near thermal noise levels for spurious and radiated noise emissions. The transmitter features a sophisticated on-chip transmit signal strength indicator (TSSI) block to keep the absolute output power variation within a tight range across process, voltage, and temperature.

Receiver

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology with built-in out-of-band attenuation enables the BCM43341 to be used in most applications with minimal off-chip filtering. For integrated handset operation, in which the Bluetooth function is integrated close to the cellular transmitter, external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

Receiver Signal Strength Indicator

The radio portion of the BCM43341 provides a Receiver Signal Strength Indicator (RSSI) signal to the baseband, so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

Local Oscillator Generation

Local Oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. The BCM43341 uses an internal RF and IF loop filter.

Calibration

The BCM43341 radio transceiver features an automated calibration scheme that is fully self contained in the radio. No user interaction is required during normal operation or during manufacturing to provide the optimal performance. Calibration optimizes the performance of all the major blocks within the radio to within 2% of optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs transparently during normal operation during the settling time of the hops and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

Section 5: Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening in the receiver.
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

Bluetooth 4.0 Features

The BBC supports all Bluetooth 4.0 features, with the following benefits:

- Dual-mode classic Bluetooth and classic Low Energy (BT and BLE) operation.
- Low Energy Physical Layer
- Low Energy Link Layer
- Enhancements to HCI for Low Energy
- Low Energy Direct Test mode
- AES encryption

Note: The BCM43341 is compatible with the Bluetooth Low Energy operating mode, which provides a dramatic reduction in the power consumption of the Bluetooth radio and baseband. The primary application for this mode is to provide support for low data rate devices, such as sensors and remote controls.

Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task performs a different state in the Bluetooth Link Controller.

- Major states:
  - Standby
  - Connection
- Substates:
  - Page
  - Page Scan
  - Inquiry
  - Inquiry Scan
  - Sniff
  - BLE Adv
  - BLE Scan/Initiation

Test Mode Support

The BCM43341 fully supports Bluetooth Test mode as described in Part I:1 of the *Specification of the Bluetooth System Version 3.0*. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test Mode, the BCM43341 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - Eight-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

Bluetooth Power Management Unit

The Bluetooth Power Management Unit (PMU) provides power management features that can be invoked by either software through power management registers or packet handling in the baseband core. The power management functions provided by the BCM43341 are:

- RF Power Management
- Host Controller Power Management
- BBC Power Management
- FM Power Management

RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver. The transceiver then processes the power-down functions accordingly.

Host Controller Power Management

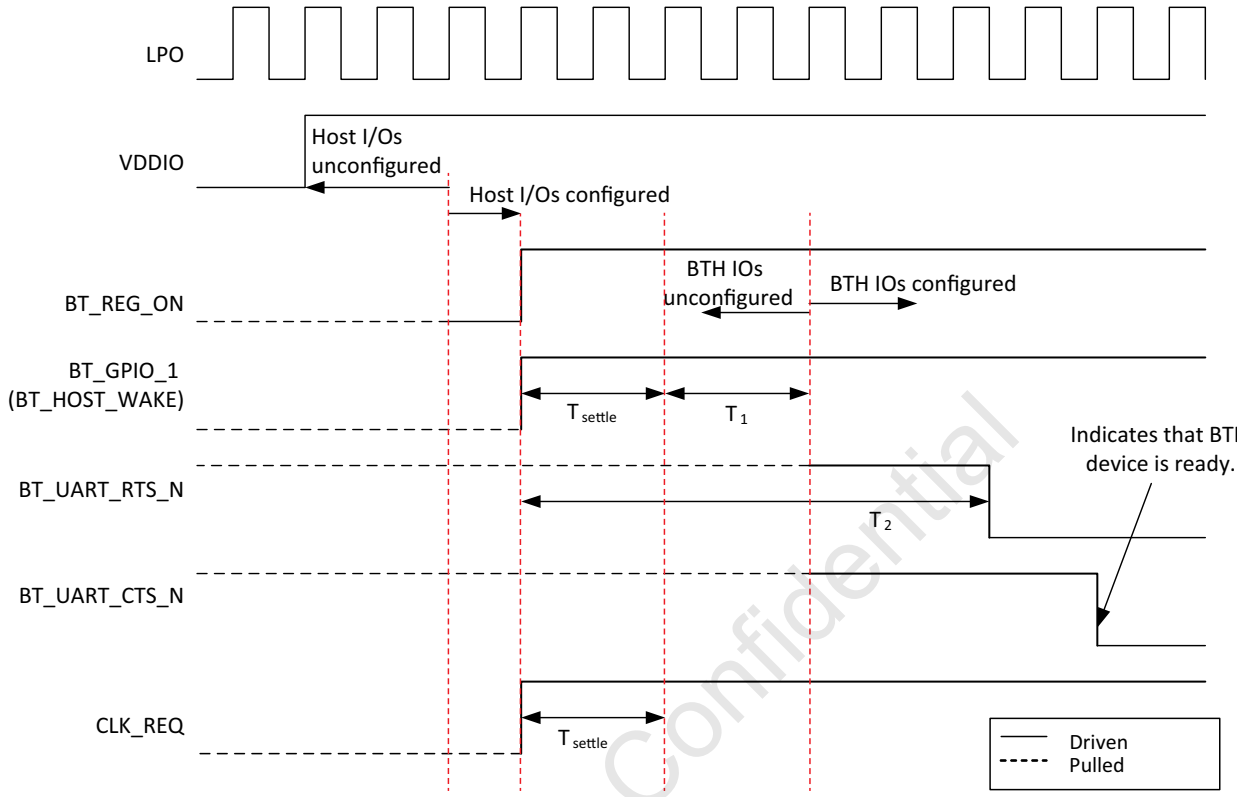
When running in UART mode, the BCM43341 may be configured so that dedicated signals are used for power management hand-shaking between the BCM43341 and the host. The basic power saving functions supported by those hand-shaking signals include the standard Bluetooth defined power savings modes and standby modes of operation.

Table 6 describes the power-control hand-shake signals used with the UART interface.

Table 6: Power Control Pin Description

Signal	*Type*	*Description*
BT_DEV_WAKE	I	Bluetooth device wake-up: Signal from the host to the BCM43341 indicating that the host requires attention. • Asserted: The Bluetooth device must wake-up or remain awake. • Deasserted: The Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
BT_HOST_WAKE	O	Host wake up. Signal from the BCM43341 to the host indicating that the BCM43341 requires attention. • Asserted: host device must wake-up or remain awake. • Deasserted: host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
CLK_REQ	O	The BCM43341 asserts CLK_REQ when Bluetooth, NFC, or WLAN directs the host to turn on the reference clock. The CLK_REQ polarity is active-high. Add an external 100 kΩ pull-down resistor to ensure the signal is deasserted when the BCM43341 powers up or resets when VDDIO is present.
Note: Pad function Control Register is set to 0 for these pins.		

Figure 11: Startup Signaling Sequence



Notes:

- T_1 is the time for the BTH device to settle its IOs after a reset and ref clk settling time elapsed.
- T_2 is the time for the BT device to complete initialization and drive BT_UART_RTS_N low.
- T_{settle} is the time for the ref clk signal from the host to be guaranteed to have settled.

BBC Power Management

The following are low-power operations for the BBC:

- Physical layer packet-handling turns the RF on and off dynamically within transmit/receive packets.
- Bluetooth-specified low-power connection modes: sniff, hold, and park. While in these modes, the BCM43341 runs on the low-power oscillator and wakes up after a predefined time period.
- A low-power shutdown feature allows the device to be turned off while the host and any other devices in the system remain operational. When the BCM43341 is not needed in the system, the RF and core supplies are shut down while the I/O remains powered. This allows the BCM43341 to effectively be off while keeping the I/O pins powered so they do not draw extra current from any other devices connected to the I/O.

  During the low-power shut-down state, provided VDDIO remains applied to the BCM43341, all outputs are tristated, and most input signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system and enables the BCM43341 to be fully integrated in an embedded device to take full advantage of the lowest power-saving modes.

  Two BCM43341 input signals are designed to be high-impedance inputs that do not load the driving signal even if the chip does not have VDDIO power supplied to it: the frequency reference input (WRF_TCXO_IN) and the 32.768 kHz input (LPO). When the BCM43341 is powered on from this state, it is the same as a normal power-up, and the device does not contain any information about its state from the time before it was powered down.

FM Power Management

The BCM43341 FM subsystem can operate independently of, or in tandem with, the Bluetooth RF and BBC subsystems. The FM subsystem power management scheme operates in conjunction with the Bluetooth RF and BBC subsystems. The FM block does not have a low power state, it is either on or off.

Wideband Speech

The BCM43341 provides support for wideband speech (WBS) using on-chip Smart Audio technology. The BCM43341 can perform subband-codec (SBC), as well as mSBC, encoding and decoding of linear 16 bits at 16 kHz (256 Kbps rate) transferred over the PCM bus.

Packet Loss Concealment

Packet Loss Concealment (PLC) improves apparent audio quality for systems with marginal link performance. Bluetooth messages are sent in packets. When a packet is lost, it creates a gap in the received audio bit-stream. Packet loss can be mitigated in several ways:

- Fill in zeros.
- Ramp down the output audio signal toward zero (this is the method used in current Bluetooth headsets).
- Repeat the last frame (or packet) of the received bit-stream and decode it as usual (frame repeat).

These techniques cause distortion and popping in the audio stream. The BCM43341 uses a proprietary waveform extension algorithm to provide dramatic improvement in the audio quality. Figure 12 and Figure 13 show audio waveforms with and without Packet Loss Concealment. Broadcom PLC/BEC algorithms also support wideband speech.

Figure 12: CVSD Decoder Output Waveform Without PLC

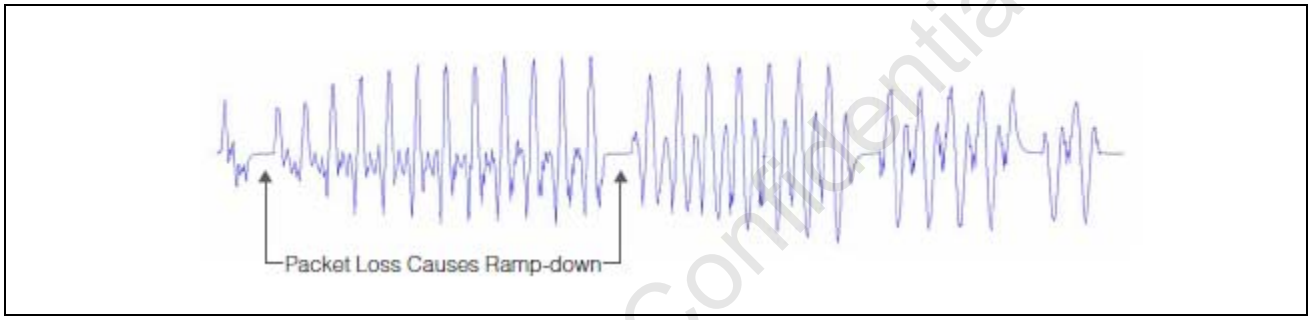
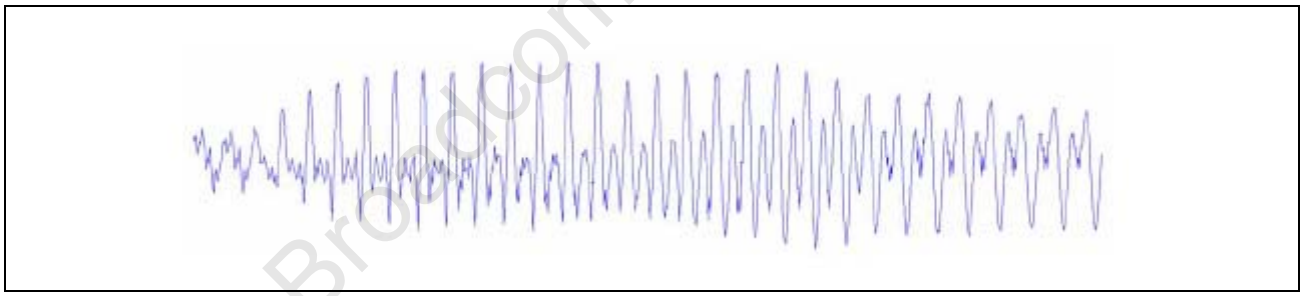


Figure 13: CVSD Decoder Output Waveform After Applying PLC



Audio Rate-Matching Algorithms

The BCM43341 has an enhanced rate-matching algorithm that uses interpolation algorithms to reduce audio stream jitter that may be present when the rate of audio data coming from the host is not the same as the Bluetooth or FM audio data rates.

Codec Encoding

The BCM43341 can support SBC and mSBC encoding and decoding for wideband speech.

Multiple Simultaneous A2DP Audio Stream

The BCM43341 has the ability to take a single audio stream and output it to multiple Bluetooth devices simultaneously. This allows a user to share his or her music (or any audio stream) with a friend.

FM Over Bluetooth

FM Over Bluetooth enables the BCM43341 to stream data from FM over Bluetooth without requiring the host to be awake. This can significantly extend battery life for usage cases where someone is listening to FM radio on a Bluetooth headset.

Burst Buffer Operation

The BCM43341 has a data buffer that can buffer data being sent over the HCI and audio transports, then send the data at an increased rate. This mode of operation allows the host to sleep for the maximum amount of time, dramatically reducing system current consumption.

Adaptive Frequency Hopping

The BCM43341 gathers link quality statistics on a channel by channel basis to facilitate channel assessment and channel map selection. The link quality is determined using both RF and baseband signal processing to provide a more accurate frequency-hop map.

Advanced Bluetooth/WLAN Coexistence

The BCM43341 includes advanced coexistence technologies that are only possible with a Bluetooth/WLAN integrated die solution. These coexistence technologies are targeted at small form-factor platforms, such as cell phones and media players, including applications such as VoWLAN + SCO and Video-over-WLAN + High Fidelity BT Stereo.

Support is provided for platforms that share a single antenna between Bluetooth and WLAN. Dual-antenna applications are also supported. The BCM43341 radio architecture allows for lossless simultaneous Bluetooth and WLAN reception for shared antenna applications. This is possible only via an integrated solution (shared LNA and joint AGC algorithm). It has superior performance versus implementations that need to arbitrate between Bluetooth and WLAN reception.

The BCM43341 integrated solution enables MAC-layer signaling (firmware) and a greater degree of sharing via an enhanced coexistence interface. Information is exchanged between the Bluetooth and WLAN cores without host processor involvement.

The BCM43341 also supports Transmit Power Control on the STA together with standard Bluetooth TPC to limit mutual interference and receiver desensitization. Preemption mechanisms are utilized to prevent AP transmissions from colliding with Bluetooth frames. Improved channel classification techniques have been implemented in Bluetooth for faster and more accurate detection and elimination of interferers (including non-WLAN 2.4 GHz interference).

The Bluetooth AFH classification is also enhanced by the WLAN core's channel information.

Fast Connection (Interlaced Page and Inquiry Scans)

The BCM43341 supports page scan and inquiry scan modes that significantly reduce the average inquiry response and connection times. These scanning modes are compatible with the Bluetooth version 2.1 page and inquiry procedures.

Section 6: Microprocessor and Memory Unit for Bluetooth

The Bluetooth microprocessor core is based on the ARM® Cortex™-M3 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. It runs software from the link control (LC) layer, up to the host controller interface (HCI).

The ARM core is paired with a memory unit that contains 652 KB of ROM memory for program storage and boot ROM, 195 KB of RAM for data scratchpad and patch RAM code. The internal ROM allows for flexibility during power-on reset to enable the same device to be used in various configurations. At power-up, the lower-layer protocol stack is executed from the internal ROM memory.

External patches may be applied to the ROM-based firmware to provide flexibility for bug fixes or features additions. These patches may be downloaded from the host to the BCM43341 through the UART transports. The mechanism for downloading via UART is identical to the proven interface of the BCM4329 and BCM4330 devices.

RAM, ROM, and Patch Memory

The BCM43341 Bluetooth core has 195 KB of internal RAM which is mapped between general purpose scratch pad memory and patch memory and 652 KB of ROM used for the lower-layer protocol stack, test mode software, and boot ROM. The patch memory capability enables the addition of code changes for purposes of feature additions and bug fixes to the ROM memory.

Reset

The BCM43341 has an integrated power-on reset circuit that resets all circuits to a known power-on state. The BT power-on reset (POR) circuit is out of reset after BT_REG_ON goes High. If BT_REG_ON is low, then the POR circuit is held in reset.

Section 7: Bluetooth Peripheral Transport Unit

PCM Interface

The BCM43341 supports two independent PCM interfaces that share the pins with the I^2S interfaces. The PCM Interface on the BCM43341 can connect to linear PCM Codec devices in master or slave mode. In master mode, the BCM43341 generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the BCM43341. The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

Slot Mapping

The BCM43341 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz, or 1024 kHz. The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

Frame Synchronization

The BCM43341 supports both short- and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

Data Formatting

The BCM43341 may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the BCM43341 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2’s complement data, left justified, and clocked MSB first.

Wideband Speech Support

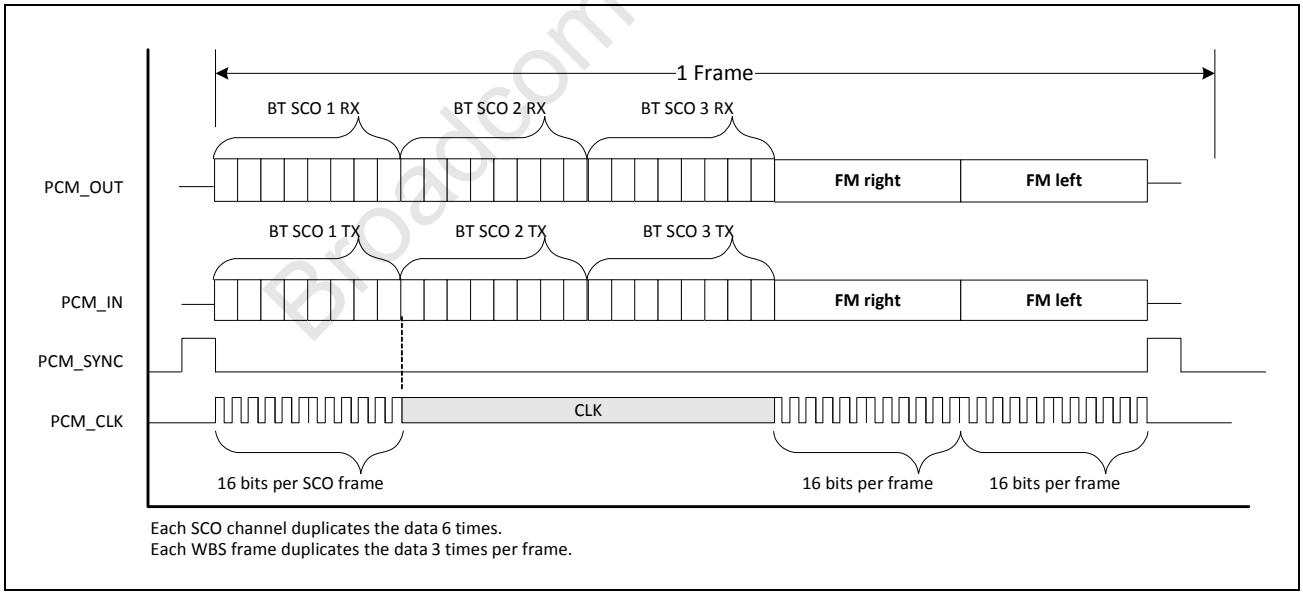
When the host encodes Wideband Speech (WBS) packets in transparent mode, the encoded packets are transferred over the PCM bus for an eSCO voice connection. In this mode, the PCM bus is typically configured in master mode for a 4 kHz sync rate with 16-bit samples, resulting in a 64 kbps bit rate. The BCM43341 also supports slave transparent mode using a proprietary rate-matching scheme. In SBC-code mode, linear 16-bit data at 16 kHz (256 kbps rate) is transferred over the PCM bus.

Multiplexed Bluetooth and FM Over PCM

In this mode of operation, the BCM43341 multiplexes both FM and Bluetooth audio PCM channels over the same interface, reducing the number of required I/Os. This mode of operation is initiated through an HCI command from the host. The format of the data stream consists of three channels: a Bluetooth channel followed by two FM channels (audio left and right). In this mode of operation, the bus data rate only supports 48 kHz operation per channel with 16 bits sent for each channel. This is done to allow the low data rate Bluetooth data to coexist in the same interface as the higher speed I^2S data. To accomplish this, the Bluetooth data is repeated six times for 8 kHz data and three times for 16 kHz data. An initial sync pulse on the PCM_SYNC line is used to indicate the beginning of the frame.

To support multiple Bluetooth audio streams within the Bluetooth channel, both 16 kHz and 8 kHz streams can be multiplexed. This mode of operation is only supported when the Bluetooth host is the master. Figure 14 shows the operation of the multiplexed transport with three simultaneous SCO connections. To accommodate additional SCO channels, the transport clock speed is increased. To change between modes of operation, the transport must be halted and restarted in the new configuration.

Figure 14: Functional Multiplex Data Diagram



Burst PCM Mode

In this mode of operation, the PCM bus runs at a significantly higher rate of operation to allow the host to duty cycle its operation and save current. In this mode of operation, the PCM bus can operate at a rate of up to 24 MHz. This mode of operation is initiated with an HCI command from the host.

PCM Interface Timing

Short Frame Sync, Master Mode

Figure 15: PCM Timing Diagram (Short Frame Sync, Master Mode)

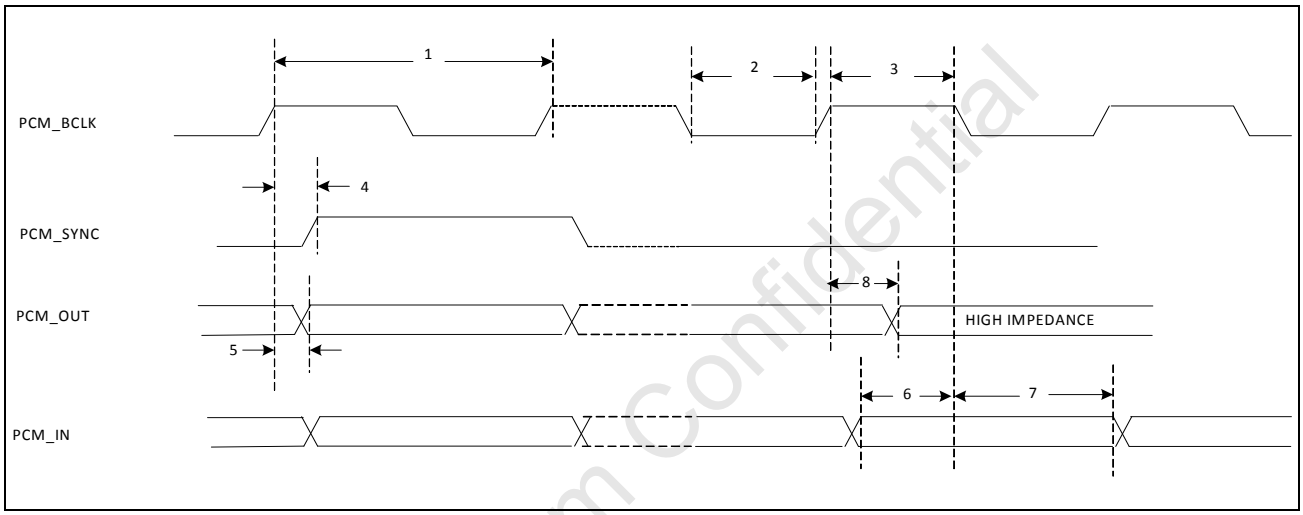


Table 7: PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Slave Mode

Figure 16: PCM Timing Diagram (Short Frame Sync, Slave Mode)

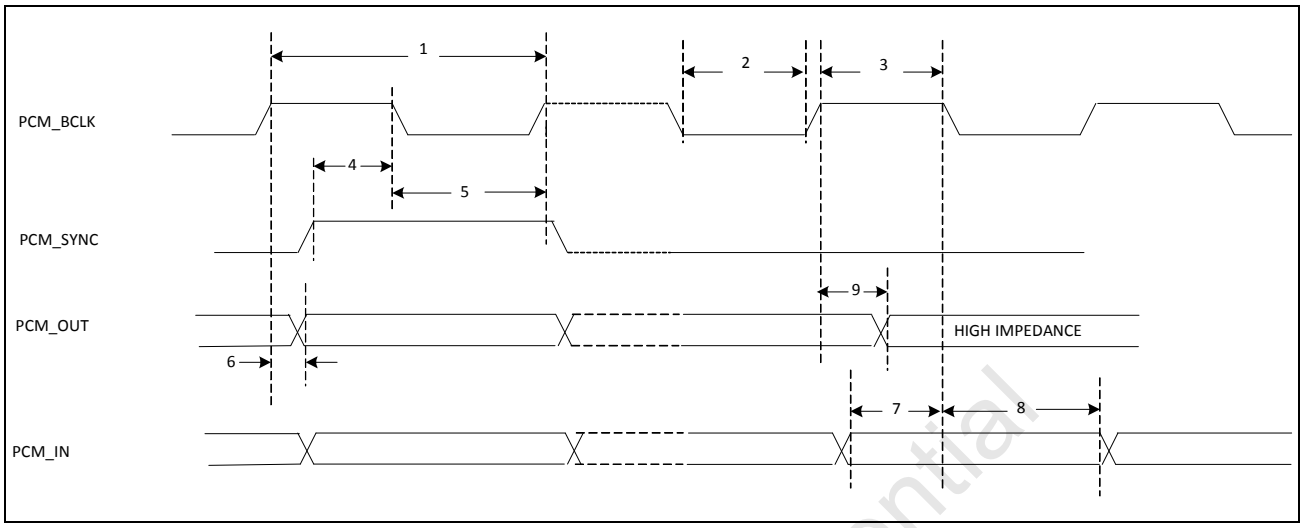


Table 8: PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Master Mode

Figure 17: PCM Timing Diagram (Long Frame Sync, Master Mode)

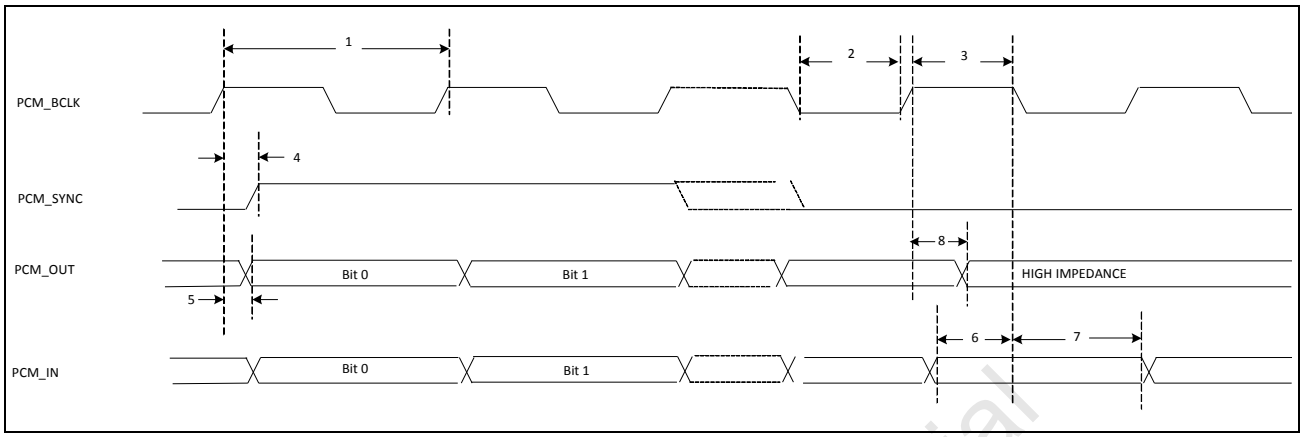


Table 9: PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Slave Mode

Figure 18: PCM Timing Diagram (Long Frame Sync, Slave Mode)

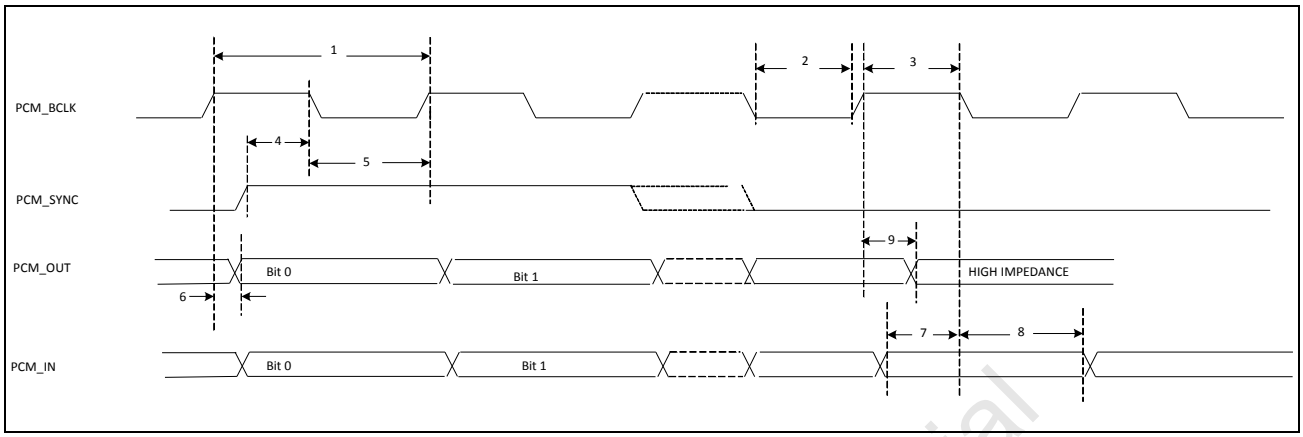


Table 10: PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Burst Mode

Figure 19: PCM Burst Mode Timing (Receive Only, Short Frame Sync)

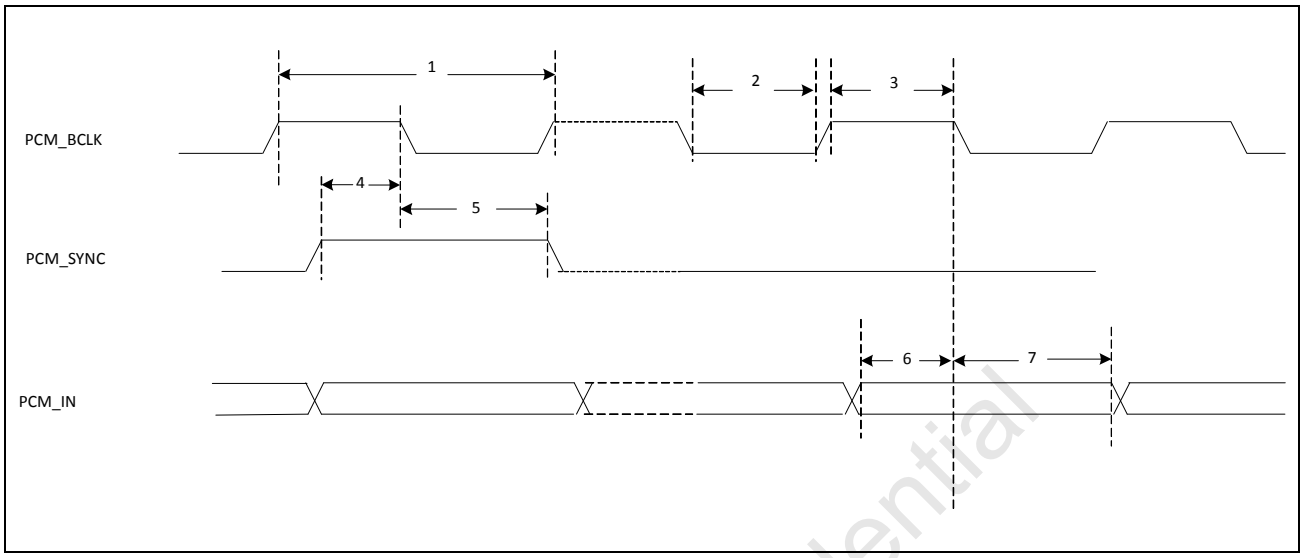


Table 11: PCM Burst Mode (Receive Only, Short Frame Sync)

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low	20.8	–	–	ns
3	PCM bit clock high	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

Long Frame Sync, Burst Mode

Figure 20: PCM Burst Mode Timing (Receive Only, Long Frame Sync)

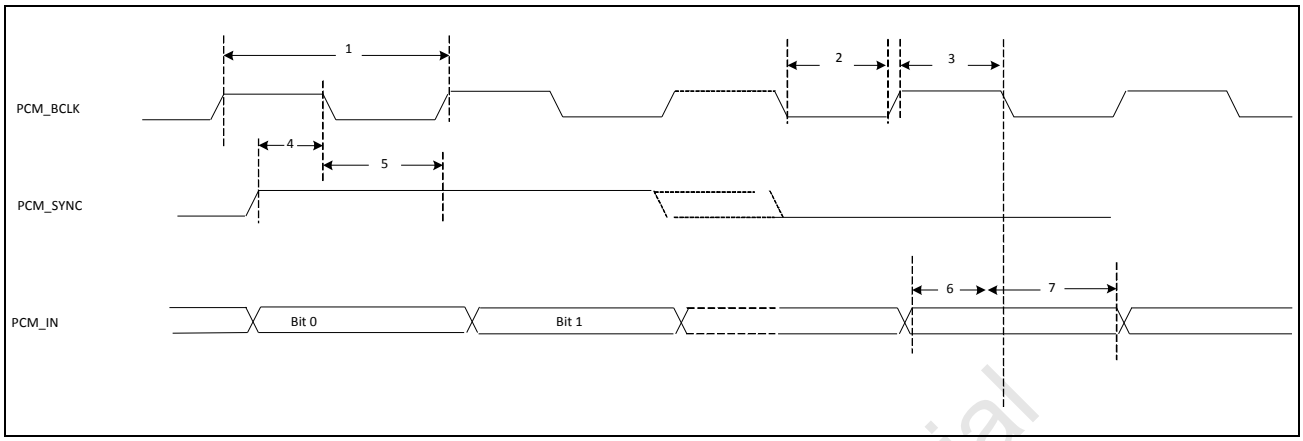


Table 12: PCM Burst Mode (Receive Only, Long Frame Sync)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low	20.8	–	–	ns
3	PCM bit clock high	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

UART Interface

The BCM43341 shares a single UART for Bluetooth and FM. The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

The UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 4.0 UART HCI specification: H4 and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (“Three-wire UART Transport Layer”). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The BCM43341 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The BCM43341 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2% (see Table 13).

Table 13: Example of Common Baud Rates

Desired Rate	*Actual Rate*	*Error (%)*
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

UART timing is defined in Figure 21 and Table 14.

Figure 21: UART Timing

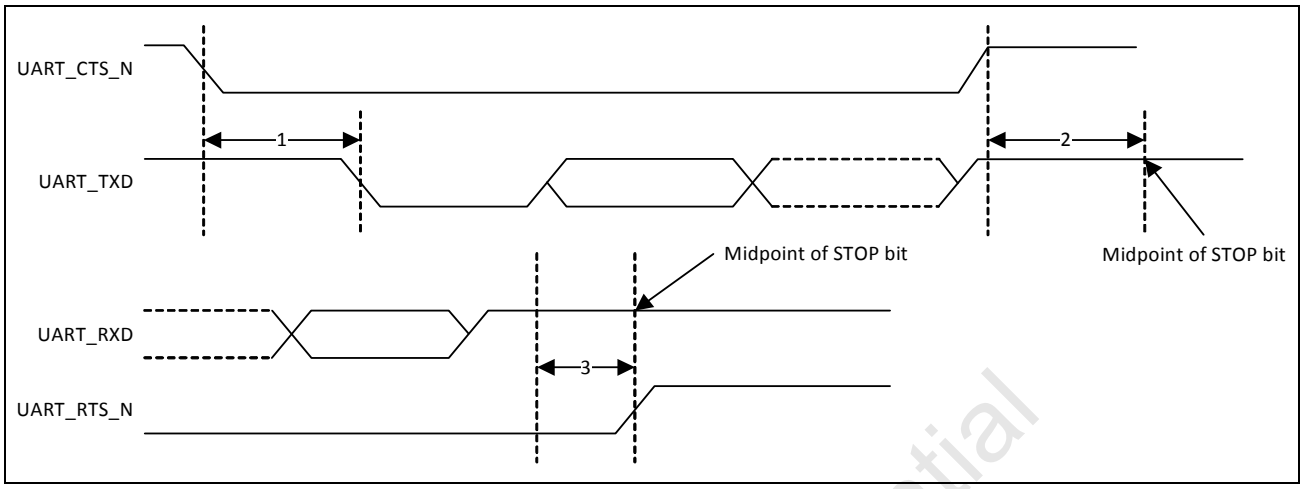


Table 14: UART Timing Specifications

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	–	0.5	Bit periods

I2S Interface

The BCM43341 supports an independent I2S digital audio port for high-fidelity FM audio or Bluetooth audio. The I2S interface supports both master and slave modes. The I2S signals are:

- I2S clock: I2S SCK
- I2S Word Select: I2S WS
- I2S Data Out: I2S SDO
- I2S Data In: I2S SDI

I2S SCK and I2S WS become outputs in master mode and inputs in slave mode, while I2S SDO always stays as an output. The channel word length is 16 bits and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I2S bus, per the I2S specification. The MSB of each data word is transmitted one bit clock cycle after the I2S WS transition, synchronous with the falling edge of bit clock. Left-channel data is transmitted when I2S WS is low, and right-channel data is transmitted when I2S WS is high. Data bits sent by the BCM43341 are synchronized with the falling edge of I2S_SCK and should be sampled by the receiver on the rising edge of I2S_SSCK.

The clock rate in master mode is either of the following:

48 kHz x 32 bits per frame = 1.536 MHz

48 kHz x 50 bits per frame = 2.400 MHz

The master clock is generated from the input reference clock using a N/M clock divider.

In the slave mode, any clock rate is supported to a maximum of 3.072 MHz.

I²S Timing

Note: Timing values specified in Table 15 are relative to high and low threshold levels.

Table 15: Timing for I²S Transmitters and Receivers

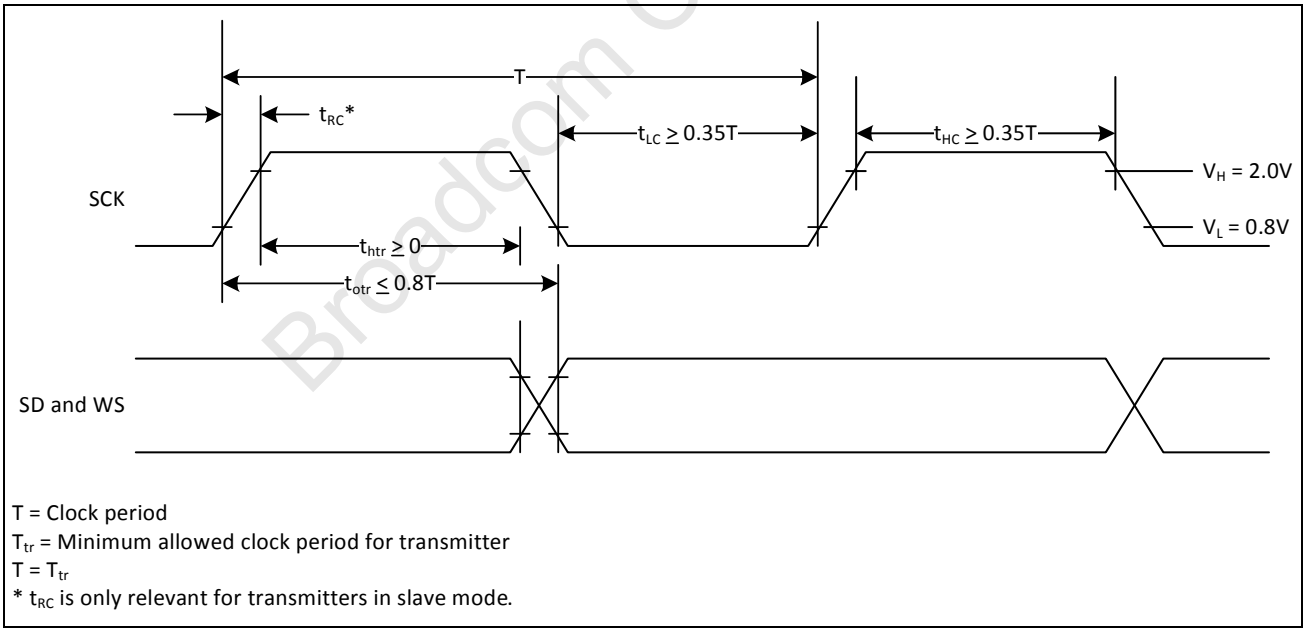
	Transmitter				Receiver				
	Lower LImit		Upper Limit		Lower Limit		Upper Limit		
	Min	Max	Min	Max	Min	Max	Min	Max	Notes
Clock Period T	T_{tr}	–	–	–	T_r	–	–	–	1
Master Mode: Clock generated by transmitter or receiver									
High t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	2
Low t_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	2
Slave Mode: Clock accepted by transmitter or receiver									
High t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	3
Low t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	3
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–	–		–	4
Transmitter									
Delay t_{dtr}	–	–	–	0.8T	–	–	–	–	5
Hold time t_{htr}	0	–	–	–	–	–	–	–	4
Receiver									
Setup time t_{sr}	–	–	–	–	–	$0.2T_r$	–	–	6
Hold time t_{hr}	–	–	–	–	–	0	–	–	6

Note:

- The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
- At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.
- In slave mode, the transmitter and receiver need a clock signal with minimum high and low periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used.
- Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.
- To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
- The data setup and hold time must not be less than the specified receiver setup and hold time.

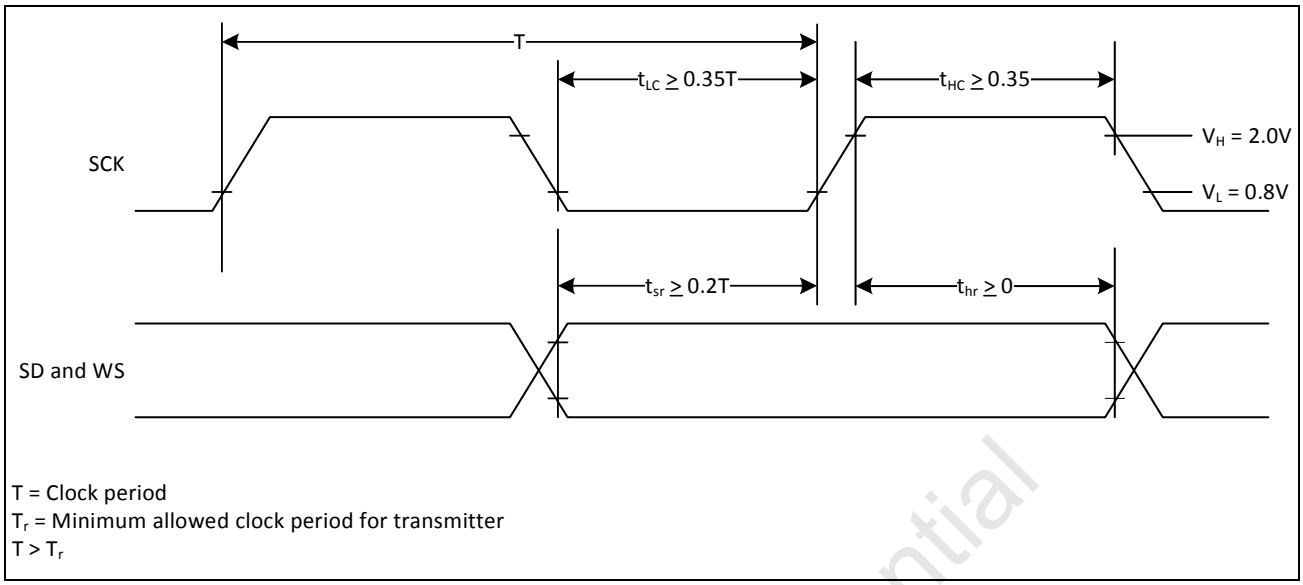
Note: The time periods specified in Figure 22 and Figure 23 on page 68 are defined by the transmitter speed. The receiver specifications must match transmitter performance.

Figure 22: I²S Transmitter Timing



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
$T = T_{tr}$
* t_{RC} is only relevant for transmitters in slave mode.

Figure 23: I2S Receiver Timing



Section 8: FM Receiver Subsystem

FM Radio

The BCM43341 includes a completely integrated FM radio receiver with RDS/RBDS covering all FM bands from 76 MHz to 108 MHz. The receiver is controlled through commands on the HCI. FM received audio is available as a stereo analog output or in digital form through I^2S or PCM. The FM radio operates from the external clock reference.

Digital FM Audio Interfaces

The FM audio can be transmitted via the shared PCM and I^2S pins, and the sampling rate is programmable. The BCM43341 supports a three-wire PCM or I^2S audio interface in either master or slave configuration. The master or slave configuration is selected using vendor specific commands over the HCI interface. In addition, multiple sampling rates are supported, derived from either the FM or Bluetooth clocks. In master mode, the clock rate is either of the following:

- 48 kHz x 32 bits per frame = 1.536 MHz
- 48 kHz x 50 bits per frame = 2.400 MHz

In slave mode, any clock rate is supported up to a maximum of 3.072 MHz.

Analog FM Audio Interfaces

The demodulated FM audio signal is available as line-level analog stereo output, generated by twin internal high SNR audio DACs.

FM Over Bluetooth

The BCM43341 can output received FM audio onto Bluetooth using one of following three links: eSCO, WBS, and A2DP. In all of the above modes, once the link has been set up, the host processor can enter sleep mode while the BCM43341 continues to stream FM audio to the remote Bluetooth device, allowing the system current consumption to be minimized.

eSCO

In this use case, the stereo FM audio is downsampled to 8 kHz and a mono or stereo stream is then sent through the Bluetooth eSCO link to a remote Bluetooth device, typically a headset. Two Bluetooth voice connections must be used to transport stereo.

Wideband Speech Link

In this case, the stereo FM audio is downsampled to 16 kHz and a mono or stereo stream is then sent through the Bluetooth wideband speech link to a remote Bluetooth device, typically a headset. Two Bluetooth voice connections must be used to transport stereo.

A2DP

In this case, the stereo FM audio is encoded by the on-chip SBC encoder and transported as an A2DP link to a remote Bluetooth device. Sampling rates of 48 kHz, 44.1 kHz, and 32 kHz joint stereo are supported. An A2DP lite stack is implemented in the BCM43341 to support this use case, which eliminates the need to route the SBC-encoded audio back to the host to create the A2DP packets.

Autotune and Search Algorithms

The BCM43341 supports a number of FM search and tune functions that allows the host to implement many convenient user functions, which are accessed through the Broadcom FM stack.

- Tune to Play—Allows the FM receiver to be programmed to a specific frequency.
- Search for SNR > Threshold—Checks the power level of the available channel and the estimated SNR of the channel to help achieve precise control of the expected sound quality for the selected FM channel. Specifically, the host can adjust its SNR requirements to retrieve a signal with a specific sound quality, or adjust this to return the weakest channels.
- Alternate Frequency Jump—Allows the FM receiver to automatically jump to an alternate FM channel that carries the same information, but has a better SNR. For example, when traveling, a user may pass through a region where a number of channels carry the same station. When the user passes from one area to the next, the FM receiver can automatically switch to another channel with a stronger signal to spare the user from having to manually change the channel to continue listening to the same station.

Audio Features

A number of features are implemented in the BCM43341 to provide the best possible audio experience for the user.

- Mono/Stereo Blend or Switch—The BCM43341 provides automatic control of the stereo or mono settings based on the FM signal carrier-to-noise ratio (C/N). This feature is used to maintain the best possible audio SNR based on the FM channel condition. Two modes of operation are supported:
  - Blend—In this mode, fine control of stereo separation is used to achieve optimal audio quality over a wide range of input C/N. The amount of separation is fully programmable. In Figure 24, the separation is programmed to maintain a minimum 50 dB SNR across the blend range.
  - Switch—In this mode, the audio switches from full stereo to full mono at a predetermined level to maintain optimal audio quality. The stereo-to-mono switch point and the mono-to-stereo switch points are fully programmable to provide the desired amount of audio SNR. In Figure 25, the switch point is programmed to switch to mono to maintain a 40 dB SNR.

Figure 24: Example Blend/Switch Usage

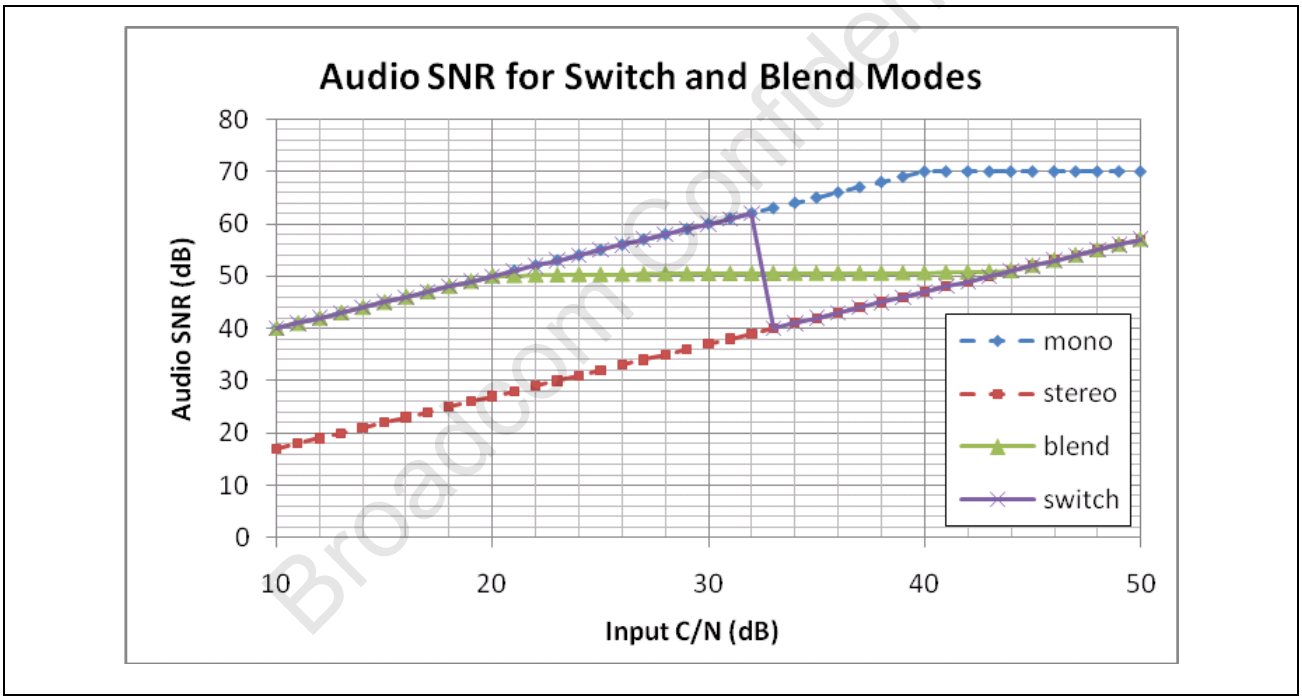
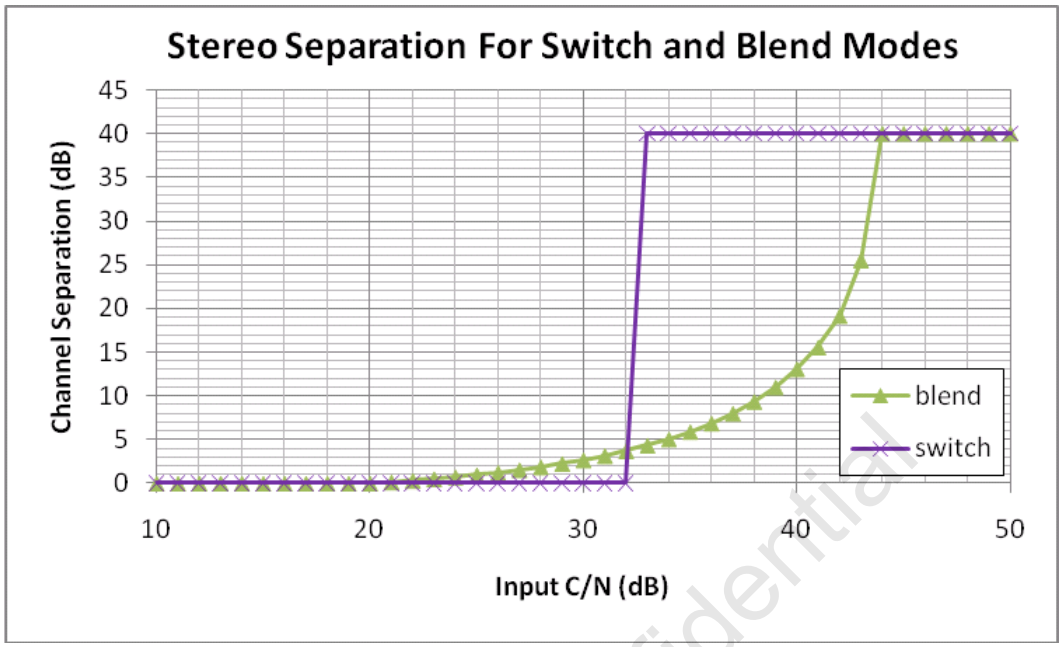
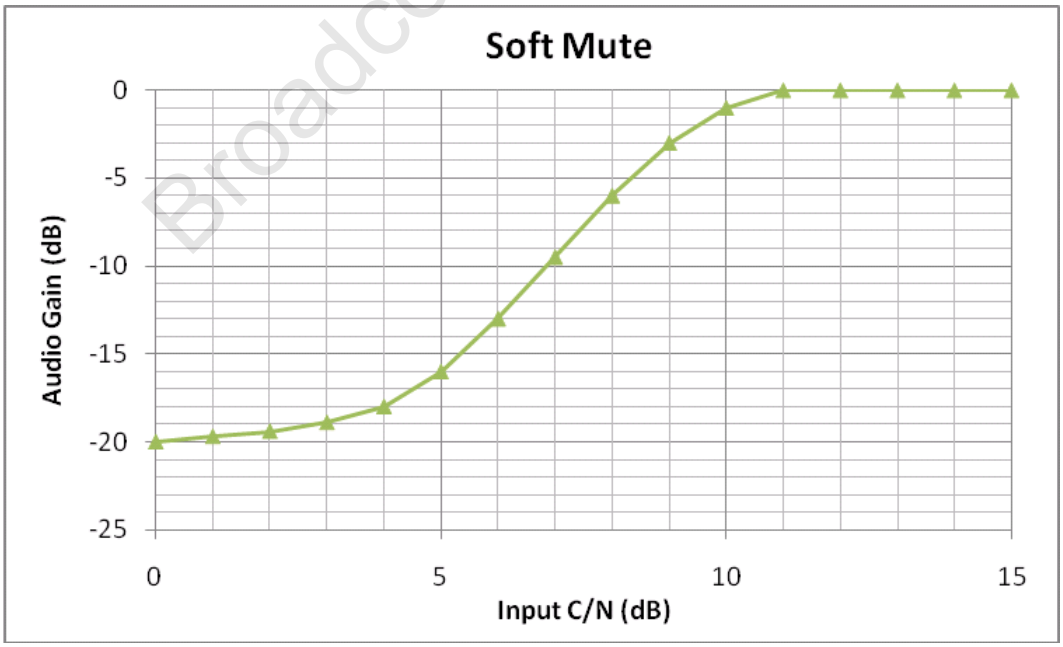


Figure 25: Example Blend/Switch Separation



- Soft Mute—Improves the user experience by dynamically muting the output audio proportionate to the FM signal C/N. This prevents the user from being assaulted with a blast of static. The mute characteristic is fully programmable to accommodate fine tuning of the output signal level. An example mute characteristic is shown in Figure 26.

Figure 26: Example Soft Mute Characteristic



- High Cut—A programmable high-cut filter is provided to reduce the amount of high-frequency noise caused by static in the output audio signal. Like the soft mute circuit, it is fully programmable to allow for any amount of high cut based on the FM signal C/N.
- Audio Pause Detect—The FM receiver monitors the magnitude of the audio signal and notifies the host through an interrupt when the magnitude of the signal has fallen below the threshold set for a programmable period. This feature can be used to provide alternate frequency jumps during periods of silence to minimize disturbances to the listener. Filtering techniques are used within the audio pause detection block to provide more robust presence-to-silence detection and silence-to-presence detection.
- Automatic Antenna Tuning—The BCM43341 has an on-chip automatic antenna tuning network. When used with a single off-chip inductor, the on-chip circuitry automatically chooses an optimal on-chip matching component to obtain the highest signal strength for the desired frequency. The high-Q nature of this matching network simultaneously provides out-of-band blocking protection as well as a reduction of radiated spurious emissions from the FM antenna. It is designed to accommodate a wide range of external wire antennas.

RDS/RBDS

The BCM43341 integrates a RDS/RBDS modem, the decoder includes programmable filtering and buffering functions. The RDS/RBDS data can be read out through the HCI interface.

In addition, the RDS/RBDS receive functionality supports the following:

- Block decoding, error correction and synchronization
- Flywheel synchronization feature, allowing the host to set parameters for acquisition, maintenance, and loss of sync. (It is possible to set up the BCM43341 such that synch is achieved when a minimum of two good blocks (error free) are decoded in sequence. The number of good blocks required for sync is programmable.)
- Storage capability up to 126 blocks of RDS data
- Full or partial block B match detect and interrupt to host
- Audio pause detection with programmable parameters
- Program Identification (PI) code detection and interrupt to host
- Automatic frequency jump
- Block E filtering
- Soft mute
- Signal dependent mono/stereo blend

Section 9: WLAN Global Functions

WLAN CPU and Memory Subsystem

The BCM43341 includes an integrated ARM Cortex-M3™ processor with internal RAM and ROM. The ARM Cortex-M3 processor is a low-power processor that features low gate count, low interrupt latency, and low-cost debug. It is intended for deeply embedded applications that require fast interrupt response features. The processor implements the ARM architecture v7-M with support for Thumb®-2 instruction set. ARM Cortex-M3 delivers 30% more performance gain over ARM7TDMI®.

At 0.19 µW/MHz, the Cortex-M3 is the most power efficient general purpose microprocessor available, outperforming 8- and 16-bit devices on MIPS/µW. It supports integrated sleep modes.

ARM Cortex-M3 uses multiple technologies to reduce cost through improved memory utilization, reduced pin overhead, and reduced silicon area. ARM Cortex-M3 supports independent buses for code and data access (ICode/DCode and system buses). ARM Cortex-M3 supports extensive debug features including real time trace of program execution.

On-chip memory for the CPU includes 512 KB SRAM and 640 KB ROM.

One-Time Programmable Memory

Various hardware configuration parameters may be stored in an internal 3072-bit One-Time Programmable (OTP) memory, which is read by the system software after device reset. In addition, customer-specific parameters, including the system vendor ID and the MAC address can be stored, depending on the specific board design.

The initial state of all bits in an unprogrammed OTP device is 0. After any bit is programmed to a 1, it cannot be reprogrammed to 0. The entire OTP array can be programmed in a single write cycle using a utility provided with the Broadcom WLAN manufacturing test tools. Alternatively, multiple write cycles can be used to selectively program specific bytes, but only bits which are still in the 0 state can be altered during each programming cycle.

Prior to OTP programming, all values should be verified using the appropriate editable nvram.txt file, which is provided with the reference board design package.

GPIO Interface

On the WLBGA package, there are 8 GPIO pins available on the WLAN section of the BCM43341 that can be used to connect to various external devices.

Upon power up and reset, these pins become tristated. Subsequently, they can be programmed to be either input or output pins via the GPIO control register.

External Coexistence Interface

An external handshake interface is available to enable signaling between the device and an external co-located wireless device, such as GPS, WiMAX, LTE, or UWB, to manage wireless medium sharing for optimum performance. The coexistence signals in Figure 27 and Table 16 can be enabled by software on the indicated GPIO pins.

Figure 27: LTE Coexistence Interface

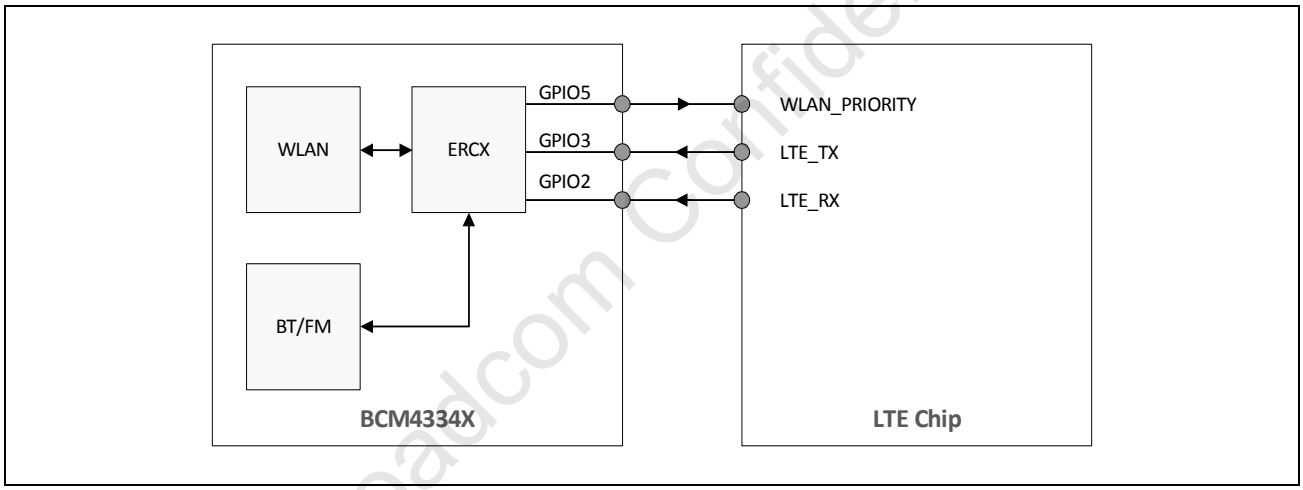


Table 16: External Coexistence Interface

Coexistence Signal	*GPIO Name*	*Type*	*Comment*
ERCX_TX_CONF/ WLAN_PRIORITY	GPIO_5	Output	Notify LTE of request to sleep
ERCX_FREQ/LTE_TX	GPIO_3	Input	Notify WLAN RX of requirement to sleep
ERCX_RF_ACTIVE/LTE_RX	GPIO_2	Input	Notify WLAN TX to reduce TX power

UART Interface

One UART interface can be enabled by software as an alternate function on pins WL_GPIO4 and WL_GPIO_5. Provided primarily for debugging during development, this UART enables the BCM43341 to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART and provides a FIFO size of 64 × 8 in each direction.

JTAG Interface

The BCM43341 supports the IEEE 1149.1 JTAG boundary scan standard for performing device package and PCB assembly testing during manufacturing. In addition, the JTAG interface allows Broadcom to assist customers by using proprietary debug and characterization test tools during board bring-up. Therefore, it is highly recommended to provide access to the JTAG pins by means of test points or a header on all PCB designs.

Section 10: WLAN Host Interfaces

SDIO v2.0

The BCM43341 WLAN section supports SDIO version 2.0, including the following modes:

DS: Default speed up to 25 MHz, including 1- and 4-bit modes (3.3V signaling)
HS: High speed up to 50 MHz (3.3V signaling)

It also has the ability to map the interrupt signal onto a GPIO pin for applications requiring an interrupt different than what is provided by the SDIO interface. The ability to force control of the gated clocks from within the device is also provided. SDIO mode is enabled using the strapping option pins strap_host_ifc_[3:1].

Three functions are supported:

- Function 0 standard SDIO function (Max BlockSize/ByteCount = 32B)
- Function 1 backplane function to access the internal system-on-chip (SoC) address space (Max BlockSize/ByteCount = 64B)
- Function 2 WLAN function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount = 512B)

SDIO Pin Descriptions

Table 17: SDIO Pin Description

SD 4-Bit Mode		*SD 1-Bit Mode*		*gSPI Mode*	
DATA0	Data line 0	DATA	Data line	DO	Data output
DATA1	Data line 1 or Interrupt	IRQ	Interrupt	IRQ	Interrupt
DATA2	Data line 2 or Read Wait	RW	Read Wait	NC	Not used
DATA3	Data line 3	N/C	Not used	CS	Card select
CLK	Clock	CLK	Clock	SCLK	Clock
CMD	Command line	CMD	Command line	DI	Data input

Figure 28: Signal Connections to SDIO Host (SD 4-Bit Mode)

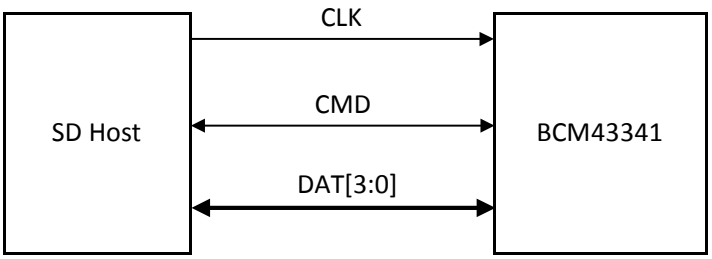


Figure 29: Signal Connections to SDIO Host (SD 1-Bit Mode)

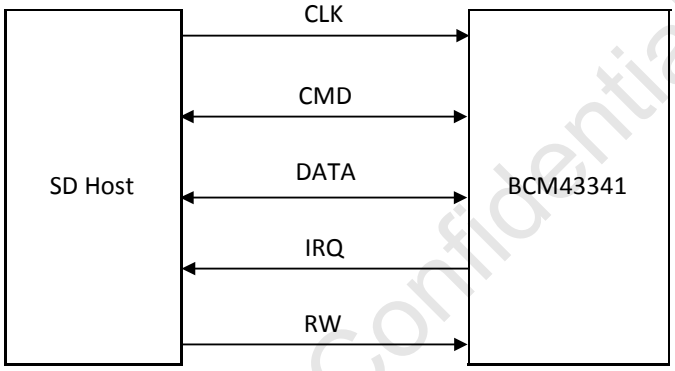
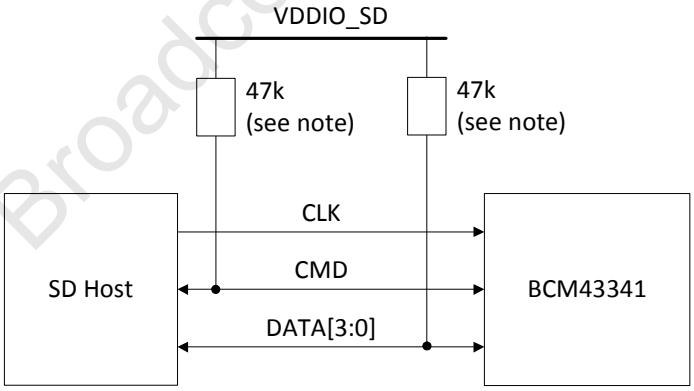


Figure 30: SDIO Pull-Up Requirements



Note: Per Section 6 of the SDIO specification, 10 to 100 kohm pull-ups are required on the four DATA lines and the CMD line. This requirement must be met during all operating states by using external pull-up resistors or properly programming internal SDIO Host pull-ups. The BCM43341 does not have internal pull-ups on these lines.

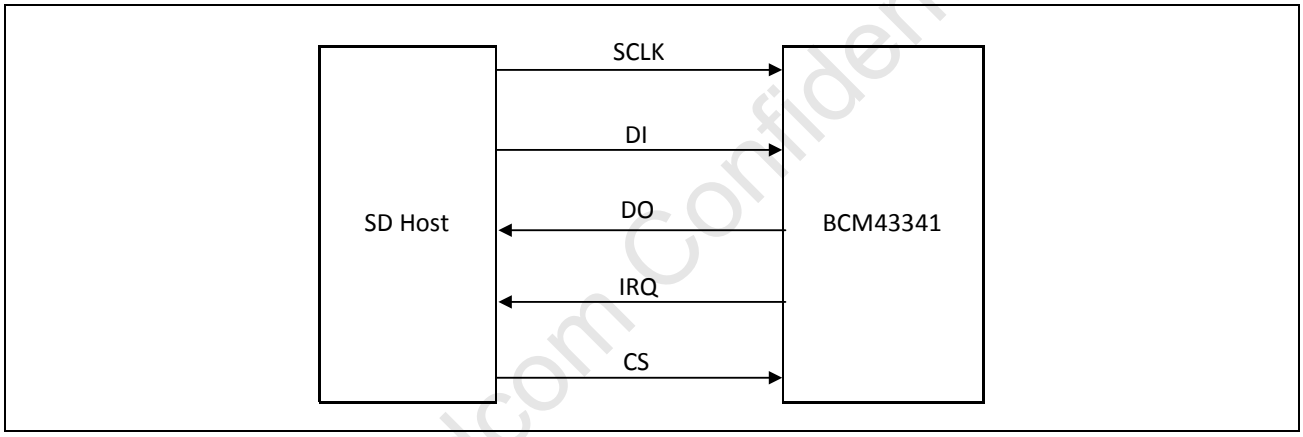
Generic SPI Mode

In addition to the full SDIO mode, the BCM43341 includes the option of using the simplified generic SPI (gSPI) interface/protocol. Characteristics of the gSPI mode include:

- Supports up to 48 MHz operation
- Supports fixed delays for responses and data from device
- Supports alignment to host gSPI frames (16 or 32 bits)
- Supports up to 2 KB frame size per transfer
- Supports little endian (default) and big endian configurations
- Supports configurable active edge for shifting
- Supports packet transfer through DMA for WLAN

gSPI mode is enabled using the strapping option pins strap_host_ifc_[3:1].

Figure 31: Signal Connections to SDIO Host (gSPI Mode)



SPI Protocol

The SPI protocol supports both 16-bit and 32-bit word operation. Byte endianness is supported in both modes. Figure 32 and Figure 33 show the basic write and write/read commands.

Figure 32: gSPI Write Protocol

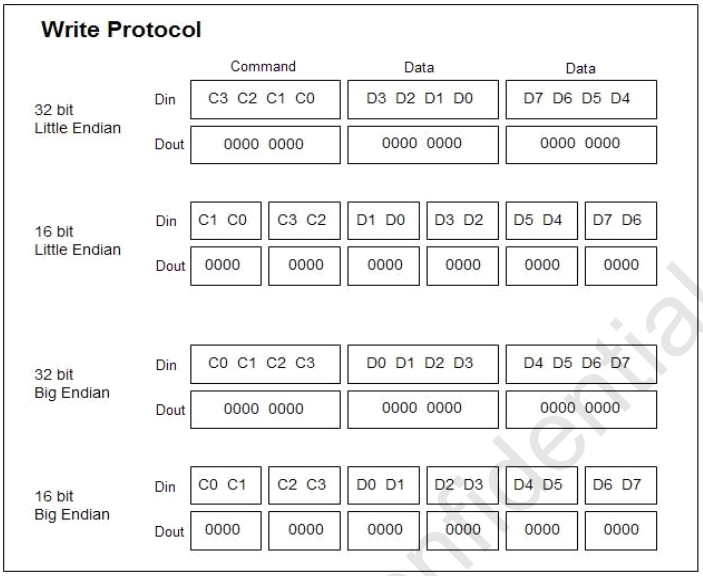
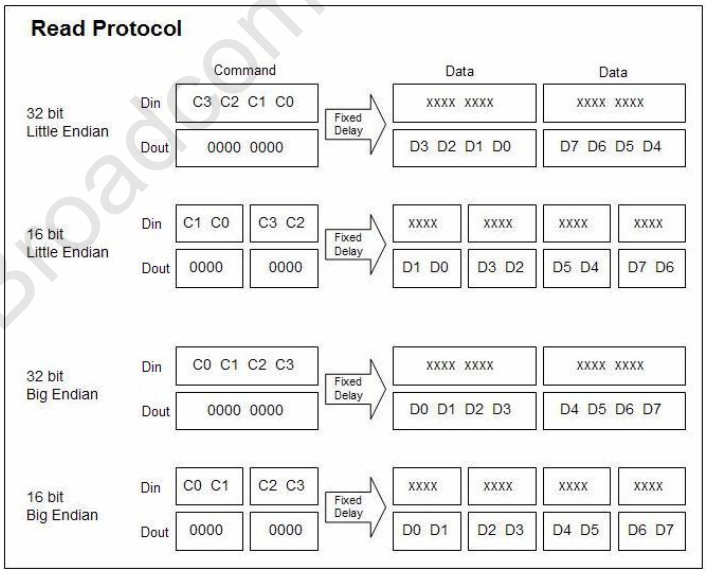


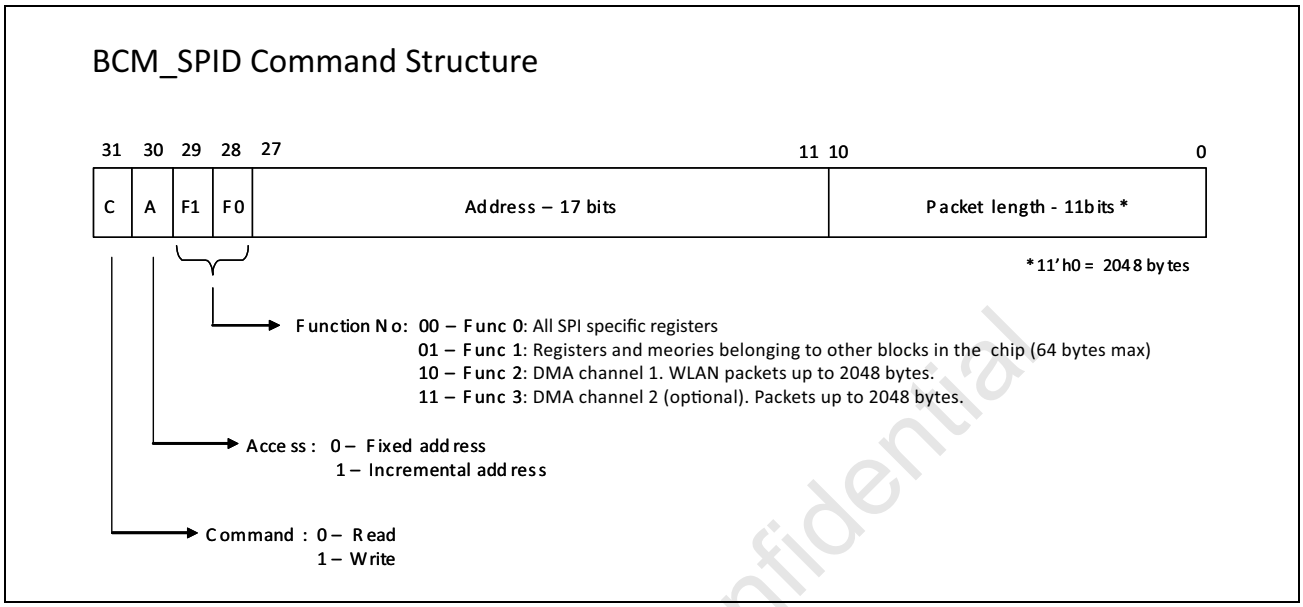
Figure 33: gSPI Read Protocol



Command Structure

The gSPI command structure is 32 bits. The bit positions and definitions are as shown in Figure 34.

Figure 34: gSPI Command Structure



Write

The host puts the first bit of the data onto the bus half a clock-cycle before the first active edge following the CS going low. The following bits are clocked out on the falling edge of the gSPI clock. The device samples the data on the active edge.

Write/Read

The host reads on the rising edge of the clock requiring data from the device to be made available before the first rising clock edge of the clock burst for the data. The last clock edge of the fixed delay word can be used to represent the first bit of the following data word. This allows data to be ready for the first clock edge without relying on asynchronous delays.

Read

The read command always follows a separate write to set up the WLAN device for a read. This command differs from the write/read command in the following respects: a) chip selects go high between the command/address and the data and b) the time interval between the command/address is not fixed.

Status

The gSPI interface supports status notification to the host after a read/write transaction. This status notification provides information about any packet errors, protocol errors, information about available packet in the RX queue, etc. The status information helps in reducing the number of interrupts to the host. The status-reporting feature can be switched off using a register bit, without any timing overhead. The gSPI bus timing for read/write transactions with and without status notification are as shown in Figure 35 and Figure 36 on page 83. See Table 18 on page 83 for information on status field details.

Figure 35: gSPI Signal Timing Without Status (32-bit big endian shown)

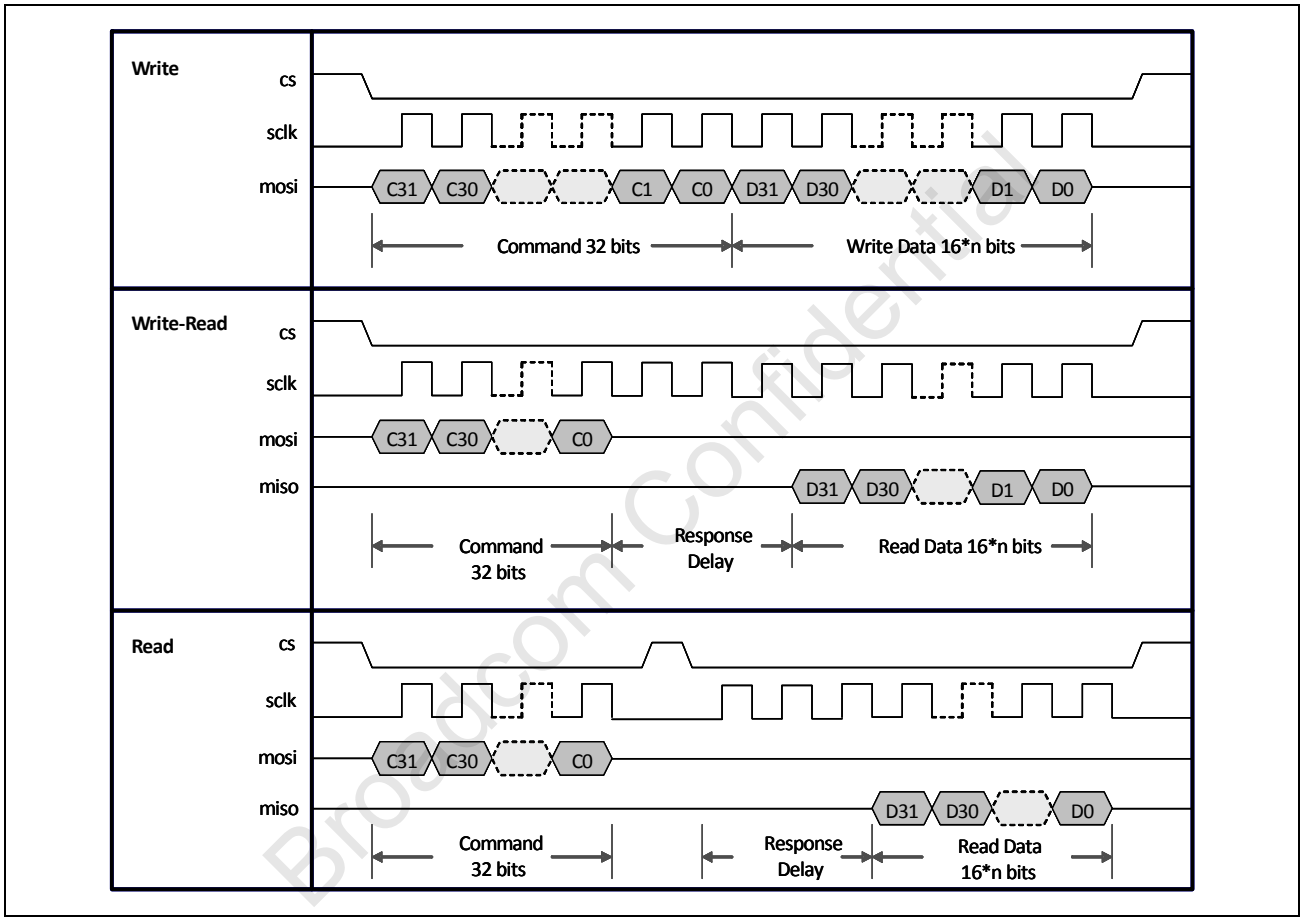


Figure 36: gSPI Signal Timing with Status (Response Delay = 0) (32-bit big endian shown)

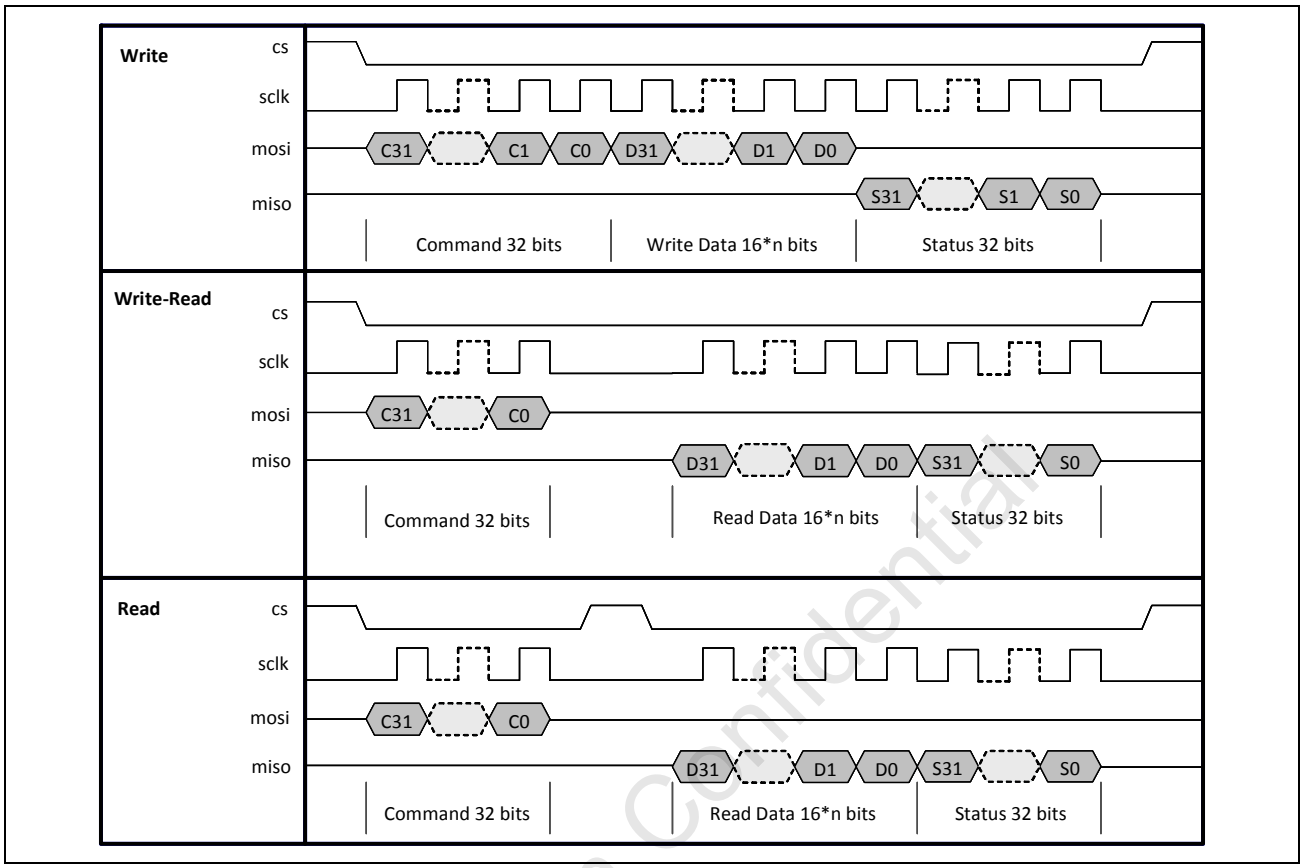


Table 18: gSPI Status Field Details

Bit	*Name*	*Description*
0	Data not available	The requested read data is not available
1	Underflow	FIFO underflow occurred due to current (F2, F3) read command
2	Overflow	FIFO overflow occurred due to current (F1, F2, F3) write command
3	F2 interrupt	F2 channel interrupt
4	F3 interrupt	F3 channel interrupt
5	F2 RX Ready	F2 FIFO is ready to receive data (FIFO empty)
6	F3 RX Ready	F3 FIFO is ready to receive data (FIFO empty)
7	Reserved	–
8	F2 Packet Available	Packet is available/ready in F2 TX FIFO
9:19	F2 Packet Length	Length of packet available in F2 FIFO
20	F3 Packet Available	Packet is available/ready in F3 TX FIFO
21:31	F3 Packet Length	Length of packet available in F3 FIFO

gSPI Host-Device Handshake

To initiate communication through the gSPI after power-up, the host needs to bring up the WLAN/Chip by writing to the wake-up WLAN register bit. Writing a 1 to this bit will start up the necessary crystals and PLLs so that the BCM43341 is ready for data transfer. The device can signal an interrupt to the host indicating that the device is awake and ready. This procedure also needs to be followed for waking up the device in sleep mode. The device can interrupt the host using the WLAN IRQ line whenever it has any information to pass to the host. On getting an interrupt, the host needs to read the interrupt and/or status register to determine the cause of interrupt and then take necessary actions.

Boot-Up Sequence

After power-up, the gSPI host needs to wait 150 ms for the device to be out of reset. For this, the host needs to poll with a read command to F0 addr 0x14. Address 0x14 contains a predefined bit pattern. As soon as the host gets a response back with the correct register content, it implies that the device has powered up and is out of reset. After that, the host needs to set the wakeup-WLAN bit (F0 reg 0x00 bit 7). The wakeup-WLAN issues a clock request to the PMU.

For the first time after power-up, the host must wait for the availability of low power clock inside the device. Once that is available, the host must write to a PMU register to set the crystal frequency, which turns on the PLL. After the PLL is locked, the chipActive interrupt is issued to the host. This interrupt indicates the device awake/ready status. See Table 19 for information on gSPI registers.

In Table 19, the following notation is used for register access:

- R: Readable from host and CPU
- W: Writable from host
- U: Writable from CPU

Table 19: gSPI Registers

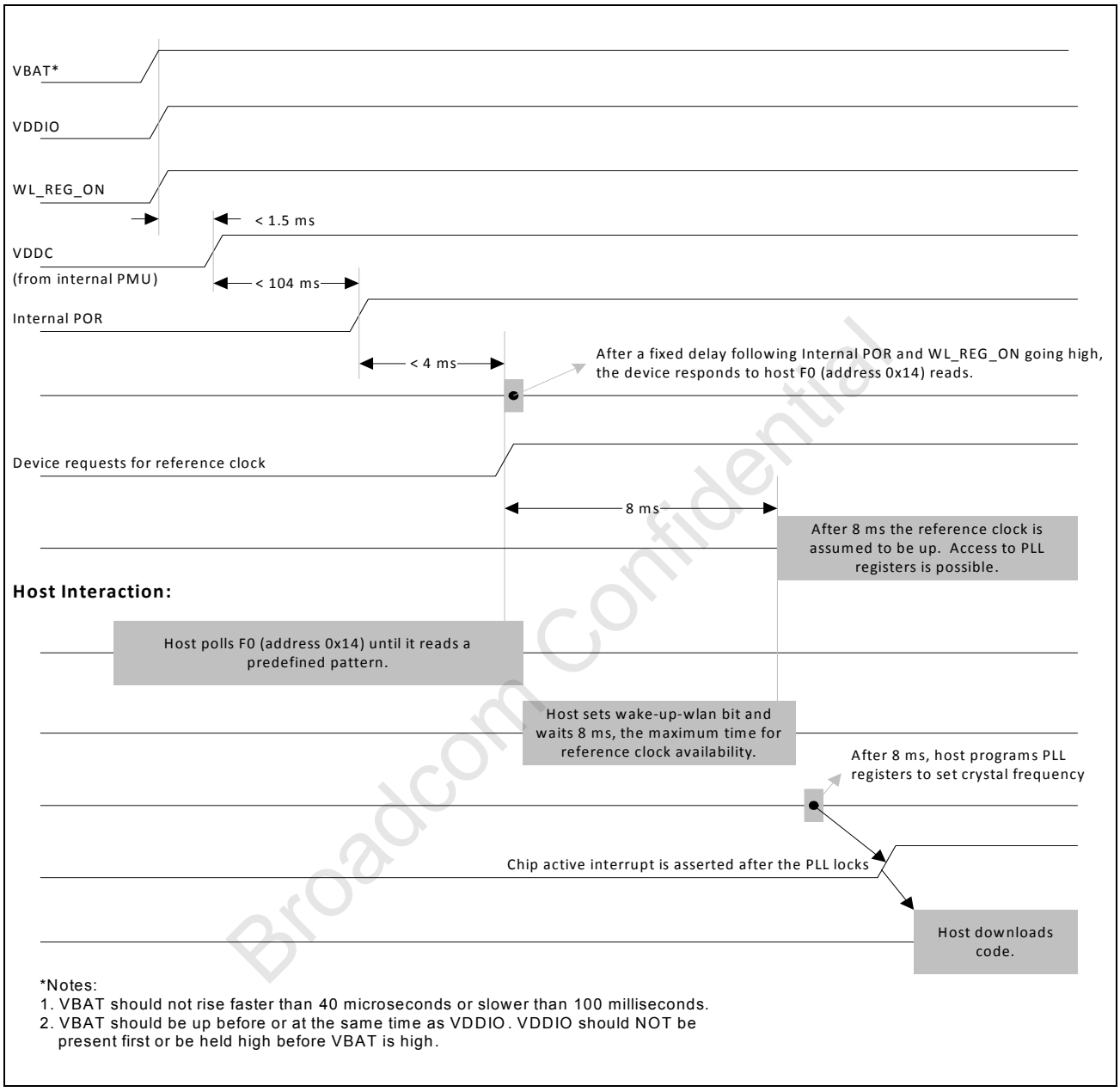
Address	Register	Bit	Access	Default	Description
x0000	Word length	0	R/W/U	0	0: 16 bit word length 1: 32 bit word length
	Endianness	1	R/W/U	0	0: Little Endian 1: Big Endian
	High-speed mode	4	R/W/U	1	0: Normal mode. RX and TX at different edges. 1: High speed mode. RX and TX on same edge (default).
	Interrupt polarity	5	R/W/U	1	0: Interrupt active polarity is low 1: Interrupt active polarity is high (default)
	Wake-up	7	R/W	0	A write of 1 will denote a wake-up command from the host to the device. This will be followed by an F2 Interrupt from the gSPI device to the host, indicating device awake status.
x0001	Response delay	7:0	R/W/U	8‘h04	Configurable read response delay in multiples of 8 bits

Table 19: gSPI Registers (Cont.)

Address	Register	Bit	Access	Default	Description
x0002	Status enable	0	R/W	1	0: no status sent to host after read/write 1: status sent to host after read/write
	Interrupt with status	1	R/W	0	0: do not interrupt if status is sent 1: interrupt host even if status is sent
	Response delay for all	2	R/W	0	0: response delay applicable to F1 read only 1: response delay applicable to all function read
x0003	Reserved	–	–	–	–
x0004	Interrupt register	0	R/W	0	Requested data not available; Cleared by writing a 1 to this location
		1	R	0	F2/F3 FIFO underflow due to last read
		2	R	0	F2/F3 FIFO overflow due to last write
		5	R	0	F2 packet available
		6	R	0	F3 packet available
		7	R	0	F1 overflow due to last write
x0005	Interrupt register	5	R	0	F1 Interrupt
		6	R	0	F2 Interrupt
		7	R	0	F3 Interrupt
x0006–x0007	Interrupt enable register	15:0	R/W/U	16'hE0E7	Particular Interrupt is enabled if a corresponding bit is set
x0008–x000B	Status register	31:0	R	32'h0000	Same as status bit definitions
x000C–x000D	F1 info register	0	R	1	F1 enabled
		1	R	0	F1 ready for data transfer
		13:2	R/U	12'h40	F1 max packet size
x000E–x000F	F2 info register	0	R/U	1	F2 enabled
		1	R	0	F2 ready for data transfer
		15:2	R/U	14'h800	F2 max packet size
x0010–x0011	F3 info register	0	R/U	1	F3 enabled
		1	R	0	F3 ready for data transfer
		15:2	R/U	14'h800	F3 max packet size
x0014–x0017	Test–Read only register	31:0	R	32'hFEEDBEAD	This register contains a predefined pattern, which the host can read and determine if the gSPI interface is working properly.
x0018–x001B	Test–R/W register	31:0	R/W/U	32'h00000000	This is a dummy register where the host can write some pattern and read it back to determine if the gSPI interface is working properly.

Figure 37 shows the WLAN boot-up sequence from power-up to firmware download.

Figure 37: WLAN Boot-Up Sequence



HSIC Interface

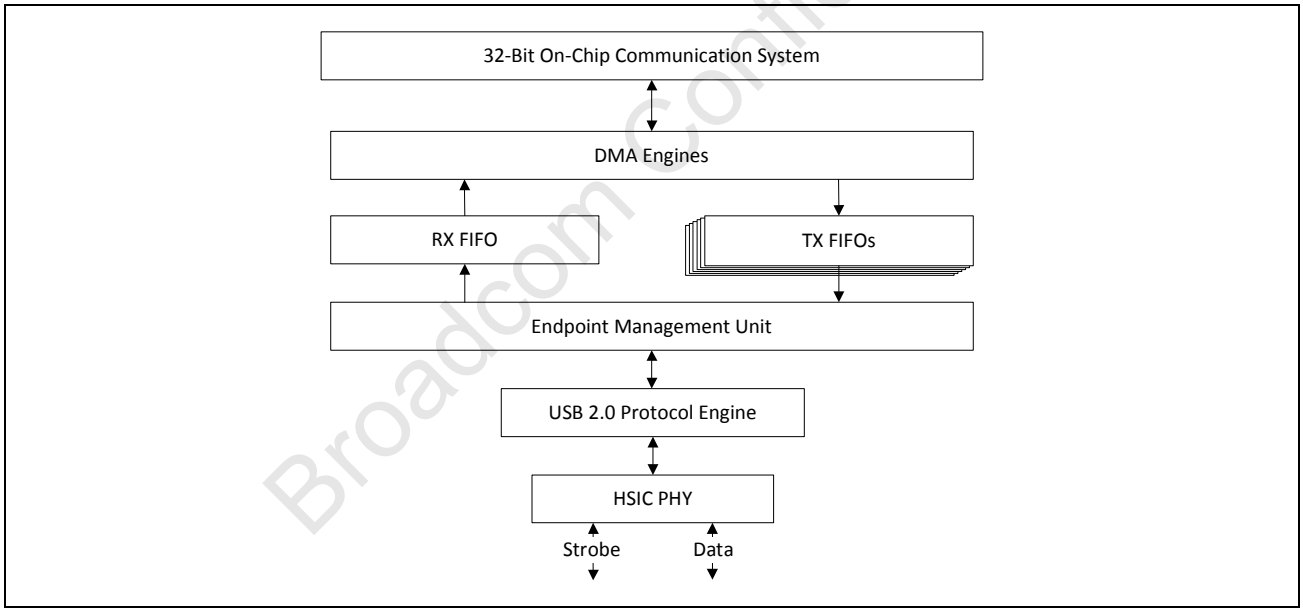
As an alternative to SDIO, an HSIC host interface can be enabled using the strapping option pins strap_host_ifc_[3:1]. HSIC is a simplified derivative of the USB2.0 interface designed to replace a standard USB PHY and cable for short distances (up to 10 cm) on board point-to-point connections. Using two signals, a bidirectional data strobe (STROBE) and a bidirectional DDR data signal (DATA), it provides high-speed serial 480 Mbps data transfers that are 100% host driver compatible with traditional USB 2.0 cable-connected topologies.

Figure 38 shows the blocks in the HSIC device core.

Key features of HSIC include:

- High-speed 480 Mbps data rate
- Source-synchronous serial interface using 1.2V LVCMOS signal levels
- No power consumed except when a data transfer is in progress
- Maximum trace length of 10 cm.
- No Plug-n-Play support, no hot attach/removal

Figure 38: HSIC Device Block Diagram



Section 11: Wireless LAN MAC and PHY

MAC Features

The BCM43341 WLAN media access controller (MAC) supports features specified in the IEEE 802.11 base standard, and amended by IEEE 802.11n. The salient features are listed below:

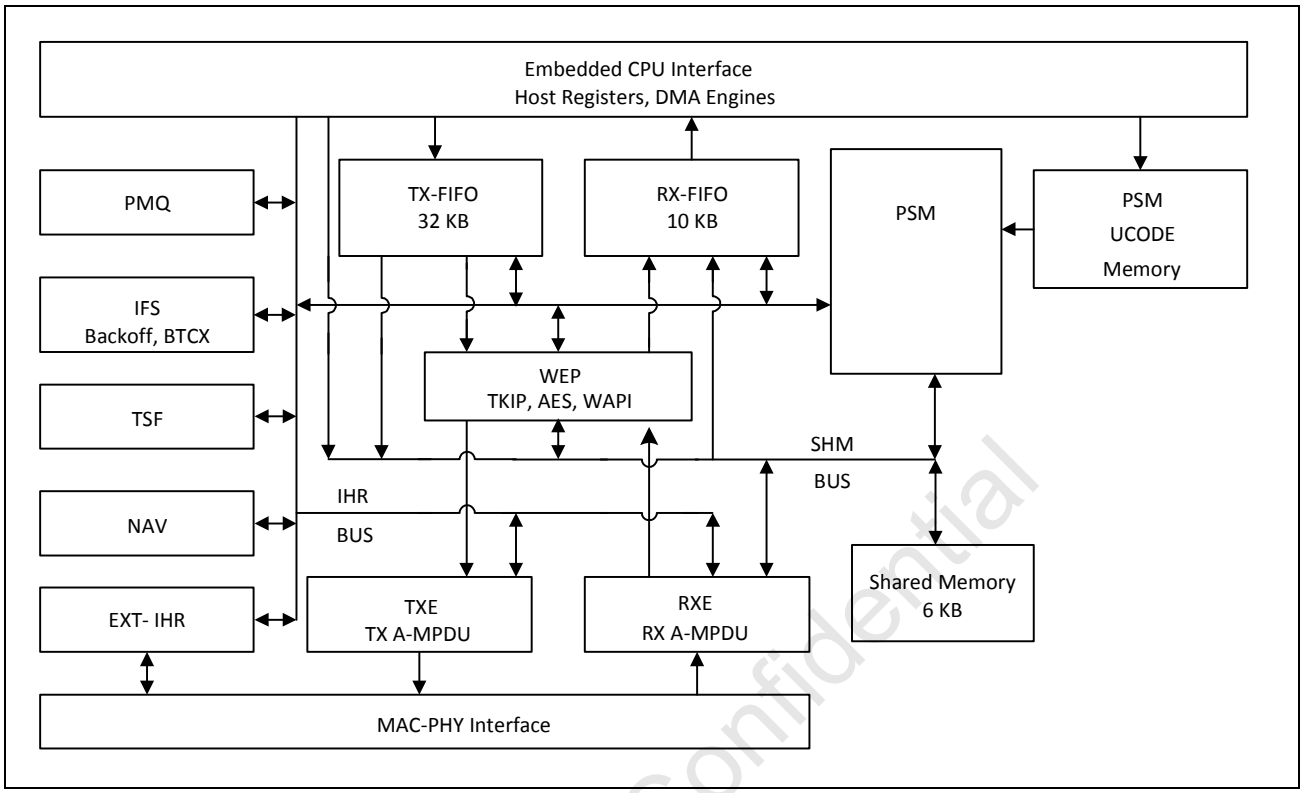
- Transmission and reception of aggregated MPDUs (A-MPDU)
- Support for power management schemes, including WMM power-save, power-save multi-poll (PSMP) and multiphase PSMP operation
- Support for immediate ACK and Block-ACK policies
- Interframe space timing support, including RIFS
- Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges
- Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware
- Hardware offload for AES-CCMP, legacy WEP ciphers, WAPI, and support for key management
- Support for coexistence with Bluetooth and other external radios
- Programmable independent basic service set (IBSS) or infrastructure basic service set functionality
- Statistics counters for MIB support

MAC Description

The BCM43341 WLAN MAC is designed to support high-throughput operation with low-power consumption. It does so without compromising the Bluetooth coexistence policies, thereby enabling optimal performance over both networks. In addition, several power saving modes have been implemented that allow the MAC to consume very little power while maintaining network-wide timing synchronization. The architecture diagram of the MAC is shown in Figure 39 on page 89.

The following sections provide an overview of the important modules in the MAC.

Figure 39: WLAN MAC Architecture



PSM

The programmable state machine (PSM) is a micro-coded engine, which provides most of the low-level control to the hardware, to implement the IEEE 802.11 specification. It is a microcontroller that is highly optimized for flow control operations, which are predominant in implementations of communication protocols. The instruction set and fundamental operations are simple and general, which allows algorithms to be optimized until very late in the design process. It also allows for changes to the algorithms to track evolving IEEE 802.11 specifications.

The PSM fetches instructions from the microcode memory. It uses the shared memory to obtain operands for instructions, as a data store, and to exchange data between both the host and the MAC data pipeline (via the SHM bus). The PSM also uses a scratchpad memory (similar to a register bank) to store frequently accessed and temporary variables.

The PSM exercises fine-grained control over the hardware engines, by programming internal hardware registers (IHR). These IHRs are co-located with the hardware functions they control, and are accessed by the PSM via the IHR bus.

The PSM fetches instructions from the microcode memory using an address determined by the program counter, instruction literal, or a program stack. For ALU operations the operands are obtained from shared memory, scratchpad, IHRs, or instruction literals, and the results are written into the shared memory, scratchpad, or IHRs.

There are two basic branch instructions: conditional branches and ALU based branches. To better support the many decision points in the IEEE 802.11 algorithms, branches can depend on either a readily available signals from the hardware modules (branch condition signals are available to the PSM without polling the IHRs), or on the results of ALU operations.

WEP

The wired equivalent privacy (WEP) engine encapsulates all the hardware accelerators to perform the encryption and decryption, and MIC computation and verification. The accelerators implement the following cipher algorithms: legacy WEP, WPA TKIP, WPA2 AES-CCMP.

The PSM determines, based on the frame type and association information, the appropriate cipher algorithm to be used. It supplies the keys to the hardware engines from an on-chip key table. The WEP interfaces with the TXE to encrypt and compute the MIC on transmit frames, and the RXE to decrypt and verify the MIC on receive frames.

TXE

The transmit engine (TXE) constitutes the transmit data path of the MAC. It coordinates the DMA engines to store the transmit frames in the TXFIFO. It interfaces with WEP module to encrypt frames, and transfers the frames across the MAC-PHY interface at the appropriate time determined by the channel access mechanisms.

The data received from the DMA engines are stored in transmit FIFOs. The MAC supports multiple logical queues to support traffic streams that have different QoS priority requirements. The PSM uses the channel access information from the IFS module to schedule a queue from which the next frame is transmitted. Once the frame is scheduled, the TXE hardware transmits the frame based on a precise timing trigger received from the IFS module.

The TXE module also contains the hardware that allows the rapid assembly of MPDUs into an A-MPDU for transmission. The hardware module aggregates the encrypted MPDUs by adding appropriate headers and pad delimiters as needed.

RXE

The receive engine (RXE) constitutes the receive data path of the MAC. It interfaces with the DMA engine to drain the received frames from the RXFIFO. It transfers bytes across the MAC-PHY interface and interfaces with the WEP module to decrypt frames. The decrypted data is stored in the RXFIFO.

The RXE module contains programmable filters that are programmed by the PSM to accept or filter frames based on several criteria such as receiver address, BSSID, and certain frame types.

The RXE module also contains the hardware required to detect A-MPDUs, parse the headers of the containers, and disaggregate them into component MPDUS.

IFS

The IFS module contains the timers required to determine interframe space timing including RIFS timing. It also contains multiple backoff engines required to support prioritized access to the medium as specified by WMM.

The interframe spacing timers are triggered by the cessation of channel activity on the medium, as indicated by the PHY. These timers provide precise timing to the TXE to begin frame transmission. The TXE uses this information to send response frames or perform transmit frame-bursting (RIFS or SIFS separated, as within a TXOP).

The backoff engines (for each access category) monitor channel activity, in each slot duration, to determine whether to continue or pause the backoff counters. When the backoff counters reach 0, the TXE gets notified, so that it may commence frame transmission. In the event of multiple backoff counters decrementing to 0 at the same time, the hardware resolves the conflict based on policies provided by the PSM.

The IFS module also incorporates hardware that allows the MAC to enter a low-power state when operating under the IEEE power save mode. In this mode, the MAC is in a suspended state with its clock turned off. A sleep timer, whose count value is initialized by the PSM, runs on a slow clock and determines the duration over which the MAC remains in this suspended state. Once the timer expires the MAC is restored to its functional state. The PSM updates the TSF timer based on the sleep duration ensuring that the TSF is synchronized to the network.

The IFS module also contains the PTA hardware that assists the PSM in Bluetooth coexistence functions.

TSF

The timing synchronization function (TSF) module maintains the TSF timer of the MAC. It also maintains the target beacon transmission time (TBTT). The TSF timer hardware, under the control of the PSM, is capable of adopting timestamps received from beacon and probe response frames in order to maintain synchronization with the network.

The TSF module also generates trigger signals for events that are specified as offsets from the TSF timer, such as uplink and downlink transmission times used in PSMP.

NAV

The network allocation vector (NAV) timer module is responsible for maintaining the NAV information conveyed through the duration field of MAC frames. This ensures that the MAC complies with the protection mechanisms specified in the standard.

The hardware, under the control of the PSM, maintains the NAV timer and updates the timer appropriately based on received frames. This timing information is provided to the IFS module, which uses it as a virtual carrier-sense indication.

MAC-PHY Interface

The MAC-PHY interface consists of a data path interface to exchange RX/TX data from/to the PHY. In addition, there is an programming interface, which can be controlled either by the host or the PSM to configure and control the PHY.

WLAN PHY Description

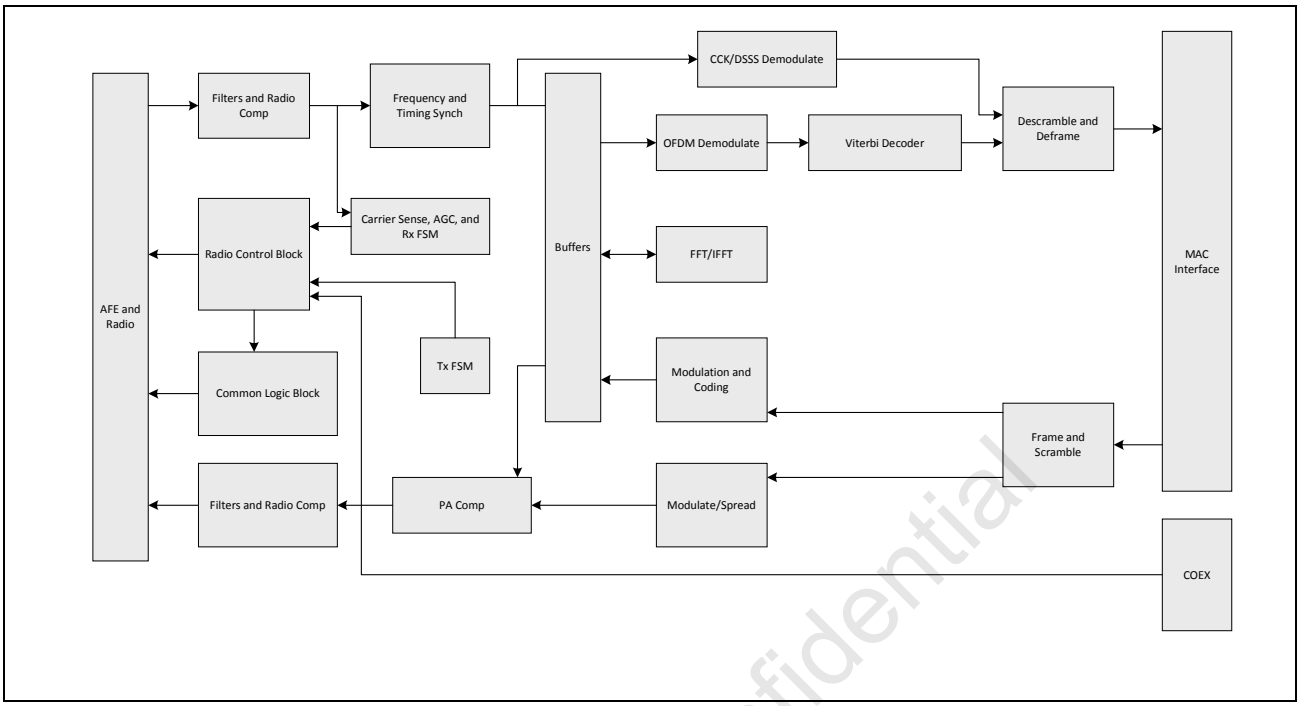
The BCM43341 WLAN Digital PHY is designed to comply with IEEE 802.11a/b/g/n single-stream to provide wireless LAN connectivity supporting data rates from 1 Mbps to 150 Mbps for low-power, high-performance handheld applications.

The PHY has been designed to work with interference, radio nonlinearity, and impairments. It incorporates efficient implementations of the filters, FFT and Viterbi decoder algorithms. Efficient algorithms have been designed to achieve maximum throughput and reliability, including algorithms for carrier sense/rejection, frequency/phase/timing acquisition and tracking, channel estimation and tracking. The PHY receiver also contains a robust IEEE 802.11b demodulator. The PHY carrier sense has been tuned to provide high throughput for IEEE 802.11g/11b hybrid networks with Bluetooth coexistence. It has also been designed for shared single antenna systems between WL and BT to support simultaneous RX-RX.

PHY Features

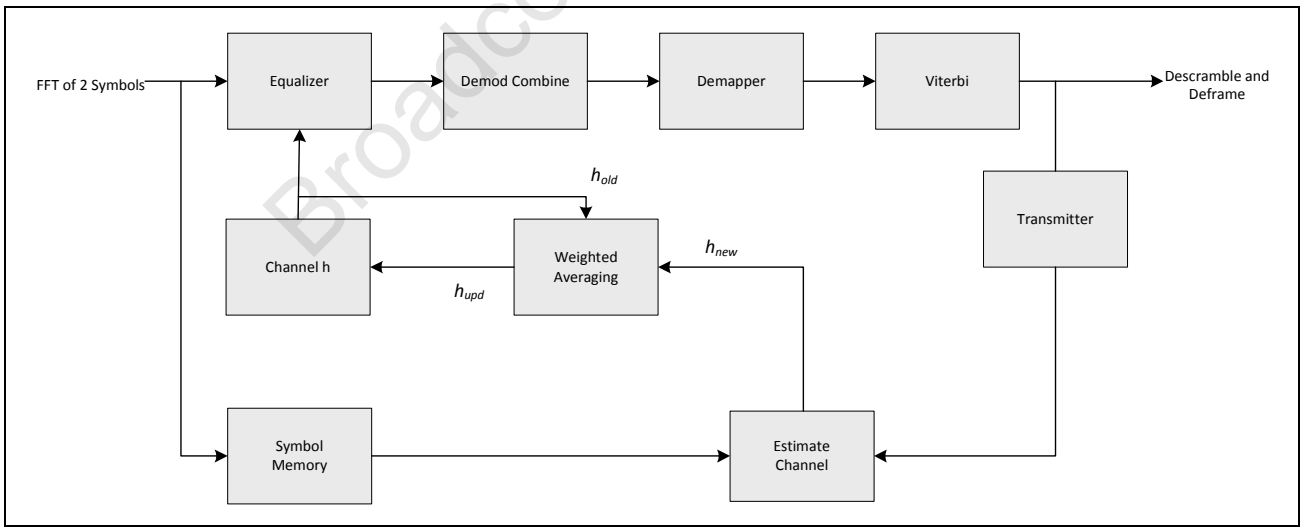
- Supports IEEE 802.11a, 11b, 11g, and 11n single-stream PHY standards.
- IEEE 802.11n single-stream operation in 20 MHz and 40 MHz channels
- Supports Optional Short GI and Green Field modes in TX and RX.
- Supports optional space-time block code (STBC) receive of two space-time streams.
- TX LDPC for improved range and power efficiency
- Supports IEEE 802.11h/k for worldwide operation.
- Advanced algorithms for low power, enhanced sensitivity, range, and reliability
- Algorithms to improve performance in presence of Bluetooth
- Simultaneous RX-RX (WL-BT) architecture
- Automatic gain control scheme for blocking and non blocking application scenario for cellular applications
- Closed loop transmit power control
- Digital RF chip calibration algorithms to handle CMOS RF chip non-idealities
- On-the-fly channel frequency and transmit power selection
- Supports per packet RX antenna diversity.
- Designed to meet FCC and other worldwide regulatory requirements.

Figure 40: WLAN PHY Block Diagram



One of the key features of the PHY is its space-time block coding (STBC) capability. The STBC scheme can obtain diversity gains in a fading channel environment. On a connection with an access point that uses multiple transmit antennas and supports STBC, the BCM43341 can process two space-time streams to improve receiver performance. Figure 41 is a block diagram showing the STBC implementation in the receive path.

Figure 41: STBC Implementation in the Receive Path



In STBC mode, symbols are processed in pairs. Equalized output symbols are linearly combined and decoded. The channel estimate is refined on every pair of symbols using the received symbols and reconstructed symbols.

Section 12:WLAN Radio Subsystem

The BCM43341 includes an integrated dual-band WLAN RF transceiver that has been optimized for use in 2.4 GHz and 5 GHz Wireless LAN systems. It has been designed to provide low-power, low-cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM or 5 GHz U-NII bands. The transmit and receive sections include all on-chip filtering, mixing, and gain control functions.

Receiver Path

The BCM43341 has a wide dynamic range, direct conversion receiver. It employs high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band or the entire 5 GHz U-NII band. Control signals are available that can support the use of optional external low noise amplifiers (LNA), which can increase the receive sensitivity by several dB.

Transmit Path

Baseband data is modulated and upconverted to the 2.4 GHz ISM or 5-GHz U-NII bands, respectively. The BCM43341 includes an on-chip regulator which regulates VBAT down to 3.3V for the BCM43341 on-chip linear Power Amplifiers. Closed-loop output power control is provided by means of internal a-band and g-band power detectors.

Calibration

The BCM43341 features dynamic and automatic on-chip calibration to continually compensate for temperature and process variations across components. This enables the BCM43341 to be used in high-volume applications, because calibration routines are not required during manufacturing testing. These calibration routines are performed periodically in the course of normal radio operation. Examples of some of the automatic calibration algorithms are baseband filter calibration for optimum transmit and receive performance and LOFT calibration for carrier leakage reduction. In addition, I/Q Calibration, R Calibration, and VCO Calibration are performed on-chip. No per-board calibration is required in manufacturing test, which helps to minimize test time and cost during large volume production.

Section 13: NFC Subsystem

General Description

The NFC core in the BCM43341 is a fully NFC Forum-compliant, highly integrated, low-power NFC controller. It leverages the flexibility of multiple secure element interfaces to support two Single Wire Protocol (SWP) interfaces. This means that, in addition to the platform UICC (SIM card), the BCM43341 can also interface with an SWP-based embedded secure element. The BCM43341 incorporates the PPSE and AID routing functionality for support of multiple applications across multiple secure elements and execution environments

Operational Modes

The operational modes as defined by the NFC Forum and are supported by the BCM43341. The following operational modes, as defined by the NFC Forum and NFC standards are supported by the BCM43341.

Peer Mode

The BCM43341, along with its software stack, fully supports Peer mode. In Peer mode, the BCM43341 is capable of acting as both an initiator and a target.

This mode of operation allows for well-formed transmission of application data from one NFC device to another NFC device.

Peer mode utilizes the Link Layer Control Protocol (LLCP) defined by the NFC Forum. The physical layer and portions of the MAC layer standards are defined in NFCIP-1 standard ISO/IEC 18092 (ECMA 340). A Peer mode initiator is responsible for beginning communication with a Peer mode target. The initiator is also responsible for generating the RF field. The BCM43341 supports both Active and Passive Communications modes.

Reader/Writer Mode

In the Reader/Writer mode, the BCM43341 acts as a reader or writer of low-cost NFC Forum-defined contactless tags. There are four tag types that are mandated by the NFC Forum. Broadcom is the exclusive supplier of Tag Type 1 – which is ideal for simple pairing, business card, and all nonpayment applications. For further information on the BCM20203, the Broadcom Topaz Tag (NFC Forum Tag 1), contact your Broadcom representative.

The BCM43341 is capable of detecting, reading, and writing to any of the NFC Forum-supported tag types.

Card Emulation Mode

In Card Emulation mode, the NFC system issues and responds to commands in the same way as a contactless smart card. The use cases for Card and Tag Emulation mode include payment and ticketing.

The BCM43341 supports full Tag and Card Emulation mode when paired with a suitable Secure Element or host device.

ISO Standards

The BCM43341 supports several RF and ISO standards at various bit rates, up to and including 424 kbps. A list of the ISO and JIS standards that are supported by the BCM43341 are listed in Table 20.

Table 20: ISO/IEC 14443 A and B, FeliCa, and NFC Forum Modes

Standard	*Reader/Initiator*			*Tag/Target*		
Data Rate (kbps)	106	212	424	106	212	424
ISO/IEC 14443 A	✓	✓	✓	✓	✓	✓
ISO/IEC 14443 B	✓	✓	✓	✓	✓	✓
ISO/IEC 14443 B – Prime	–	–	–	✓	✓	✓
ISO/IEC 18092/ECMA 340 Active	✓	✓	✓	✓	✓	✓
ISO/IEC 18092/ECMA 340 Passive	✓	✓	✓	✓	✓	✓
JIS (X) 6319-4 FeliCa	–	✓	✓	–	✓	✓

The BCM43341 also supports reader and tag modes for ISO/IEC 15693[1]. A list of supported bit rates can be found in Table 21.

Table 21: ISO/IEC 15693 Supported Bit Rates

Communications Mode	*VICC to VCD*				*VCD to VICC*	
Subcarrier	Single		Dual		N/A	
Data Rate (kbps)	6.62	26.48	6.67	26.69	1.65	26.48
Reader Support	✓	✓	–[a]	–[a]	✓	✓
Tag Support	✓	✓	✓	✓	✓	✓

a. Reader version supports only Single Subcarrier mode.

1. The host can define Single or Multiple State Machine capabilities, which can alter ISO/IEC 15693 availability. See “Multiple Technology Support and Automatic Standard Detection” on page 100 for more information.

Radio Modes

The BCM43341 supports several modes of operation to enable the NFC use cases.

Initiator Mode

As the initiator in either R/W or Peer mode, the BCM43341 will generate the field used for communication. The size of the field is subject to the antenna used and the current drive of the BCM43341. The peak antenna drive current is determined by the effective impedance of the antenna network and the voltage drive setting. The BCM43341 supports some variable drive levels to assist in power management.

The antenna drive strength is shown in Table 22.

Table 22: Antenna Drive

Minimum	*Maximum*	*Steps*
70 mA pk	200 mA pk	3 dB

The supply mode uses an internal analog rail of 2.5V (nominal), which can be monitored on the VDDA_CAP pin.

Mode Switch

To discover the presence of a tag or a Peer mode target while operating in Initiator mode, the BCM43341 supports mode switch polling according to the NFC Forum “Activity” specification. Once set to active polling, the BCM43341 generates a field for a certain sequence of protocols and looks for a response.

For maximum flexibility and optimal power management, the duration that the BCM43341 generates a field at each interval is also firmware configurable. The Mode switch, as defined by the NFC Forum “Activity” specification, consists of a series of discovery periods and is configured according to the NFC Forum NFC Controller Interface (NCI) specification. Currently, NCI specifications highlight two parameters to define the discovery period used by the firmware.

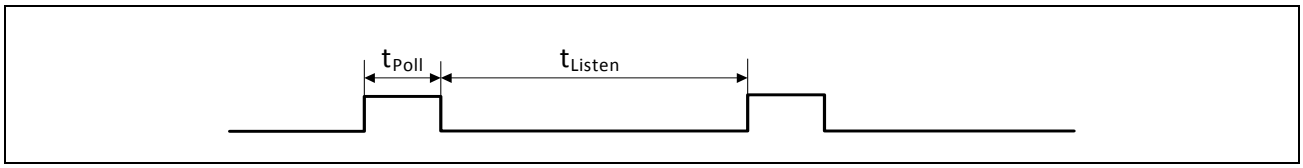
- Listen Duration (acting as a target): May range from 0 ms to 65535 ms in 1 ms increments.
- Total Duration (total of acting as a target and acting as an initiator): May range from 0 ms to 65535 ms in 1 ms increments.

The time available for acting as an initiator is Total Duration - Listen Duration. If the initiator polls do not need all this allocated time, then the BCM43341 may enter a power saving mode.

By configuring these three parameters (technology, interval, and duration) the user can optimize the BCM43341 for their particular use case, and make the appropriate system-level response time- and power-consumption trade-offs.

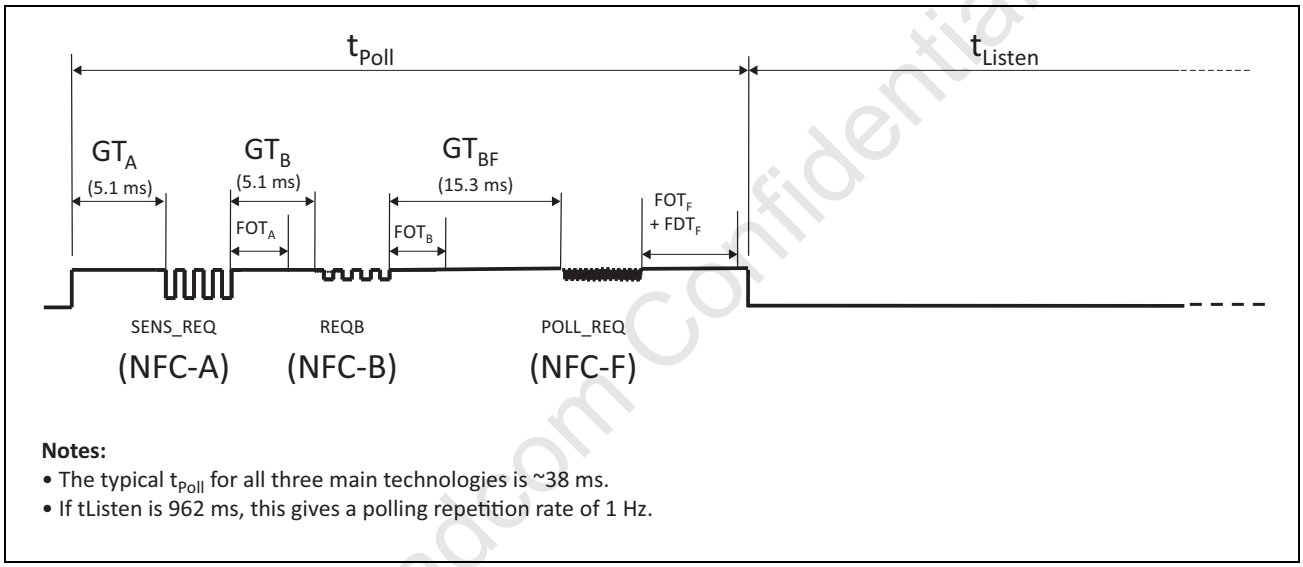
The BCM43341 implements the NFC Forum-defined mode switch, which the host can use to configure and set the FW in the BCM43341 to periodically wake up and poll for targets of the various technology types.

Figure 42: NFC Forum Mode Switch Polling and Listening



A typical poll cycle can be used to attempt to discover targets of NFC-A, NFC-B, and NFC-F. This involves generating the carrier field for approximately 38 ms and sending the REQA, REQB, and POLL_F commands to activate and elicit a response from any tags or peer mode targets that are present.

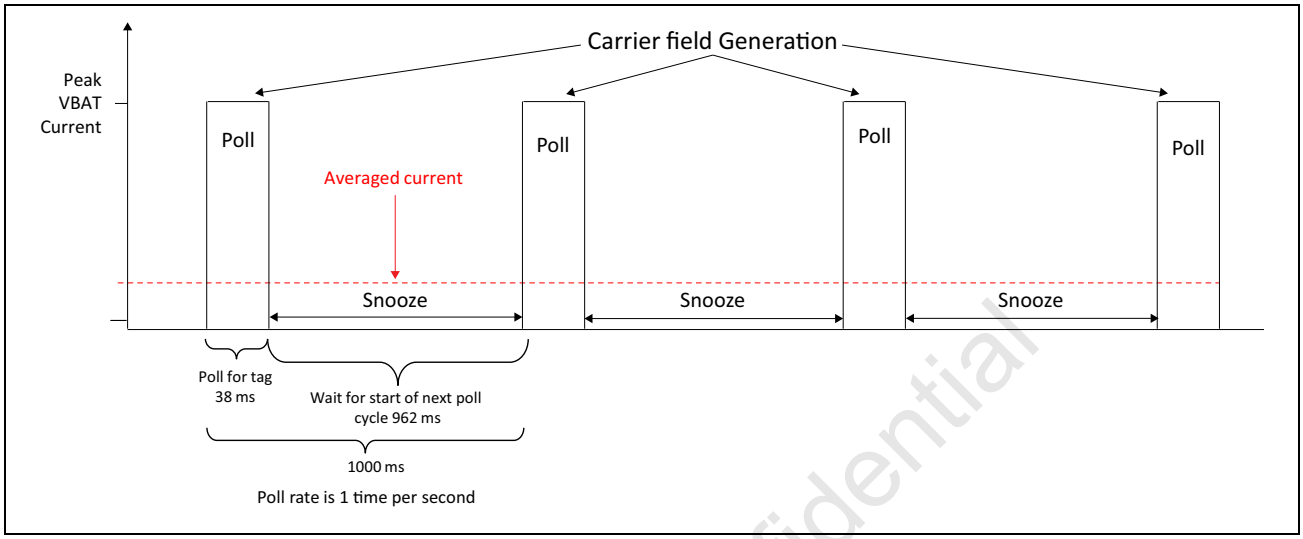
Figure 43: Forum Mode Switch Polling for NFC-A, NFC-B, and NFC-F



Notes:
- The typical t_{Poll} for all three main technologies is ~38 ms.
- If tListen is 962 ms, this gives a polling repetition rate of 1 Hz.

During the time of each poll event, the BCM43341 draws a peak current from the VBAT supply (see Figure 44). The level of this peak current depends on the characteristics of the antenna design and the environment of the antenna, as well as internal drive level and gain settings within the BCM43341 configuration.

Figure 44: Representation of Averaged Duty-Cycle Current



Low Power Target Detection

The BCM43341 has the ability to use a Low Power Target Detection (LPTD) mode, where a target can be an NFC tag, card, or an NFC device in Listener mode, to save current consumption (see Figure 45 on page 100). In this mode, the device periodically wakes and tries to sense the presence of a tag. It does so without initiating a full A, B, and F poll. If a tag load is detected, then normal A, B, and F polling is initiated. If a load or change in environment is not detected, then the device returns to its snooze state.

To fully optimize battery power usage, Broadcom has developed an efficient time/current algorithm for detecting the presence of a target by the BCM43341.

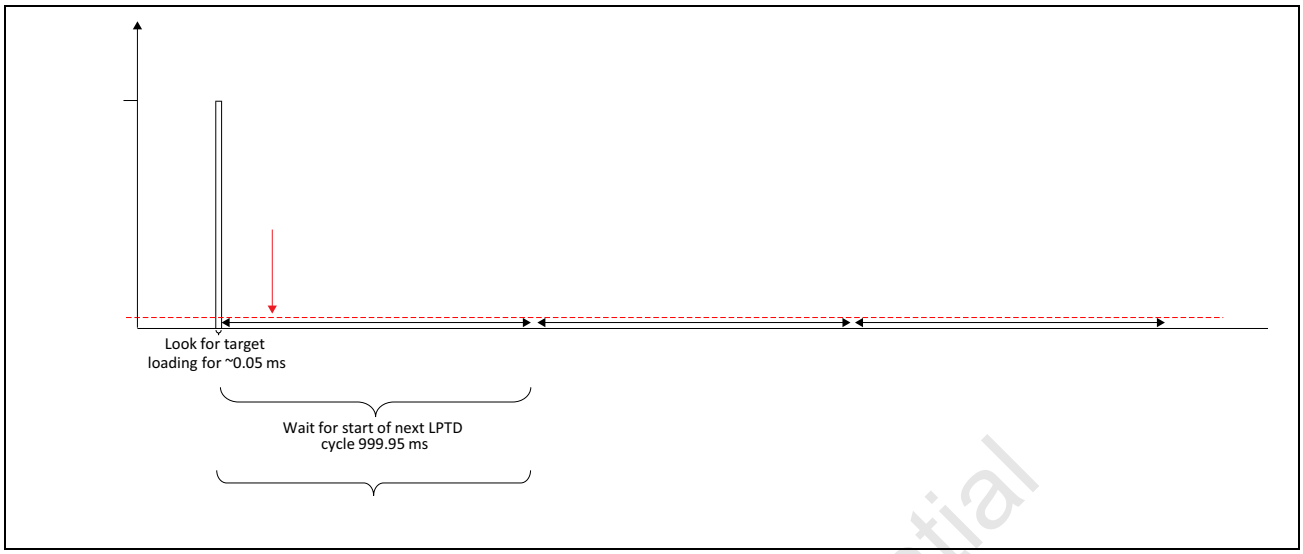
Instead of the conventional mode switch poll sequence, the BCM43341 can “sniff” for very brief durations to detect the presence of a tuned circuit or disturbance of the environment in the proximity of the NFC antenna. This results in a very much reduced duration of field generation and peak current drain.

The “sniff” detects the presence of a target, but does not detect which technology type caused the trigger. The LPTD algorithm is always a pre-cursor to a full poll event, which is used to qualify the trigger generated by the LPTD algorithm and discover the technology type just like a standard mode switch full poll event would.

A “false alarm rate” can occur when the LPTD can be triggered by metallic objects, but any trigger will be qualified by a full poll event and therefore can be discounted if it is not a real target.

The control algorithm includes a background calibration, so it auto-adjusts to a background baseline to account for drift and changing conditions.

Figure 45: Principle of Low Power Target Detection (LPTD) Mode



Multiple Technology Support and Automatic Standard Detection

The BCM43341 has the ability to act as a Proximity Integrated Circuit Card (PICC) or Vicinity Integrated Circuit Card (VICC) for any of the technologies it supports (ISO/IEC 14443A, ISO/IEC 14443B, ISO/IEC 14443B-Prime, JIS (X) 6319-4, ISO/IEC 15693). The technology used is determined by both software configuration and the nature of the coupling device into the carrier field of which the BCM43341 is introduced.

The BCM43341 automatically detects and identifies, from the field generated by the initiator device, the technology that is requested. It then responds accordingly, assuming it has been configured by software to support a particular application on that given technology.

The BCM43341 has the capability of emulating targets of multiple technologies (A, B, F, ISO/IEC 15693, Calypso) at the same time. An NFC Forum initiator, following the activity specification, identifies all applications supported by targets in the field by polling using A, B, and F technologies. The initiator will then select one of the targets for subsequent communication.

The BCM43341 can emulate targets in two modes, and the mode can be changed over the NCI interface. In both modes, the BCM43341 supports emulation of multiple NFC-F targets.

In the default mode, the BCM43341 listen device maintains a single state machine and responds to the technology (A, B, F, ISO/IEC 15693, Calypso) of the first poll command that matches one of its emulated targets. After responding to this poll command, polls from other technologies are ignored until a carrier is dropped.

In the second mode, the BCM43341 listen device maintains multiple state machines and behaves virtually like multiple devices. This allows the host to have multiple applications listening at the same time, and announcing all of its applications to an NFC Forum initiator and not just the application of the first matching technology. For example, a BCM43341-enabled device could announce both credit card emulation and LLCP. This is achieved by the BCM43341 responding to all polling commands (A, B, F, ISO/IEC 15693, Calypso) and only restrict itself to a specific technology once it has responded to the first non-polling command (A, B, F) or any ISO/IEC 15693 or Calypso command.

NFC Host Interfaces

The BCM43341 supports UART, I^2C-compatible BSC, and SPI for the host interface physical transport layer. The host interface type is selected upon power-up boot, depending upon the state of the NFC_SPI_INT pin.

- NFC_SPI_INT pulled low—The UART interface will be selected
- NFC_SPI_INT pulled high—The I^2C-compatible BSC slave interface will be selected.
- NFC_SPI_INT floating—The SPI interface will be selected.

After boot, the NFC_SPI_INT signal will function as the SPI interrupt output. During power-up boot, the external host must leave this pin floating, as in the case of a tristate or input pin. The external host must also ignore interrupts from this signal for a period of 10 milliseconds after boot-up.

The NFC host interface pins are multiplexed onto shared signals as defined in Table 23.

Table 23: NFC Host Interface Multiplexing

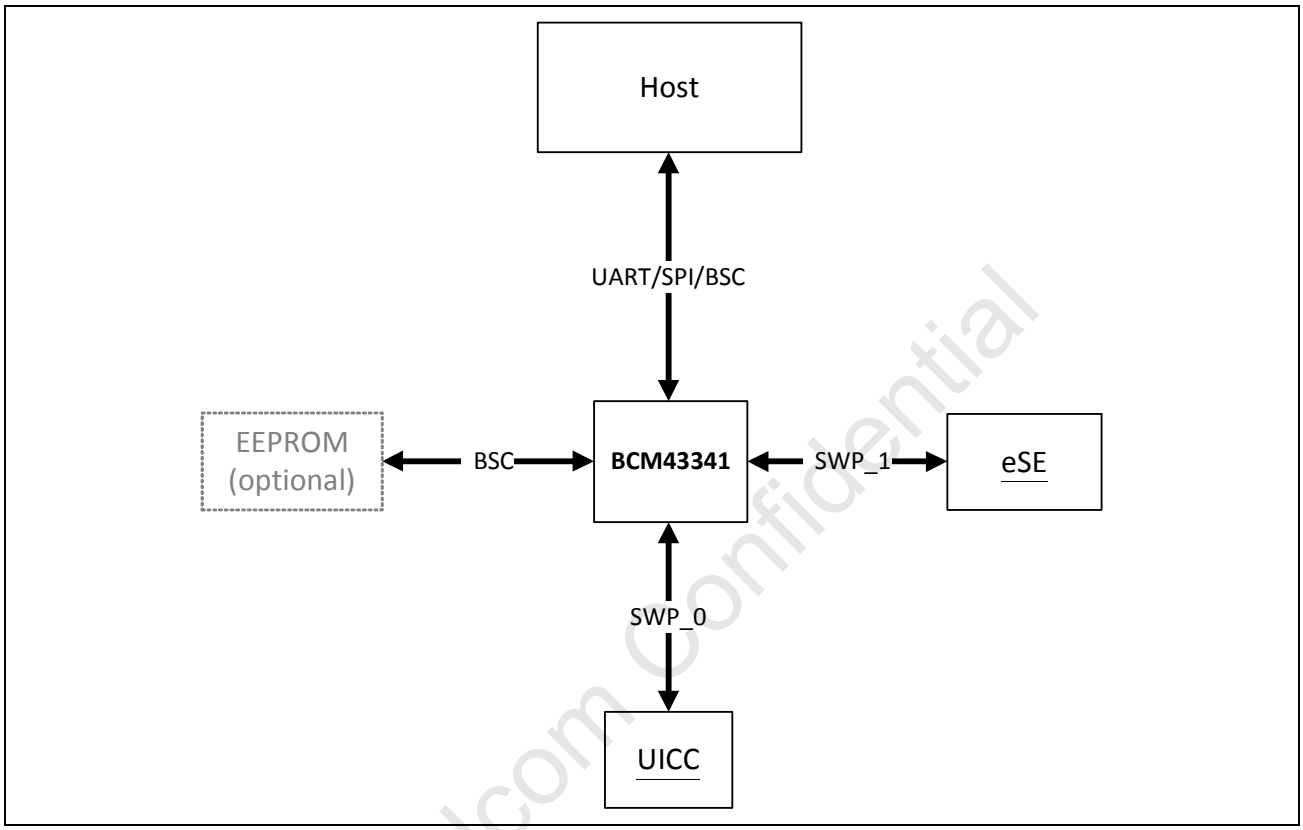
UART	*BSC*	*SPI*
NFC_CTS[a]	I2C_REQ	SPI_CS
NFC_RTS[a,b]	I2C_SCL	SPI_MISO
NFC_URX[a]	–	SPI_CLK
NFC_UTX[a]	I2C_SDA	SPI_MOSI
Pull low	Pull high	**NFC_SPI_INT**[a]

a. Bold text indicates pin name.
b. Needs external pull-up

NFC Secure Element Configuration Options

Figure 46 shows the NFC secure element configuration.

Figure 46: NFC Secure Element Configuration



Source of Secure Personality and Persistence Data

The BCM43341 supports NVM on either external EEPROM or eSE. Contact your Broadcom support representative for details. Table 24 shows how to configure pull-ups and pull-downs on NFC_SDA and NFC_SCL to select between EEPROM or eSE as the source of NVM data. The state of NFC_SDA and NFC_SCL is sampled during the BCM43341 boot process.

Table 24: Secure Personality and Persistence Data Settings

NFC_SDA	*NFC_SCL*	*Mode*
Pull-down	Don't care	eSE attached and used for restore
Pull-up	Pull-up	EEPROM attached and used for restore
Pull-up	Pull-down	Proprietary mode

NFC Secure Element Interfaces

Single Wire Protocol

The BCM43341 supports two entirely independent SWP data and power supply interfaces, which are labeled as SWP_0 and SWP_1. The SWP_0 interface supports both Class B and Class C Universal Integrated Circuit Cards (UICCs). The SWP_1 interface supports 1.8V secure elements or a Class C UICC.

- Master mode
- Full Power and CE3/CE1 Low Power modes—the following bit rates are supported:
  - 106 Kbps
  - 212 Kbps
  - 424 Kbps
  - 847 Kbps
  - 969 Kbps

  Extended bit-rate support (1.507 Mbps) is available in Full Power mode. (The maximum speed achievable will be dependant on the level of parasitic capacitance due to PCB tracking on any particular design implementation.)
- Host programmable high impedance or pull down on pin (default is pull-down)
- Dedicated RX and TX 32-byte frame buffers

Power for the UICC connected to the SWP_0 interface can be supplied as follows:

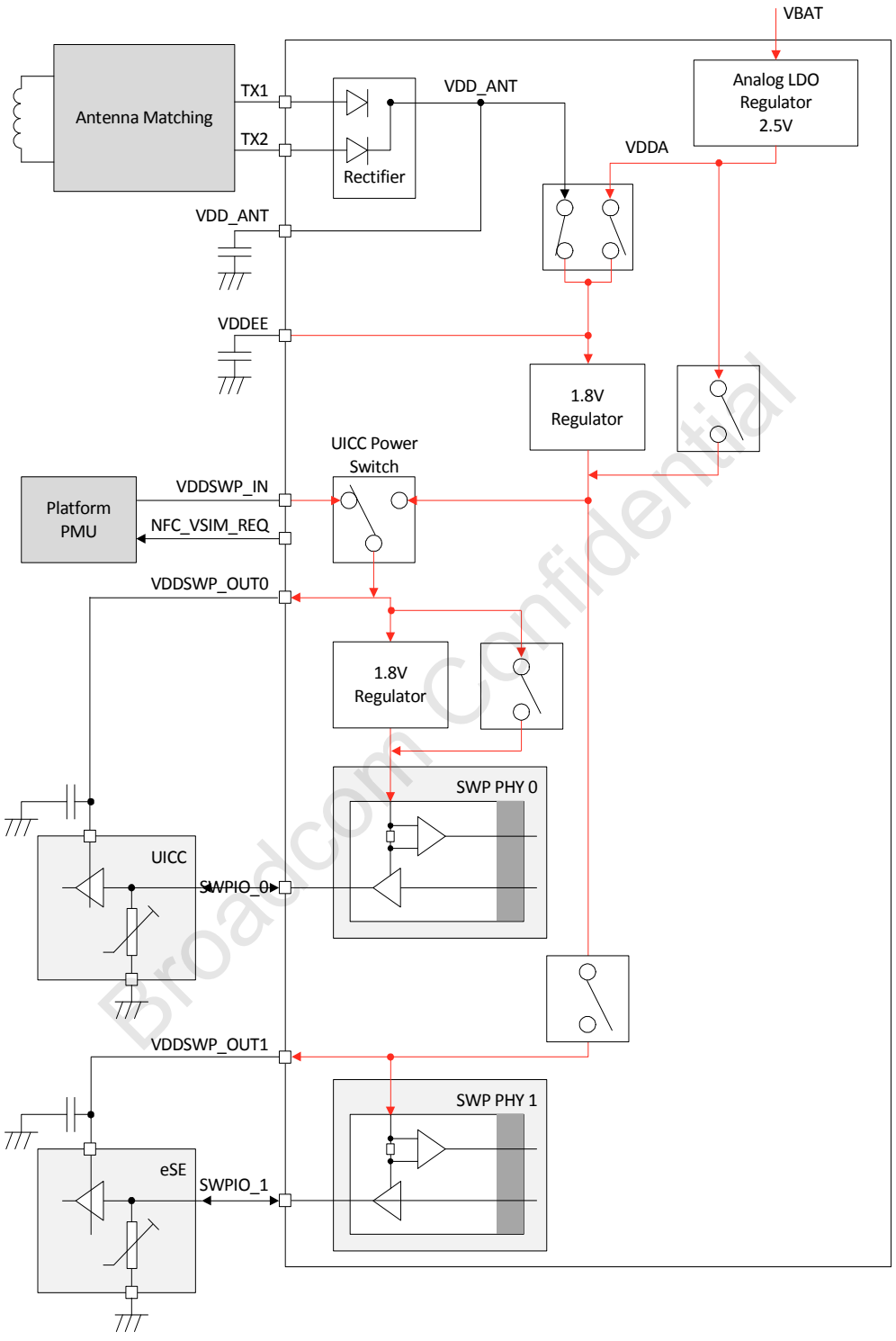
- Derived from the host platform PMU via VDDSWP_IN at 1.8V and 3V.
- Derived from VBAT via internal regulators at 1.8V.
- Derived from field power at 1.8V.

Power for the secure element connected to the SWP_1 interface can be supplied as follows:

- Derived from VBAT via internal regulators at 1.8V.
- Derived from field power at 1.8V.

Note: In low-power card emulation modes, only one SWP interface may be used at a time. In full-power modes, if it is required that both SWP interfaces are used at the same time, then SWP_0 power must be derived from the host platform PMU via VDDSWP_IN.

Figure 47: Secure Element Power Switching Architecture



NOTE: Not all switch combinations are valid.

The Single-Wire Protocol (SWP) interfaces implemented in the BCM43341 are compatible with ETSI TS 102 613. This provides connectivity to a SWP-enabled SIM card or UICC for Tag Emulation and Reader modes. They are available in both Battery-On and Battery-Off modes, but Initiator mode is supported only in Battery-On mode.

The BCM43341 is able to detect the presence of a standards-compliant UICC interface. This is accomplished by proceeding through the initialization process. The BCM43341 puts the SWP in ACTIVATED state. When it receives the ACT_SYNC over the SWP interface, a correct interface connection is confirmed.

The SWP interface protocols conform to ETSI 102-613 v9.1.0 and ETSI 102-622 v9.0.0.

Nonvolatile Memory Interface

For CE-1 Battery-off operation, an external NVM is used as the source of secure personality and persistence information. Either an EEPROM or an eSE can provide this NVM functionality.

The BCM43341 BSC bus forms a BSC master and interfaces with EEPROM NVM devices. Bus tie-off resistors are required in all applications. Pull-up resistors are required on the SCL and SDA pins to the VDD_EE pin.

The recommended EEPROM specification is ≥ 32 KB (256 kbits), 400 kHz, 1.7–5.5V with double-byte addressing.

In applications where a suitable embedded secure element (eSE) is connected to the SWP_1 interface, this can be used as the source of personality and persistence information, instead of the EEPROM. See Table 24 on page 102 for details on how to select the method of operation.

NFC Microprocessor and Memory Unit

The microprocessor core is based on the ARM CM0 processor. It runs embedded software from the link control (LC) layer up to the NFC controller interface (NCI). The ARM core is paired with a memory unit that contains 144 KB of ROM for program storage and boot ROM and 42 KB of RAM.

Configuration settings and embedded software patches may be downloaded to be applied to the ROM-based firmware to provide flexibility for bug fixes or features additions using the secure download mechanism. For applications circuits without NVM present, as these patches are normally downloaded from the host to the BCM43341 through the NCI host interface, and this must be performed at every power sequence of the BCM43341. Verification of this secure download can entail a delay of approximately 2.8 seconds while the device checks the authenticity of the signed data set (see Figure 48 on page 107, but disregard NVM programming time because NVM is not present).

Typically, the application circuit for a system designed for NFC payments will include NVM, which can be used for storage and subsequent retrieval of the configuration and patch data. This means that the host secure download mechanism only has to operate once in order to install the necessary data into this local NVM (see Figure 18 on page 44 for an example of the likely “one-time” download time sequence, which in this case includes the NVM programming time). Then, during each subsequent power-up sequence, the data will be restored from NVM and will not incur any host download or verification delays (see Figure 50 on page 108 for the time sequence for each subsequent boot-up from cold).

The adoption of a secure download mechanism means that direct access to all internal register space is normally disabled. During development and debug activity, this strong de-bug feature of Broadcom chips can be temporarily re-enabled by connection of an external hardware key fixture. Contact your Broadcom support representative for details.

The microprocessor, ROM and RAM, secure patch downloaded controller, and other ARM components, such as the interrupt controller, all reside on a single AHB bus. This system is clocked by a dedicated All-Digital Frequency-Locked Loop (AD-FLL). The AD-FLL is continuously tunable up to 24 MHz. The microprocessor/AHB system clock can therefore be programmed to the optimal frequency dictated by the processing demands.

Secure patch download timing and NFC boot-up timing are defined in Figure 48, Figure 49, and Figure 50.

Figure 48: NFC Boot-Up Sequence (Secure Patch Download) from Snooze

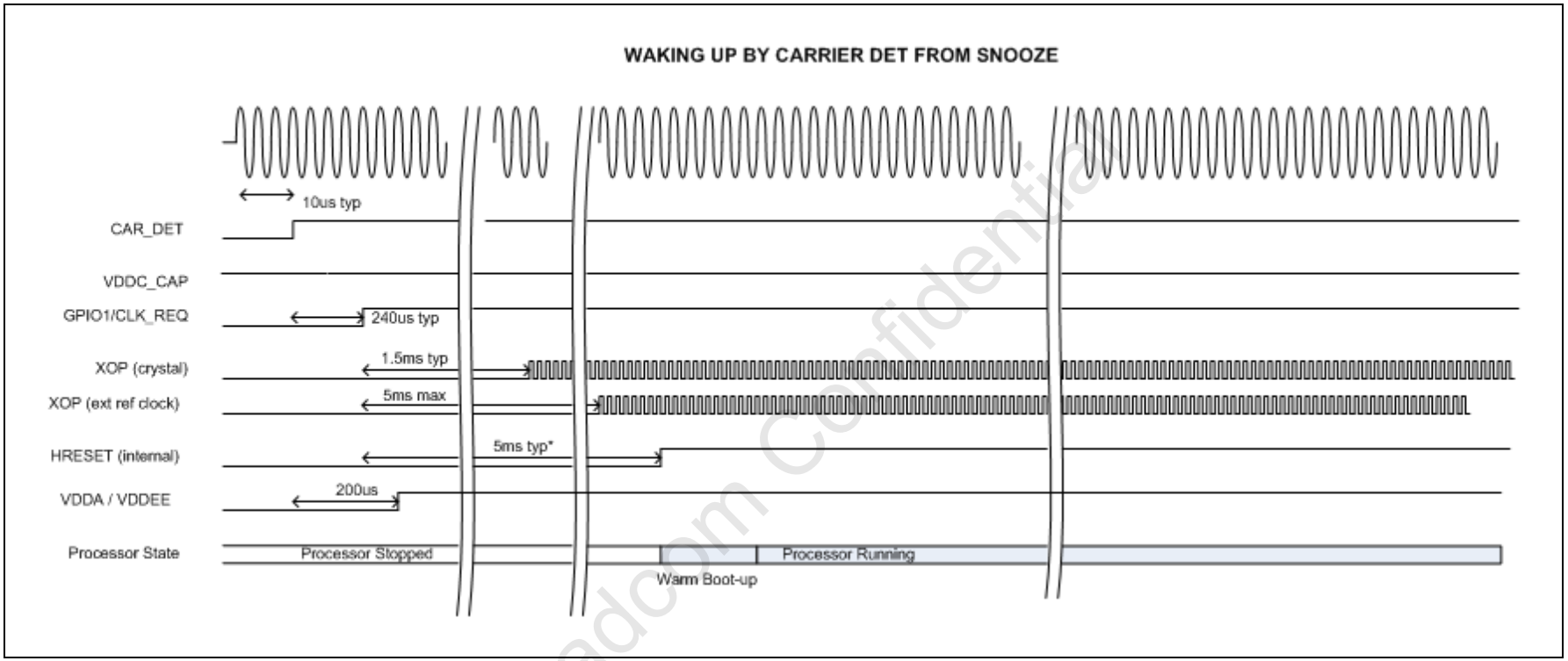


Figure 49: NFC Boot-Up Sequence (Secure Patch Download) from Low Power Mode

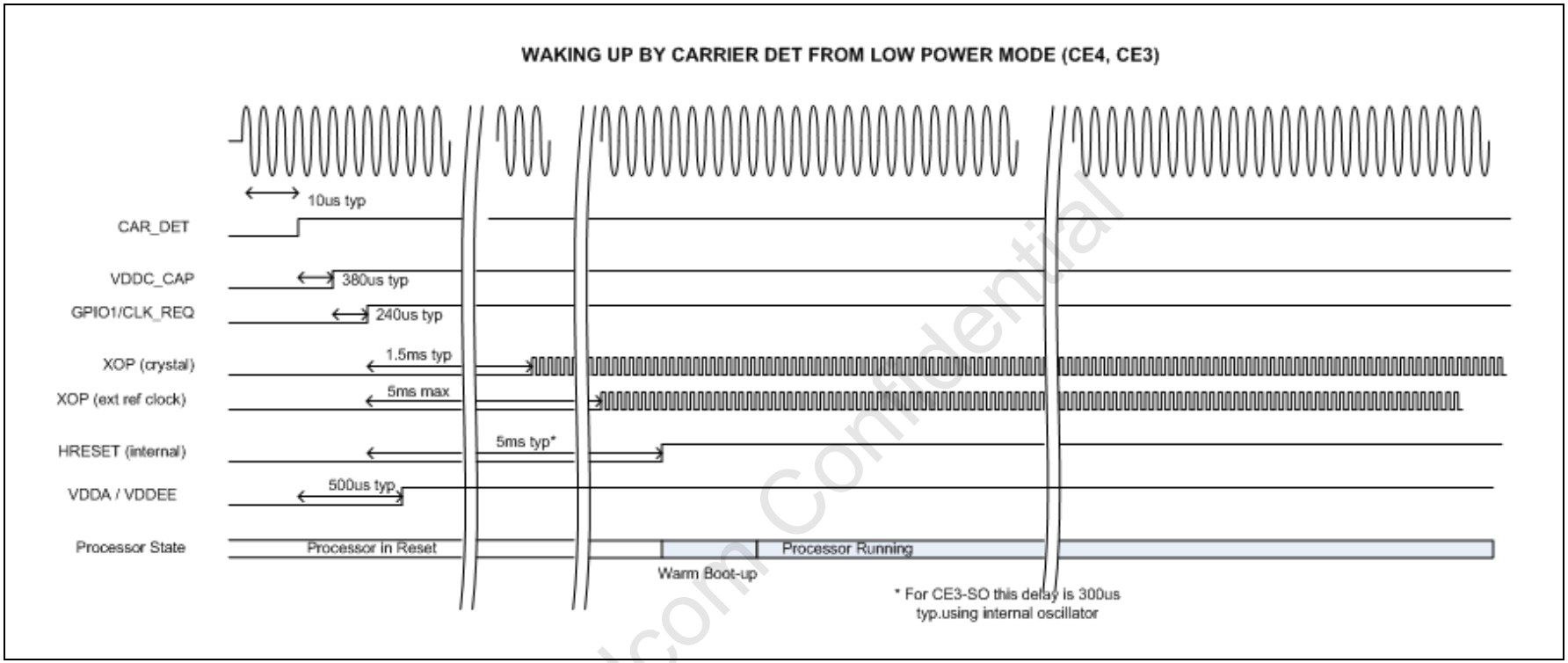
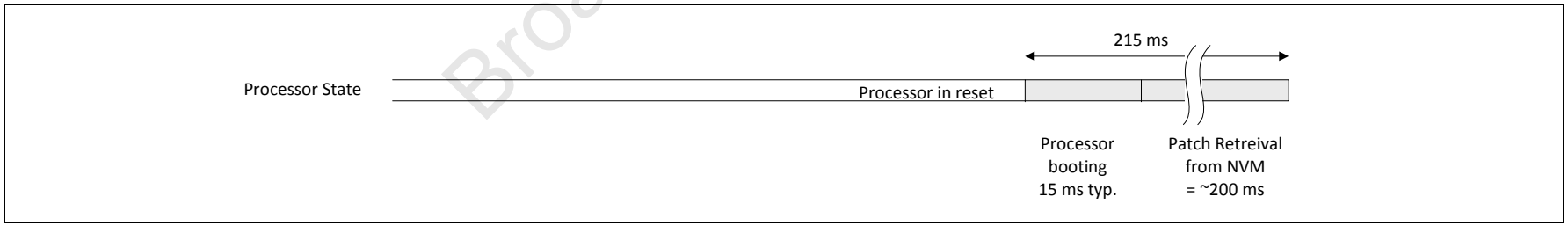


Figure 50: NFC Boot-Up Timing



NFC V_{BATT} Monitor

The V_{BATT} Monitor block is used as part of the power level control. In the low power mode, even though the rest of the system is powered down, the battery is used to keep the personality data stored in the battery-backed memory. V_{BATT} Monitor is used by the BCM43341 to control movement from one power state to the next lower power state. This block can be pre-programmed by the host with threshold values for comparators that are used to monitor the battery level to shut down the system and stop the current draw to prevent damage to the battery.

Card Emulation and Field Power Harvesting Clock

Card Emulation mode does not require a high-speed reference clock; the tag function block recovers its clock from the incoming carrier field.

NFC Operation Requirement

The reference clock (XTAL) for NFC is provided through the BT and FM section. Therefore, the BT_VDD and FM_VDD supplies need to be connected to use NFC.

Section 14: Pinout and Signal Descriptions

Signal Assignments

Figure 51 shows the WLBGA ball map. Table 25 on page 111 contains the signal description for all packages.

Figure 51: 141-Bump BCM43341 WLBGA Ball Map (Bottom View)

	11	10	9	8	7	6	5	4	3	2	1	
A	FM_LNAVCOVDD	FM_RFIN	BT_VCOVDD	BT_LNAVDD	BT_RF	BT_PAVDD	WRF_RFIN_2G	WRF_RFOUT_2G	WRF_PAPMU_VOUT_LDO3P3	WRF_RFOUT_5G	WRF_PAPMU_VBAT_VDD5P0	A
B	FM_VCOVSS	FM_LNAVSS	BT_VCOVSS	BT_PLLVDD	BT_PAVSS	BT_IFVSS	WRF_PA2G_VBAT_VDD3P3		WRF_CBUCK_PAVDD1P5		WRF_PAPMU_GND	B
C	FM_AOUT2		FM_PLLVSS	BT_IFVDD	BT_PLLVSS			WRF_PA2G_VBAT_GND3P3	WRF_PA5G_VBAT_GND3P3	WRF_PA5G_VBAT_GND3P3	WRF_RFIN_5G	C
D	FM_AOUT1	FM_PLLVDD		BT_I2S_WS	BT_I2S_CLK	VSSC	WRF_LNA_2G_GND1P2	WRF_PADRV_VBAT_VDD3P3	WRF_PADRV_VBAT_GND3P3	WRF_GPIO_OUT	WRF_LNA_5G_GND1P2	D
E	CLK_REQ	BT_DEV_WAKE	VDDC	BT_PCM_OUT	BT_I2S_DO		WRF_RX_GND1P2	WRF_TX_GND1P2			WRF_VCO_GND1P2	E
F	LPO_IN	BT_HOST_WAKE	BT_PCM_IN	BT_PCM_CLK	BT_PCM_SYNC		WRF_AFE_GND1P2	WRF_BUCK_VDD1P5	WL_GPIO_1	WRF_SYNTH_VDD1P2	WRF_XTAL_CAB_VDD1P2	F
G	BT_UART_CTS_N	BT_UART_TXD	NFC_RTS	RF_SW_CTRL_3	VSSC	RF_SW_CTRL_2	WL_GPIO_6	WL_GPIO_2	WL_GPIO_0	WRF_SYNTH_GND1P2	WRF_XTAL_CAB_XOP	G
H	BT_UART_RTS_N	BT_UART_RXD	VDDIO	RF_SW_CTRL_4	VDDC	RF_SW_CTRL_1	WL_GPIO_5	WL_GPIO_3	WRF_TCXO_VDD1P8	WRF_XTAL_CAB_GND1P2	WRF_XTAL_CAB_XON	H
J	NFC_GPIO1	NFC_REG_PU	NFC_CTS	NFC_SDA	WL_GPIO_4	VDDIO_RF	WL_GPIO_12	VDDIO	WRF_TCXO_CKIN2V	BT_REG_ON	WL_REG_ON	J
K	NFC_VCO_VDD	NFC_VCO_VSS	NFC_SPI_INT	NFC_SCL	NFC_GPIO0		SDIO_DATA_2	SDIO_DATA_3	RREFHSIC	HSIC_DATA	VDDC	K
L	NFC_PLL_VDD	NFC_PLL_VSS	NFC_VSSC	NFC_SWPIO_0	NFC_UTX	RF_SW_CTRL_0	SDIO_DATA_0	SDIO_DATA_1	HSIC_DVDD1P2_OUT	HSIC_STROBE	HSIC_AGND12PLL	L
M	NFC_VDD_ADC	NFC_VSS_ADC	NFC_SWPIO_1	PMU_NFC_VSS	NFC_URX	SDIO_CLK	SDIO_CMD	JTAG_SEL		VSSC	PMU_AVSS	M
N	NFC_VDDSWPIN_0	NFC_VDDSWP_0	NFC_VDDSE	NFC_VSSA	PMU_NFC_VDDC_CAP	VSSC		VOUT_2P5	VOUT_CLDO	SR_VDDBATA5V	SR_VLX	N
P	NFC_VDDEE	NFC_VDDANT	NFC_TX2	NFC_TX1	PMU_NFC_VDDA_CAP	PMU_NFC_VBAT	VDDC	VOUT_LNLDO	LDO_VDD1P5	SR_VDDBATP5V	SR_PVSS	P
	11	10	9	8	7	6	5	4	3	2	1	

Top layer metal restrict

Depopulated

Signal Descriptions

The signal name, type, and description of each pin in the BCM43341 is listed in Table 25. The symbols shown under Type indicate pin directions (I/O = bidirectional, I = input, O = output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any. See also Table 26 on page 119 for resistor strapping options.

Table 25: WLBGA Signal Descriptions

WLBGA Ball	Signal Name	Type	Description
WLAN RF Signal Interface			
A5	WRF_RFIN_2G	I	2.4G RF input
C1	WRF_RFIN_5G	I	5G RF input
A4	WRF_RFOUT_2G	O	2.4G RF output
A2	WRF_RFOUT_5G	O	5G RF output
D2	WRF_GPIO_OUT	I/O	–
RF Control Signals			
L6	RF_SW_CTRL_0	O	RF switch enable
H6	RF_SW_CTRL_1	O	RF switch enable
G6	RF_SW_CTRL_2	O	RF switch enable
G8	RF_SW_CTRL_3	O	RF switch enable
H8	RF_SW_CTRL_4	O	RF switch enable
SDIO Bus Interface			
M6	SDIO_CLK	I	SDIO clock input
M5	SDIO_CMD	I/O	SDIO command line
L5	SDIO_DATA_0	I/O	SDIO data line 0
L4	SDIO_DATA_1	I/O	SDIO data line 1. Also used as a strapping option (see Table 26 on page 119).
K5	SDIO_DATA_2	I/O	SDIO data line 2. Also used as a strapping option (see Table 26 on page 119).
K4	SDIO_DATA_3	I/O	SDIO data line 3

Note: Per Section 6 of the SDIO specification, 10 to 100 kohm pull-ups are required on the four DATA lines and the CMD line. This requirement must be met during all operating states by using external pull-up resistors or properly programming internal SDIO Host pull-ups.

Table 25: WLBGA Signal Descriptions (Cont.)

WLBGA Ball	Signal Name	Type	Description
JTAG Interface			
M4	JTAG_SEL	I/O	JTAG select: Connect this pin high (VDDIO) in order to use GPIO_2 through GPIO_5 and GPIO_12 as JTAG signals. Otherwise, if this pin is left as a NO_CONNECT, its internal pull-down selects the default mode that allows GPIOs 2, 3, 4, 5, and 12 to be used as GPIOs. **Note:** See "WLAN GPIO Interface" on page 112 for the JTAG signal pins.
HSIC Interface			
L2	HSIC_STROBE	I	HSIC Strobe
K2	HSIC_DATA	I/O	HSIC Data
K3	RREFHSIC	I	HSIC reference resistor input. If HSIC is used, connect this pin to ground via a 51Ω 5% resistor.
WLAN GPIO Interface			
G3	WL_GPIO_0	I/O	This pin can be programmed by software to be a GPIO.
F3	WL_GPIO_1	I/O	This pin can be programmed by software to be a GPIO or an AP_READY or HSIC_HOST_READY input from the host indicating that it is awake.
G4	WL_GPIO_2	I/O	This pin can be programmed by software to be a GPIO, the JTAG TCK or an HSIC_READY output to the host, indicating that the device is ready to respond with a CONNECT when it sees IDLE on the HSIC bus.
H4	WL_GPIO_3	I/O	This pin can be programmed by software to be a GPIO or the JTAG TMS signal.
J7	WL_GPIO_4	I/O	This pin can be programmed by software to be a GPIO, the JTAG TDI signal, the UART RX signal, or as the WLAN_HOST_WAKE output indicating that host wake-up should be performed.
H5	WL_GPIO_5	I/O	This pin can be programmed by software to be a GPIO, the JTAG TDO signal or the UART TX signal.
G5	WL_GPIO_6	I/O	GPIO pin. ***Note:*** Some GPIOs are also used as strapping options (see Table 26 on page 119).

Table 25: WLBGA Signal Descriptions (Cont.)

WLBGA Ball	Signal Name	Type	Description
J5	WL_GPIO_12	I/O	This pin can be programmed by software to be a GPIO or the JTAG TRST_L signal. GPIO12 has an internal pull-down by default if JTAG_SEL is low. When JTAG_SEL is high, GPIO12 is used as JTAG_TRST_L and is pulled up. This pin is also used as WLAN_DEV_WAKE, an out-of- band wake-up signal when the host wants to wake WLAN from the deep sleep mode. ***Note:*** Some GPIOs are also used as strapping options (see Table 26 on page 119).
Clocks			
H1	WRF_XTAL_CAB_XON	O	XTAL oscillator output
G1	WRF_XTAL_CAB_XOP	I	XTAL oscillator input
J3	WRF_TCXO_CKIN2V	I	TCXO buffered input. When not using a TCXO this pin should be connected to ground.
E11	CLK_REQ	O	External system clock request—Used when the system clock is not provided by a dedicated crystal (for example, when a shared TCXO is used). Asserted to indicate to the host that the clock is required. Shared by BT, NFC, and WLAN. Can also be programmed as the BT_I2S_DI input pin if CLK_REQ functionality is not required.
F11	LPO_IN	I	External sleep clock input (32.768 kHz)
Bluetooth/FM Receiver			
A7	BT_RF	I/O	Bluetooth transceiver RF antenna port
D11	FM_AOUT1	O	FM analog output 1
C11	FM_AOUT2	O	FM analog output 2
A10	FM_RFIN	I	FM radio antenna port
Bluetooth PCM			
F8	BT_PCM_CLK	I/O	PCM clock; can be master (output) or slave (input)
F9	BT_PCM_IN	I	PCM data input sensing
E8	BT_PCM_OUT	O	PCM data output
F7	BT_PCM_SYNC	I/O	PCM sync; can be master (output) or slave (input)

Table 25: WLBGA Signal Descriptions (Cont.)

WLBGA Ball	Signal Name	Type	Description
Bluetooth UART and Wake			
G11	BT_UART_CTS_N	I	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.
H11	BT_UART_RTS_N	O	UART request-to-send. Active-low request-to-send signal for the HCI UART interface.
H10	BT_UART_RXD	I	UART serial input. Serial data input for the HCI UART interface.
G10	BT_UART_TXD	O	UART serial output. Serial data output for the HCI UART interface.
E10	BT_DEV_WAKE	I/O	DEV_WAKE or general-purpose I/O signal
F10	BT_HOST_WAKE	I/O	HOST_WAKE or general-purpose I/O signal
Note: By default, the Bluetooth BT WAKE signals provide GPIO/WAKE functionality, and the UART pins provide UART functionality. Through software configuration, the PCM interface can also be routed over the BT_WAKE/UART signals as follows: • PCM_CLK on the UART_RTS_N pin • PCM_OUT on the UART_CTS_N pin • PCM_SYNC on the BT_HOST_WAKE pin • PCM_IN on the BT_DEV_WAKE pin In this case, the BT HCI transport included sleep signaling will operate using UART_RXD and UART_TXD; that is, using a 3-Wire UART Transport.			
Bluetooth/FM I^2S			
D7	BT_I2S_CLK	I/O	I^2S clock; can be master (output) or slave (input)
E7	BT_I2S_DO	I/O	I^2S data output
D8	BT_I2S_WS	I/O	I^2S WS; can be master (output) or slave (input)
NFC Host Interface (UART, SPI or BSC. See Table 23 on page 101***)***			
J9	NFC_CTS	I	UART clear-to-send
G9	NFC_RTS	O	UART request-to-send
M7	NFC_URX	I	UART receive
L7	NFC_UTX	O	UART transmit
NFC GPIO			
K7	NFC_GPIO0	I/O	General Purpose I/O
J11	NFC_GPIO1	I/O	General Purpose I/O; can be configured to be NFC_VSIM_REQ.

Table 25: WLBGA Signal Descriptions (Cont.)

WLBGA Ball	Signal Name	Type	Description
NFC Single Wire Protocol			
L8	NFC_SWPIO_0	I/O	Single Wire Protocol I/O
M9	NFC_SWPIO_1	I/O	Single Wire Protocol I/O
NFC EEPROM Interface			
K8	NFC_SCL	O	BSC clock for EEPROM
J8	NFC_SDA	I/O	BSC data for EEPROM
NFC Antenna Interface			
P8	NFC_TX1	I/O	NFC Antenna Transmit/Receive pin 1
P9	NFC_TX2	I/O	NFC Antenna Transmit/Receive pin 2
NFC MIscellaneous Interface Pins			
K9	NFC_SPI_INT	I/O	Host interface selection and SPI interrupt to host in SPI mode only
Miscellaneous			
J1	WL_REG_ON	I	Used by PMU to power up or power down the internal BCM43341 regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
J2	BT_REG_ON	I	Used by PMU to power up or power down the internal BCM43341 regulators used by the Bluetooth/FM section. Also, when deasserted, this pin holds the Bluetooth/FM section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
Integrated Voltage Regulators			
N2	SR_VDDBATA5V	I	Quiet VBAT
P2	SR_VDDBATP5V	I	Power VBAT
N1	SR_VLX	O	CBUCK switching regulator output. See Table 44 on page 153 for details of the inductor and capacitor required on this output.
P3	LDO_VDD1P5	I	Input for the LNLDO, CLDO, and HSIC LDOs. It is also the voltage feedback pin for the CBUCK regulator.
P4	VOUT_LNLDO	O	Output of low-noise LNLDO
N3	VOUT_CLDO	O	Output of core LDO

Table 25: WLBGA Signal Descriptions (Cont.)

WLBGA Ball	Signal Name	Type	Description
Bluetooth Power Supplies			
A6	BT_PAVDD	I	Bluetooth PA power supply
A8	BT_LNAVDD	I	Bluetooth LNA power supply
C8	BT_IFVDD	I	Bluetooth IF block power supply
B8	BT_PLLVDD	I	Bluetooth RF PLL power supply
A9	BT_VCOVDD	I	Bluetooth RF power supply
FM Receiver Power Supplies			
D10	FM_PLLVDD	I	FM PLL power supply
A11	FM_LNAVCOVDD	I	FM VCO and receiver power supply pin
WLAN Power Supplies			
F4	WRF_BUCK_VDD1P5	I	Internal LDO supply from CBUCK for VCO, AFE, TX, and RX
B3	WRF_CBUCK_PAVDD1P5	I	NO_CONNECT
B5	WRF_PA2G_VBAT_VDD3P3	I	2G PA 3.3V Supply
D4	WRF_PADRV_VBAT_VDD3P3	I	3.3V supply for A/G band PAD
A1	WRF_PAPMU_VBAT_VDD5P0	I	PAPMU VBAT power supply
A3	WRF_PAPMU_VOUT_LDO3P3	O	PAPMU 3.3V LDO output voltage
F2	WRF_SYNTH_VDD1P2	I	Synth VDD 1.2V input
H3	WRF_TCXO_VDD1P8	I	Supply to the WRF_TCXO_CKIN input buffer. When not using a TCXO, this pin should be connected to ground.
F1	WRF_XTAL_CAB_VDD1P2	I	XTAL oscillator supply
NFC Power Supplies			
P10	NFC_VDDANT	O	Field power supply rectifier output, large external cap for battery-off
K11	NFC_VCO_VDD	I	NFC VCO supply
L11	NFC_PLL_VDD	I	NFC PLL supply
M11	NFC_VDD_ADC	I	Decoupling, need linking to VDDC_CAP through the target PCB
N10	NFC_VDDSWP_0	O	UICC supply out 0
N11	NFC_VDDSWPIN_0	I	Platform UICC supply in
P11	NFC_VDDEE	O	1.7–2.75V supply voltage for EEPROM
N9	NFC_VDDSE	O	Secure Element (SE) power output (SWP1 / UICC1)
P6	PMU_NFC_VBAT	I	Battery supply
P7	PMU_NFC_VDDA_CAP	O	Analog LDO supply decoupling (2.5V)
N7	PMU_NFC_VDDC_CAP	O	Decoupling, links VDDADC, VDD_XTAL, and VDD_VCO via the target PCB
J10	NFC_REG_PU	I	Regulator power control from host

Table 25: WLBGA Signal Descriptions (Cont.)

WLBGA Ball	Signal Name	Type	Description
Miscellaneous Power Supplies			
L3	HSIC_DVDD1P2_OUT	O	1.2V supply for HSIC interface. This pin can be NO_CONNECT when HSIC is not used.
E9	VDDC_E9	I	Core supply for WLAN and BT.
H7	VDDC_H7	I	
K1	VDDC_K1	I	
P5	VDDC_P5	I	
H9	VDDIO_H9	I	I/O supply (1.8–3.3V). For the WLBGA package, this is the supply for both SDIO and other I/O pads.
J4	VDDIO_J4	I	
J6	VDDIO_RF	I	I/O supply for RF switch control pads (3.3V)
N4	VOUT_2P5	O	2.5V LDO output
Ground			
B7	BT_PAVSS	I	Bluetooth PA ground
B6	BT_IFVSS	I	1.2V Bluetooth IF block ground
C7	BT_PLLVSS	I	Bluetooth RF PLL ground
B9	BT_VCOVSS	I	1.2V Bluetooth RF ground
B11	FM_VCOVSS	I	FM VCO ground
B10	FM_LNAVSS	I	FM receiver ground
C9	FM_PLLVSS	I	FM PLL ground
L1	HSIC_AGND12PLL	I	HSIC PLL ground
N8	NFC_VSSA		Ground
M10	NFC_VSS_ADC		Ground
L9	NFC_VSSC		Ground
L10	NFC_PLL_VSS		Ground
K10	NFC_VCO_VSS		Ground
M1	PMU_AVSS	I	Quiet ground
M8	PMU_NFC_VSS	I	NFC PMU ground
P1	SR_PVSS	I	Power ground
D6	VSSC_D6	I	Core ground for WLAN and BT
G7	VSSC_G7	I	
M2	VSSC_M2	I	
N6	VSSC_N6	I	
G2	WRF_SYNTH_GND1P2	I	Synth ground
F5	WRF_AFE_GND1P2	I	AFE ground
D5	WRF_LNA_2G_GND1P2	I	2 GHz internal LNA ground
D1	WRF_LNA_5G_GND1P2	I	5 GHz internal LNA ground
C4	WRF_PA2G_VBAT_GND3P3	I	2.4 GHz PA ground

Table 25: WLBGA Signal Descriptions (Cont.)

WLBGA Ball	Signal Name	Type	Description
C2	WRF_PA5G_VBAT_GND3P3_C2	I	5 GHz PA ground
C3	WRF_PA5G_VBAT_GND3P3_C3		
B1	WRF_PAPMU_GND	I	PMU ground
D3	WRF_PADRV_VBAT_GND3P3	I	PA driver ground
E5	WRF_RX_GND1P2	I	RX ground
E4	WRF_TX_GND1P2	I	TX ground
E1	WRF_VCO_GND1P2	I	VCO/LOGEN ground
H2	WRF_XTAL_CAB_GND1P2	I	XTAL ground

WLAN GPIO Signals and Strapping Options

The pins listed in Table 26 on page 119 are sampled at power-on reset (POR) to determine the various operating modes. Sampling occurs a few milliseconds after an internal POR or deassertion of the external POR. After the POR, each pin assumes the GPIO or alternative function specified in the signal descriptions table. Each strapping option pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to GND, using a 10 kΩ resistor or less.

Note: Refer to the reference board schematics for more information.

Table 26: WLAN GPIO Functions and Strapping Options (Advance Information)

Pin Name	*WLBG A Pin #*	*Default*	*Function*	*Description*
SDIO_DATA_1	F9	0	strap_host_ifc_1	The three strap pins strap_host_ifc_[3:1] select the host interface[a] to enable: • 0XX: SDIO • 10X: gSPI • 110: normal HSIC • 111: bootloader-less HSIC
SDIO_DATA_2	G8	0	strap_host_ifc_2	• 0: select gSPI mode • 1: select SDIO mode
GPIO_6/ SPI_MODE_SEL	J6	0	strap_host_ifc_3	• 0: select SDIO mode • 1: select HSIC mode
JTAG_SEL	M4	N/A	JTAG select	• JTAG select: Connect this pin high (VDDIO) in order to use GPIO_2 through GPIO_5 and GPIO_12 as JTAG signals. Otherwise, if this pin is left as a NO_CONNECT, its internal Pull-down selects the default mode that allows GPIOs 2, 3, 4, 5, and 12 to be used as GPIOs. ***Note:*** See "WLAN GPIO Interface" on page 112 for the JTAG signal pins.

a. The unused host interface is tristated. However, the SDIO lines have internal pulls activated when in HSIC mode (see Table 28: "I/O States," on page 121). There are no bus-keepers on the HSIC interface when it is not in use.

CIS Select Options

CIS select options are defined in Table 27.

Table 27: CIS Select

OTPEnabled	*CIS Source*	*OTP State*	*ChipID Source*
0	Default	OFF	Default
1	OTP if programmed, else default	ON	OTP if programmed, else default

I/O States

The following notations are used in Table 28:

- I: Input signal
- O: Output signal
- I/O: Input/Output signal
- PU = Pulled up
- PD = Pulled down
- NoPull = Neither pulled up nor pulled down

Table 28: I/O States

Name	*I/O*	*Keeper*	*Active Mode*	*Low Power State/ Sleep (All Power Present)*	*Power-down (BT_REG_ON and WL_REG_ON Held Low)*	*Out-of-Reset; Before SW Download (BT_REG_ON=1; WL_REG_ON=1)*	*(WL_REG_ON=1 and BT_REG_ON=0) and VDDIOs Are Present*	*(WL_REG_ON=0 and BT_REG_ON=1) and VDDIOs Are Present*	*Power Rail*
WL_REG_ON	I	N	Input; PD (pull-down can be disabled)	Input; PD (pull-down can be disabled)	Input; PD (of 200K)	Input; PD (of 200k)	Input; PD (of 200k)	–	–
BT_REG_ON	I	N	Input; PD (pull down can be disabled)	Input; PD (pull down can be disabled)	Input; PD (of 200K)	Input; PD (of 200k)	Input; PD (of 200k)	–	–
CLK_REQ	I/O	Y	Open drain or push-pull (programmable). Active high.	Open drain or push-pull (programmable). Active high	PD	Open drain. Active high.	Open drain. Active high.	–	BT_VDDO
BT_HOST_WAKE	I/O	Y	I/O; PU, PD, NoPull (programmable)	I/O; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PD	Input, PD	–	BT_VDDO
BT_DEV_WAKE	I/O	Y	I/O; PU, PD, NoPull (programmable)	Input; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PD	Input, PD	–	BT_VDDO
BT_UART_CTS	I	Y	Input; NoPull	Input; NoPull	High-Z, NoPull	Input; PU	Input; PU	–	BT_VDDO
BT_UART_RTS	O	Y	Output; NoPull	Output; NoPull	High-Z, NoPull	Input; PU	Input; PU	–	BT_VDDO
BT_UART_RXD	I	Y	Input; PU	Input; NoPull	High-Z, NoPull	Input; PU	Input; PU	–	BT_VDDO
BT_UART_TXD	O	Y	Output; NoPull	Output; NoPull	High-Z, NoPull	Input; PU	Input; PU	–	BT_VDDO
SDIO_DATA_0	I/O	N	HSIC MODE -> PU; SDIO MODE -> NoPull	HSIC MODE -> PU; SDIO MODE -> NoPull	HSIC MODE -> NoPull; SDIO MODE -> NoPull	HSIC MODE -> PU; SDIO MODE -> NoPull	HSIC MODE -> PU; SDIO MODE -> NoPull	–	WL_VDDIO

Table 28: I/O States (Cont.)

Name	I/O	Keeper	Active Mode	Low Power State/ Sleep (All Power Present)	Power-down (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset; Before SW Download (BT_REG_ON=1; WL_REG_ON=1)	(WL_REG_ON=1 and BT_REG_ON=0) and VDDIOs Are Present	(WL_REG_ON=0 and BT_REG_ON=1) and VDDIOs Are Present	Power Rail
SDIO_DATA_1	I/O	N	HSIC MODE -> PD; SDIO MODE -> NoPull	HSIC MODE -> PD; SDIO MODE -> NoPull	HSIC MODE -> NoPull; SDIO MODE -> NoPull	HSIC MODE -> PD; SDIO MODE -> PD	HSIC MODE -> PD; SDIO MODE -> NoPull	–	WL_VDDIO
SDIO_DATA_2	I/O	N	HSIC MODE -> PU; SDIO MODE -> NoPull	HSIC MODE -> PU; SDIO MODE -> NoPull	HSIC MODE -> NoPull; SDIO MODE -> NoPull	HSIC MODE -> PU; SDIO MODE -> PD	HSIC MODE -> PU; SDIO MODE -> NoPull	–	WL_VDDIO
SDIO_DATA_3	I/O	N	HSIC MODE -> PU; SDIO MODE -> NoPull	HSIC MODE -> PU; SDIO MODE -> NoPull	HSIC MODE -> NoPull; SDIO MODE -> NoPull	HSIC MODE -> PU; SDIO MODE -> NoPull	HSIC MODE -> PU; SDIO MODE -> NoPull	–	WL_VDDIO
SDIO_CMD	I/O	N	HSIC MODE -> PU; SDIO MODE -> NoPull	HSIC MODE -> PU; SDIO MODE -> NoPull	HSIC MODE -> NoPull; SDIO MODE -> NoPull	HSIC MODE -> PU; SDIO MODE -> NoPull	HSIC MODE -> PU; SDIO MODE -> NoPull	–	WL_VDDIO
SDIO_CLK	I	N	HSIC MODE -> PD; SDIO MODE -> NoPull	HSIC MODE -> PD; SDIO MODE -> NoPull	HSIC MODE -> NoPull; SDIO MODE -> NoPull	HSIC MODE -> PD; SDIO MODE -> NoPull	HSIC MODE -> PD; SDIO MODE -> NoPull	–	WL_VDDIO
BT_PCM_CLK	I/O	Y	Input; NoPull (Note 4)	Input; NoPull (Note 4)	High-Z, NoPull	Input, PD	Input, PD	–	BT_VDDO
BT_PCM_IN	I/O	Y	Input; NoPull (Note 4)	Input; NoPull (Note 4)	High-Z, NoPull	Input, PD	Input, PD	–	BT_VDDO
BT_PCM_OUT	I/O	Y	Input; NoPull (Note 4)	Input; NoPull (Note 4)	High-Z, NoPull	Input, PD	Input, PD	–	BT_VDDO
BT_PCM_SYNC	I/O	Y	Input; NoPull (Note 4)	Input; NoPull (Note 4)	High-Z, NoPull	Input, PD	Input, PD	–	BT_VDDO
BT_I2S_WS	I/O	Y	Input; NoPull (Note 5)	Input; NoPull (Note 5)	High-Z, NoPull	Input, PD	Input, PD	–	BT_VDDO
BT_I2S_CLK	I/O	Y	Input; NoPull (Note 5)	Input; NoPull (Note 5)	High-Z, NoPull	Input, PD	Input, PD	–	BT_VDDO
BT_I2S_DO	I/O	Y	Input; NoPull (Note 5)	Input; NoPull (Note 5)	High-Z, NoPull	Input, PD	Input, PD	–	BT_VDDO
JTAG_SEL	I	Y	PD	PD	PD	PD	PD	PD	WL_VDDIO
GPIO_0	I/O	Y	PD	PD	NoPull	PD	PD	PD	WL_VDDIO
GPIO_1	I/O	Y	NoPull	NoPull	NoPull	NoPull	NoPull	NoPull	WL_VDDIO
GPIO_2	I/O	Y	PU	PU	NoPull	PU	PU	PU	WL_VDDIO
GPIO_3	I/O	Y	JTAG_SEL = 1 PU; jtag_sel=0 PD	jtag_sel=1 PU; jtag_sel=0 PD	NoPull	jtag_sel=1 PU; jtag_sel=0 PD	jtag_sel=1 PU; jtag_sel=0 PD	jtag_sel = 1 PU; jtag_sel = 0 PD	WL_VDDIO
GPIO_4	I/O	Y	jtag_sel=1 PU; jtag_sel=0 PD	jtag_sel=1 PU; jtag_sel=0 PD	NoPull	jtag_sel=1 PU; jtag_sel=0 PD	jtag_sel=1 PU; jtag_sel=0 PD	jtag_sel = 1 PU; jtag_sel = 0 PD	WL_VDDIO

Table 28: I/O States (Cont.)

Name	I/O	Keeper	Active Mode	Low Power State/ Sleep (All Power Present)	Power-down (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset; Before SW Download (BT_REG_ON=1; WL_REG_ON=1)	(WL_REG_ON=1 and BT_REG_ON=0) and VDDIOs Are Present	(WL_REG_ON=0 and BT_REG_ON=1) and VDDIOs Are Present	Power Rail
GPIO_5	I/O	Y	NoPull	NoPull	NoPull	NoPull	NoPull	NoPull	WL_VDDIO
GPIO_6	I/O	Y	PD	PD	NoPull	PD	PD	PD	WL_VDDIO
GPIO_12	I/O	Y	jtag_sel=1 PU; jtag_sel=0 PD	jtag_sel=1 PU; jtag_sel=0 PD	NoPull	jtag_sel=1 PU; jtag_sel=0 PD	jtag_sel=1 PU; jtag_sel=0 PD	PU	WL_VDDIO

Note:

1. Keeper column: N=pad has no keeper. Y=pad has a keeper. Keeper is always active except in Power-down state.
2. If there is no keeper, and it is an input and there is Nopull, then the pad should be driven to prevent leakage due to floating pad (e.g., SDIO_CLK).
3. In the Power-down state (xx_REG_ON=0): High-Z; NoPull => the pad is disabled because power is not supplied.
4. Depending on whether the PCM interface is enabled and the configuration of PCM is in master or slave mode, it can be either output or input.
5. Depending on whether the I^2S interface is enabled and the configuration of I^2S is in master or slave mode, it can be either output or input.
6. GPIO_6 is input-only during the Low-Power and Deep-Sleep modes.
7. GPIO_0 through GPIO_5 and GPIO_12 can be configured to operate as inputs or outputs in Deep-Sleep mode before entering the mode.
8. The GPIO pull states for the Active and Low-Power states are hardware defaults. They can all be subsequently programmed as pull-ups or pull-downs.
9. Regarding GPIO pins, the following are the pull-up and pull-down values for both 3.3V and 1.8V VDDIO:

	Minimum (kΩ)	Typical (kΩ)	Maximum (kΩ)
3.3V VDDIO, Pull-downs:	51.5	44.5	38
3.3V VDDIO, Pull-ups:	37.4	39.5	44.5
1.8V VDDIO, Pull-downs:	64	83	116
1.8V VDDIO, Pull-ups:	65	86	118

Section 15: DC Characteristics

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Absolute Maximum Ratings

Caution! The absolute maximum ratings in Table 29 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 29: Absolute Maximum Ratings

Rating	Symbol	Value	Unit
DC supply for VBAT and PA driver supply:	VBAT	–0.5 to +6.0	V
DC supply voltage for digital I/O	VDDIO	–0.5 to 3.9	V
DC supply voltage for RF switch I/Os	VDDIO_RF	–0.5 to 3.9	V
DC input supply voltage for CLDO and LNLDO1	–	–0.5 to 1.575	V
DC supply voltage for RF analog	VDDRF	–0.5 to 1.32	V
DC supply voltage for core	VDDC	–0.5 to 1.32	V
WRF_TCXO_VDD	–	–0.5 to 3.63	V
Maximum undershoot voltage for I/O	$V_{undershoot}$	–0.5	V
Maximum overshoot voltage for I/O	$V_{overshoot}$	0.5	V
Maximum Junction Temperature	T_j	125	°C

Environmental Ratings

The environmental ratings are shown in Table 30.

Table 30: Environmental Ratings

Characteristic	Value	Units	Conditions/Comments
Ambient Temperature (T_A)	–30 to +85	°C	Functional operation[a]
Storage Temperature	–40 to +125	°C	–
Relative Humidity	Less than 60	%	Storage
	Less than 85	%	Operation

a. Functionality is guaranteed but specifications require derating at extreme temperatures; see the specification tables for details.

Electrostatic Discharge Specifications

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

Table 31: ESD Specifications

Pin Type	Symbol	Condition	ESD Rating	Unit
ESD, Handling Reference: NQY00083, Section 3.4, Group D9, Table B	ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/JESD22-A114	2000	V
Machine Model (MM)	ESD_HAND_MM	Machine model contact	100	V
CDM	ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/JESD22-C101	500	V

Recommended Operating Conditions and DC Characteristics

Caution! Functional operation is not guaranteed outside of the limits shown in Table 32 and operation outside these limits for extended periods can adversely affect long-term reliability of the device.

Table 32: Recommended Operating Conditions and DC Characteristics

		Value			
Parameter	***Symbol***	***Minimum***	***Typical***	***Maximum***	***Unit***
DC supply voltage for VBAT	VBAT	2.9[a]	–	4.8[b]	V
DC supply voltage for core	VDD	1.14	1.2	1.26	V
DC supply voltage for RF blocks in chip	VDDRF	1.14	1.2	1.26	V
DC supply voltage for TCXO input buffer	WRF_TCXO_VDD	1.62	1.8	1.98	V
DC supply voltage for digital I/O	VDDIO, VDDIO_SD	1.71	–	3.63	V
DC supply voltage for RF switch I/Os	VDDIO_RF	3.13	3.3	3.46	V
Internal POR threshold	Vth_POR	0.4	–	0.7	V
SDIO Interface I/O Pins					
For VDDIO_SD = 1.8V:					
Input high voltage	VIH	1.27	–	–	V
Input low voltage	VIL	–	–	0.58	V
Output high voltage @ 2 mA	VOH	1.40	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
For VDDIO_SD = 3.3V:					
Input high voltage	VIH	0.625 × VDDIO	–	–	V
Input low voltage	VIL	–	–	0.25 × VDDIO	V
Output high voltage @ 2 mA	VOH	0.75 × VDDIO	–	-	V
Output low voltage @ 2 mA	VOL	–	–	0.125 × VDDIO	V

Table 32: Recommended Operating Conditions and DC Characteristics (Cont.)

Parameter	Symbol	Value			Unit
		Minimum	Typical	Maximum	
Other Digital I/O Pins					
For VDDIO = 1.8V:					
Input high voltage	VIH	0.65 × VDDIO	–	–	V
Input low voltage	VIL	-	–	0.35 × VDDIO	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.45	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
For VDDIO = 3.3V:					
Input high voltage	VIH	2.00	–	–	V
Input low voltage	VIL	–	–	0.80	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.40	V
RF Switch Control Output Pins[c]					
For VDDIO_RF = 3.3V:					
Output high voltage	VOH	VDDIO – 0.4	–	–	V
Output low voltage	VOL	–	–	0.40	V
Input capacitance	C_{IN}	–	–	5	pF

a. The BCM43341 is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.0V < VBAT < 4.8V.
b. The maximum continuous voltage is 4.8V. Voltages up to 5.5V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
c. Programmable 2 mA to 16 mA drive strength. Default is 10 mA.

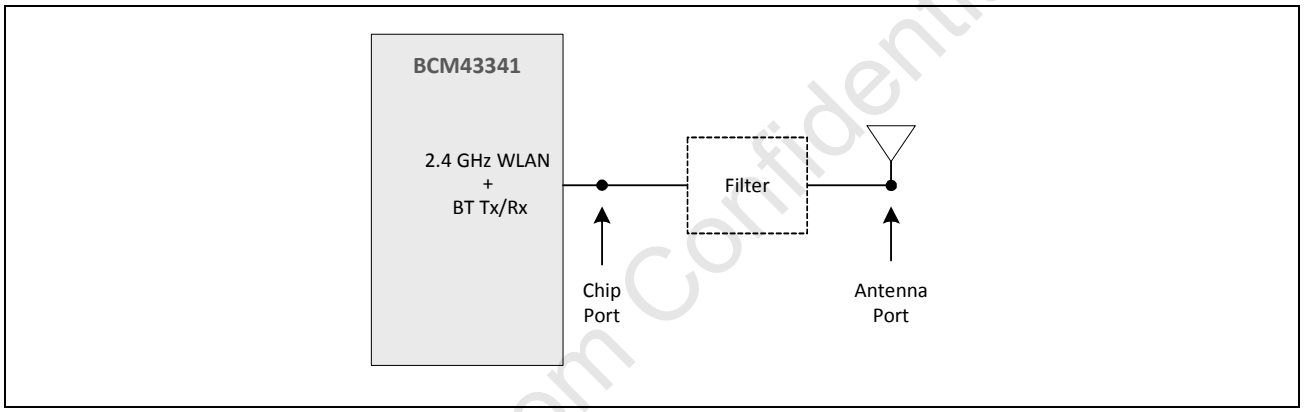
Section 16: Bluetooth RF Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, limit values apply for the conditions specified in Table 30: “Environmental Ratings,” on page 125 and Table 32: “Recommended Operating Conditions and DC Characteristics,” on page 126. Typical values apply for the following conditions:

- VBAT = 3.6V
- Ambient temperature +25°C

Figure 52: RF Port Location for Bluetooth Testing



Note: All Bluetooth specifications are measured at the Chip port unless otherwise specified.

Table 33: Bluetooth Receiver RF Specifications

Parameter	*Conditions*	*Minimum*	*Typical*	*Maximum*	*Unit*
Note: The specifications in this table are measured at the Chip port output unless otherwise specified.					
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity	GFSK, 0.1% BER, 1 Mbps	–	–92.5	–	dBm
	π/4–DQPSK, 0.01% BER, 2 Mbps	–	–94.5	–	dBm
	8–DPSK, 0.01% BER, 3 Mbps	–	–88.5	–	dBm
Input IP3	–	–16	–	–	dBm
Maximum input at antenna	–	–	–	–20	dBm
Interference Performance[a]					
C/I co-channel	GFSK, 0.1% BER	–	–	11	dB
C/I 1-MHz adjacent channel	GFSK, 0.1% BER	–	–	0.0	dB
C/I 2-MHz adjacent channel	GFSK, 0.1% BER	–	–	–30	dB
C/I ≥ 3-MHz adjacent channel	GFSK, 0.1% BER	–	–	–40	dB
C/I image channel	GFSK, 0.1% BER	–	–	–9	dB
C/I 1-MHz adjacent to image channel	GFSK, 0.1% BER	–	–	–20	dB
C/I co-channel	π/4–DQPSK, 0.1% BER	–	–	13	dB
C/I 1-MHz adjacent channel	π/4–DQPSK, 0.1% BER	–	–	0.0	dB
C/I 2-MHz adjacent channel	π/4–DQPSK, 0.1% BER	–	–	–30	dB
C/I ≥ 3-MHz adjacent channel	π/4–DQPSK, 0.1% BER	–	–	–40	dB
C/I image channel	π/4–DQPSK, 0.1% BER	–	–	–7	dB
C/I 1-MHz adjacent to image channel	π/4–DQPSK, 0.1% BER	–	–	–20	dB
C/I co-channel	8–DPSK, 0.1% BER	–	–	21	dB
C/I 1 MHz adjacent channel	8–DPSK, 0.1% BER	–	–	5.0	dB
C/I 2 MHz adjacent channel	8–DPSK, 0.1% BER	–	–	–25	dB
C/I ≥ 3-MHz adjacent channel	8–DPSK, 0.1% BER	–	–	–33	dB
C/I Image channel	8–DPSK, 0.1% BER	–	–	0.0	dB
C/I 1-MHz adjacent to image channel	8–DPSK, 0.1% BER	–	–	–13	dB
Out-of-Band Blocking Performance (CW)					
30–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000–2399 MHz	0.1% BER	–	–27	–	dBm
2498–3000 MHz	0.1% BER	–	–27	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	dBm
Out-of-Band Blocking Performance, Modulated Interferer (LTE)					

Table 33: Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
		GFSK (1 Mbps)			
2310Mhz	LTE band40 TDD 20M BW	–	–20	–	dBm
2330MHz	LTE band40 TDD 20M BW	–	–21	–	dBm
2350MHz	LTE band40 TDD 20M BW	–	–22	–	dBm
2370MHz	LTE band40 TDD 20M BW	–	–23	–	dBm
2510MHz	LTE band7 FDD 20M BW	–	–26	–	dBm
2530MHz	LTE band7 FDD 20M BW	–	–25	–	dBm
2550MHz	LTE band7 FDD 20M BW	–	–25	–	dBm
2570MHz	LTE band7 FDD 20M BW	–	–24	–	dBm
		π/4 DPSK (2 Mbps)			
2310Mhz	LTE band40 TDD 20M BW	–	–20	–	dBm
2330MHz	LTE band40 TDD 20M BW	–	–20	–	dBm
2350MHz	LTE band40 TDD 20M BW	–	–22	–	dBm
2370MHz	LTE band40 TDD 20M BW	–	–23	–	dBm
2510MHz	LTE band7 FDD 20M BW	–	–26	–	dBm
2530MHz	LTE band7 FDD 20M BW	–	–25	–	dBm
2550MHz	LTE band7 FDD 20M BW	–	–25	–	dBm
2570MHz	LTE band7 FDD 20M BW	–	–24	–	dBm
		8DPSK (3 Mbps)			
2310Mhz	LTE band40 TDD 20M BW	–	–21	–	dBm
2330MHz	LTE band40 TDD 20M BW	–	–21	–	dBm
2350MHz	LTE band40 TDD 20M BW	–	–23	–	dBm
2370MHz	LTE band40 TDD 20M BW	–	–24	–	dBm
2510MHz	LTE band7 FDD 20M BW	–	–26	–	dBm
2530MHz	LTE band7 FDD 20M BW	–	–25	–	dBm
2550MHz	LTE band7 FDD 20M BW	–	–25	–	dBm
2570MHz	LTE band7 FDD 20M BW	–	–24	–	dBm
Out-of-Band Blocking Performance, Modulated Interferer (Non-LTE)					
		GFSK (1 Mbps)[a]			
698–716 MHz	WCDMA	–	–13	–	dBm
776–849 MHz	WCDMA	–	–13	–	dBm
824–849 MHz	GSM850	–	–13	–	dBm
824–849 MHz	WCDMA	–	–13	–	dBm
880–915 MHz	E-GSM	–	–13	–	dBm
880–915 MHz	WCDMA	–	–13	–	dBm
1710–1785 MHz	GSM1800	–	–19	–	dBm
1710–1785 MHz	WCDMA	–	–19	–	dBm
1850–1910 MHz	GSM1900	–	–20	–	dBm

Table 33: Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
1850–1910 MHz	WCDMA	–	–20	–	dBm
1880–1920 MHz	TD-SCDMA	–	–20	–	dBm
1920–1980 MHz	WCDMA	–	–20	–	dBm
2010–2025 MHz	TD–SCDMA	–	–21	–	dBm
2500–2570 MHz	WCDMA	–	–23	–	dBm
	π/4 DPSK (2 Mbps)[a]				
698–716 MHz	WCDMA	–	–11	–	dBm
776–794 MHz	WCDMA	–	–11	–	dBm
824–849 MHz	GSM850	–	–12	–	dBm
824–849 MHz	WCDMA	–	–12	–	dBm
880–915 MHz	E-GSM	–	–12	–	dBm
880–915 MHz	WCDMA	–	–12	–	dBm
1710–1785 MHz	GSM1800	–	–17	–	dBm
1710–1785 MHz	WCDMA	–	–17	–	dBm
1850–1910 MHz	GSM1900	–	–19	–	dBm
1850–1910 MHz	WCDMA	–	–18	–	dBm
1880–1920 MHz	TD-SCDMA	–	–19	–	dBm
1920–1980 MHz	WCDMA	–	–19	–	dBm
2010–2025 MHz	TD-SCDMA	–	–21	–	dBm
2500–2570 MHz	WCDMA	–	–23	–	dBm
	8DPSK (3 Mbps)[a]				
698–716 MHz	WCDMA	–	–13	–	dBm
776–794 MHz	WCDMA	–	–12	–	dBm
824–849 MHz	GSM850	–	–13	–	dBm
824–849 MHz	WCDMA	–	–13	–	dBm
880–915 MHz	E-GSM	–	–13	–	dBm
880–915 MHz	WCDMA	–	–13	–	dBm
1710–1785 MHz	GSM1800	–	–18	–	dBm
1710–1785 MHz	WCDMA	–	–18	–	dBm
1850–1910 MHz	GSM1900	–	–20	–	dBm
1850–1910 MHz	WCDMA	–	–19	–	dBm
1880–1920 MHz	TD-SCDMA	–	–20	–	dBm
1920–1980 MHz	WCDMA	–	–20	–	dBm
2010–2025 MHz	TD-SCDMA	–	–21	–	dBm
2500–2570 MHz	WCDMA	–	–24	–	dBm
RX LO Leakage					
2.4 GHz band	–	–	–90.0	–80.0	dBm

Table 33: Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Spurious Emissions					
30 MHz–1 GHz		–	–95	–62	dBm
1–12.75 GHz		–	–70	–47	dBm
869–894 MHz		–	–147	–	dBm/Hz
925–960 MHz		–	–147	–	dBm/Hz
1805–1880 MHz		–	–147	–	dBm/Hz
1930–1990 MHz		–	–147	–	dBm/Hz
2110–2170 MHz		–	–147	–	dBm/Hz

a. The Bluetooth reference level for the required signal at the Bluetooth chip port is 3 dB higher than the typical sensitivity level.

Table 34: Bluetooth Transmitter RF Specifications[a]

Parameter	Conditions	Minimum	Typical	Maximum	Unit
General					
Frequency range		2402	–	2480	MHz
Basic rate (GFSK) TX power at Bluetooth		–	11.0	–	dBm
QPSK TX Power at Bluetooth		–	8.0	–	dBm
8PSK TX Power at Bluetooth		–	8.0	–	dBm
Power control step		2	4	8	dB
GFSK In-Band Spurious Emissions					
–20 dBc BW	–	–	.93	1	MHz
EDR In-Band Spurious Emissions					
1.0 MHz < |M – N| < 1.5 MHz	M – N = the frequency range for which the spurious emission is measured relative to the transmit center frequency.	–	–38	–26.0	dBc
1.5 MHz < |M – N| < 2.5 MHz		–	–31	–20.0	dBm
|M – N| ≥ 2.5 MHz[b]		–	–43	–40.0	dBm
Out-of-Band Spurious Emissions					
30 MHz to 1 GHz	–	–	–	–36.0 [c,d]	dBm
1 GHz to 12.75 GHz	–	–	–	–30.0 [d,e,f]	dBm
1.8 GHz to 1.9 GHz	–	–	–	–47.0	dBm
5.15 GHz to 5.3 GHz	–	–	–	–47.0	dBm
GPS Band Spurious Emissions					
Spurious emissions	–	–	–103	–	dBm
Out-of-Band Noise Floor[g]					
65–108 MHz	FM RX	–	–147	–	dBm/Hz
776–794 MHz	CDMA2000	–	–147	–	dBm/Hz
869–960 MHz	cdmaOne, GSM850	–	–147	–	dBm/Hz
925–960 MHz	E-GSM	–	–147	–	dBm/Hz
1570–1580 MHz	GPS	–	–146	–	dBm/Hz
1805–1880 MHz	GSM1800	–	–145	–	dBm/Hz
1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–144	–	dBm/Hz
2110–2170 MHz	WCDMA	–	–141	–	dBm/Hz

a. Unless otherwise specified, the specifications in this table are measured at the chip output port, and output power specifications are with the temperature correction algorithm and TSSI enabled.
b. Typically measured at an offset of ±3 MHz.
c. The maximum value represents the value required for Bluetooth qualification as defined in the v4.0 specification.
d. The spurious emissions during Idle mode are the same as specified in Table 34 on page 133.
e. Specified at the Bluetooth Antenna port.
f. Meets this specification using a front-end band-pass filter.
g. Transmitted power in cellular and FM bands at the Bluetooth Antenna port. See Figure 52 on page 128 for location of the port.

Table 35: Local Oscillator Performance

Parameter	Minimum	Typical	Maximum	Unit
LO Performance				
Lock time	–	72	–	µs
Initial carrier frequency tolerance	–	±25	±75	kHz
Frequency Drift				
DH1 packet	–	±8	±25	kHz
DH3 packet	–	±8	±40	kHz
DH5 packet	–	±8	±40	kHz
Drift rate	–	5	20	kHz/50 µs
Frequency Deviation				
00001111 sequence in payload[a]	140	155	175	kHz
10101010 sequence in payload[b]	115	140	–	kHz
Channel spacing	–	1	–	MHz

a. This pattern represents an average deviation in payload.
b. Pattern represents the maximum deviation in payload for 99.9% of all frequency deviations.

Table 36: BLE RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Frequency range	–	2402		2480	MHz
RX sense[a]	GFSK, 0.1% BER, 1 Mbps	–	–94.5	–	dBm
TX power[b]	–	–	8.5	–	dBm
Mod Char: delta f1 average	–	225	255	275	kHz
Mod Char: delta f2 max[c]	–	99.9	–	–	%
Mod Char: ratio	–	0.8	0.95	–	%

a. The Bluetooth tester is set so that Dirty TX is on.
b. BLE TX power can be increased to compensate for front-end losses such as BPF, diplexer, switch, and so forth). The output is capped at 12 dBm out. The BLE TX power at the antenna port cannot exceed the 10 dBm specification limit.
c. At least 99.9% of all delta F2 max frequency values recorded over 10 packets must be greater than 185 kHz.

Section 17: FM Receiver Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, limit values apply for the conditions specified inTable 30: “Environmental Ratings,” on page 125 and Table 32: “Recommended Operating Conditions and DC Characteristics,” on page 126. Typical values apply for the following conditions:

- VBAT = 3.6V
- Ambient temperature +25°C

Table 37: FM Receiver Specifications

Parameter	Conditions[a]	Minimum	Typical	Maximum	Units
RF Parameters					
Operating frequency[b]	Frequencies inclusive	65	–	108	MHz
Sensitivity[c]	FM only, SNR ≥ 26 dB	–	–0.5	–	dBµV EMF
		–	0.95	–	µV EMF
		–	–6.5	–	dBµV
Receiver adjacent channel selectivity[c,d]	Measured for 30 dB SNR at audio output. Signal of interest: 23 dBµV EMF (14.1 µV EMF)				
	At ±200 kHz.	–	51	–	dB
	At ±300 kHz.	–	62	–	dB
Intermediate signal plus noise-to-noise ratio (S + N)/N, stereo[c]	Vin = 20 dBµV (10 µV EMF)	45	53	–	dB
Intermodulation performance[c,d]	Blocker level increased until desired at 30 dB SNR Wanted Signal: 33 dBµV EMF (45 µV EMF) Modulated Interferer: At f_{Wanted} ± 400 kHz and ±4 MHz CW Interferer: At f_{Wanted} ± 800 kHz and ± 8 MHz	–	55	–	dBc
AM suppression, mono[c]	Vin = 23 dBµV EMF (14.1 µV EMF). AM at 400 Hz with m = 0.3. No A-weighted or any other filtering applied.	40	–	–	dB

Table 37: FM Receiver Specifications (Cont.)

Parameter	Conditions[a]	Minimum	Typical	Maximum	Units
RDS					
RDS sensitivity[e,f]	RDS deviation = 1.2 kHz	–	16	–	dBµV EMF
		–	6.3	–	µV EMF
		–	10	–	dBµV
	RDS deviation = 2 kHz	–	12	–	dBµV EMF
		–	4	–	µV EMF
		–	6	–	dBµV
RDS selectivity[f]	Wanted Signal: 33 dBµV EMF (45 µV EMF), 2 kHz RDS deviation Interferer: Δf = 40 kHz, fmod = 1 kHz				
	±200 kHz	–	49	–	dB
	±300 kHz	–	52	–	dB
	±400 kHz	–	52	–	dB
RF Input					
RF input impedance	–	1.5	–	–	kΩ
Antenna tuning cap	–	2.5	–	30	pF
Maximum input level[c]	SNR > 26 dB	–	–	113	dBµV EMF
		–	–	446	mV EMF
		–	–	107	dBµV
RF conducted emissions	Local oscillator breakthrough measured on the reference port	–	–	–55	dBm
	869–894 MHz, 925–960 MHz, 1805–1880 MHz, and 1930–1990 MHz. GPS.	–	–	–90	dBm

Table 37: FM Receiver Specifications (Cont.)

Parameter	Conditions[a]	Minimum	Typical	Maximum	Units
RF blocking levels at the FM antenna input with a 40 dB SNR (assumes a 50Ω input and excludes spurs)	GSM850, E-GSM (standard); BW = 0.2 MHz. 824–849 MHz, 880–915 MHz.	–	7	–	dBm
	GSM 850, E-GSM (edge); BW = 0.2 MHz. 824–849 MHz, 880–915 MHz.	–	0	–	dBm
	GSM DCS 1800, PCS 1900 (standard, edge); BW = 0.2 MHz. 1710–1785 MHz, 1850–1910 MHz.	–	12	–	dBm
	WCDMA: II (I), III (IV,X); BW = 5 MHz. 1710–1785 MHz (1710–1755 MHz, 1710–1770 MHz), 1850–1980 MHz (1920–1980 MHz).	–	12	–	dBm
	WCDMA: V (VI), VIII, XII, XIII, XIV; BW = 5 MHz. 824–849 MHz (830–840 MHz), 880–915 MHz.	–	5	–	dBm
	CDMA2000, CDMA One; BW = 1.25 MHz. 776–794 MHz, 824–849 MHz, 887–925 MHz.	–	0	–	dBm
	CDMA2000, CDMA One; BW= 1.25 MHz. 1750–1780 MHz, 1850–1910 MHz, 1920–1980 MHz.	–	12	–	dBm
	Bluetooth; BW = 1 MHz. 2402–2480 MHz.	–	11	–	dBm
	LTE, Band 38, Band 40, XGP Band	–	11	–	dBm
	WLAN-g/b; BW = 20 MHz. 2400–2483.5 MHz.	–	11	–	dBm
	WLAN-a; BW = 20 MHz. 4915–5825 MHz.	–	6	–	dBm
Tuning					
Frequency step	–	10	–	–	kHz
Settling time	Single frequency switch in any direction to a frequency within the 88–108 MHz or 76–90 MHz bands. Time measured to within 5 kHz of the final frequency.	–	150	–	µs
Search time	Total time for an automatic search to sweep from 88–108 MHz or 76–90 MHz (or in the reverse direction) assuming no channels are found.	–	–	8	sec

Table 37: FM Receiver Specifications (Cont.)

Parameter	Conditions[a]	Minimum	Typical	Maximum	Units
General Audio					
Audio output level[g]	–	–14.5	–	–12.5	dBFS
Maximum audio output level[h]	–	–	–	0	dBFS
DAC audio output level	Conditions: Vin = 66 dBµV EMF (2 mV EMF), Δf = 22.5 kHz, fmod = 1 kHz, Δf Pilot = 6.75 kHz	72	–	88	mVrms
Maximum DAC audio output level[h]	–	–	333	–	mVrms
Audio DAC output level difference[i]	–	–1	–	1	dB
Left and right AC mute	FM input signal fully muted with DAC enabled	60	–	–	dB
Left and right hard mute	FM input signal fully muted with DAC disabled	80	–	–	dB
Soft mute attenuation and start level	Muting is performed dynamically, proportional to the desired FM input signal C/N. The muting characteristic is fully programmable. See “Audio Features” on page 71.				
Maximum signal plus noise-to-noise ratio (S + N)/N, mono[i]	–	–	69	–	dB
Maximum signal plus noise-to-noise ratio (S + N)/N, stereo[g]	–	–	64	–	dB
Total harmonic distortion, mono	Vin = 66 dBµV EMF(2 mV EMF):				
	Δf = 75 kHz, fmod = 400 Hz.	–	–	0.8	%
	Δf = 75 kHz, fmod = 1 kHz.	–	–	0.8	%
	Δf = 75 kHz, fmod = 3 kHz.	–	–	0.8	%
	Δf = 100 kHz, fmod = 1 kHz.	–	–	1.0	%
Total harmonic distortion, stereo	Vin = 66 dBµV EMF (2 mV EMF), Δf = 67.5 kHz, fmod = 1 kHz, ∆f pilot = 6.75 kHz, L = R	–	–	1.5	%
Audio spurious products[i]	Range from 300 Hz to 15 kHz with respect to a 1 kHz tone.	–	–	–60	dBc
Audio bandwidth, upper (–3 dB point)	Vin = 66 dBµV EMF (2 mV EMF) Δf = 8 kHz, for 50 µs	15	–	–	kHz
Audio bandwidth, lower (–3 dB point)		–	–	20	Hz
Audio in-band ripple	100 Hz to 13 kHz, Vin = 66 dBµV EMF (2 mV EMF), Δf = 8 kHz, for 50 µs.	–0.5	–	0.5	dB
Deemphasis time constant tolerance	With respect to 50 and 75 µs.	–	–	±5	%

Table 37: FM Receiver Specifications (Cont.)

Parameter	Conditions[a]	Minimum	Typical	Maximum	Units
RSSI range	With 1 dB resolution and ±5 dB accuracy at room temperature.	3	–	83	dBµV EMF
		1.41	–	1.41E+4	µV EMF
		–3	–	77	dBµV
Stereo Decoder					
Stereo channel separation	Forced Stereo mode Vin = 66 dBµV EMF (2 mV EMF), Δf = 67.5 kHz, fmod = 1 kHz, △f Pilot = 6.75 kHz, R = 0, L = 1	–	48	–	dB
Mono stereo blend and switching	Dynamically proportional to the desired FM input signal C/N. The blending and switching characteristics are fully programmable. See "Audio Features" on page 71.				
Pilot suppression	Vin = 66 dBµV EMF (2 mV EMF), Δf = 75 kHz, fmod = 1 kHz.	46	–	–	dB
Pause Detection					
Audio level at which a pause is detected	Relative to 1-kHz tone, Δf = 22.5 kHz.	–	–	–	–
	4 values in 3 dB steps	–21	–	–12	dB
Audio pause duration	4 values	20	–	40	ms

a. The following conditions are applied to all relevant tests unless otherwise indicated: Preemphasis and deemphasis of 50 µs, R = L for mono, BAF = 300 Hz to 15 kHz, A-weighted filtering applied.
b. Contact your Broadcom representative for applications operating between 65–76 MHz.
c. Signal of interest: Δf = 22.5 kHz, fmod = 1 kHz.
d. Interferer: Δf = 22.5 kHz, fmod = 1 kHz.
e. RDS sensitivity numbers are for 87.5–108 MHz only.
f. Vin = Δf = 32 kHz, fmod = 1 kHz, Δf pilot = 7.5 kHz, and with an interferer for 95% of blocks decoded with no errors after correction, over a sample of 5000 blocks.
g. Vin = 66 dBµV EMF (2 mV EMF), Δf = 22.5 kHz, fmod = 1 kHz, Δf pilot = 6.75 kHz.
h. Vin = 66 dBµV EMF (2 mV EMF), Δf = 100 kHz, fmod = 1 kHz, Δf pilot = 6.75 kHz.
i. Vin = 66 dBµV EMF (2 mV EMF), Δf = 22.5 kHz, fmod = 1 kHz.

Section 18: WLAN RF Specifications

Introduction

The BCM43341 includes an integrated dual-band direct conversion radio that supports either the 2.4 GHz band or the 5 GHz band. The BCM43341 does not provide simultaneous 2.4 GHz and 5 GHz operation. This section describes the RF characteristics of the 2.4 GHz and 5 GHz portions of the radio.

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, limit values apply for the conditions specified inTable 30: “Environmental Ratings,” on page 125 and Table 32: “Recommended Operating Conditions and DC Characteristics,” on page 126. Typical values apply for the following conditions:

- VBAT = 3.6V
- Ambient temperature +25°C

Figure 53: WLAN Port Locations (5 GHz)

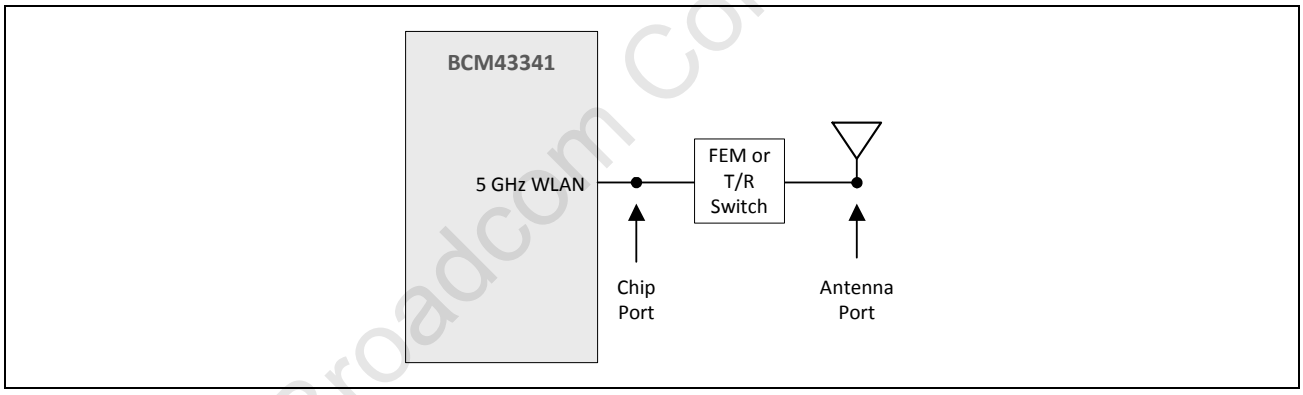
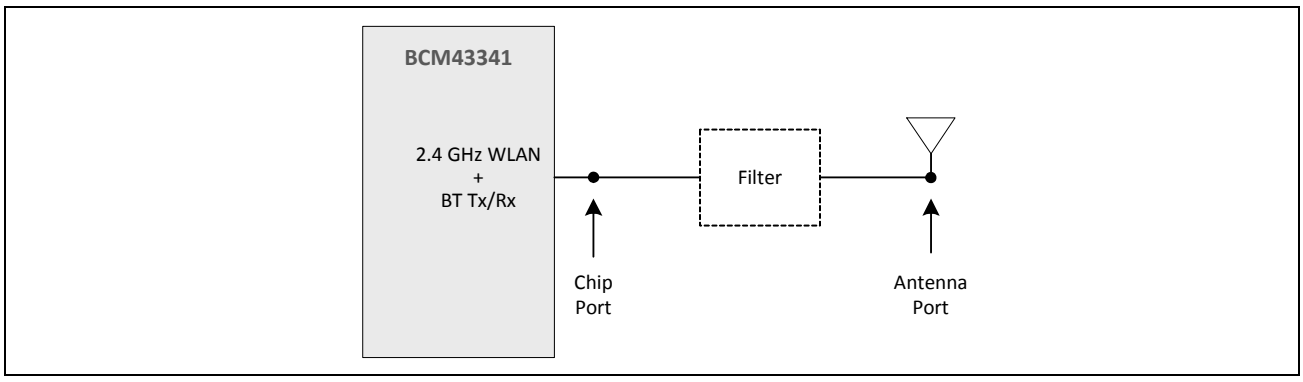


Figure 54: WLAN Port Locations (2.4 GHz)



Note: All WLAN specifications are measured at the chip port, unless otherwise specified.

2.4 GHz Band General RF Specifications

Table 38: 2.4 GHz Band General RF Specifications

Item	*Condition*	*Minimum*	*Typical*	*Maximum*	*Unit*
TX/RX switch time	Including TX ramp down	–	–	5	µs
RX/TX switch time	Including TX ramp up	–	–	2	µs
Power-up and power-down ramp time	DSSS/CCK modulations	–	–	< 2	µs

WLAN 2.4 GHz Receiver Performance Specifications

Note: The specifications in Table 39 are measured at the chip port, unless otherwise specified.

Table 39: WLAN 2.4 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Frequency range	–	2400	–	2500	MHz
RX sensitivity (8% PER for 1024 octet PSDU)[a]	1 Mbps DSSS	–	–99	–	dBm
	2 Mbps DSSS	–	–95	–	dBm
	5.5 Mbps CCK	–	–93	–	dBm
	11 Mbps CCK	–	–89	–	dBm
RX sensitivity (10% PER for 1024 octet PSDU)[a]	6 Mbps OFDM	–	–92	–	dBm
	9 Mbps OFDM	–	–92	–	dBm
	12 Mbps OFDM	–	–89	–	dBm
	18 Mbps OFDM	–	–87	–	dBm
	24 Mbps OFDM	–	–84	–	dBm
	36 Mbps OFDM	–	–82	–	dBm
	48 Mbps OFDM	–	–78	–	dBm
	54 Mbps OFDM	–	–77	–	dBm
RX sensitivity (10% PER for 4096 octet PSDU)[a,b.] Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates	(GF)			
	MCS0	–	–92	–	dBm
	13 Mbps MCS 1	–	–88	–	dBm
	6.5 Mbps MCS 2	–	–86	–	dBm
	MCS 3	–	–84	–	dBm
	MCS 4	–	–81	–	dBm
	MCS 5	–	–76	–	dBm
	MCS 6	–	–75	–	dBm
	MCS 7	–	–73	–	dBm
RX sensitivity (10% PER for 4096 octet PSDU)[a,b.] Defined for default parameters: GF, 800 ns GI, and non-STBC.	40 MHz channel spacing for all MCS rates	(GF)			
	MCS 0	–	–89	–	dBm
	MCS 1	–	–85	–	dBm
	MCS 2	–	–83	–	dBm
	MCS 3	–	–81	–	dBm
	MCS 4	–	–78	–	dBm
	MCS 5	–	–74	–	dBm
	MCS 6	–	–71	–	dBm
	MCS 7	–	–69	–	dBm

Table 39: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
RX sensitivity (10% PER for 4096 octet PSDU)[a,c.] Defined for default parameters: Mixed mode, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates (Mixed mode)					
	MCS0		–	–91.0	–	dBm
	MCS 1		–	–87.9	–	dBm
	MCS 2		–	–85.5	–	dBm
	MCS 3		–	–82.8	–	dBm
	MCS 4		–	–79.9	–	dBm
	MCS 5		–	–76.2	–	dBm
	MCS 6		–	–74.6	–	dBm
	MCS 7		–	–72.6	–	dBm
RX sensitivity (10% PER for 4096 octet PSDU)[a,b.] Defined for default parameters: Mixed mode, 800 ns GI, and non-STBC.	40 MHz channel spacing for all MCS rates (Mixed mode)					
	MCS 0		–	–89.0	–	dBm
	MCS 1		–	–85.4	–	dBm
	MCS 2		–	–83.2	–	dBm
	MCS 3		–	–80.6	–	dBm
	MCS 4		–	–77.4	–	dBm
	MCS 5		–	–72.3	–	dBm
	MCS 6		–	–70.6	–	dBm
	MCS 7		–	–69.0	–	dBm
Blocking level for 3dB RX sensitivity degradation (without external filtering)[d]	776–794 MHz	CDMA2000	–12.3	–	–	dBm
	824–849 MHz[e]	cdmaOne	–9.4	–	–	dBm
	824–849 MHz	GSM850	–2.7	–	–	dBm
	880–915 MHz	E-GSM	–3.4	–	–	dBm
	1710–1785 MHz	GSM1800	–9	–	–	dBm
	1850–1910 MHz	GSM1800	–8.8	–	–	dBm
	1850–1910 MHz	cdmaOne	–22.4	–	–	dBm
	1850–1910 MHz	WCDMA	–18.6	–	–	dBm
	1920–1980 MHz	WCDMA	–22.5	–	–	dBm
	2496–2690 MHz	LTE + 3 dB desense	–37.2	–	–	dBm
	2300–2400 MHz	LTE + 3 dB desense	–37.2	–	–	dBm
	2300–2370 MHz	LTE + 3 dB desense	–37.2	–	–	dBm
	2570–2620 MHz	LTE + 3 dB desense	–37.2	–	–	dBm
	2545–2575 MHz	LTE + 3 dB desense	–37.2	–	–	dBm
In-band static CW jammer immunity (fc – 8 MHz < fcw < + 8 MHz)	RX PER < 1%, 54 Mbps OFDM, 1000 octet PSDU for: (RxSens + 23 dB < Rxlevel < max input level)		–80	–	–	dBm

Table 39: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Input In-Band IP3[a]	Maximum LNA gain		–	–15.5	–	dBm
	Minimum LNA gain		–	–1.5	–	dBm
Maximum Receive Level @ 2.4 GHz	@ 1, 2 Mbps (8% PER, 1024 octets)		–3.5	–	–	dBm
	@ 5.5, 11 Mbps (8% PER, 1024 octets)		–9.5	–	–	dBm
	@ 6–54 Mbps (10% PER, 1024 octets)		–19.5	–	–	dBm
	@ MCS0–7 rates (10% PER, 4095 octets)		–19.5	–	–	dBm
LPF 3 dB Bandwidth	–		9	–	10	MHz
Adjacent channel rejection-DSSS (Difference between interfering and desired signal at 8% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	***Desired and interfering signal 30 MHz apart***					
	1 Mbps DSSS	–74 dBm	35	–	–	dB
	2 Mbps DSSS	–74 dBm	35	–	–	dB
	Desired and interfering signal 25 MHz apart					
	5.5 Mbps DSSS	–70 dBm	35	–	–	dB
	11 Mbps DSSS	–70 dBm	35	–	–	dB
Adjacent channel rejection-OFDM (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
Adjacent channel rejection MCS0–7 (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/ Notes)	MCS7	–61 dBm	–2	–	–	dB
	MCS6	–62 dBm	–1	–	–	dB
	MCS5	–63 dBm	0	–	–	dB
	MCS4	–67 dBm	4	–	–	dB
	MCS3	–71 dBm	8	–	–	dB
	MCS2	–74 dBm	11	–	–	dB
	MCS1	–76 dBm	13	–	–	dB
	MCS0	–79 dBm	16	–	–	dB
Maximum receiver gain	–	–	–	105	–	dB
Gain control step	–	–	–	3	–	dB
RSSI accuracy[f]	Range –98 dBm to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB
Return loss	Z_o = 50Ω, across the dynamic range		6	10	–	dB
Receiver cascaded NF	At maximum gain		–	3.5	–	

a. Derate by 1.5 dB for –30 °C to –10°C and 55°C to 85°C.
b. Sensitivity degradations for alternate settings in MCS modes. MM: 0.5 dB drop, SGI: 2 dB drop, and STBC: 0.75 dB drop.

c. Sensitivity degradations for alternate settings in MCS modes. MM: 0.5 dB drop, SGI: 2 dB drop, and STBC: 0.75 dB drop.
d. The cellular standard listed for each band indicates the type of modulation used to generate the interfering signal in that band for the purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.
e. The blocking levels are valid for channels 1 to 11. (For higher channels, the performance may be lower due to third harmonic signals (3 × 824 MHz) falling within band.)
f. The minimum and maximum values shown have a 95% confidence level.

WLAN 2.4 GHz Transmitter Performance Specifications

Note: The specifications in Table 40 are measured at the chip port output, unless otherwise specified.

Table 40: WLAN 2.4 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		2400	–	2500	MHz
Transmitted power in cellular and FM bands (–18 dBm at the antenna port, 90% duty cycle, OFDM)[a]	76–108 MHz	FM RX	–	–166	–	dBm/Hz
	776–794 MHz	CDMA2000	–	–166	–	dBm/Hz
	869–960 MHz	cdmaOne, GSM850	–	–165	–	dBm/Hz
	925–960 MHz	E-GSM	–	–165	–	dBm/Hz
	1570–1580 MHz	GPS	–	–155	–	dBm/Hz
	1805–1880 MHz	GSM1800	–	–147	–	dBm/Hz
	1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–141	–	dBm/Hz
	2010–2170 MHz	WCDMA	–	–138	–	dBm/Hz
	2400–2483 MHz	BT/WLAN	–	–	–	dBm/Hz
	2.4 GHz	GPS/ GLONASS	–	–147	–	dBm/MHz
	2.4 GHz	2170 MHz band	–	–131		dBm/MHz
	2.4 GHz	LTE Band 40	–	–109		dBm/Hz
	2.4 GHz	LTE Band 7	–	–121		dBm/Hz
	2.4 GHz	LTE Band 38	–	–115		dBm/Hz
	2.4 GHz	LTE Band 41	–	–104		dBm/Hz
	2.4 GHz	LTE Band XGP	–	–110		dBm/Hz
Harmonic level (at 18 dBm with 100% duty cycle)	4.8–5.0 GHz	2nd harmonic	–	–	–48.4	dBm/1 MHz
	7.2–7.5 GHz	3rd harmonic	–	–	–56.9	dBm/1 MHz
TX power at chip port for highest power level setting at 25°C, VBAT = 3.6V, spectral mask and EVM compliance[b]	1 Mbps DSSS	0 dBm	–	20	–	dBm
	6 Mbps	–3 dBm	–	19.5	–	dBm
	54 Mbps	–6 dBm	–	18	–	dBm
	MCS7 (20 MHz)		–	16.5	–	dBm
	MCS7 (40 MHz)		–	16.5	–	dBm
	MCS7 (20 MHz, SGI)		–	16.5	–	dBm
	MCS7 (40 MHz, SGI)		–	16.5	–	dBm
Phase noise	37.4 MHz Crystal, Integrated from 10 kHz to 10 MHz		–	0.5	–	Degrees

Table 40: WLAN 2.4 GHz Transmitter Performance Specifications (Cont.)

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
TX power control dynamic range	–	30	–	–	dB
Carrier suppression	–	15	–	–	dBc
Gain control step	–	–	0.25	–	dB
Return loss at Chip port TX	Z_o = 50Ω	4	6	–	dB

a. The cellular standards listed indicate only typical usages of that band in some countries. Other standards may also be used within those bands.
b. Derate by 2 dB for –30°C to –10°C and 55°C to 85°C.

WLAN 5 GHz Receiver Performance Specifications

Note: The specifications in Table 41 are measured at the chip port input, unless otherwise specified.

Table 41: WLAN 5 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Frequency range	–	4900	–	5845	MHz
RX sensitivity (10% PER for 1000 octet PSDU)[a]	6 Mbps OFDM	–	–90.5	–	dBm
	9 Mbps OFDM	–	–90.5	–	dBm
	12 Mbps OFDM	–	–87.5	–	dBm
	18 Mbps OFDM	–	–85.5	–	dBm
	24 Mbps OFDM	–	–82.5	–	dBm
	36 Mbps OFDM	–	–80.5	–	dBm
	48 Mbps OFDM	–	–76.5	–	dBm
	54 Mbps OFDM	–	–73.5	–	dBm
RX sensitivity (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates (GF)				
	MCS 0	–	–90.5	–	dBm
	MCS 1	–	–86.5	–	dBm
	MCS 2	–	–84.5	–	dBm
	MCS 3	–	–82.5	–	dBm
	MCS 4	–	–78.5	–	dBm
	MCS 5	–	–73.5	–	dBm
	MCS 6	–	–71.5	–	dBm
	MCS 7	–	–70.5	–	dBm
RX sensitivity (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, and non-STBC.	40 MHz channel spacing for all MCS rates (GF)				
	MCS 0	–	–87.5	–	dBm
	MCS 1	–	–84.5	–	dBm
	MCS 2	–	–81.5	–	dBm
	MCS 3	–	–80.5	–	dBm
	MCS 4	–	–76.5	–	dBm
	MCS 5	–	–71.5	–	dBm
	MCS 6	–	–69.5	–	dBm
	MCS 7	–	–68.5	–	dBm

Table 41: WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
RX sensitivity (10% PER for 4096 octet PSDU)[a] Defined for default parameters: Mixed mode, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates (Mixed mode)					
	MCS 0		–	–89.5	–	dBm
	MCS 1		–	–86.4	–	dBm
	MCS 2		–	–84.0	–	dBm
	MCS 3		–	–81.3	–	dBm
	MCS 4		–	–78.4	–	dBm
	MCS 5		–	–74.7	–	dBm
	MCS 6		–	–73.1	–	dBm
	MCS 7		–	–71.1	–	dBm
RX sensitivity (10% PER for 4096 octet PSDU)[a] Defined for default parameters: Mixed mode, 800 ns GI, and non-STBC.	40 MHz channel spacing for all MCS rates (Mixed mode)					
	MCS 0		–	–87.5	–	dBm
	MCS 1		–	–83.9	–	dBm
	MCS 2		–	–81.7	–	dBm
	MCS 3		–	–79.1	–	dBm
	MCS 4		–	–75.9	–	dBm
	MCS 5		–	–70.8	–	dBm
	MCS 6		–	–69.1	–	dBm
	MCS 7		–	–67.5	–	dBm
Blocking level for 1 dB RX sensitivity degradation (without external filtering)[b]	776–794 MHz	CDMA2000	–21	–	–	dBm
	824–849 MHz	cdmaOne	–20	–	–	dBm
	824–849 MHz	GSM850	–12	–	–	dBm
	880–915 MHz	E-GSM	–12	–	–	dBm
	1710–1785 MHz	GSM1800	–15	–	–	dBm
	1850–1910 MHz	GSM1800	–15	–	–	dBm
	1850–1910 MHz	cdmaOne	–20	–	–	dBm
	1850–1910 MHz	WCDMA	–24	–	–	dBm
	1920–1980 MHz	WCDMA	–24	–	–	dBm
Input In-Band IP3[a]	Maximum LNA gain		–	–15.5	–	dBm
	Minimum LNA gain		–	–1.5	–	dBm
Maximum receive level @ 5.24 GHz	@ 6, 9, 12 Mbps		–29.5	–	–	dBm
	@ 18, 24, 36, 48, 54 Mbps		–29.5	–	–	dBm
LPF 3 dB bandwidth	–		9	–	18	MHz

Table 41: WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Adjacent channel rejection (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
	65 Mbps OFDM	–61 dBm	–2	–	–	dB
Alternate adjacent channel rejection (Difference between interfering and desired signal (40 MHz apart) at 10% PER for 1000[c] octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–78.5 dBm	32	–	–	dB
	9 Mbps OFDM	–77.5 dBm	31	–	–	dB
	12 Mbps OFDM	–75.5 dBm	29	–	–	dB
	18 Mbps OFDM	–73.5 dBm	27	–	–	dB
	24 Mbps OFDM	–70.5 dBm	24	–	–	dB
	36 Mbps OFDM	–66.5 dBm	20	–	–	dB
	48 Mbps OFDM	–62.5 dBm	16	–	–	dB
	54 Mbps OFDM	–61.5 dBm	15	–	–	dB
	65 Mbps OFDM	–60.5 dBm	14	–	–	dB
Maximum receiver gain	–		–	100	–	dB
Gain control step	–		–	3	–	dB
RSSI accuracy[d]	Range –98 dBm to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB
Return loss	Z_o = 50Ω		6	10	–	dB
Receiver cascaded noise figure	At maximum gain		–	5.0	–	dB

a. Derate by 1.5 dB for –30 °C to –10°C and 55°C to 85°C.
b. The cellular standard listed for each band indicates the type of modulation used to generate the interfering signal in that band for the purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.
c. For 65 Mbps, the size is 4096.
d. The minimum and maximum values shown have a 95% confidence level.

WLAN 5 GHz Transmitter Performance Specifications

Note: The specifications in Table 42 are measured at the chip port, unless otherwise specified.

Table 42: WLAN 5 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		4900	–	5845	MHz
Transmitted power in cellular and FM bands (–18 dBm at the antenna port, >90% duty cycle, OFDM)[a]	76–108 MHz	FM RX	–	< –168	–	dBm/Hz
	776–794 MHz	–	–	–168	–	dBm/Hz
	869–960 MHz	cdmaOne, GSM850	–	–170	–	dBm/Hz
	925–960 MHz	E-GSM	–	–170	–	dBm/Hz
	1570–1580 MHz	GPS	–	–168	–	dBm/Hz
	1805–1880 MHz	GSM1800	–	–169	–	dBm/Hz
	1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–169	–	dBm/Hz
	2110–2170 MHz	WCDMA	–	–169	–	dBm/Hz
	2400–2483 MHz	BT/WLAN	–	–166	–	dBm/Hz
	2300–2690	LTE	–	–167	–	dBm/Hz
Harmonic level (at 17 dBm)	9.8–11.570 GHz	2nd harmonic	–	–48.6	–	dBm/MHz
TX power at chip port for highest power level setting at 25°C, VBAT = 3.6V, spectral mask and EVM compliance[b]	6 Mbps		–	19	–	dBm
	54 Mbps		–	17	–	dBm
	MCS0 (20 MHz)		–	19.5	–	dBm
	MCS7 (20 MHz)		–	16.5	–	dBm
	MCS7 (40 MHz)		–	16.5	–	dBm
	MCS7 (20 MHz, SGI)		–	16.5	–	dBm
	MCS7 (40 MHz, SGI)		–	16.5	–	dBm
Phase noise	37.4 MHz crystal, Integrated from 10 kHz to 10 MHz		–	0.7	–	Degrees
TX power control dynamic range	–		30	–	–	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB
Return loss	Z_o = 50Ω		–	6	–	dB

a. The cellular standards listed indicate only typical usages of that band in some countries. Other standards may also be used within those bands.
b. Derate by 2 dB for –30°C to –10°C and 55°C to 85°C.

General Spurious Emissions Specifications

Table 43: General Spurious Emissions Specifications

Parameter	*Condition/Notes*		*Min*	*Typ*	*Max*	*Unit*
Frequency range	–		2400	–	2500	MHz
General Spurious Emissions						
TX Emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–	–62	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–	–47	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–	–53	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–	–53	dBm
RX/standby Emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–78	–63	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–68.5[a]	–53	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–96	–53	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–96	–53	dBm

a. For frequencies other than 3.2 GHz, the emissions value is –96 dBm. The value presented in table is the result of LO leakage at 3.2 GHz.

Section 19: Internal Regulator Electrical Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Functional operation is not guaranteed outside of the specification limits provided in this section.

Core Buck Switching Regulator

Table 44: Core Buck Switching Regulator (CBUCK) Specifications

Specification	Notes	Min	Typ	Max	Units
Input supply voltage (DC), VBAT	DC voltage range inclusive of disturbances.	2.9	3.6	4.8[a]	V
PWM mode switching frequency, Fsw	Forced PWM without FLL enabled.	2.8	4	5.2	MHz
	Forced PWM with FLL enabled.	3.6	4	4.4	MHz
PWM output current	–	–	–	372[b]	mA
Output current limit	–	–	1390	–	mA
Output voltage range	Programmable, 30 mV steps. Default = 1.35V (bits = 0000).	1.2	1.35	1.5	Volts
PWM output voltage DC accuracy	Includes load and line regulation. Forced PWM mode.	–4	–	4	%
	Total DC accuracy after trim.	–2	–	2	%
PWM ripple voltage, static	Measure with 20 MHz BW limit. Static Load. Max ripple based on: VBAT < 4.8V, Vout = 1.35V, Fsw = 4 MHz, 2.2 µH inductor, L > 1.05 µH, capacitor + Board total-ESR < 20 mΩ, Cout > 1.9 µF, ESL < 200 pH.	–	7	20	mVpp
PWM mode peak efficiency (Peak efficiency is at 200 mA load. The following conditions apply to all inductor types: Forced PWM, 200 mA, Vout = 1.35V, VBAT = 3.6V, Fsw = 4 MHz, at 25°C.)	2.5 x 2 mm LQM2HPN2R2NG0, L = 2 µH, DCR = 80 mΩ ±25%, ACR < 1Ω.	79	85	–	%
	0805-size LQM21PN2R2NGC, L = 2.1 µH, DCR=230 mΩ ±25%, ACR < 2Ω.	78	84	–	%
	0603-size MIPSTZ1608D2R2B, L = 1 µH, DCR = 240 mΩ ±25%, ACR < 2Ω.	74	81	–	%

Table 44: Core Buck Switching Regulator (CBUCK) Specifications (Cont.)

Specification	Notes	Min	Typ	Max	Units
PFM mode efficiency	10 mA load current, Vout = 1.35V, VBAT = 3.6V, 20C Cap + Board total-ESR < 20 mΩ, Cout = 4.7 µF, ESL < 200 pH, FLL= OFF 0603-size MIPSTZ1608D2R2B, L = 2.2 µH, DCR = 240 mΩ ±25%, ACR < 2Ω.	67	77	–	%
LPOM efficiency	1 mA load current, Vout = 1.35V, VBAT = 3.6V, 20C Cap + board total-ESR < 20 mΩ, Cout = 4.7 µF, ESL < 200 pH, FLL = OFF 0603-size MIPSTZ1608D2R2B, L = 2.2 µH, DCR = 240Ω ±25%, ACR < 2Ω.	55	65	–	%
Start-up time from power down	VIO already on and steady. Time from REG_ON rising edge to CLDO reaching 1.2V. Includes 256 µsec typical Vddc_ok_o delay.	–	903	1106	µs
External inductor, L[c]	–	–	2.2	–	µH
External output capacitor, Cout[c]	Ceramic, X5R, 0402, ESR < 30 mΩ at 4 MHz, ±20%, 6.3V, 4.7 µF, Murata® GRM155R60J475M	2[d]	4.7	–	µF
External input capacitor, Cin[c]	For SR_VDDBATP5V pin. Ceramic, X5R, 0603, ESR < 30 mΩ at 4 MHz, ±20%, 6.3V, 4.7 µF, Murata GRM155R60J475M.	0.67[d]	4.7	–	µF
Input supply voltage ramp-up time	0 to 4.3V	40	–	100,000	µs

a. The maximum continuous voltage is 4.8V. Voltages up to 5.5V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
b. At junction temperature 125°C.
c. Refer to *PCB Layout Guidelines and Component Selection for Optimized PMU Performance* (4334-AN200-R) for component selection details.
d. The minimum value refers to the residual capacitor value after taking into account part-to-part tolerance, DC-bias, temperature, and aging.

3.3V LDO (LDO3P3)

Table 45: LDO3P3 Specifications

Parameters	*Conditions*	*Min.*	*Typ.*	*Max.*	*Units*
Input supply voltage, Vin	Minimum = Vo+0.2V = 3.5V (for Vo = 3.3V) dropout voltage requirement must be met under max load for performance specs.	2.9	3.6	4.8	V
Nominal output voltage, Vo	Default = 3.3V	–	3.3	–	V
Output voltage programmability	Range	2.4	–	3.4	V
	Accuracy at any step (including Line/Load regulation), load > 0.1 mA	–5		+5	%
Dropout voltage	At maximum load	–	–	200	mV
Output current	–	0.001	–	450	mA
Quiescent current	No load; Vin = Vo + 0.2V	–	66	85	µA
	Maximum load @ 450mA; Vin = Vo + 0.2V		4	4.5	mA
Leakage current	Powerdown mode (at 85°C junction temperature)	–	1.5	5	µA
Line regulation	Vin from (Vo + 0.2V) to 4.8V, maximum load	–		3.5	mV/V
Load regulation	load from 1–450 mA, Vin = 3.6V	–	0.3	0.45	mV/mA
Load step error	Load from 1mA-200mA-400mA in 1 q5s and 400mA-200mA-1mA in 1 µs; Vin ≥ (Vo + 0.2V); Co = 4.7 µF	–	–	70	mV
PSRR	VBAT ≥ 3.6V, Vo = 3.3V, Co = 4.7 µF, maximum load, 100 Hz to 100 kHz	20	–	–	dB
LDO turn-on time	LDO turn-on time when rest of chip is up	–	160	250	µs
Output current limit	–	–	800		mA
In-rush current	Vin = Vo + 0.2V to 4.8V, Co = 4.7 µF, no load	–		280	mA
External output capacitor, Co	Ceramic, X5R, 0402, (ESR: 5m-240mohm), ±10%, 10V	1.0	4.7	5.64	µF
External input capacitor	For SR_VDDBATA5V pin (shared with Bandgap) ceramic, X5R, 0402, ±10%, 10V. Not needed if sharing VBAT cap 4.7 µF with SR_VDDBATP5V.	–	4.7	–	µF

2.5V LDO (LDO2P5)

Table 46: LDO2P5 Specifications

Specification	Notes	Min.	Typ.	Max.	Unit
Input supply voltage	Min= 2.52+0.15=2.67V Dropout voltage requirement must be met under the maximum load for performance specifications.	2.9	3.6	4.8	V
Output current	–	–	–	70	mA
Output voltage, Vo	default = 2.52V	2.4	2.52	3.4	V
Dropout voltage	at max load			150	mV
Output voltage DC Accuracy	include Line/Load regulation	–5		+5	%
Quiescent current	No load	–	8	–	µA
Line regulation	Vin from (Vo + 0.15V) to 4.8V, maximum load	–11		11	mV
Load Regulation	Load from 1–70 mA (subject to parasitic resistance of package and board). Vin = 2.52 + 0.15V to 4.8V	–	15	31	mV
Leakage current	Powerdown mode. At Junction Temp 85°C	–	–	5	µA
PSRR	VBAT ≥ 3.6V, Vo = 2.52V, Co = 2.2 µF, maximum load, 100 Hz to 100 kHz	20	–	–	dB
LDO turn-on time	LDO turn-on time when rest of chip is up	–	–	260	µs
In-rush current during turn-on	from its output capacitor in fully-discharged state	–	–	100	mA
External output capacitor, Co	Ceramic, X5R, 0402, (ESR: 5m-240mohm), ±20%, 6.3V	0.7[a]	2.2	2.64	µF
External input capacitor	For SR_VDDBATA5V pin (shared with Bandgap) ceramic, X5R, 0402, ±10%, 10V. Not needed if sharing the VBAT capacitor 4.7 µF with SR_VDDBATP5V.	–	1	–	µF

a. Minimum cap value refers to residual cap value after taking into account part–to–part tolerance, DC–bias, temperature, aging

HSICDVDD LDO

Table 47: HISCDVDD LDO Specifications

Specification	Notes	Min	Typ	Max	Units
Input supply voltage	Min = 1.2V + 0.1V = 1.3V. Dropout voltage requirement must be met under maximum load for performance specifications.	1.3	1.35	1.5	V
Output current	–	–	–	80	mA
Output voltage, V_o	Step size 25 mV. Default = 1.2V.	1.1	1.2	1.275	V
Dropout voltage	At maximum load. Includes 100 mΩ routing resistors at input and output.	–	–	100	mV
Output voltage DC accuracy	Including line/load regulation.	–4	–	4	%
Quiescent current	No load. Dependent on programming. ldo_cntl_i[43], ldo_cntl_i[41] to support different external capacitor loads.	–	182	–	µA
PSRR at 1 kHz	Input ≥ 1.35V, 50 to 300 pF, V_o = 1.2V		–	–	
	Load: 80 mA	24			dB
	Load: 40 mA	39			dB
PSRR at 10 kHz	Input ≥ 1.35V, 50 to 300 pF, V_o = 1.2V		–	–	
	Load: 80 mA	24			dB
	Load: 40 mA	38			dB
PSRR at 100 kHz	Input ≥ 1.35V, 50 to 300 pF, V_o = 1.2V		–	–	
	Load: 80 mA	15			dB
	Load: 40 mA	27			dB
Output Capacitor, C_o	Internal capacitor = Sum of supply decoupling caps and supply-to-ground routing parasitic capacitance. Output capacitor dependent on programming.	–	1000	–	pF

CLDO

Table 48: CLDO Specifications

Specification	Notes	Min	Typ	Max	Units
Input supply voltage, V_{in}	Min = 1.2 + 0.1V = 1.3V. Dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output current	–	0.1	–	150	mA
Output voltage, V_o	Programmable in 25 mV steps. Default = 1.2V, load from 0.1–150 mA	1.1	1.2	1.275	V
Dropout voltage	At max load	–	–	100	mV
Output voltage DC accuracy[a]	Includes line/load regulation	–4	–	+4	%
	After trim, load from 0.1–150 mA, includes line/load regulation. $V_{in} > V_o + 0.1V$.	–2	–	+2	%
Quiescent current	No load	–	10	–	µA
Line regulation	V_{in} from (V_o + 0.1V) to 1.5V, maximum load	–	–	7	mV/V
Load regulation	Load from 1 mA to 150 mA	–	15	25	µV/mA
Leakage current	Power-down	–	–	10	µA
PSRR	@1 kHz, Vin ≥ 1.5V, C_o = 1 µF	20	–		dB
Start-up time of PMU	VIO up and steady. Time from the REG_ON rising edge to the CLDO reaching 1.2V. Includes 256 µs vddc_ok_o delay.	–	–	1106	µs
LDO turn-on time	Chip already powered up.	–	–	180	µs
In-rush current during turn-on	From its output capacitor in a fully-discharged state	–	–	150	mA
External output capacitor, C_o[b]	Total ESR: 30 mΩ–200 mΩ	0.67[c]	1	–	µF
External input capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from the CBUCK output. Total ESR (trace/capacitor): 30 mΩ–200 mΩ	–	1	–	µF

a. Load from 0.1 to 150 mA.
b. Refer to *PCB Layout Guidelines and Component Selection for Optimized PMU Performance* (4334-AN200-R) for component selection details.
c. The minimum value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

LNLDO

Table 49: LNLDO Specifications

Specification	*Notes*	*Min*	*Typ*	*Max*	*Units*
Input supply voltage, Vin	Min = $1.2V_o$ + 0.1V = 1.3V. Dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output current	–	0.1	–	104	mA
Output voltage, V_o	Programmable in 25 mV steps. Default = 1.2V	1.1	1.2	1.275	V
Dropout voltage	At maximum load	–	–	100	mV
Output voltage DC accuracy[a]	includes line/load regulation, load from 0.1 to 150 mA	–4	–	+4	%
Quiescent current	No load	–	44	–	µA
Line regulation	V_{in} from (V_o + 0.1V) to 1.5V, max load	–	–	7	mV/V
Load regulation	Load from 1 mA to 104 mA	–	15	25	µV/mA
Leakage current	Power-down	–	–	10	µA
Output noise	@30 kHz, 60 mA load, C_o = 1 µF @100 kHz, 60 mA load, C_o = 1 µF	–	–	60 35	nV/root-Hz nV/root-Hz
PSRR	@ 1kHz, input > 1.3V, C_o= 1 µF, V_o = 1.2V	20	–	–	dB
Start-up time of PMU	VIO up and steady. Time from the REG_ON rising edge to the LNLDO reaching 1.2V. Includes 256 µs vddc_ok_o delay.	–	–	1106	µs
LDO turn-on time	Chip already powered up.	–	–	180	µs
In-rush current during turn-on	From its output capacitor in a fully-discharged state	–	–	150	mA
External output capacitor, C_o[b]	Total ESR (trace/capacitor): 30–200 mΩ	0.67[c]	1	–	µF
External input capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from the CBUCK output. Total ESR (trace/capacitor): 30–200 mΩ	–	1	–	µF

a. Load from 0.1 to 104 mA.
b. Refer to *PCB Layout Guidelines and Component Selection for Optimized PMU Performance* (4334-AN200-R) for component selection details.
c. The minimum value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

Section 20: System Power Consumption

Note:

- Values in this data sheet are design goals and are subject to change based on the results of device characterization.
- Unless otherwise stated, these values apply for the conditions specified in Table 32: "Recommended Operating Conditions and DC Characteristics," on page 126.

WLAN Current Consumption

The WLAN current consumption measurements are shown in Table 50.

All values in Table 50 are with the Bluetooth and NFC cores in reset (that is, Bluetooth, NFC, and FM are off).

Table 50: Typical WLAN Power Consumption

Mode	Bandwidth (MHz)	Band (GHz)	VBAT = 3.6V, VDDIO = 1.8V, T_A 25°C	
			VBAT (mA)	Vio[a] (µA)
Sleep Modes				
Leakage (OFF)	–	–	0.004	220
SLEEP[b]	–	–	0.005	220
IEEE Power Save, DTIM 1[c]	–	–	1.06	220
IEEE Power Save DTIM 3[d]	–	–	0.321	220
Active Modes				
RX (Listen)[e, f]	–	–	44.4	200
RX (Active)[f, g, h]	–	–	57.7	200
TX CCK, 11 Mbps (20.5 dBm @ chip)[h, i, j]	HT20	2.4	325	200
TX, MCS7 (17.5 dBm @ chip)[h, i, j]	HT20	2.4	254	200
TX, MCS7 (17.5 dBm @ chip)[h, i, j]	HT40	2.4	270	200
TX OFDM, 54 Mbps (18 dBm @ chip)[h, i, j]	HT20	2.4	263	200
TX, MCS7 (15 dBm @ chip)[h, i, j]	HT20	5	261	200
TX, MCS7 (15 dBm @ chip)[h, i, j]	HT40	5	283	200
TX OFDM, 54 Mbps (16 dBm @ chip)[h, i, j]	HT20	5	271	200

a. Vio is specified with all pins idle and not driving any loads.
b. Idle between beacons.
c. Beacon interval = 100 ms; beacon duration = 1.9 ms @ 1Mbps (Integrated Sleep + wakeup + beacon)
d. Beacon interval = 300 ms; beacon duration = 1.9 ms @ 1Mbps (Integrated Sleep + wakeup + beacon)
e. Carrier sense (CCA) when no carrier present.
f. Carrier sense (CS) detect/packet RX.

g. Applicable to all supported rates.
h. Duty Cycle = 100%
i. TX output power is measured at the chip-out side.
j. The items of active modes are measured under the real association/throughput with the wireless AP.

Bluetooth, BLE, and FM Current Consumption

The Bluetooth and FM current consumption measurements are shown in Table 51.

Note:

- The WLAN and NFC cores are in reset (WL_REG_ON = low) for all measurements provided in Table 51.
- For FM measurements, the Bluetooth core is in Sleep mode.
- The BT current consumption numbers are measured based on GFSK TX output power = 8 dBm.

Table 51: Bluetooth and FM Current Consumption

Operating Mode	*VBAT (3.6V)*	*VDDIO (1.8V)*	*Unit*
Sleep	6	133	µA
SCO HV3 master	10.1	–	mA
3DH5/3DH1 master	18.1	–	mA
DM1/DH1 master	22.9	–	mA
DM3/DH3 master	27.0	–	mA
DM5/DH5 master	28.3	–	mA
2EV3	7.5	0.1	mA
FMRX I^2S audio	6.7	–	mA
BLE scan[a]	169	131	µA
BLE connected (1 second)	43	132	µA

a. No devices present; 1.28 second interval with a scan window of 11.25 ms.

NFC Typical Current Consumption

Note:

- The current consumption values in Table 52 are provisional. These values will be updated after additional data is available. The values are typical for a specific version of the firmware configuration.
- The WLAN, BT, and FM cores are in reset for all measurements provided in Table 52.

Table 52: NFC Current Consumption Figures[a]

Mode	*Description*	*Settings*	*Conditions*	*Typical Current from V_{BATT}*	*Unit*
Shutdown	NFC_REG_PU = Low	–	–	3.813	µA
Sleep	–	–	–	86.975	µA
Snooze standby	Background current drain when in-between poll events: listening for incoming carrier.	–	Digital LDO on, carrier detector on, internal LPO timer running to provide periodic wake-up.	87.533	µA
Polling (peak current)[b]	During Mode Switch Polling. The peak current during the time that the chip is generating a field (for example, during the 38 ms when polling for NFC-A, B, and F).	High Supply Mode during poll (VDDA_CAP = 2.5V) TX pin signal nominally 1.6V pk-pk	R_L = 36Ω	185.70	mA
			R_L = 16.2Ω	211.72	mA
			R_L = 12.1Ω	229.38	mA
			R_L = 8Ω	257.36	mA
Low Power Target Detection (averaged current during LPTD operation)[b]	LPTD algorithm “sniffing” for approximately 50 µs, 3 times per second (depends on level of analog LDO in-rush). Snooze mode in-between sniffs.	High Supply Mode during LPTD “sniff” (VDDA_CAP = 2.5V)	R_L = 8Ω	938.361[c]	µA
Target Mode	CE and P2P Target Mode operation during a transaction.	–	–	12.209	mA
CE_Level_4	Standby (register retention and carrier detector on).	–	–	10.904	µA
	CE transaction with UICC: Full battery powered.	–	Excludes 5 mA typically required for SE and 1 mA SWP signaling.	12.12	mA

Table 52: NFC Current Consumption Figures[a] (Cont.)

Mode	Description	Settings	Conditions	Typical Current from V_{BATT}	Unit
CE_Level_3	Standby (register retention and carrier detector on).	–	–	10.893	µA
	CE transaction with UICC: Using residual battery power.	–	Excludes 5 mA typically required for SE and 1 mA SWP signaling.	12.147	mA
CE_Level_2	Standby (register retention only).	–	–	10.78	µA
	CE transaction with UICC: all except registers powered by field.	–	–	61.207	µA
CE_Level_1	Standby and CE transaction with UICC: everything powered by field.	–	–	–	µA

a. The values in this table were measured on TBA.
b. During initiator mode, when the device is generating the carrier field, the VBAT supply current will be heavily dependent on the antenna drive output current. The antenna drive TX pin current is a function of the internal supply mode, the internal amplifier gain settings for the output signal swing, and the effective impedance of the antenna network. The High/Low Supply Mode and associated output signal swing is given in the “Settings” column and the antenna load is represented by an AC coupled resistive load RL, given in the “Conditions” column.
c. Depending on setup.

Section 21: Interface Timing and AC Characteristics

SDIO/gSPI Timing

SDIO Default Mode Timing

SDIO default mode timing is shown by the combination of Figure 55 and Table 53.

Figure 55: SDIO Bus Timing (Default Mode)

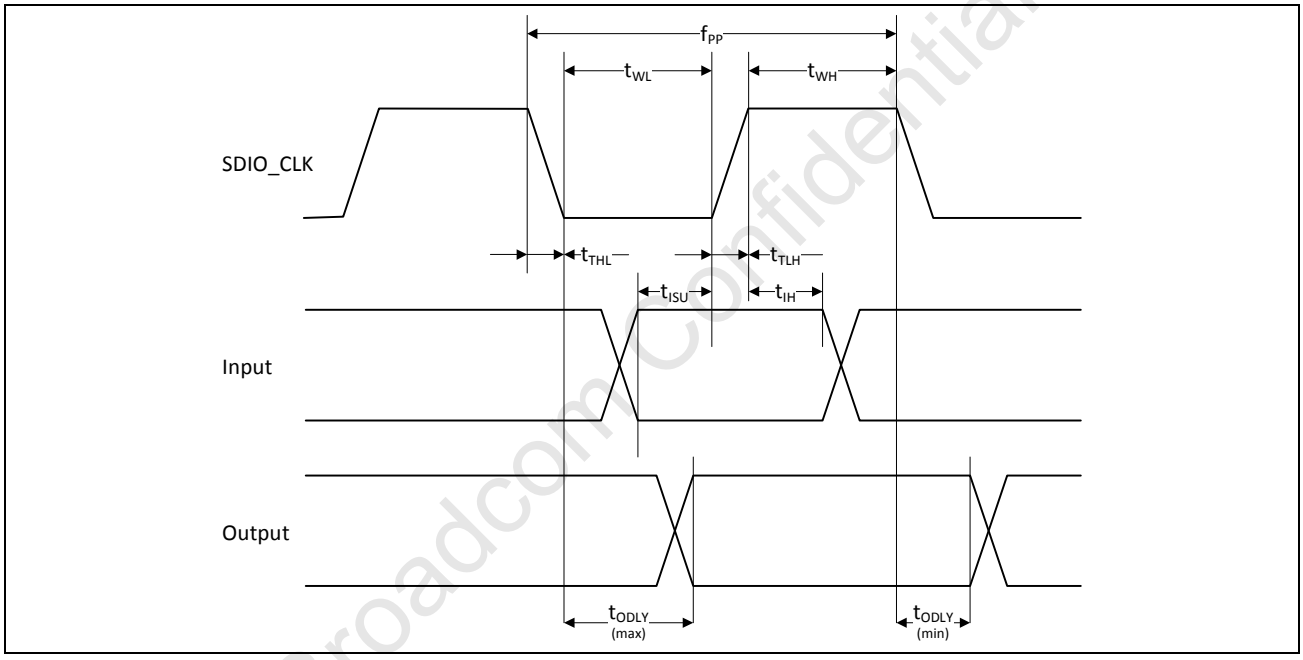


Table 53: SDIO Bus Timing[a] Parameters (Default Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer mode	fPP	0	–	25	MHz
Frequency – Identification mode	fOD	0	–	400	kHz
Clock low time	tWL	10	–	–	ns
Clock high time	tWH	10	–	–	ns
Clock rise time	tTLH	–	–	10	ns
Clock low time	tTHL	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					

Table 53: SDIO Bus Timing[a] Parameters (Default Mode) (Cont.)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input setup time	tISU	5	–	–	ns
Input hold time	tIH	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	–	14	ns
Output delay time – Identification mode	tODLY	0	–	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

SDIO High-Speed Mode Timing

SDIO high-speed mode timing is shown by the combination of Figure 56 and Table 54.

Figure 56: SDIO Bus Timing (High-Speed Mode)

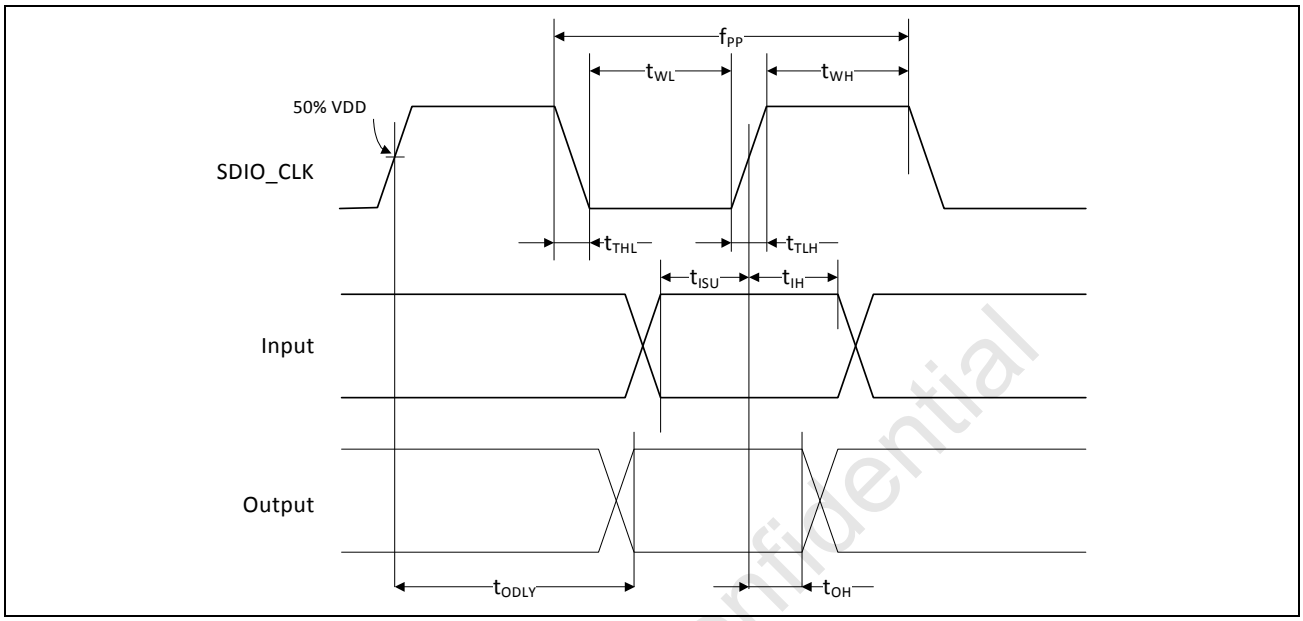


Table 54: SDIO Bus Timing[a] Parameters (High-Speed Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (all values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer Mode	fPP	0	–	50	MHz
Frequency – Identification Mode	fOD	0	–	400	kHz
Clock low time	tWL	7	–	–	ns
Clock high time	tWH	7	–	–	ns
Clock rise time	tTLH	–	–	3	ns
Clock low time	tTHL	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	tISU	6	–	–	ns
Input hold Time	tIH	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	tODLY	–	–	14	ns
Output hold time	tOH	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

gSPI Signal Timing

The gSPI host and device always use the rising edge of clock to sample data.

Figure 57: gSPI Timing

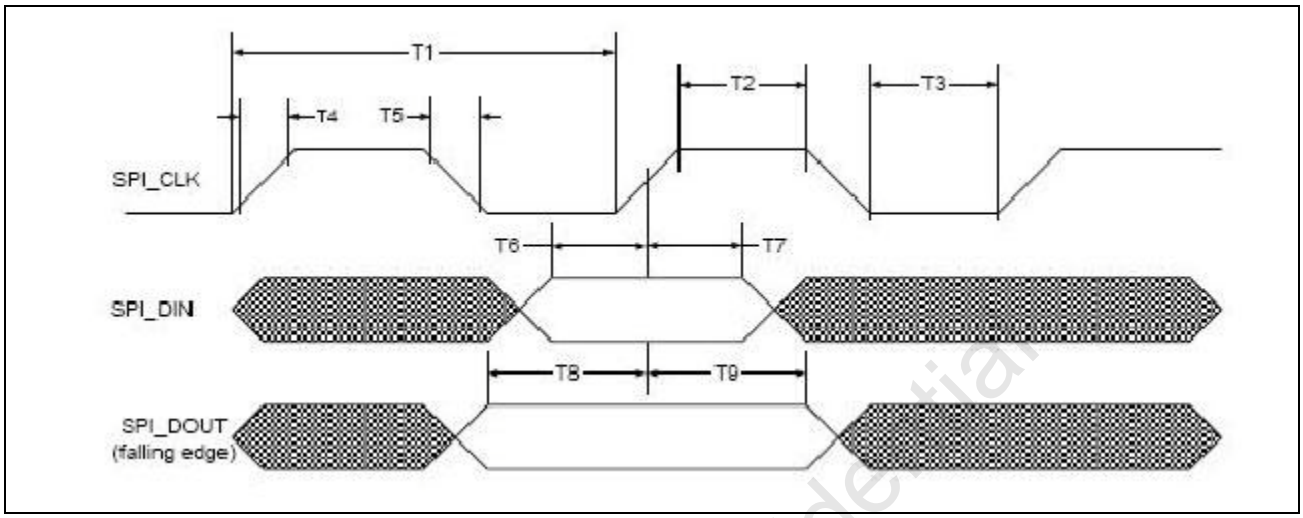


Table 55: gSPI Timing Parameters

Parameter	*Symbol*	*Minimum*	*Maximum*	*Units*	*Note*
Clock period	T1	20.8	–	ns	F_{max} = 48 MHz
Clock high/low	T2/T3	(0.45 × T1) – T4	(0.55 × T1) – T4	ns	–
Clock rise/fall time[a]	T4/T5	–	2.5	ns	Measured from 10% to 90% of VDDIO
Input setup time	T6	5.0	–	ns	Setup time, SIMO valid to SPI_CLK active edge
Input hold time	T7	5.0	–	ns	Hold time, SPI_CLK active edge to SIMO invalid
Output setup time	T8	5.0	–	ns	Setup time, SOMI valid before SPI_CLK rising
Output hold time	T9	5.0	–	ns	Hold time, SPI_CLK active edge to SOMI invalid
CSX to clock[b]	–	7.86	–	ns	CSX fall to 1st rising edge
Clock to CSX[a]	–	–	–	ns	Last falling edge to CSX high

a. Limit applies when SPI_CLK = Fmax. For slower clock speeds, longer rise/fall times are acceptable provided that the transitions are monotonic and the setup and hold time limits are complied with.
b. SPI_CSx remains active for entire duration of gSPI read/write/write-read transaction (overall words for multiple-word transaction)

HSIC Interface Specifications

Table 56: HSIC Timing Parameters

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*	*Comments*
HSIC signaling voltage	V_{DD}	1.1	1.2	1.3	V	–
I/O voltage input low	V_{IL}	–0.3	–	0.35 × V_{DD}	V	–
I/O Voltage input high	V_{IH}	0.65 × V_{DD}	–	V_{DD} + 0.3	V	–
I/O voltage output low	V_{OL}	–	–	0.25 × V_{DD}	V	–
I/O voltage output high	V_{OH}	0.75 × V_{DD}	–	–	V	–
I/O pad drive strength	O_D	40	–	60	Ω	Controlled output impedance driver
I/O weak keepers	I_L	20	–	70	µA	–
I/O input impedance	Z_I	100	–	–	kΩ	–
Total capacitive load[a]	C_L	3	–	14	pF	–
Characteristic trace impedance	T_I	45	50	55	Ω	–
Circuit board trace length	T_L	–	–	10	cm	–
Circuit board trace propagation skew[b]	T_S	–	–	15	ps	–
STROBE frequency[c]	F_{STROBE}	239.988	240	240.012	MHz	± 500 ppm
Slew rate (rise and fall) STROBE and DATA[C]	T_{slew}	0.60 × V_{DD}	1.0	1.2	V/ns	Averaged from 30% ~ 70% points
Receiver data setup time (with respect to STROBE)[c]	T_s	300	–	–	ps	Measured at the 50% point
Receiver data hold time (with respect to STROBE)[c]	T_b	300	–	–	ps	Measured at the 50% point

a. Total Capacitive Load (C_L), includes device Input/Output capacitance, and capacitance of a 50Ω PCB trace with a length of 10 cm.
b. Maximum propagation delay skew in STROBE or DATA with respect to each other. The trace delay should be matched between STROBE and DATA to ensure that the signal timing is within specification limits at the receiver.
c. Jitter and duty cycle are not separately specified parameters, they are incorporated into the values in the table above.

JTAG Timing

Table 57: JTAG Timing Characteristics

Signal Name	Period	Output Maximum	Output Minimum	Setup	Hold
TCK	125 ns	–	–	–	–
TDI	–	–	–	20 ns	0 ns
TMS	–	–	–	20 ns	0 ns
TDO	–	100 ns	0 ns	–	–
$\overline{\text{JTAG\_TRST}}$	250 ns	–	–	–	–

Section 22: Power-Up Sequence and Timing

Sequencing of Reset and Regulator Control Signals

The BCM43341 has three signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states (see Figure 58, Figure 59 on page 171, and Figure 60 and Figure 61 on page 172). The timing values indicated are minimum required values; longer delays are also acceptable.

Note:

- The WL_REG_ON and BT_REG_ON signals are ORed in the BCM43341. The diagrams show both signals going high at the same time (as would be the case if both REG signals were controlled by a single host GPIO). If two independent host GPIOs are used (one for WL_REG_ON and one for BT_REG_ON), then only one of the two signals needs to be high to enable the BCM43341 regulators.
- The reset requirements for the Bluetooth core are also applicable for the FM core. In other words, if FM is to be used, then the Bluetooth core must be enabled.
- The BCM43341 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold (see Table 32: “Recommended Operating Conditions and DC Characteristics,” on page 126). Wait at least 150 ms after VDDC and VDDIO are available before initiating SDIO accesses.
- VBAT should not rise faster than 40 µs. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

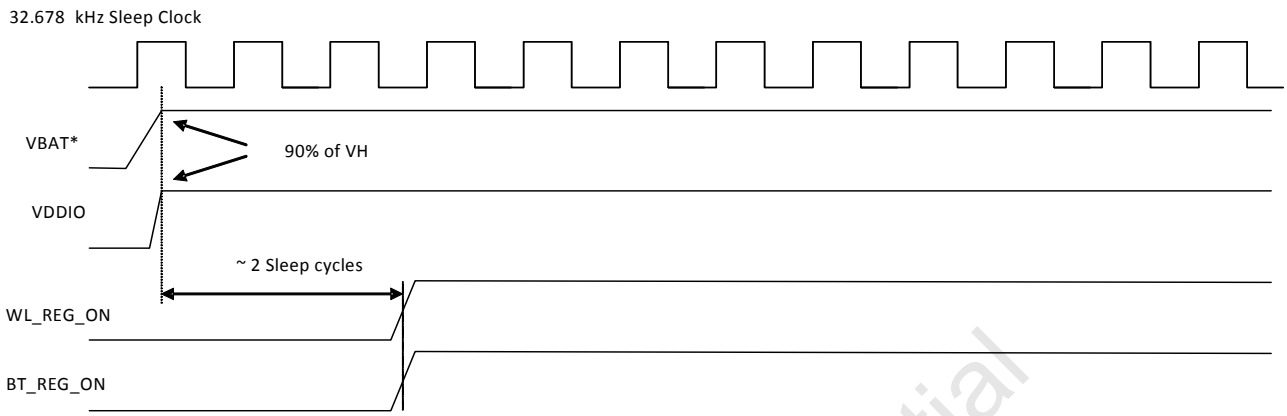
Description of Control Signals

- **WL_REG_ON**: Used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal BCM43341 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.
- **BT_REG_ON**: Used by the PMU (OR-gated with WL_REG_ON) to power up the internal BCM43341 regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset.

Note: For both the WL_REG_ON and BT_REG_ON pins, there should be at least a 10 msec time delay between consecutive toggles (where both signals have been driven low). This is to allow time for the CBUCK regulator to discharge. If this delay is not followed, then there may be a VDDIO in-rush current on the order of 36 mA during the next PMU cold start.

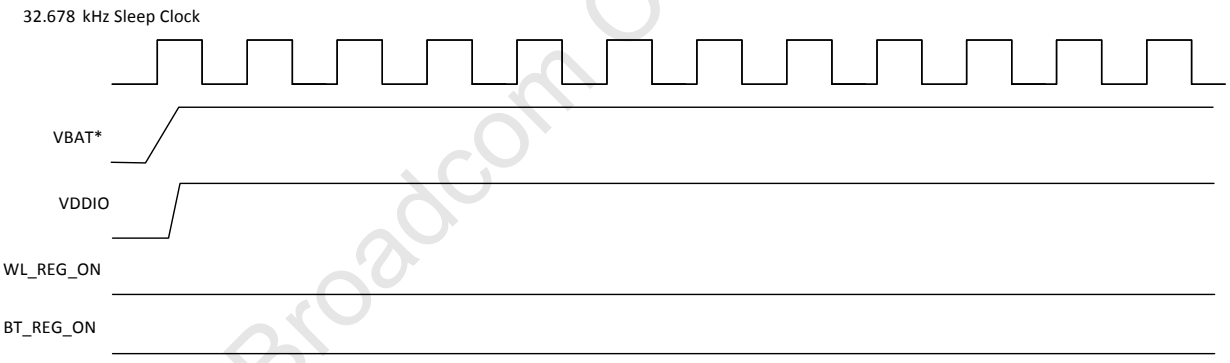
Control Signal Timing Diagrams

Figure 58: WLAN = ON, Bluetooth = ON



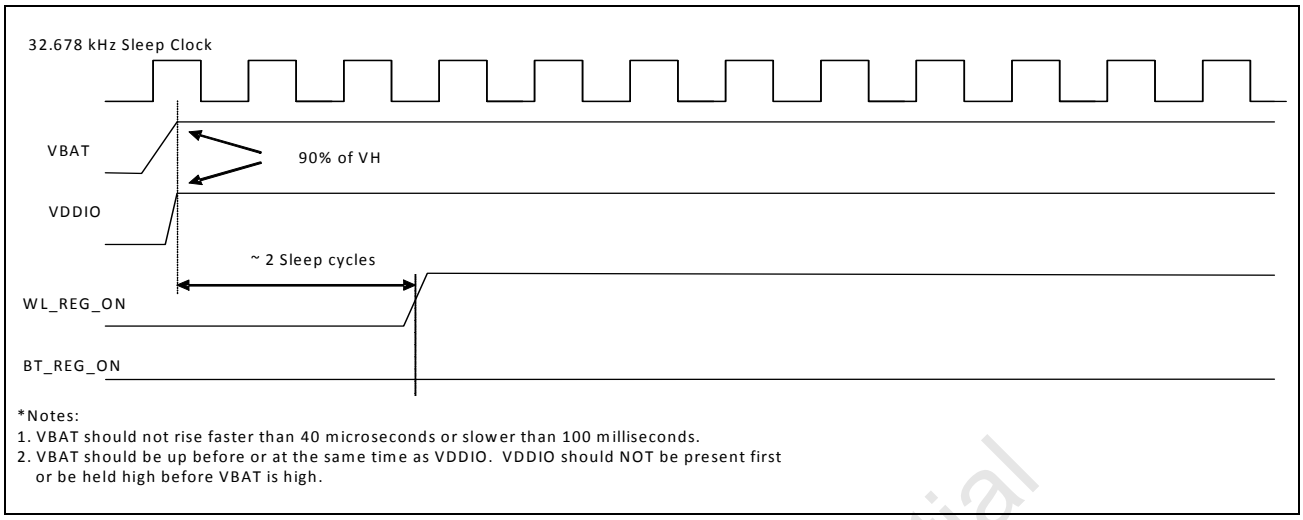
*Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 59: WLAN = OFF, Bluetooth = OFF



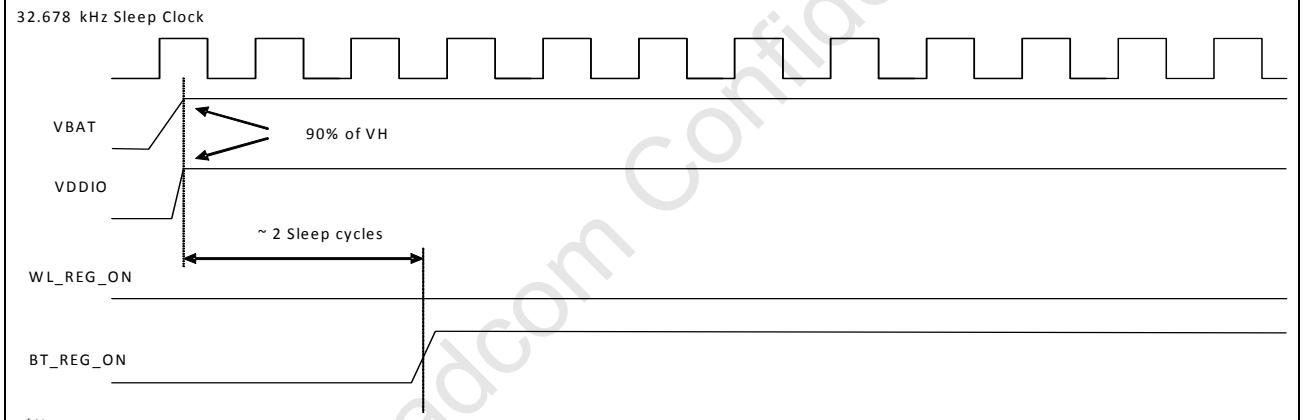
*Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 60: WLAN = ON, Bluetooth = OFF



*Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 61: WLAN = OFF, Bluetooth = ON



*Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Section 23: NFC Antenna Interface

Overview

The BCM43341 supports a 2-pin antenna interface, which requires minimal external components, none of which are active. Figure 20 and Figure 21 show two recommended interface circuit topologies.

Figure 62: Recommended Antenna Interface Circuit (1 of 2)

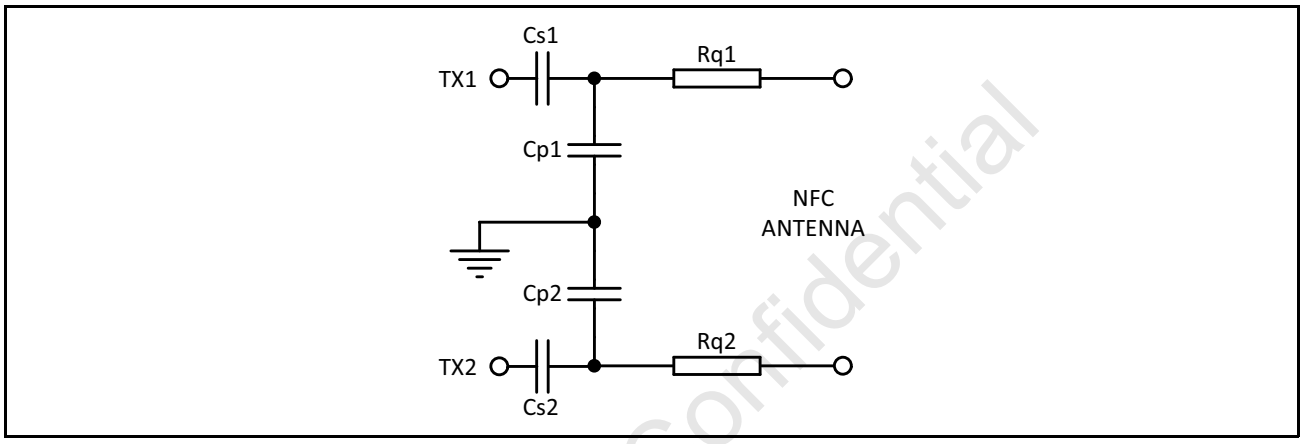
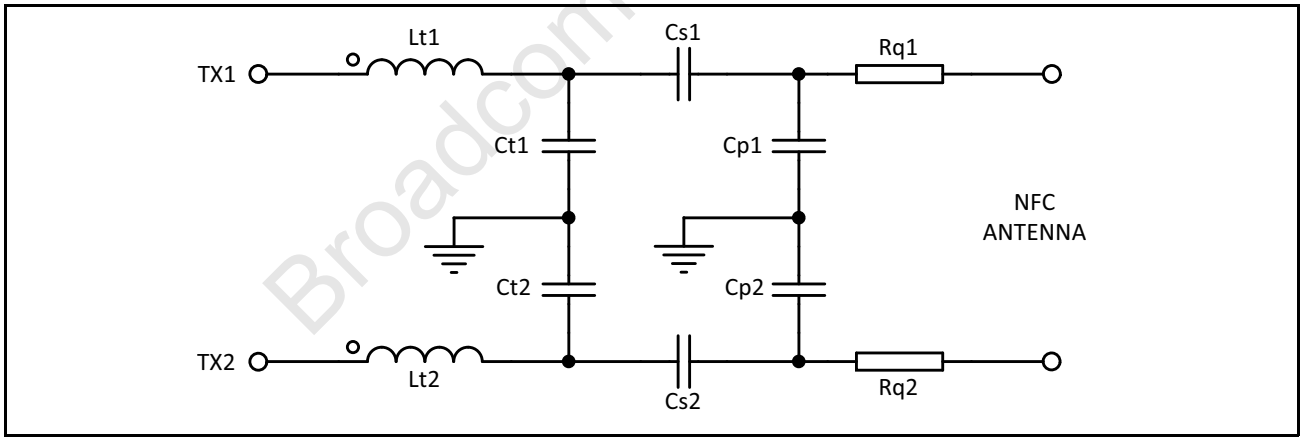


Figure 63: Recommended Antenna Interface Circuit (2 of 2)



Note: Work with your local Broadcom representative when selecting an antenna design to gain Applications support and for guidance on component values.

Section 24: Package Information

Package Thermal Characteristics

Table 58: Package Thermal Characteristics[a]

Characteristic	*WLBGA*
θ_{JA} (°C/W) (value in still air)	36.8
θ_{JB} (°C/W)	5.93
θ_{JC} (°C/W)	2.82
Ψ_{JT} (°C/W)	9.26
Ψ_{JB} (°C/W)	16.93
Maximum Junction Temperature T_j	114.08
Maximum Power Dissipation (W)	1.198

a. No heat sink, TA = 70°C. This is an estimate, based on a 4-layer PCB that conforms to EIA/JESD51–7 (101.6 mm × 101.6 mm × 1.6 mm) and P = 1.198W continuous dissipation.

Junction Temperature Estimation and PSI_{JT} Versus $THETA_{JC}$

Package thermal characterization parameter PSI–J_T (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) versus using the junction-to-case thermal resistance parameter Theta–J_C (θ_{JC}). The reason for this is that θ_{JC} assumes that all the power is dissipated through the top surface of the package case. In actual applications, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is:

$$T_J = T_T + P \times \Psi_{JT}$$

Where:

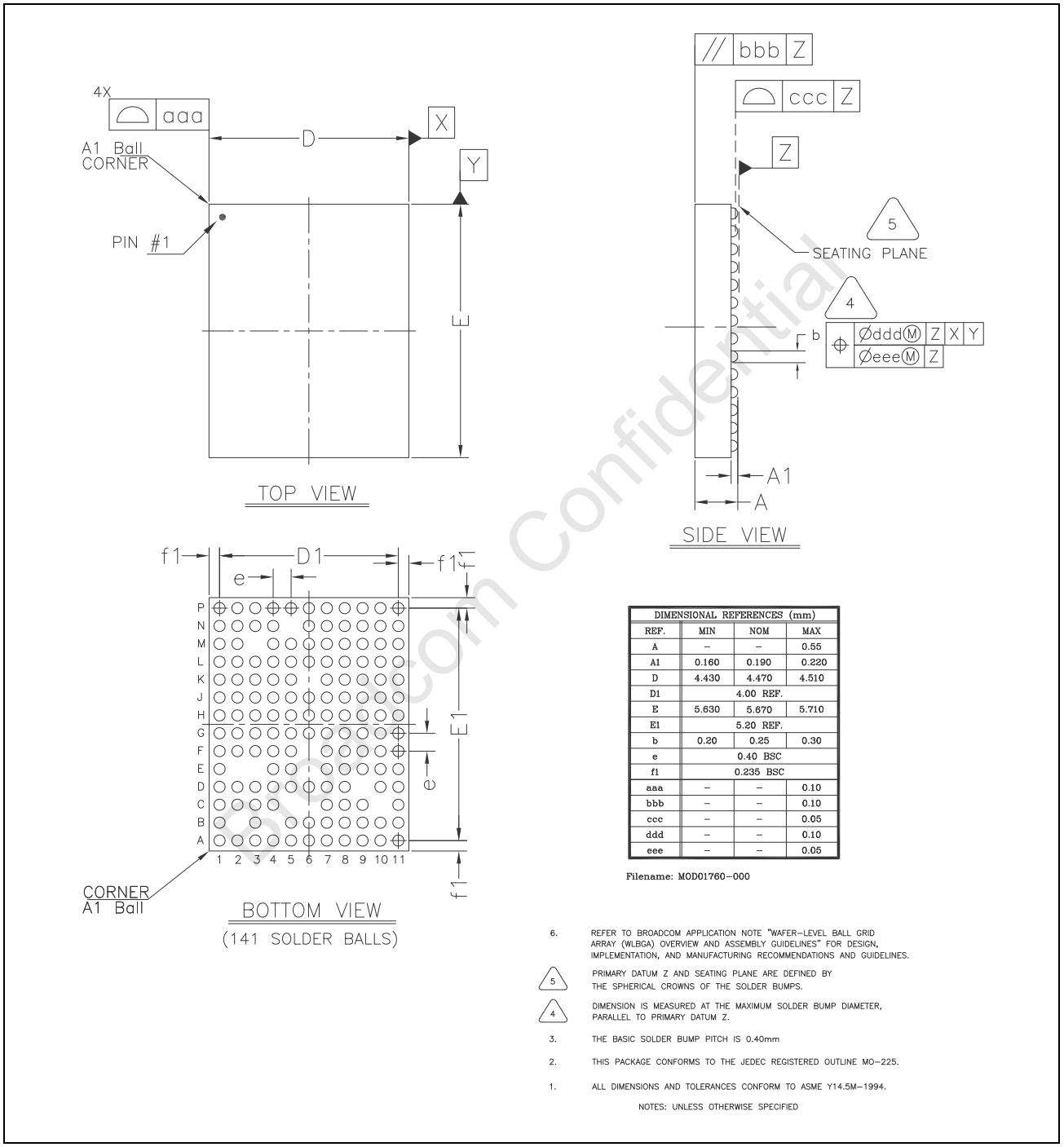
- T_J = Junction temperature at steady-state condition (°C)
- T_T = Package case top center temperature at steady-state condition (°C)
- P = Device power dissipation (Watts)
- Ψ_{JT} = Package thermal characteristics; no airflow (°C/W)

Environmental Characteristics

For environmental characteristics data, see Table 30: “Environmental Ratings,” on page 125.

Section 25: Mechanical Information

Figure 64: 141-Ball WLBGA Package Mechanical Information



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	0.55
A1	0.160	0.190	0.220
D	4.430	4.470	4.510
D1		4.00 REF.	
E	5.630	5.670	5.710
E1		5.20 REF.	
b	0.20	0.25	0.30
e		0.40 BSC	
f1		0.235 BSC	
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.05
ddd	–	–	0.10
eee	–	–	0.05

Filename: MOD01760–000

6. REFER TO BROADCOM APPLICATION NOTE "WAFER–LEVEL BALL GRID ARRAY (WLBGA) OVERVIEW AND ASSEMBLY GUIDELINES" FOR DESIGN, IMPLEMENTATION, AND MANUFACTURING RECOMMENDATIONS AND GUIDELINES.

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BUMPS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BUMP DIAMETER, PARALLEL TO PRIMARY DATUM Z.

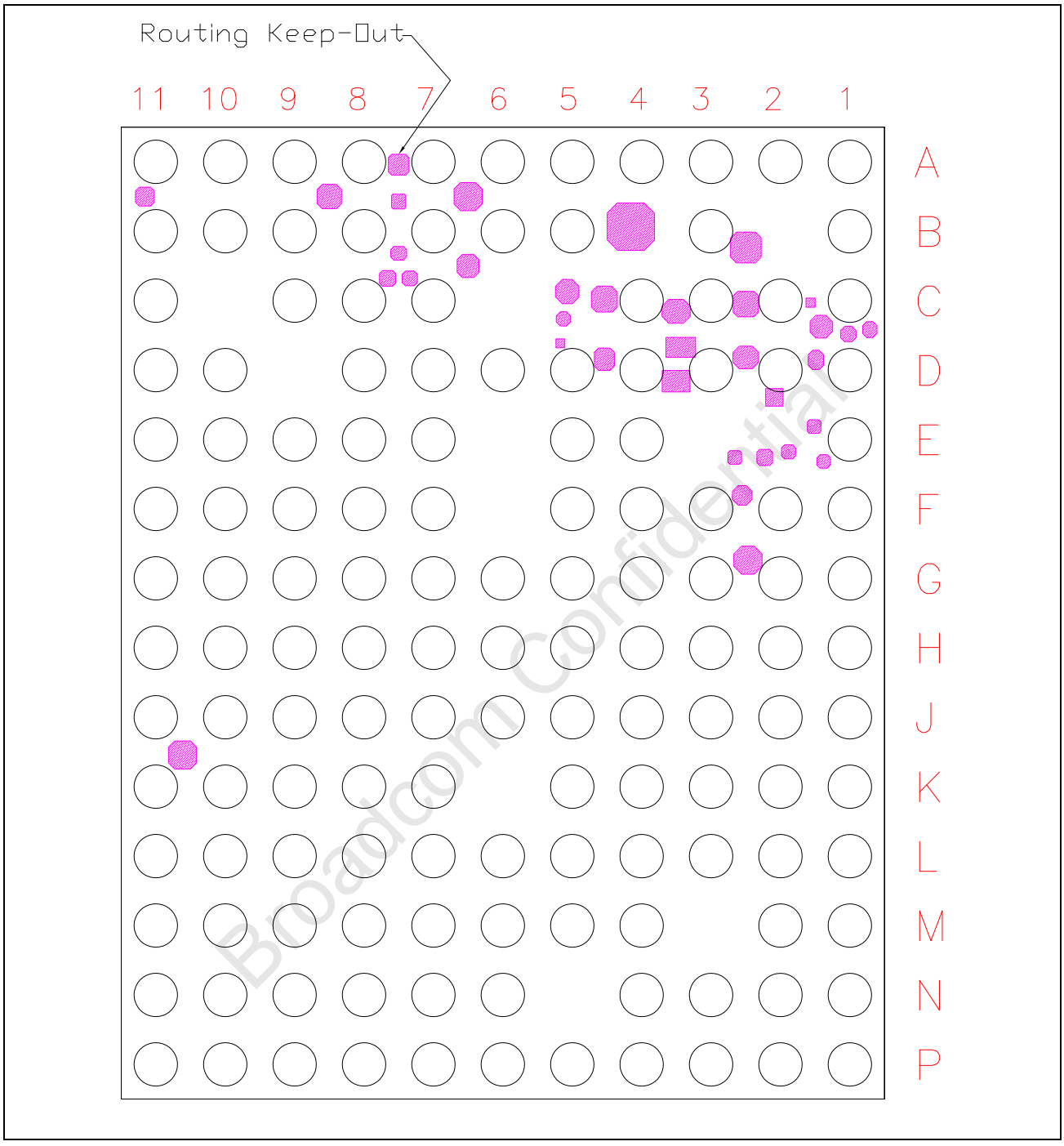
3. THE BASIC SOLDER BUMP PITCH IS 0.40mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO–225.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 65: WLBGA Keep-Out Areas for PCB Layout—Bottom View



Note: No top-layer metal is allowed in keep-out areas.

Section 26: Ordering Information

Part Number	*Package*	*Description*	*Operating Ambient Temperature*
BCM43341XKUBG	141 ball WLBGA (5.67 mm × 4.47 mm, 0.4 mm pitch)	Dual-band 2.4 GHz and 5 GHz WLAN + BT 4.0 + FM + NFC	–30°C to +85°C
BCM43341HKUBG	141 ball WLBGA (5.67 mm × 4.47 mm, 0.4 mm pitch)	Dual-band 2.4 GHz and 5 GHz WLAN + BT 4.0 + FM + NFC + BSP	–30°C to +85°C

Appendix A: Acronyms and Abbreviations

Acronym	*Definition*
AD-FLL	All-Digital Frequency-Locked Loop
AID	Application Identifier
BLE	Bluetooth Low Energy
BSC	Broadcom Serial Control interface compatible with the NXP® I^2C standard
CE	Card Emulation
eSE	Embedded Secure Element
FeliCa	Felicity Card
HCI	For NFC, Host Controller Interface, defined by ETSI TS 102 622
IEC	International Electrotechnical Commission
ISO	International Organization for Standardization
JIS	Japanese Industrial Standard
LC	link control
LLCP	Link Layer Control Protocol
LPO	low power oscillator
LPTD	Low Power Target Detection
MCU	Microcontroller
NCI	NFC Controller Interface
NFC	Near Field Communication
PCD	Proximity Coupling Device
PICC	Proximity Integrated Circuit Card
PMU	Power Management Unit
PPSE	Proximity Payment System Environment
QFN	Quad Flat No leads
RFID	Radio Frequency Identification
RX	receive
SE	Secure Element
SPI	Serial Peripheral Interconnect
SWP	Single Wire Protocol
TX	transmit
UART	Universal Asynchronous Receiver/Transmitter
UICC	Universal Integrated Circuit Cards
XTAL	Crystal

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