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# FDMS2672

## N-Channel UltraFET Trench MOSFET

200V, 20A, 77mΩ

### Features

- Max  $r_{DS(on)}$  = 77mΩ at  $V_{GS} = 10V$ ,  $I_D = 3.7A$
- Max  $r_{DS(on)}$  = 88mΩ at  $V_{GS} = 6V$ ,  $I_D = 3.5A$
- Low Miller Charge
- RoHS Compliant

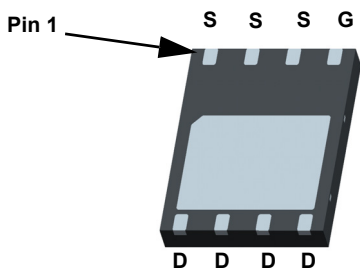


### General Description

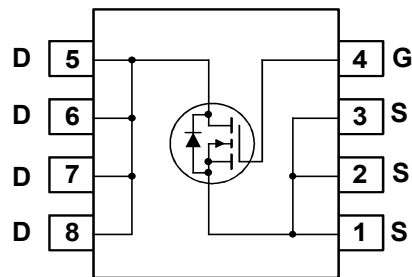
UltraFET devices combine characteristics that enable benchmark efficiency in power conversion applications. Optimized for  $r_{DS(on)}$ , low ESR, low total and Miller gate charge, these devices are ideal for high frequency DC to DC converters.

### Application

- DC - DC Conversion



Power 56 (Bottom view)



### MOSFET Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	200	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous	$T_C = 25^\circ C$ (Note 5)	20
	-Continuous	$T_C = 100^\circ C$ (Note 5)	13
	-Continuous	$T_A = 25^\circ C$ (Note 1a)	3.7
	-Pulsed	(Note 4)	96
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	33.8
$P_D$	Power Dissipation	$T_C = 25^\circ C$	78
	Power Dissipation	$T_A = 25^\circ C$ (Note 1a)	2.5
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ C$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.6	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS2672	FDMS2672	Power 56	7"	12mm	3000 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	200			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		210		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 160\text{V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2	3.1	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-10		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 3.7\text{A}$		64	77	m $\Omega$
		$V_{GS} = 6\text{V}, I_D = 3.5\text{A}$		69	88	
		$V_{GS} = 10\text{V}, I_D = 3.7\text{A}, T_J = 125^\circ\text{C}$		129	156	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{V}, I_D = 3.7\text{A}$		14		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 100\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		1740	2315	pF
$C_{oss}$	Output Capacitance			95	125	pF
$C_{rss}$	Reverse Transfer Capacitance			30	45	pF
$R_g$	Gate Resistance		0.1	1	5	$\Omega$

### Switching Characteristics

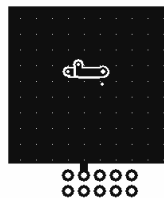
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 100\text{V}, I_D = 3.7\text{A}, V_{GS} = 10\text{V}, R_{GEN} = 6\Omega$		22	34	ns
$t_r$	Rise Time			11	22	ns
$t_{d(off)}$	Turn-Off Delay Time			36	57	ns
$t_f$	Fall Time			10	20	ns
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0\text{V}$ to $10\text{V}$	$V_{DD} = 100\text{V}, I_D = 3.7\text{A}$	30	42	nC
$Q_{gs}$	Gate to Source Gate Charge			7		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			8		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 3.7\text{A}$ (Note 2)		0.8	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 3.7\text{A}, di/dt = 100\text{A}/\mu\text{s}$		70	105	ns
$Q_{rr}$	Reverse Recovery Charge			238	357	nC

#### Notes:

1:  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $50^\circ\text{C}/\text{W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper



b.  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width  $< 300\mu\text{s}$ , Duty cycle  $< 2.0\%$ .

3:  $E_{AS}$  of  $33.8\text{mJ}$  is based on starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\text{mH}$ ,  $I_{AS} = 4.75\text{A}$ ,  $V_{DD} = 25\text{V}$ ,  $V_{GS} = 10\text{V}$ .

4: Pulsed  $I_D$  please refer to Fig 11 SOA graph for more details.

5: Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

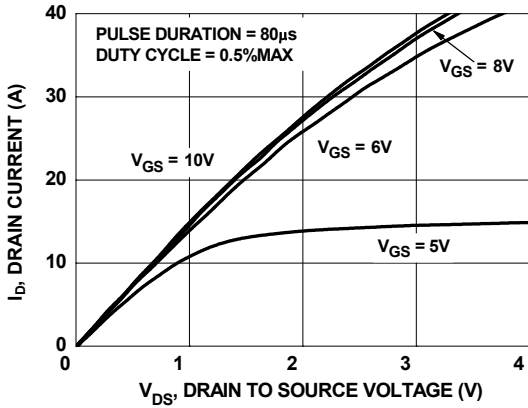


Figure 1. On Region Characteristics

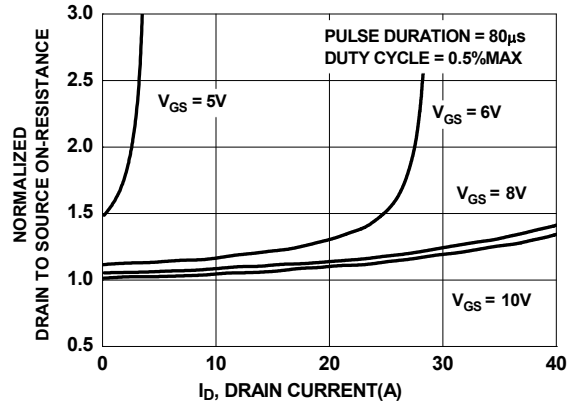


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

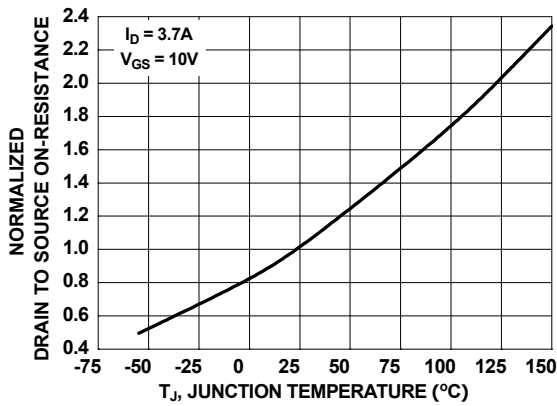


Figure 3. Normalized On Resistance vs Junction Temperature

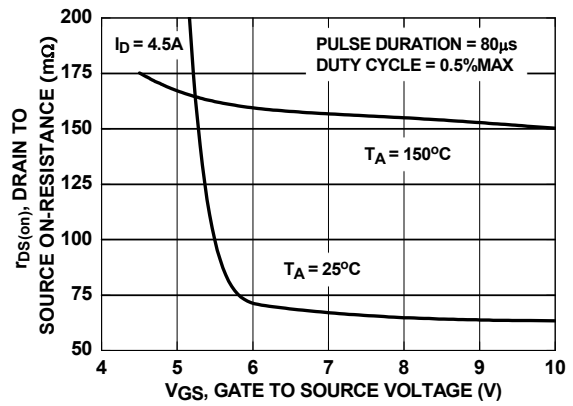


Figure 4. On-Resistance vs Gate to Source Voltage

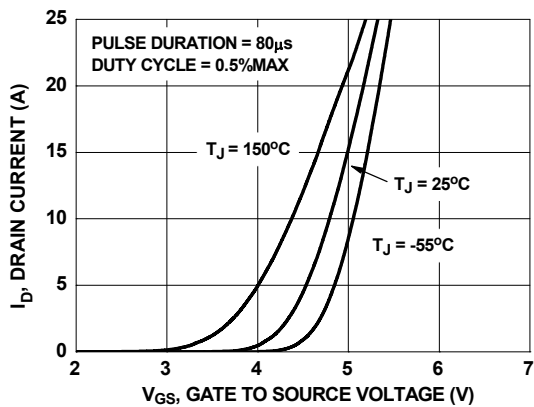


Figure 5. Transfer Characteristics

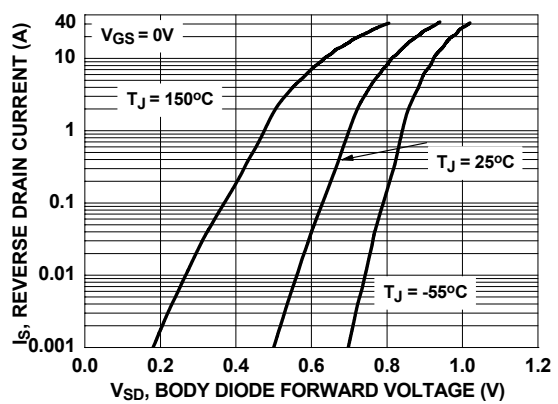
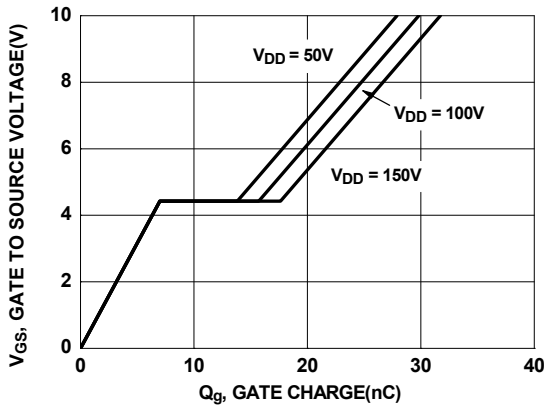
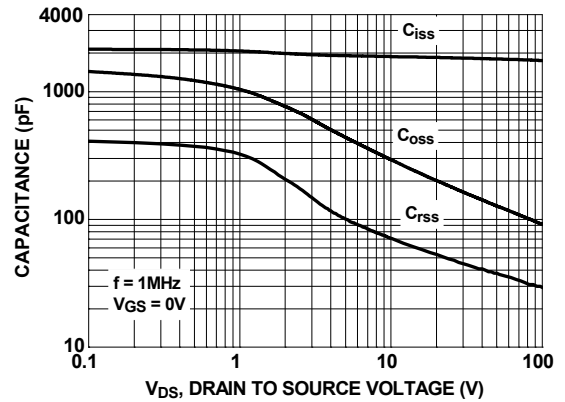


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

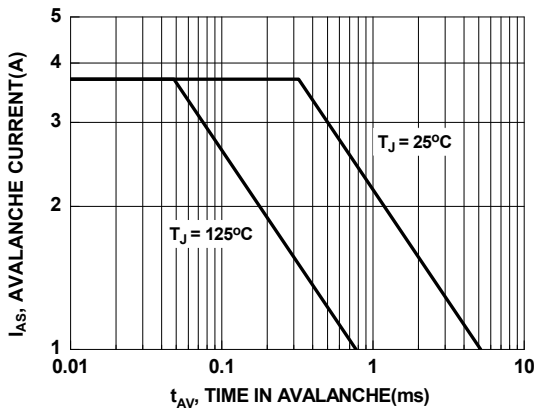
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



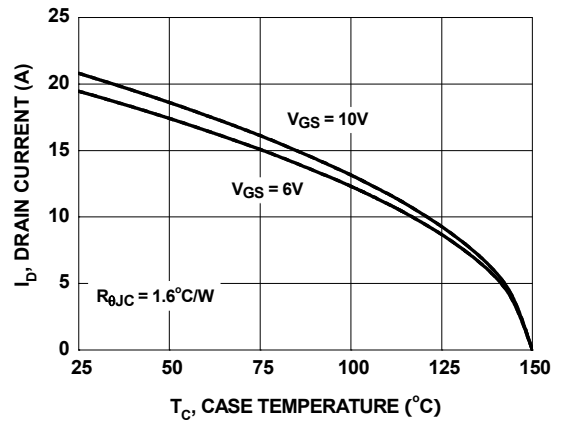
**Figure 7. Gate Charge Characteristics**



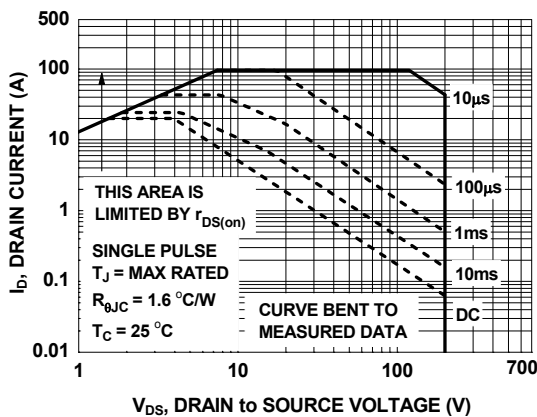
**Figure 8. Capacitance vs Drain to Source Voltage**



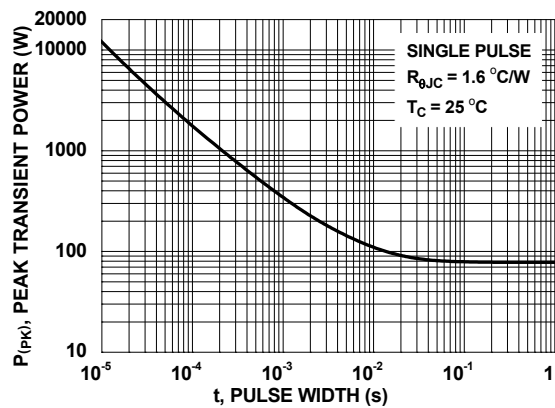
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

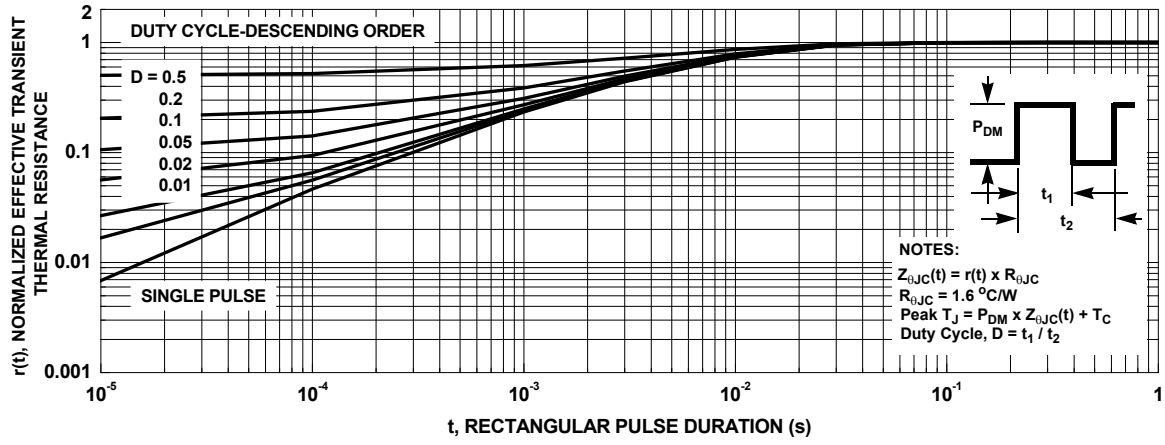


**Figure 11. Forward Bias Safe Operating Area**



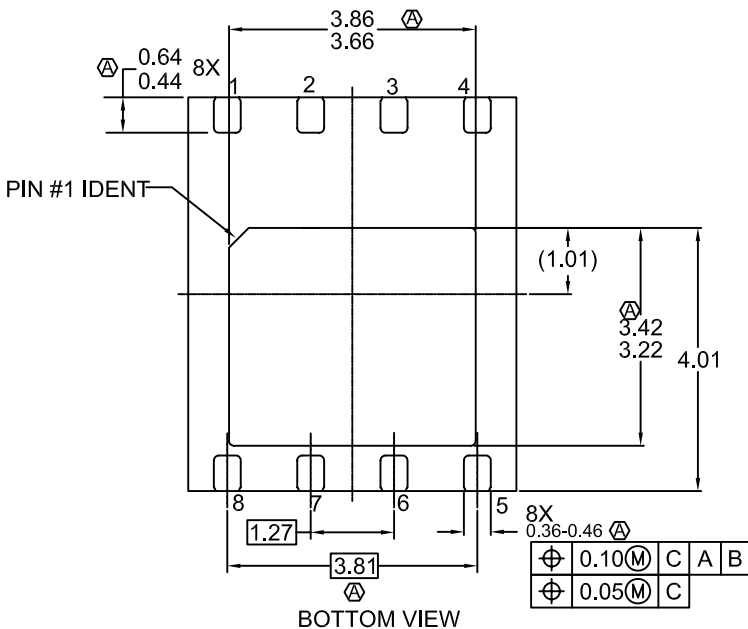
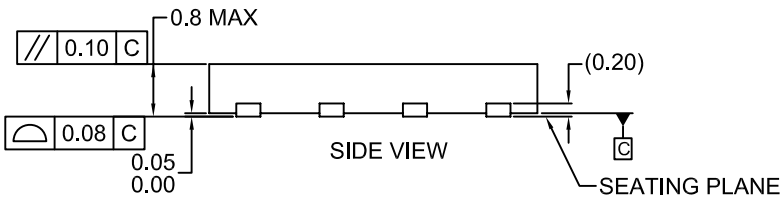
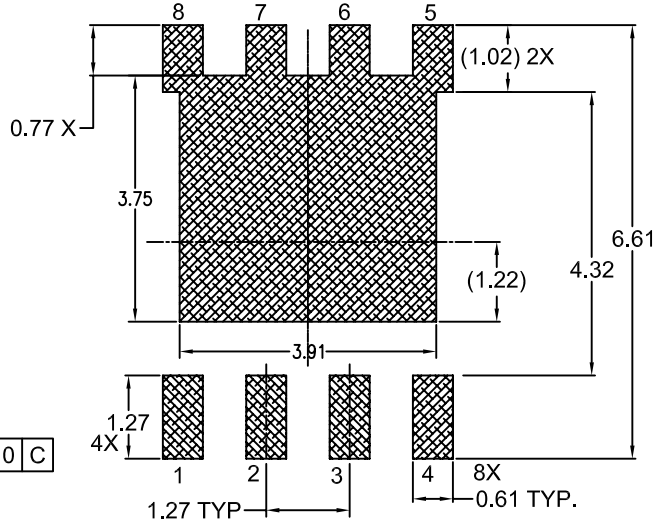
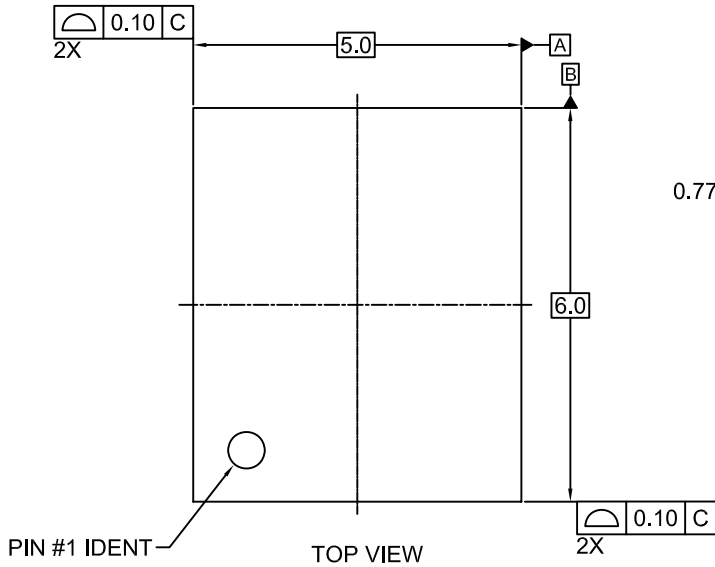
**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Case Transient Thermal Response Curve**

REVISIONS			
NBR	DESCRIPTION	DATE	NAME/SITE
1	RELEASE TO DOCUMENT CONTROL	090305	David/FSPM
2	REVISE TO CORRECT DAP SIZE	080605	David/FSPM
3	I) REVISE TO CORRECT PKG THK II) REVISE THE PKG PROFILE TOLERANCE	210306	CK/FSPM
4	ADD IN LEAD LENGTH FOR LAND PATTERN	220908	LY/FSPM



NOTES:

- A DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. TERMINALS 5,6,7 AND 8 ARE TIED TO THE EXPOSED PADDLE
- E. LANDPATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY
- F. DRAWING FILENAME: MKT-MLP08Grev4

APPROVALS	DATE	FAIRCHILD SEMICONDUCTOR™			
DRAWN LY Lim	01 Nov 08	8LD, MLP, DUAL, NON-JEDEC, 5X6 MM BODY, TIED DAP			
DFTG. CHK. LY LIM	01 Nov 08				
ENGR. CHK. DAVID	01 Nov 08				
PROJECTION		SCALE N/A	SIZE N/A	DRAWING NUMBER MKT-MLP08G	REV 4
MM		DO NOT SCALE DRAWING			SHEET 1 of 1



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| FETBench™                | mWSaver®                                       | Sync-Lock™                            |                  |
| FPS™                     | OptoHiT™                                       |                                       |                  |
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