

Features

- Formerly **FulTec** brand
- Extremely high speed performance
- Blocks high voltages and currents
- Low insertion loss
- Two TBU™ protectors in one small package
- Very high bandwidth; GHz compatible
- RoHS compliant*, UL Recognized

Applications

- Mb Ethernet port protection
- Gb Ethernet port protection
- Isolated and floating interfaces

TBU™ P650-U and P850-U Protectors

Transient Blocking Units - TBU™ Devices

Bourns® Model P650-U and P850-U products are high speed, unidirectional protection components, constructed using MOSFET semiconductor technology, designed to protect against faults caused by short circuits, AC power cross, induction and lightning surges.

The TBU™ high speed protector, triggering as a function of the MOSFET, blocks surges and provides an effective barrier behind which sensitive electronics are not exposed to large voltages or currents during surge events. The TBU™ device is provided in a surface mount DFN package and meets industry standard requirements such as RoHS and Pb Free solder reflow profiles.

Agency Approval

UL recognized component File # E315805.

Industry Standards

Description			Model
Telcordia	GR-1089	Port Type 3, 5	P650-U
		Port Type 2, 4	P850-U
ITU-T	K.20, K.20E, K.21, K.21E, K.45		P850-U

Absolute Maximum Ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V _{imp}	Maximum protection voltage for impulse faults with rise time ≥ 1 μsec	P650-Uxxx-WH	650	V
		P850-Uxxx-WH	850	
V _{rms}	Maximum protection voltage for continuous V _{rms} faults connected as a series pair (refer to page 3 Test Configuration Diagram)	P650-Uxxx-WH	300	V
		P850-Uxxx-WH	425	
T _{op}	Operating temperature range		-40 to +85	°C
T _{stg}	Storage temperature range		-65 to +150	°C

Electrical Characteristics (T_{amb} = 25 °C)

Symbol	Parameter		Min.	Typ.	Max.	Unit
I _{op}	Maximum current through the device that will not cause current blocking	P650-U180-WH			180	mA
		P650-U260-WH			260	
		P850-U180-WH			180	
		P850-U260-WH			260	
I _{trigger}	Typical current for the device to go from normal operating state to protected state	P650-U180-WH		220		mA
		P650-U260-WH		330		
		P850-U180-WH		220		
		P850-U260-WH		330		
I _{out}	Maximum current through the device	P650-U180-WH			360	mA
		P650-U260-WH			520	
		P850-U180-WH			360	
		P850-U260-WH			520	
R _{TBU}	Series resistance of the TBU™ device	P650-Uxxx-WH		6	7	Ω
		P850-Uxxx-WH		8	9	
R _{bal}	Line-to line series resistance difference between two TBU™ device				0.5	Ω
t _{block}	Maximum time for the device to go from normal operating state to protected state	P650-Uxxx-WH P850-Uxxx-WH			1	μs
I _{quiescent}	Current through the triggered TBU™ device with 50 Vdc circuit voltage			1		mA
V _{reset}	Voltage below which the triggered TBU™ device will transition to normal operating state	P650-Uxxx-WH		11		V
		P850-Uxxx-WH		14		

The P-U Series TBU™ devices are unidirectional; specifications are valid for input direction only. For the output direction, the TBU™ device is a resistor.

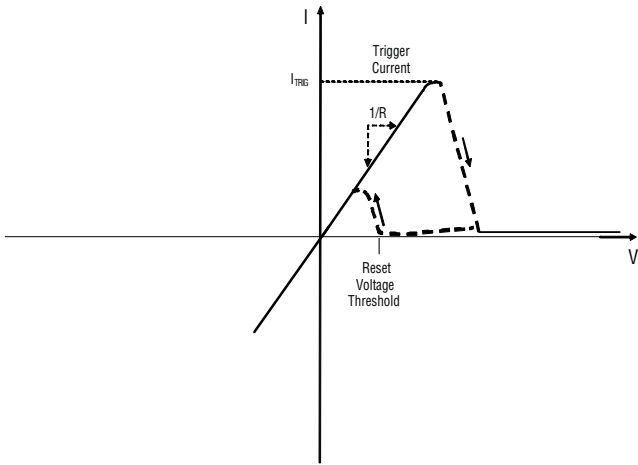
*RoHS Directive 2002/95/EC Jan 27 2003 including Annex.

Specifications are subject to change without notice.

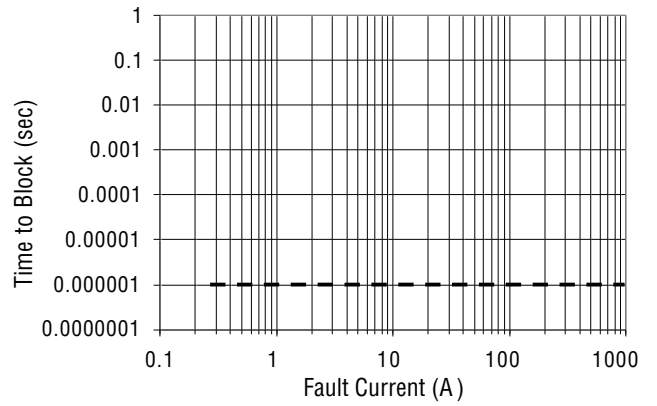
Customers should verify actual device performance in their specific applications.

Typical Performance Characteristics

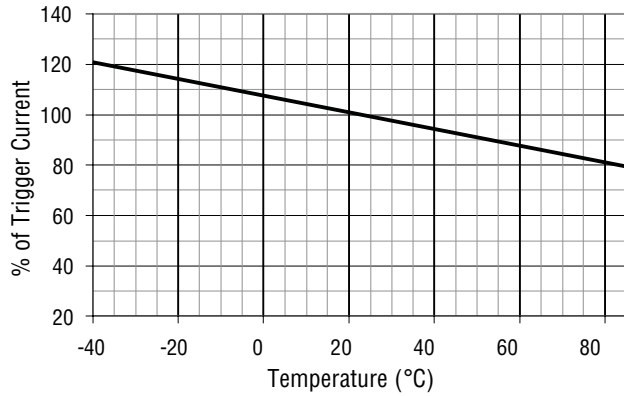
V-I Characteristics



Time to Block vs. Fault Current



Trigger Current vs. Temperature



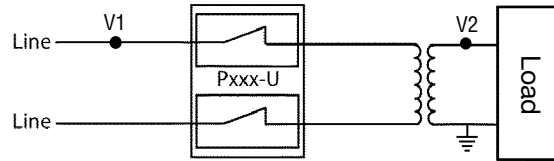
TBU™ P650-U and P850-U Protectors

BOURNS®

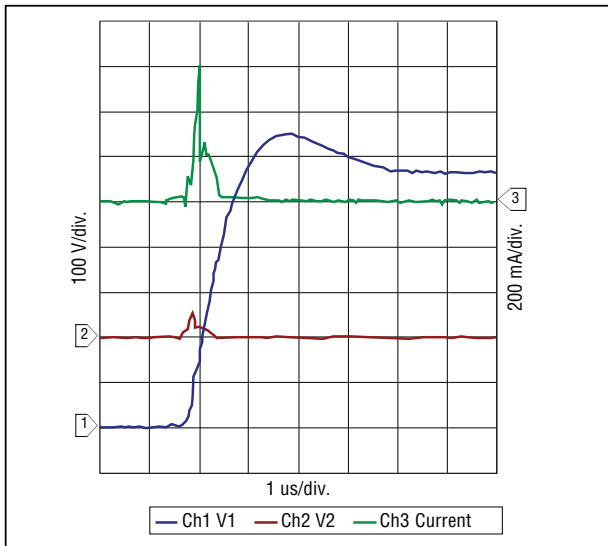
Operational Characteristics

The graphs below demonstrate the operational characteristics of the TBU. For each graph the fault voltage, protected side voltage, and current is presented.

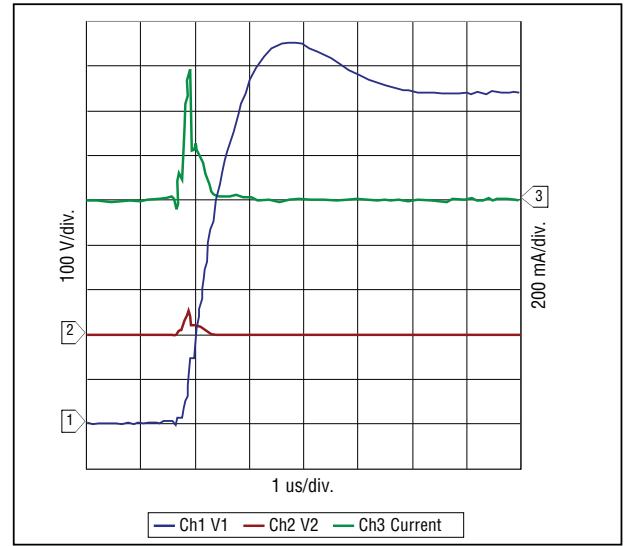
TEST CONFIGURATION DIAGRAM



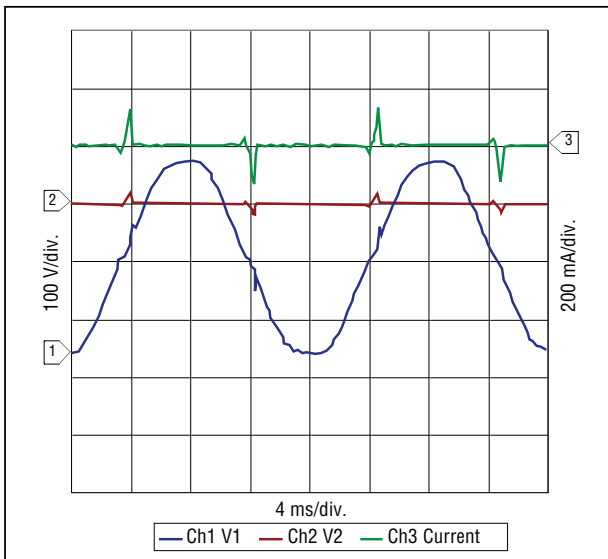
P650-U Lightning, 650 V



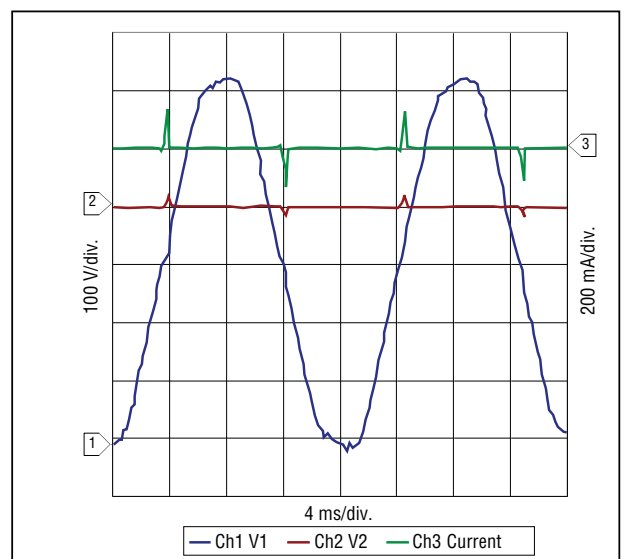
P850-U Lightning, 850 V



P650-U Power Fault, 120 Vrms, 25 A



P850-U Power Fault, 230 Vrms, 25 A

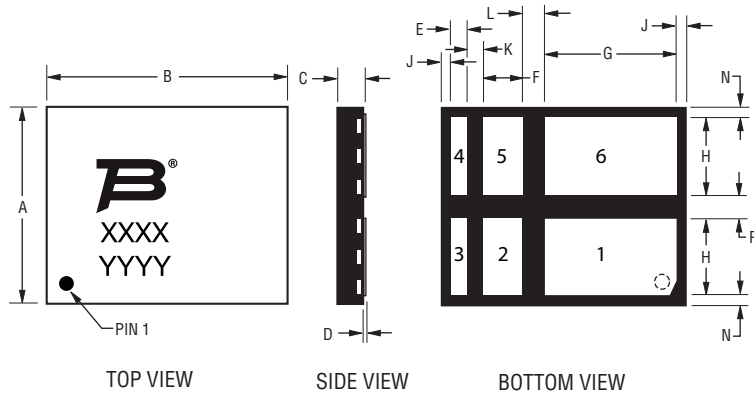


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TBU™ P650-U and P850-U Protectors

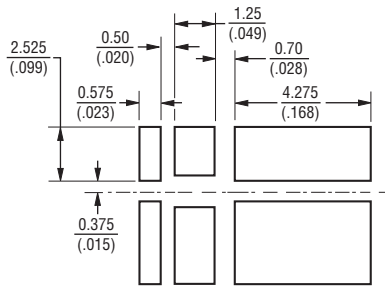
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Product Dimensions



Dim.	Min.	Typ.	Max.
A	6.15 (.242)	6.25 (.246)	6.35 (.250)
B	7.65 (.301)	7.75 (.305)	7.85 (.309)
C	0.80 (.031)	0.85 (.033)	0.90 (.035)
D	0.000 (.000)	0.025 (.001)	0.050 (.002)
E	0.50 (.020)	0.55 (.022)	0.60 (.024)
F	1.20 (.047)	1.25 (.049)	1.30 (.051)
G	4.20 (.165)	4.25 (.167)	4.30 (.169)
H	2.45 (.096)	2.50 (.098)	2.55 (.100)
J	0.20 (.008)	0.25 (.010)	0.30 (.012)
K	0.45 (.018)	0.50 (.020)	0.55 (.022)
L	0.65 (.026)	0.70 (.028)	0.75 (.030)
N	0.20 (.008)	0.25 (.010)	0.30 (.012)
P	0.70 (.028)	0.75 (.030)	0.80 (.031)
Q	3.20 (.126)	3.25 (.128)	3.30 (.130)

Recommended Pad Layout



Pad Designation

Pad #	Apply
1	In1
2	NC
3	Out1
4	Out2
5	NC
6	In2

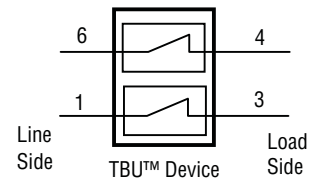
NC = Solder to PCB; do not make electrical connection, do not connect to ground.

TBU™ devices have matte-tin termination finish. Suggested layout should use non-solder mask define (NSMD). Recommended stencil thickness is 0.10-0.12 mm (.004-.005 in.) with stencil opening size 0.025 mm (.0010 in.) less than the device pad size. As when heat sinking any power device, it is recommended that, wherever possible, extra PCB copper area is allowed. For minimum parasitic capacitance, do not allow any signal, ground or power signals beneath any of the pads of the device.

Thermal Resistances

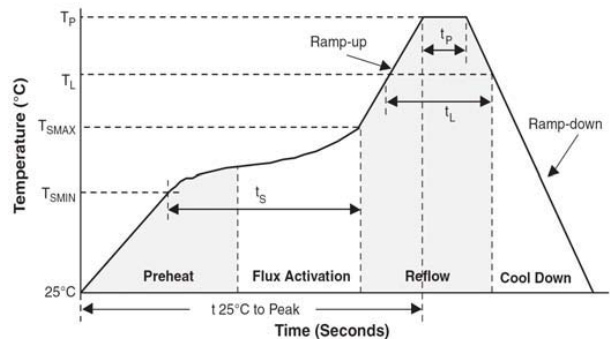
Symbol	Parameter	Value	Unit
R _{th(j-a)}	Junction to leads (package)	105	°C/W
	Junction to leads (per TBU)	202	°C/W

Block Diagram



Reflow Profile

Profile Feature	Pb-Free Assembly
Average Ramp-Up Rate (T _{smax} to T _p)	3 °C/sec. max.
Preheat	
- Temperature Min. (T _{smin})	150 °C
- Temperature Max. (T _{smax})	200 °C
- Time (t _{smin} to t _{smax})	60-180 sec.
Time maintained above:	
- Temperature (T _L)	217 °C
- Time (t _L)	60-150 sec.
Peak/Classification Temperature (T _p)	260 °C
Time within 5 °C of Actual Peak Temp. (t _p)	20-40 sec.
Ramp-Down Rate	6 °C/sec. max.
Time 25 °C to Peak Temperature	8 min. max.



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TBU™ P650-U and P850-U Protectors

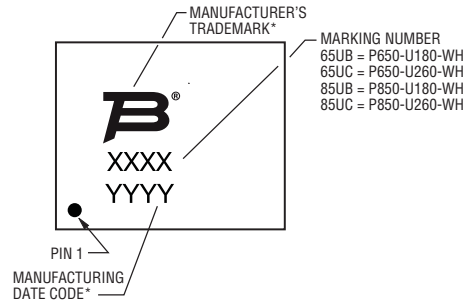


How to Order

P 650 - U 180 - WH

Form Factor _____
 P = Two TBU™ protectors in one device
 Impulse Voltage Rating _____
 650 = 650 V
 850 = 850 V
 Directional Indication for Paired Devices _____
 U = Unidirectional
 Iop Indicator _____
 180 = 180 mA
 260 = 260 mA

Typical Part Marking



- 1ST DIGIT INDICATES THE YEAR'S 6-MONTH PERIOD.
 - 2ND DIGIT INDICATES THE WEEK NUMBER IN THE 6-MONTH PERIOD.
 - 3RD & 4TH DIGITS INDICATE SPECIFIC LOT FOR THE WEEK.

6-MONTH PERIOD CODES:

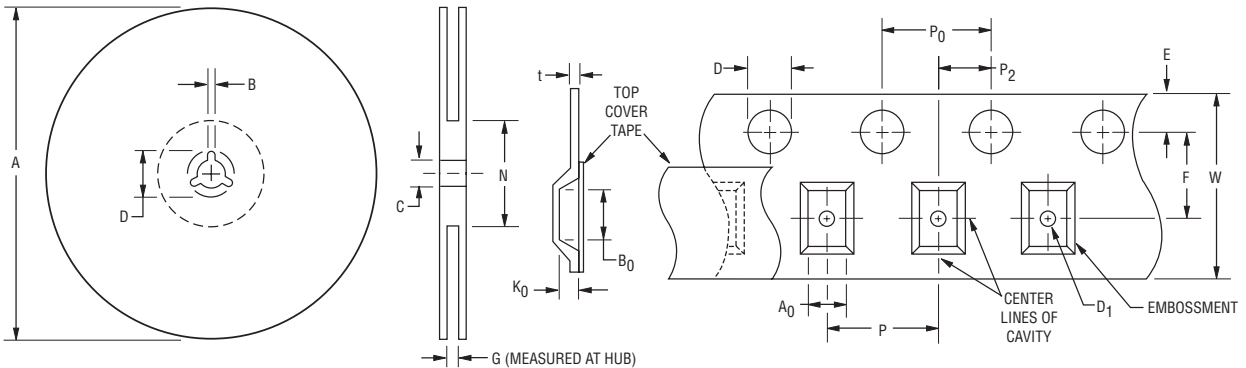
A = JAN-JUN 2009 C = JAN-JUN 2010 E = JAN-JUN 2011
 B = JUL-DEC 2009 D = JUL-DEC 2010 F = JUL-DEC 2011

EXAMPLE: ARBC

- 1ST DIGIT 'A' = JAN-JUN 2009
 - 2ND DIGIT 'R' = WEEK 18; WEEK OF APRIL 27
 - 3RD & 4TH DIGITS 'BC' = LOT SPECIFIC INFORMATION

*TRANSITION FROM FULTEC TRADEMARK AND LOT CODE TO BOURNS TRADEMARK AND DATE CODE IN 2009.

Packaging Specifications (per EIA468-B)



USER DIRECTION OF FEED
 QUANTITY: 3000 PIECES PER REEL

Device	A		B		C		D		G	N
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
P650-U, P850-U	326 (.12.835)	330.25 (.13.002)	1.5 (.059)	2.5 (.098)	12.8 (.504)	13.5 (.531)	20.2 (.795)	-	16.5 (.650)	102 (4.016)

Device	A ₀		B ₀		D		D ₁		E		F	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
P650-U, P850-U	6.5 (.256)	6.7 (.264)	8.0 (.315)	8.2 (.323)	1.5 (.059)	1.6 (.063)	1.5 (.059)	-	1.65 (.065)	1.85 (.073)	7.4 (.291)	7.6 (.299)
Device	K ₀		P		P ₀		P ₂		t		W	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
P650-U, P850-U	1.4 (.055)	1.6 (.063)	11.9 (.469)	12.1 (.476)	3.9 (.159)	4.1 (.161)	1.9 (.075)	2.1 (.083)	0.25 (.010)	0.35 (.014)	15.7 (.618)	16.3 (.642)

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DIMENSIONS: $\frac{\text{MM}}{\text{(INCHES)}}$

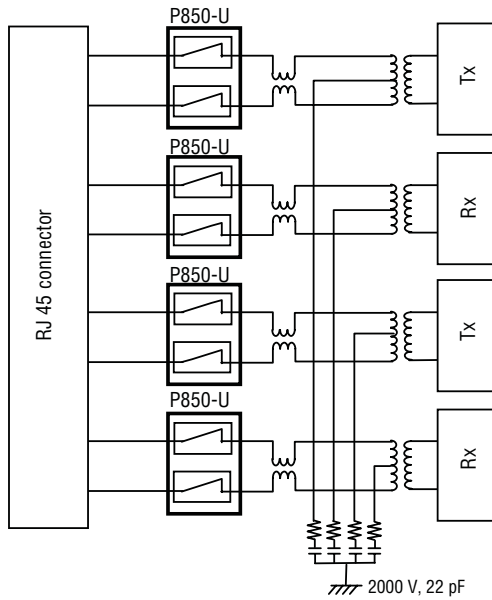
TBU™ P650-U and P850-U Protectors



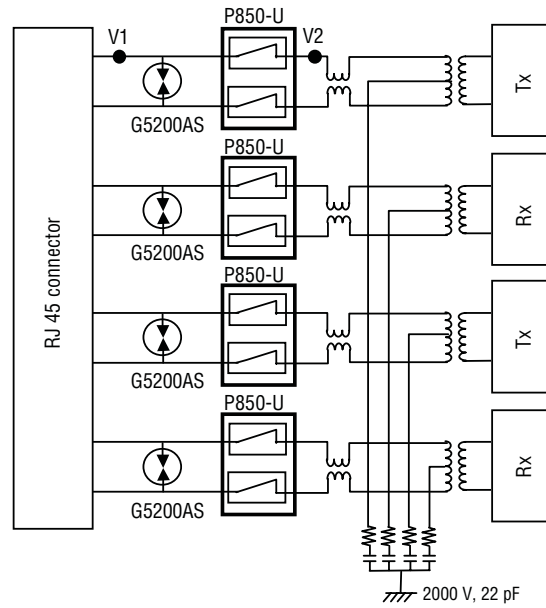
Reference Applications

A cost-effective protection solution utilizes the Bourns® TBU™ protection devices. The diagrams below illustrate common configurations of these components. The graph at the bottom demonstrates the operational characteristics of the circuit.

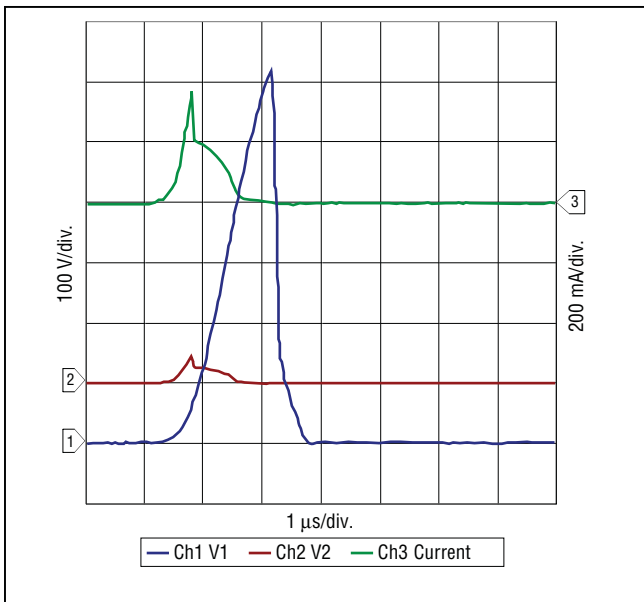
Typical Configuration Diagrams



GbE Ethernet Protection
Up to 1500 V Common-Mode Lightning Protection



GbE Ethernet Protection
Up to 6000 V Common-Mode Lightning Protection



P850-U with G5200AS 4000 V Lightning 10/700 μsec, 150 A



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