Quad Low Offset, Low Power Operational Amplifier

Data Sheet **OP400**

FEATURES

- **Low input offset voltage: 150 µV maximum**
- **Low offset voltage drift over –55°C to +125°C: 1.2 µV/°C maximum**
- **Low supply current (per amplifier): 725 µA maximum**
- **High open-loop gain: 5000 V/mV minimum**
- **Input bias current: 3 nA maximum**
- **Low noise voltage density: 11 nV/√Hz at 1 kHz**
- **Stable with large capacitive loads: 10 nF typical**
- **Available in die form**

FUNCTIONAL BLOCK DIAGRAMS

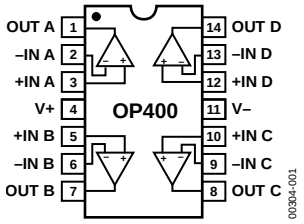


Figure 1. 14-Pin Ceramic DIP (Y-Suffix) and 14-Pin Plastic DIP (P-Suffix)

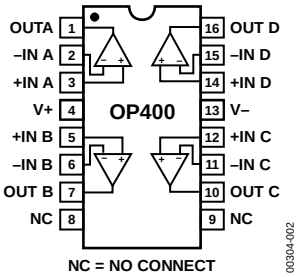


Figure 2. 16-Pin SOIC (S-Suffix)

GENERAL DESCRIPTION

The OP400 is the first monolithic quad operational amplifier that features OP77-type performance. Precision performance is not sacrificed with the OP400 to obtain the space and cost savings offered by quad amplifiers.

The OP400 features an extremely low input offset voltage of less than 150 µV with a drift of less than 1.2 µV/°C, guaranteed over the full military temperature range. Open-loop gain of the OP400 is more than 5 million into a 10 kΩ load, input bias current is less than 3 nA, CMR is more than 120 dB, and PSRR is less than 1.8 µV/V. On-chip Zener zap trimming is used to achieve the low input offset voltage of the OP400 and eliminates the need for offset nulling. The OP400 conforms to the industry-standard quad pinout, which does not have null terminals.

The OP400 features low power consumption, drawing less than 725 µA per amplifier. The total current drawn by this quad amplifier is less than that of a single OP07, yet the OP400 offers significant improvements over this industry-standard op amp. Voltage noise density of the OP400 is a low 11 nV/√Hz at 10 Hz, half that of most competitive devices.

The OP400 is an ideal choice for applications requiring multiple precision operational amplifiers and where low power consumption is critical.

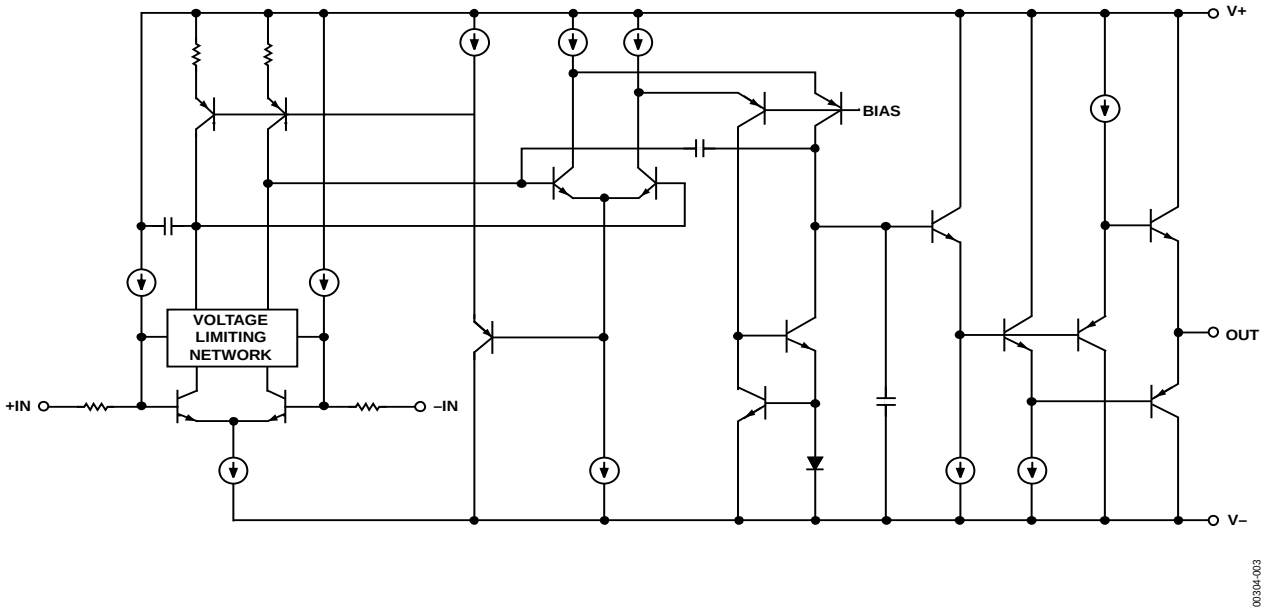


Figure 3. Simplified Schematic (One of Four Amplifiers Is Shown)

Rev. H **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **Technical Support**

www.analog.com

OP400* Product Page Quick Links

Last Content Update: 08/30/2016

Comparable Parts

View a parametric search of comparable parts

Documentation

Application Notes

- AN-256: Accurately Testing Op Amp Settling Times
- AN-357: Operational Integrators
- AN-649: Using the Analog Devices Active Filter Design Tool

Data Sheet

- OP400: Quad Low Offset, Low Power Operational Amplifier Data Sheet
- OP400: Military Data Sheet

Tools and Simulations

- OP400 SPICE Macro-Model

Reference Materials

Analog Dialogue

- Ask The Applications Engineer - 25 Op Amps Driving Capacitive Loads

Design Resources

- OP400 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

Discussions

View all OP400 EngineerZone Discussions

Sample and Buy

Visit the product page to see pricing options

Technical Support

Submit a technical question or find your regional support number

TABLE OF CONTENTS

REVISION HISTORY

1/13—Rev. G to Rev. H

Changes to Features Section and General Description Section 1
Changes to Ordering Guide 15

2/11—Rev. F to Rev. G

Added S Package to Storage Temperature Range in Table 4 5
Updated Outline Dimensions 15

12/08—Rev. E to Rev. F

Added New Figure 28, Renumbered Sequentially 10
Updated Outline Dimensions 15

1/07—Rev. D to Rev. E

Updated Format ..... Universal
Changes to Figure 1 and Figure 2 1
Removed Figure 4 4
Changes to Table 3 4
Changes to Figure 16 through Figure 19, Figure 21 8
Changes to Figure 27 9
Changes to Figure 28 10
Changes to Figure 33 13
Updated Outline Dimensions 14

3/06—Rev. C to Rev. D

Updated Format ..... Universal
Deleted Wafer Test Limits Table 4
New Package Drawing: R-14 15
Updated Outline Dimensions 15
Changes to Ordering Guide 16

6/03—Rev. B to Rev. C

Edits to Specifications 2

10/02—Rev. A to Rev. B

Addition of Absolute Maximum Ratings 5
Edits to Outline Dimensions 12

4/02—Rev. 0 to Rev. A

Edits to Features 1
Edits to Ordering Information 1
Edits to Pin Connections 1
Edits to General Descriptions 1, 2
Edits to Package Type 2

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

@ V_S = ±15 V, T_A = +25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	OP400A/E			OP400F			OP400G/H			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS												
Input Offset Voltage	V_{OS}			40	150		60	230		80	300	µV
Long-Term Input Voltage Stability				0.1			0.1			0.1		µV/mo
Input Offset Current	I_{OS}	V_{CM} = 0 V		0.1	1.0		0.1	2.0		0.1	3.5	nA
Input Bias Current	I_B	V_{CM} = 0 V		0.75	3.0		0.75	6.0		0.75	7.0	nA
Input Noise Voltage	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		0.5			0.5			0.5		µV p-p
Input Resistance Differential Mode	R_{IN}			10			10			10		MΩ
Input Resistance Common Mode	R_{INCM}			200			200			200		GΩ
Large Signal Voltage Gain	A_{VO}	V_O = ±10 V										
		R_L = 10 kΩ	5000	12,000		3000	7000		3000	7000		V/mV
		R_L = 2 kΩ	2000	3500		1500	3000		1500	3000		V/mV
Input Voltage Range[1]	IVR		±12	±13		±12	±13		±12	±13		V
Common-Mode Rejection	CMR	V_{CM} = 12 V	120	140		115	140		110	135		dB
Input Capacitance	C_{IN}			3.2			3.2			3.2		pF
OUTPUT CHARACTERISTICS												
Output Voltage Swing	V_O	R_L = 10 kΩ	±12	±12.6		±12	±12.6		±12	±12.6		V
POWER SUPPLY												
Power Supply Rejection Ratio	PSRR	V_S = 3 V to 18 V		0.1	1.8		0.1	3.2		0.2	5.6	µV/V
Supply Current per Amplifier	I_{SY}	No load		600	725		600	725		600	725	µA
DYNAMIC PERFORMANCE												
Slew Rate	SR		0.1	0.15		0.1	0.15		0.1	0.15		V/µs
Gain Bandwidth Product	GBWP	A_V = 1		500			500			500		kHz
Channel Separation	CS	V_O = 20 V p-p, f_O = 10 Hz[2]	123	135		123	135		123	135		dB
Capacitive Load Stability		A_V = 1, no oscillations		10			10			10		nF
NOISE PERFORMANCE												
Input Noise Voltage	e_n	f_O = 10 Hz[3]		22	36		22	36		22		nV/√Hz
Density[3]		f_O = 1000 Hz[3]		11	18		11	18		11		nV/√Hz
Input Noise Current	$i_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		15			15			15		pA p-p
Input Noise Current Density	i_n	f_O = 10 Hz		0.6			0.6			0.6		pA/√Hz

[1] Guaranteed by CMR test.
[2] Guaranteed but not 100% tested.
[3] Sample tested.

@ V_S = ±15 V, −55°C ≤ T_A ≤ +125°C for OP400A, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{OS}			70	270	µV
Average Input Offset Voltage Drift	TCV_{OS}			0.3	1.2	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0 V		0.1	2.5	nA
Input Bias Current	I_B	V_{CM} = 0 V		1.3	5.0	nA
Large Signal Voltage Gain	A_{VO}	V_O = ±10 V, R_L = 10 kΩ	3000	9000		V/mV
		R_L = 2 kΩ	1000	2300		
Input Voltage Range [1]	IVR		±12	±12.5		V
Common-Mode Rejection	CMR	V_{CM} = ±12 V		115	130	dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 10 kΩ	±12	±12.4		
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_O = 3 V to 18 V		0.2	3.2	µV/V
Supply Current per Amplifier	I_{SY}	No load		600	775	µA
DYNAMIC PERFORMANCE						
Capacitive Load Stability		A_V = 1, no oscillations		8		nF

[1] Guaranteed by CMR test.

@ V_S = ±15 V, −25°C ≤ T_A ≤ +85°C for OP400E/F, 0°C ≤ T_A ≤ 70°C for OP400G, −40°C ≤ T_A ≤ +85°C for OP400H, unless otherwise noted.

Table 3.

			OP400E			OP400F			OP400G/H			
Parameter	Symbol	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
INPUT CHARACTERISTICS												
Input Offset Voltage	V_{OS}			60	220		80	350		110	400	µV
Average Input Offset Voltage Drift	TCV_{OS}			0.3	1.2		0.3	2.0		0.6	2.5	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0 V										
		E, F, G grades		0.1	2.5		0.1	3.5		0.2	6.0	nA
		H grade								0.2	12.0	nA
Input Bias Current	I_B	V_{CM} = 0 V										
		E, F, G grades		0.9	5.0		0.9	10.0		1.0	12.0	nA
		H grade								1.0	20.0	nA
Large-Signal Voltage Gain	A_{VO}	V_{CM} = 0 V										
		R_L = 10 kΩ	3000	10,000		2000	5000		2000	5000		V/mV
		R_L = 2 kΩ	1500	2700		1000	2000		1000	2000		V/mV
Input Voltage Range [1]	IVR		±12	±12.5		±12	±12.5		±12	±12.5		V
Common-Mode Rejection	CMR	V_{CM} = ±12 V	115	135		110	135		105	130		dB
OUTPUT CHARACTERISTICS												
Output Voltage Swing	V_O	R_L = 10 kΩ	±12	±12.4		±12	±12.4		±12	±12.6		V
		R_L = 2 kΩ	±11	±12		±11	±12		±11	±12.2		V
POWER SUPPLY												
Power Supply Rejection Ratio	PSRR	V_S = ±3 V to ±18 V		0.15	3.2		0.15	5.6		0.3	10.0	µV/V
Supply Current per Amplifier	I_{SY}	No load		600	775		600	775		600	775	µA
DYNAMIC PERFORMANCE												
Capacitive Load Stability		No oscillations		10			10			10		nF

[1] Guaranteed by CMR test.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	±20 V
Differential Input Voltage	±30 V
Input Voltage	Supply voltage
Output Short-Circuit Duration	Continuous
Storage Temperature Range	
P, Y, S Packages	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C
Junction Temperature (T_J) Range	−65°C to +150°C
Operating Temperature Range	
OP400A	−55°C to +125°C
OP400E, OP400F	−25°C to +85°C
OP400G	0°C to 70°C
OP400H	−40°C to +85°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply to both dice and packaged parts, unless otherwise noted.

THERMAL RESISTANCE

θ_{JA} is specified for worst-case mounting conditions, that is, θ_{JA} is specified for device in socket for CERDIP and PDIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOIC package.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
14-Pin Ceramic DIP (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOIC (S)	88	23	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

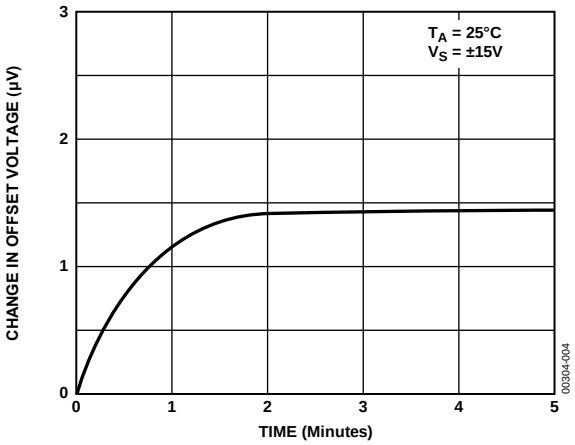


Figure 4. Warmup Drift

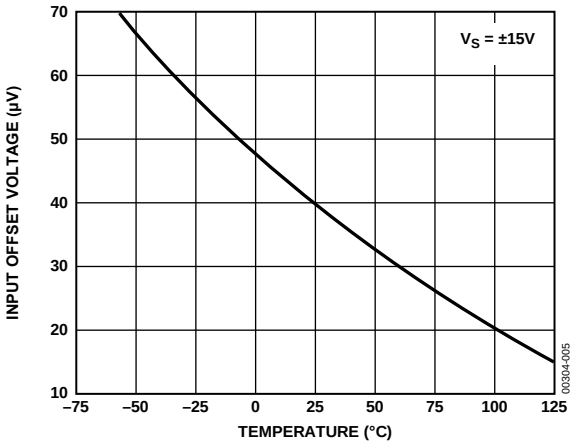


Figure 5. Input Offset Voltage vs. Temperature

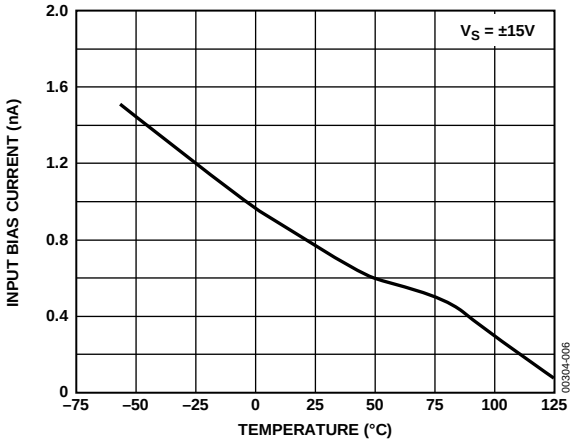


Figure 6. Input Bias Current vs. Temperature

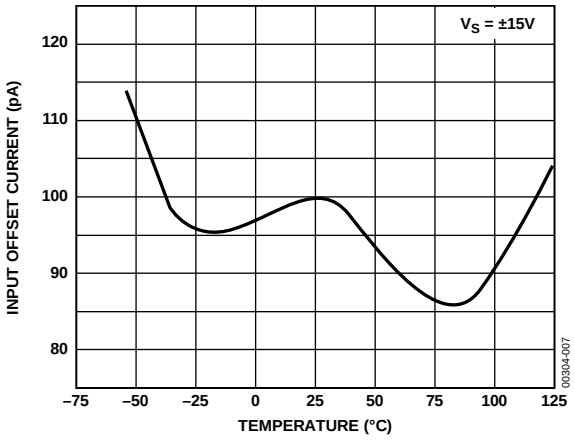


Figure 7. Input Offset Current vs. Temperature

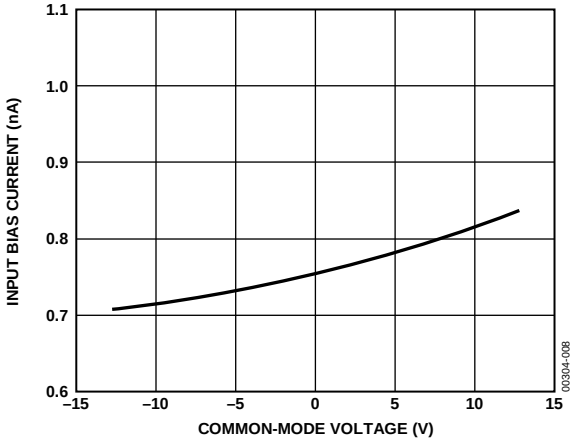


Figure 8. Input Bias Current vs. Common-Mode Voltage

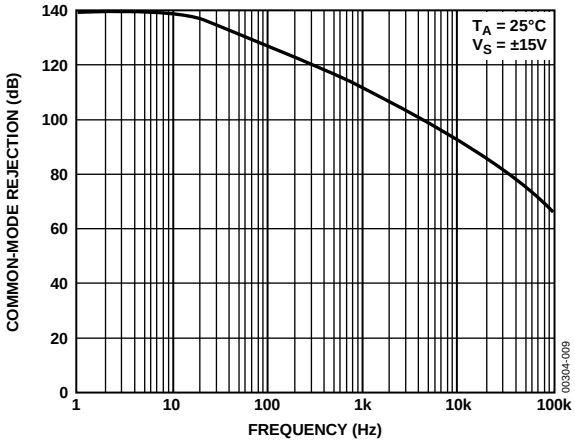


Figure 9. Common-Mode Rejection vs. Frequency

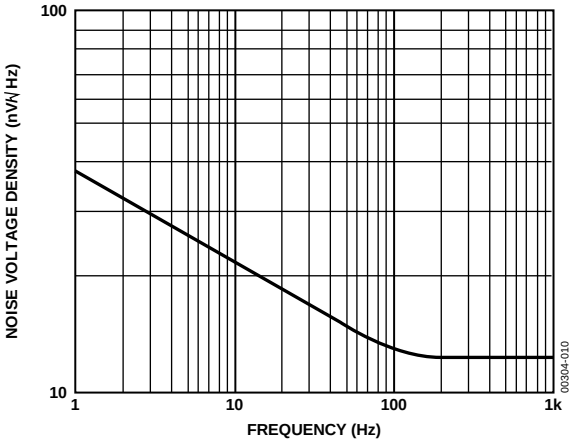


Figure 10. Noise Voltage Density vs. Frequency

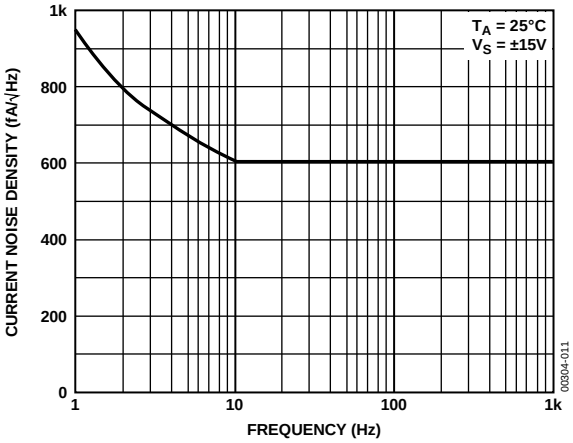


Figure 11. Current Noise Density vs. Frequency

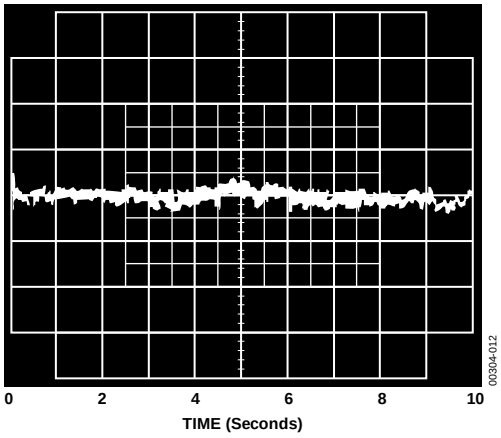


Figure 12. 0.1 Hz to 10 Hz Noise

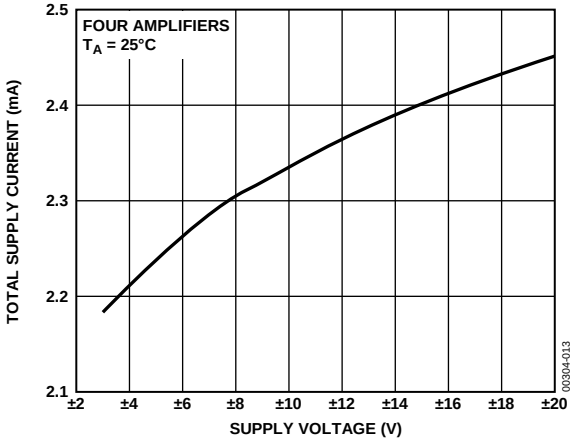


Figure 13. Total Supply Current vs. Supply Voltage

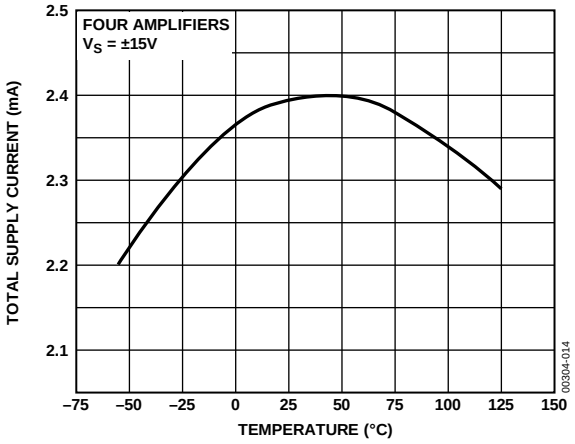


Figure 14. Total Supply Current vs. Temperature

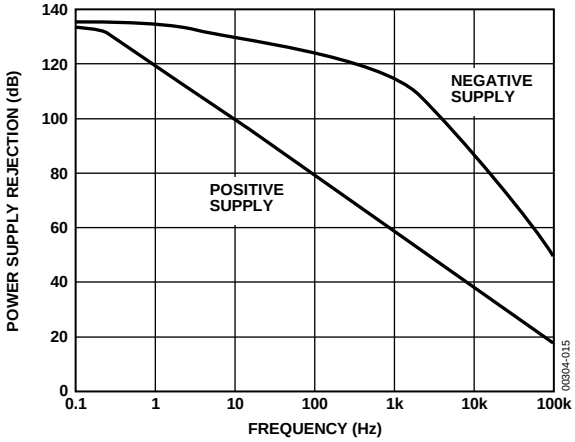


Figure 15. Power Supply Rejection vs. Frequency

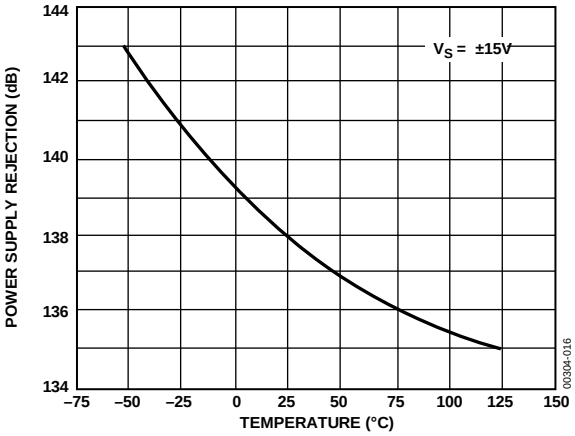


Figure 16. Power Supply Rejection vs. Temperature

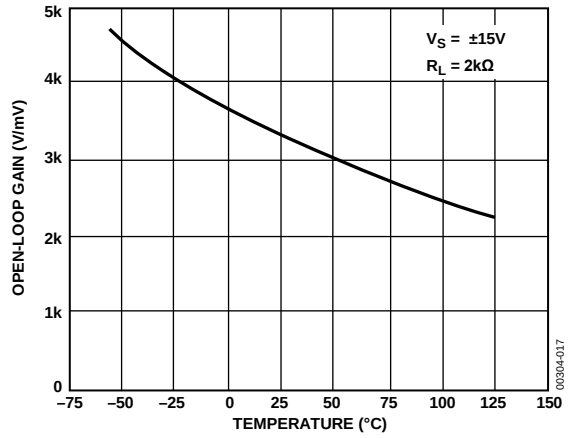


Figure 17. Open-Loop Gain vs. Temperature

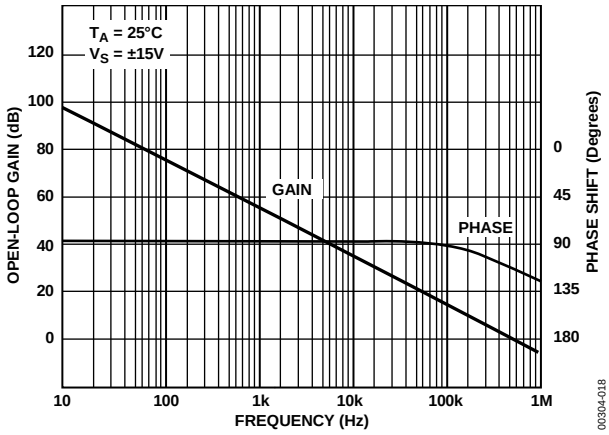


Figure 18. Open-Loop Gain and Phase Shift vs. Frequency

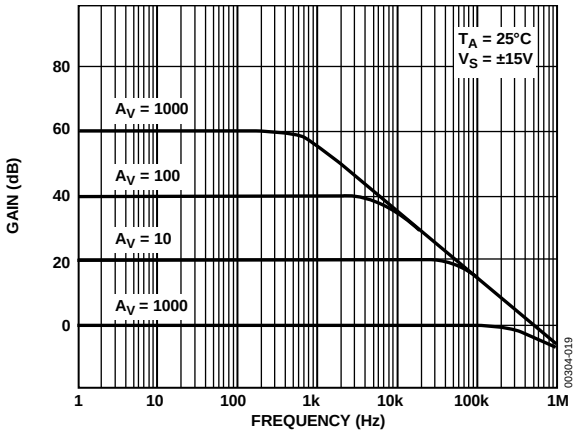


Figure 19. Closed-Loop Gain vs. Frequency

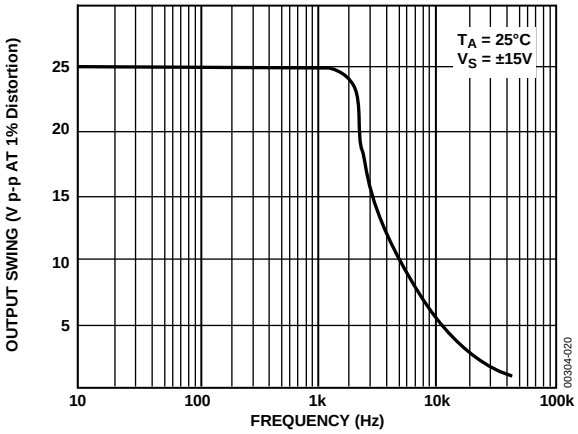


Figure 20. Maximum Output Swing Frequency

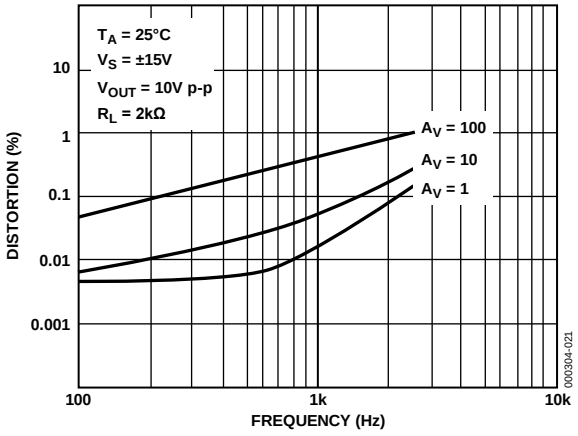


Figure 21. Total Harmonic Distortion vs. Frequency

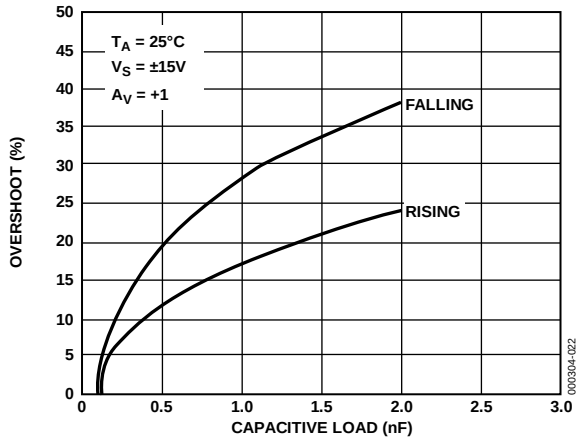


Figure 22. Overshoot vs. Capacitive Load

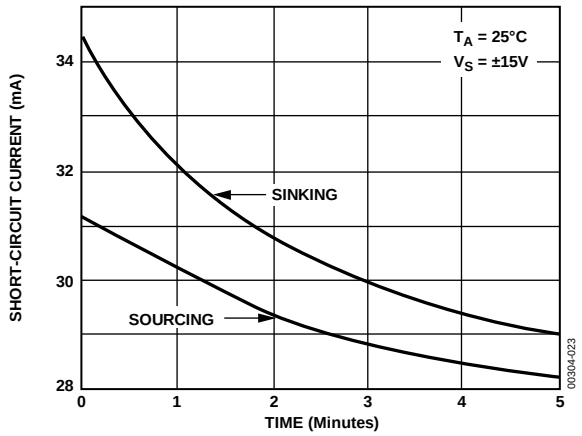


Figure 23. Short Circuit vs. Time

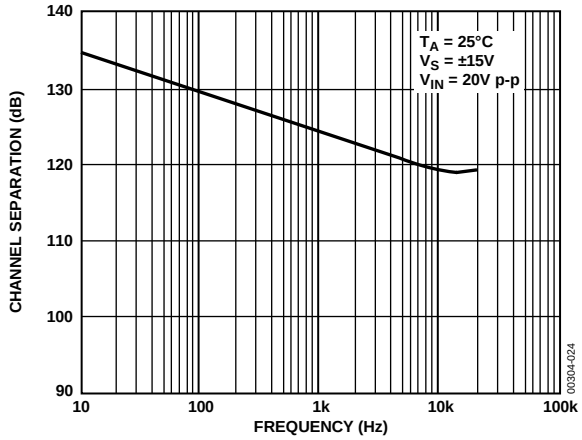


Figure 24. Channel Separation vs. Frequency

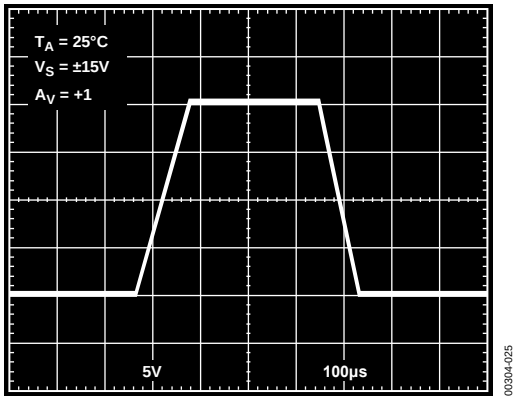


Figure 25. Large Signal Transient Response

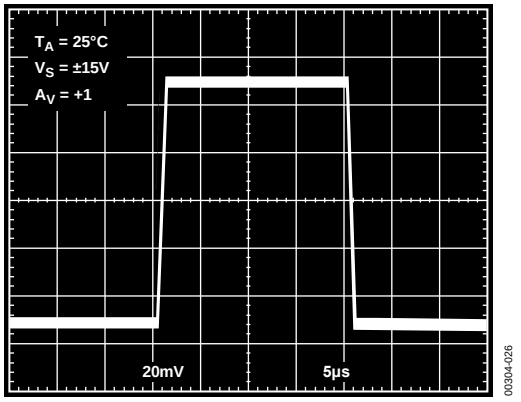


Figure 26. Small Signal Transient Response

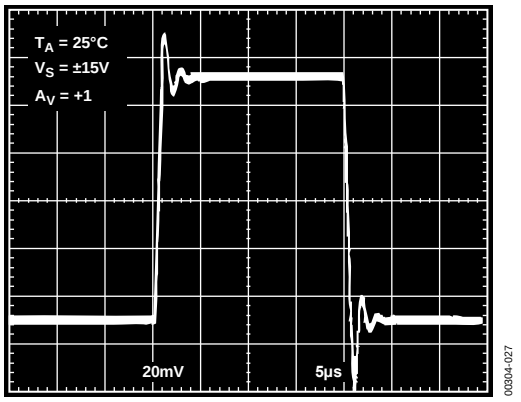


Figure 27. Small Signal Transient Response, C_{LOAD} = 1 nF

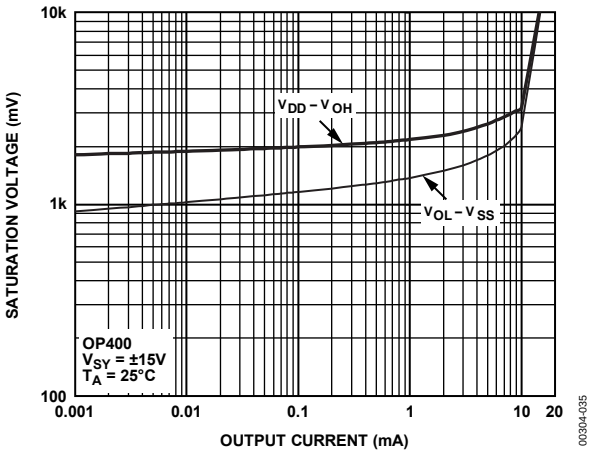


Figure 28. Saturation Voltage vs. Output Current

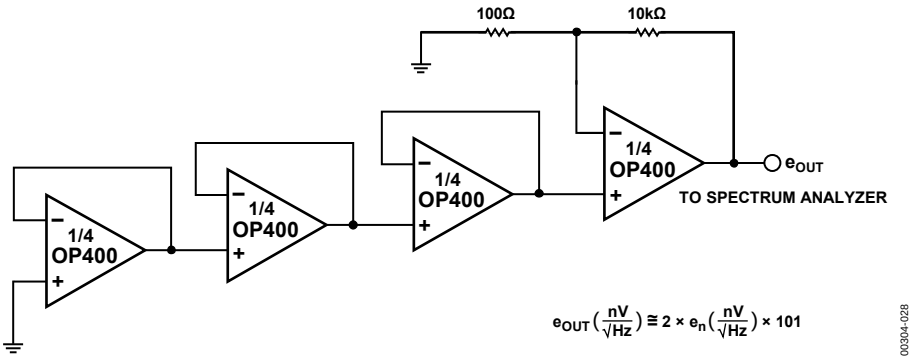


Figure 29. Noise Test Schematic

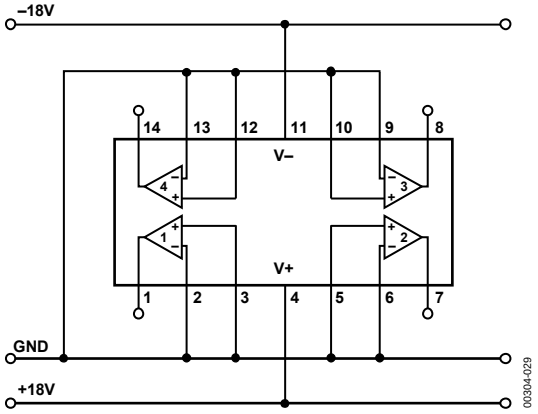


Figure 30. Burn-In Circuit

APPLICATIONS

The OP400 is inherently stable at all gains and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply decoupling is highly recommended. Proper supply decoupling reduces problems caused by supply line noise and improves the capacitive load-driving capability of the OP400.

Total supply current can be reduced by connecting the inputs of an unused amplifier to V−. This turns the amplifier off, lowering the total supply current.

DUAL LOW POWER INSTRUMENTATION AMPLIFIER

A dual instrumentation amplifier that consumes less than 33 mW of power per channel is shown in Figure 31. The linearity of the instrumentation amplifier exceeds 16 bits in gains of 5 to 200 and is better than 14 bits in gains from 200 to 1000. CMRR is above 115 dB (G = 1000). Offset voltage drift is typically 0.4 µV/°C over the military temperature range, which is comparable to the best monolithic instrumentation amplifiers. The bandwidth of the low power instrumentation amplifier is a function of gain and is shown in Table 6.

The output signal is specified with respect to the reference input, which is normally connected to analog ground. The reference input can be used to offset the output from −10 V to +10 V if required.

Table 6. Gain Bandwidth

Gain	Bandwidth
5	150 kHz
10	67 kHz
100	7.5 kHz
1000	500 Hz

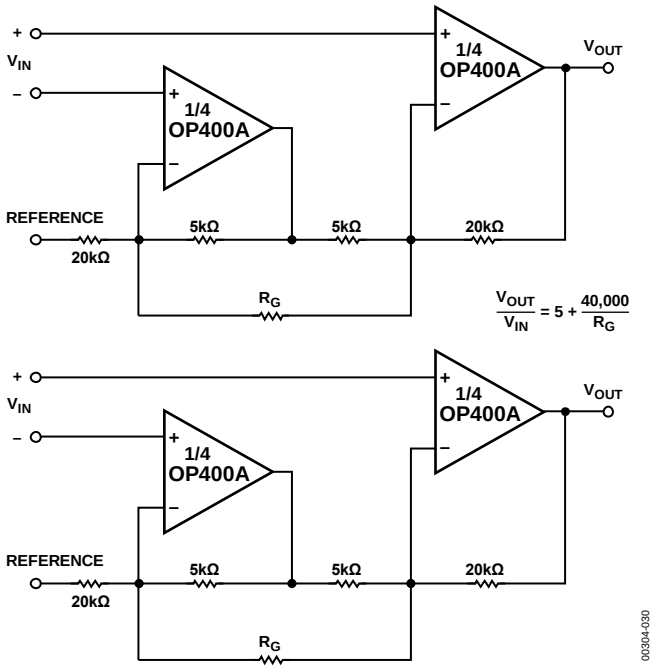


Figure 31. Dual Low Power Instrumentation Amplifier

BIPOLAR CURRENT TRANSMITTER

In the circuit of Figure 32, which is an extension of the standard three op amp instrumentation amplifier, the output current is proportional to the differential input voltage. Maximum output current is ±5 mA, with voltage compliance equal to ±10 V when using ±15 V supplies. Output impedance of the current transmitter exceeds 3 MΩ, and linearity is better than 16 bits with gain set for a full-scale input of ±100 μV.

DIFFERENTIAL OUTPUT INSTRUMENTATION AMPLIFIER

The output voltage swing of a single-ended instrumentation amplifier is limited by the supplies, normally at ±15 V, to a maximum of 24 V p-p. The differential output instrumentation amplifier shown in Figure 33 can provide an output voltage swing of 48 V p-p when operated with ±15 V supplies. The extended output swing is due to the opposite polarity of the outputs. Both outputs swing 24 V p-p, but with opposite polarity, for a total output voltage swing of 48 V p-p. The reference input can be used to set a common-mode output voltage over the range ±10 V. The PSRR of the amplifier is less than 1 μV/V with CMRR (G = 1000) better than 115 dB. Offset voltage drift is typically 0.4 μV/°C over the military temperature range.

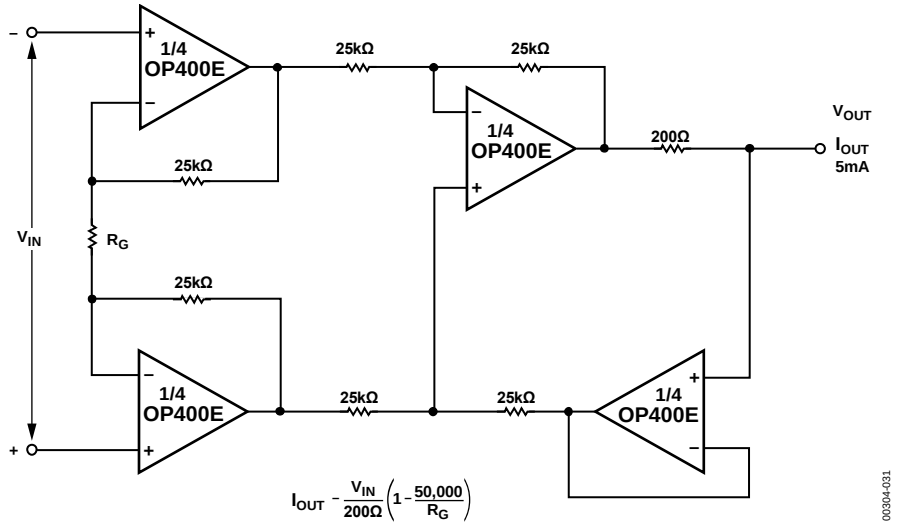


Figure 32. Bipolar Current Transmitter

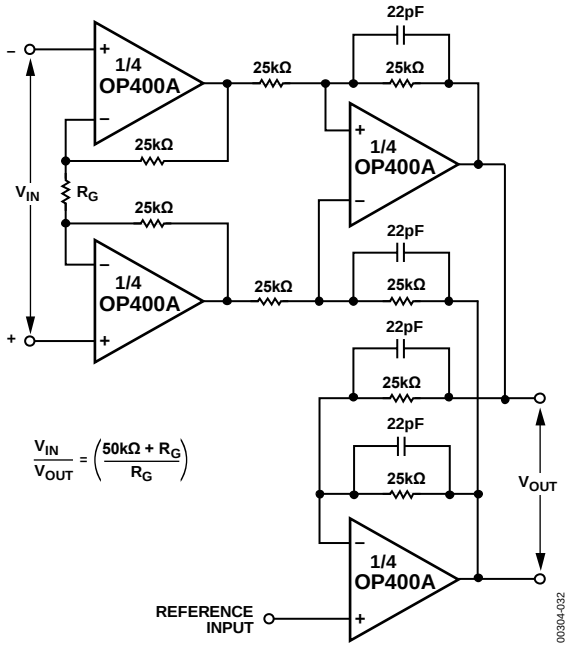


Figure 33. Differential Output Instrumentation Amplifier

MULTIPLE OUTPUT TRACKING VOLTAGE REFERENCE

Figure 34 shows a circuit that provides outputs of 10 V, 7.5 V, 5 V, and 2.5 V for use as a system voltage reference. Maximum output current from each reference is 5 mA with load regulation under 25 µV/mA. Line regulation is better than 15 µV/V, and output voltage drift is under 20 µV/°C. Output voltage noise from 0.1 Hz to 10 Hz is typically 75 µV p-p from the 10 V output and proportionately less from the 7.5 V, 5 V, and 2.5 V outputs.

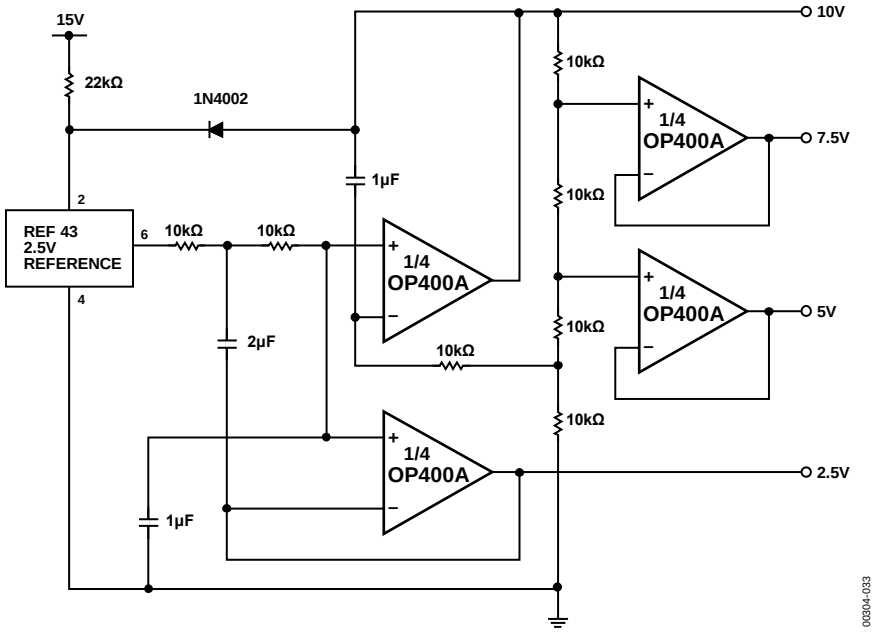
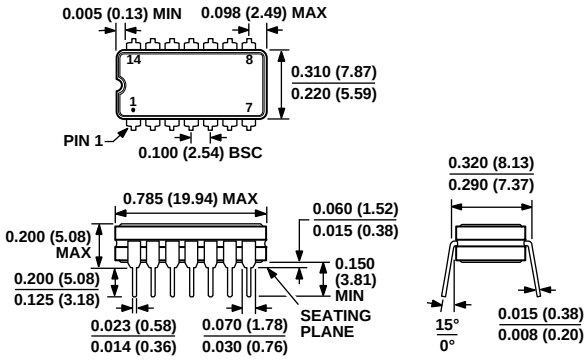


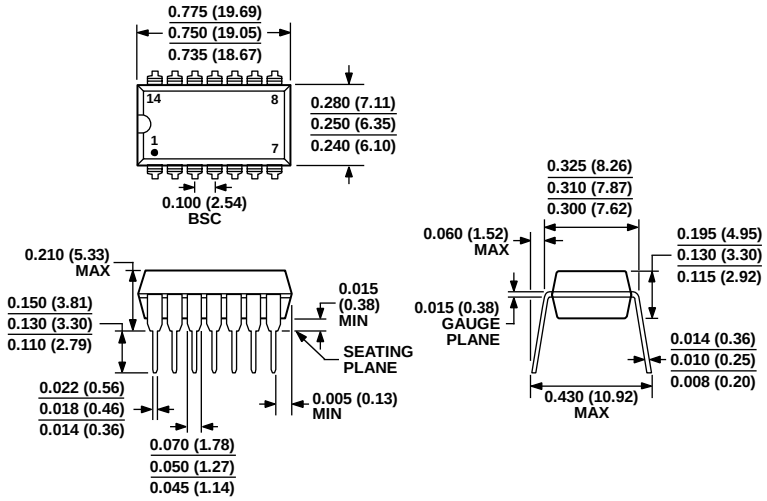
Figure 34. Multiple Output Tracking Voltage Reference

OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 35. 14-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-14)
[Y-Suffix]
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-001

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 36. 14-Lead Plastic Dual In-Line Package [PDIP]
(N-14)
[P-Suffix]
Dimensions shown in inches and (millimeters)

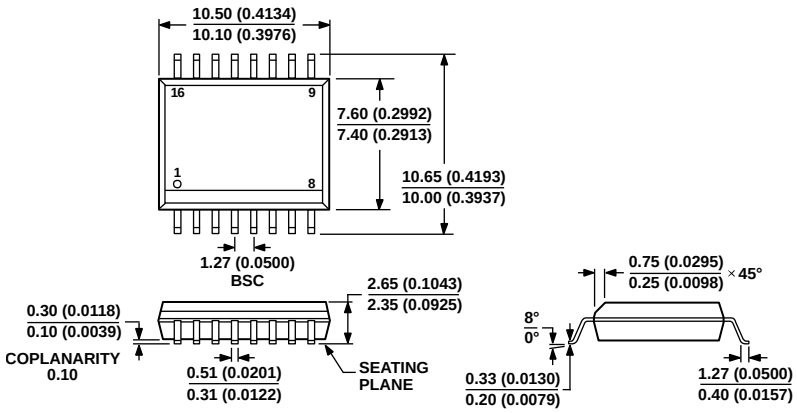


Figure 37. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-16)
[S-Suffix]
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
OP400AY	−55°C to +125°C	14-Lead CERDIP	Y-Suffix (Q-14)
OP400EY	−25°C to +85°C	14-Lead CERDIP	Y-Suffix (Q-14)
OP400FY	−25°C to +85°C	14-Lead CERDIP	Y-Suffix (Q-14)
OP400GP	0°C to +70°C	14-Lead PDIP	P-Suffix (N-14)
OP400GPZ	0°C to +70°C	14-Lead PDIP	P-Suffix (N-14)
OP400HPZ	−40°C to +85°C	14-Lead PDIP	P-Suffix (N-14)
OP400GS	0°C to +70°C	16-Lead SOIC_W	S-Suffix (RW-16)
OP400GS-REEL	0°C to +70°C	16-Lead SOIC_W	S-Suffix (RW-16)
OP400GSZ	0°C to +70°C	16-Lead SOIC_W	S-Suffix (RW-16)
OP400GSZ-REEL	0°C to +70°C	16-Lead SOIC_W	S-Suffix (RW-16)
OP400HS	−40°C to +85°C	16-Lead SOIC_W	S-Suffix (RW-16)
OP400HS-REEL	−40°C to +85°C	16-Lead SOIC_W	S-Suffix (RW-16)
OP400HSZ	−40°C to +85°C	16-Lead SOIC_W	S-Suffix (RW-16)
OP400HSZ-REEL	−40°C to +85°C	16-Lead SOIC_W	S-Suffix (RW-16)
OP400GBC		Die	

[1] Z = RoHS Compliant Part.

SMD PARTS AND EQUIVALENTS

SMD Part Number[1]	Analog Devices Equivalent
5962-8777101M3A	OP400ATCMDA
5962-8777101MCA	OP400AYMDA

[1] For military processed devices, please refer to the standard microcircuit drawing (SMD) available at the Defense Supply Center Columbus website.

NOTES

D00304-0-1/13(H)