

PCMF2DFN1; PCMF3DFN1

Common-mode EMI filter for differential channels with integrated ESD protection

Rev. 2 — 28 April 2014

Product data sheet

1. Product profile

1.1 General description

The devices are common-mode ElectroMagnetic Interference (EMI) filters with integrated ElectroStatic Discharge (ESD) protection for two and three differential channels. The devices are designed to provide low insertion loss for differential high-speed signals on each channel while unwanted common-mode signals are attenuated.

Each differential channel incorporates two signal lines that are coupled by integrated coils. Diodes provide protection to downstream components from ESD voltages up to ± 15 kV on each signal line.

Table 1. Product overview

Type number	Number of channels	Package		
		Name	Version	
PCMF2DFN1	2	DFN2520-9	SOT1333-1	XSON9
PCMF3DFN1	3	DFN4020-14	SOT1334-1	XSON14

1.2 Features and benefits

- Two and three differential channels common-mode EMI filter with integrated ESD protection
- Superior common-mode suppression over a wide frequency range
- ESD protection up to ± 15 kV contact discharge according to IEC 61000-4-2
- Maximum package height: 0.5 mm

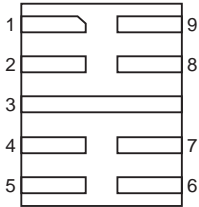
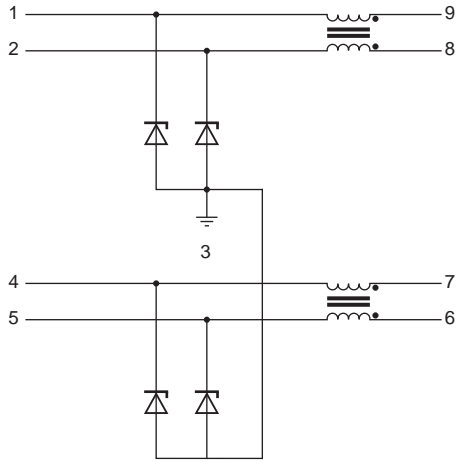
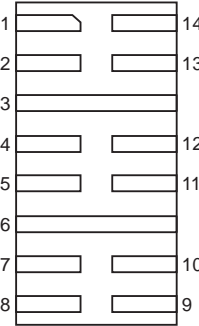
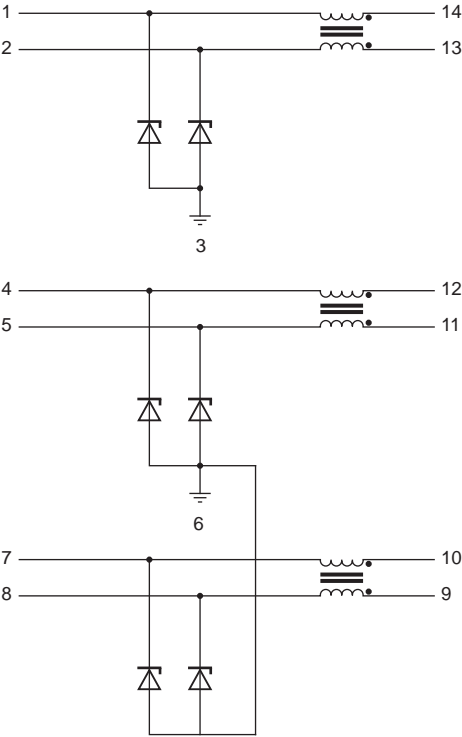
1.3 Applications

- Smartphone, cellular and cordless phone
- MIPI D-PHY as used in Camera Serial Interface (CSI) and Display Serial Interface (DSI)
- General-purpose EMI and Radio-Frequency Interference (RFI) filter and downstream ESD protection
- Tablet PC and Mobile Internet Device (MID)
- High-Definition Multimedia Interface (HDMI)



2. Pinning information

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
PCMF2DFN1 (SOT1333-1)				
1	CH1_IN+	input channel 1	 <p>Transparent top view DFN2520-9</p>	 <p>aaa-007385</p>
2	CH1_IN-	input channel 1		
3	GND	ground		
4	CH2_IN+	input channel 2		
5	CH2_IN-	input channel 2		
6	CH2_OUT-	output channel 2		
7	CH2_OUT+	output channel 2		
8	CH1_OUT-	output channel 1		
9	CH1_OUT+	output channel 1		
PCMF3DFN1 (SOT1334-1)				
1	CH1_IN+	input channel 1	 <p>Transparent top view DFN4020-14</p>	 <p>aaa-007384</p>
2	CH1_IN-	input channel 1		
3	GND_1	ground 1		
4	CH2_IN+	input channel 2		
5	CH2_IN-	input channel 2		
6	GND_2	ground 2		
7	CH3_IN+	input channel 3		
8	CH3_IN-	input channel 3		
9	CH3_OUT-	output channel 3		
10	CH3_OUT+	output channel 3		
11	CH2_OUT-	output channel 2		
12	CH2_OUT+	output channel 2		
13	CH1_OUT-	output channel 1		
14	CH1_OUT+	output channel 1		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PCMF2DFN1	DFN2520-9	plastic extremely thin small outline package; no leads; 9 terminals; body 2 × 2.5 × 0.5 mm	SOT1333-1
PCMF3DFN1	DFN4020-14	plastic extremely thin small outline package; no leads; 14 terminals; body 2 × 4 × 0.5 mm	SOT1334-1

4. Marking

Table 4. Marking codes

Type number	Marking code
PCMF2DFN1	MP1
PCMF3DFN1	CMFMP1

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage		-0.5	5	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4; all input pins to ground			
		contact discharge	-15	15	kV
		air discharge	-15	15	kV
		IEC 61000-4-2, level 4; all output pins to ground			
		contact discharge	-2	2	kV
		air discharge	-2	2	kV
T_{stg}	storage temperature		-55	+125	°C
T_{amb}	ambient temperature		-40	+85	°C

6. Characteristics

6.1 Channel characteristics

Table 6. Channel characteristics

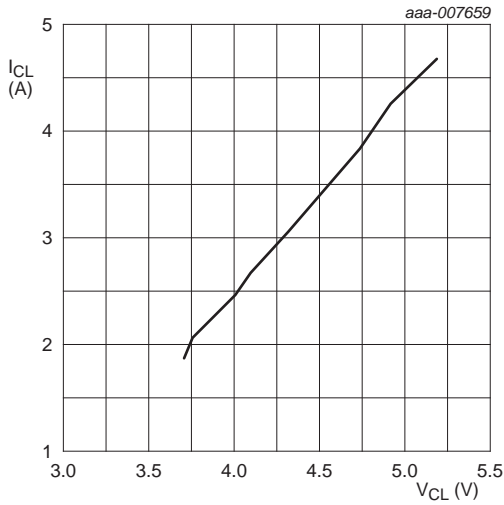
$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{s(ch)}$	channel series resistance	single line; input to output	-	5	-	Ω
C_d	diode capacitance	$f = 1\text{ MHz}$; $V_I = 2.5\text{ V}$ [1]	-	0.6	0.75	pF
I_{RM}	reverse leakage current	per line; $V_I = 5\text{ V}$	-	-	100	nA
V_{BR}	breakdown voltage	$I_R = 10\text{ mA}$	6	-	9	V
V_F	forward voltage	$I_F = 10\text{ mA}$	0.6	-	1.1	V
R_{dyn}	dynamic resistance	TLP [2]				
		positive transient	-	0.6	-	Ω
		negative transient	-	0.6	-	Ω
		surge [3]				
		positive transient	-	0.6	-	Ω
		negative transient	-	0.6	-	Ω
V_{CL}	clamping voltage	positive transient; $I_{PP} = 4\text{ A}$ [3]	-	4.8	-	V
		negative transient; $I_{PP} = -5\text{ A}$ [3]	-	-3.6	-	V
		TLP; $I_{CL} = 8\text{ A}$	-	8	-	V
		TLP; $I_{CL} = 12\text{ A}$	-	10.5	-	V
		TLP; $I_{CL} = 16\text{ A}$	-	13.4	-	V
		TLP; $I_{CL} = -8\text{ A}$	-	-6	-	V
		TLP; $I_{CL} = -12\text{ A}$	-	-8.4	-	V
		TLP; $I_{CL} = -16\text{ A}$	-	-10.7	-	V

[1] This parameter is guaranteed by design.

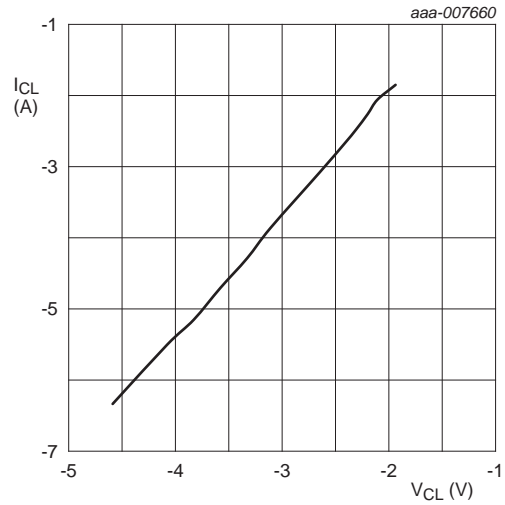
[2] 100 ns Transmission Line Pulse (TLP); 50 Ω ; pulser at 70 to 90 ns.

[3] According to IEC 61000-4-5 (8/20 μs).



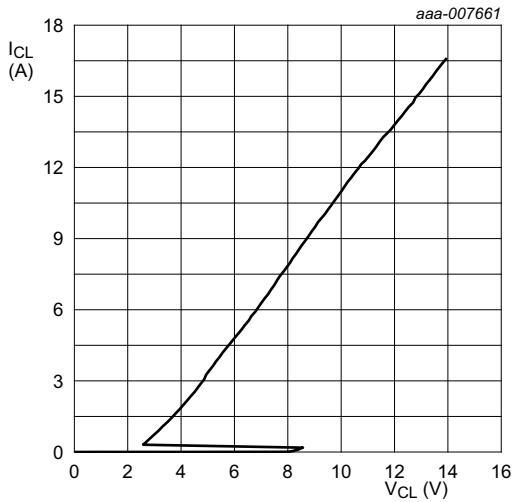
IEC 61000-4-5; $t_p = 8/20 \mu s$; positive pulse

Fig 1. Dynamic resistance with positive clamping; typical values



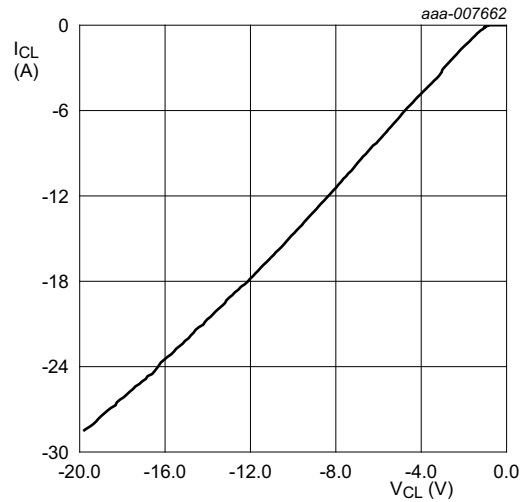
IEC 61000-4-5; $t_p = 8/20 \mu s$; negative pulse

Fig 2. Dynamic resistance with negative clamping; typical values



$t_p = 100 ns$; Transmission Line Pulse (TLP)

Fig 3. Dynamic resistance with positive clamping; typical values



$t_p = 100 ns$; Transmission Line Pulse (TLP)

Fig 4. Dynamic resistance with negative clamping; typical values

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

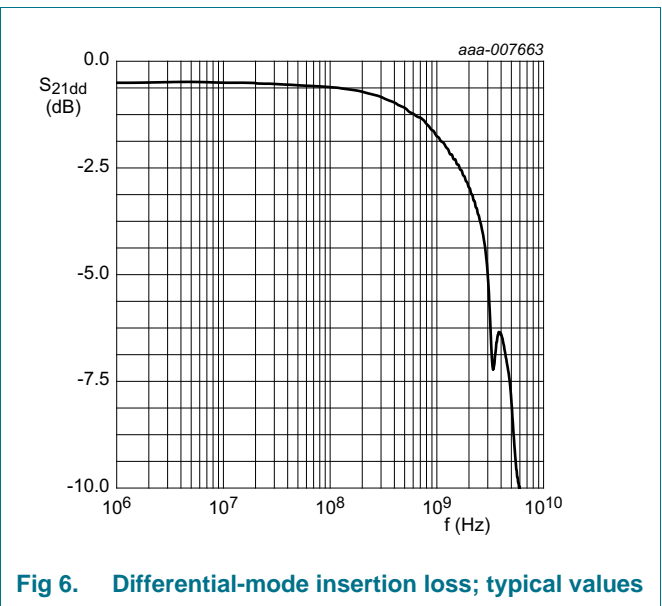
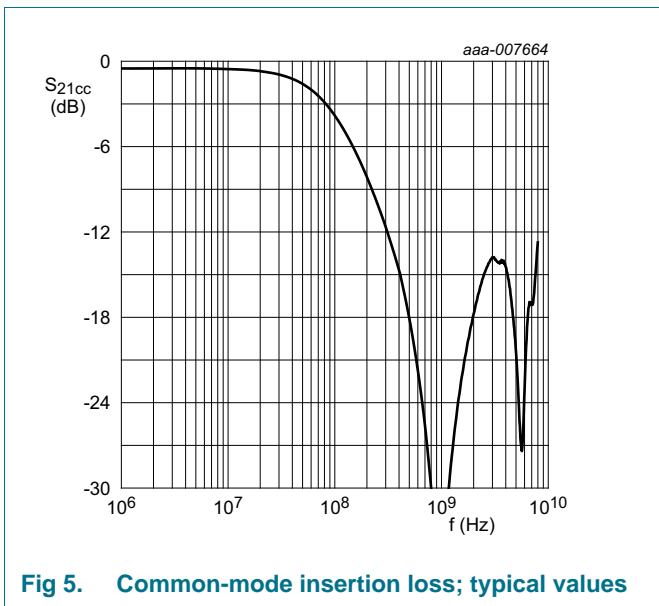
6.2 Frequency characteristics

Table 7. Frequency characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Common mode: S_{21cc}						
α_{il}	insertion loss		[1]			
		$f = 400 \text{ MHz}$	-	15	-	dB
		$f = 800 \text{ MHz}$	-	30	-	dB
		$f = 5 \text{ GHz}$	-	21	-	dB
Differential mode: S_{21dd}						
α_{il}	insertion loss	$f = 1 \text{ MHz}$	[1]	0.6	-	dB
f_{-3dB}	cut-off frequency		[1][2]	2.2	-	GHz

[1] Measured with 4-port network analyzer; $R_{gen} = 50 \Omega$; $R_L = 50 \Omega$.

[2] Normalized to attenuation at 1 MHz.



7. Application information

7.1 Application diagram

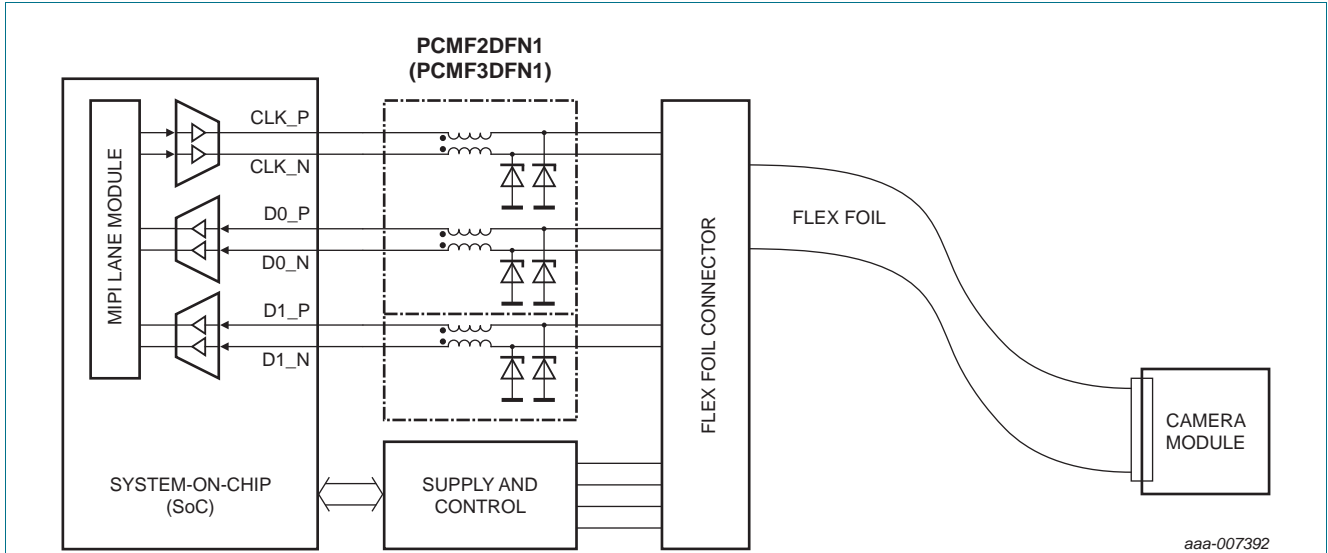


Fig 7. Application diagram for MIPI D-PHY CSI

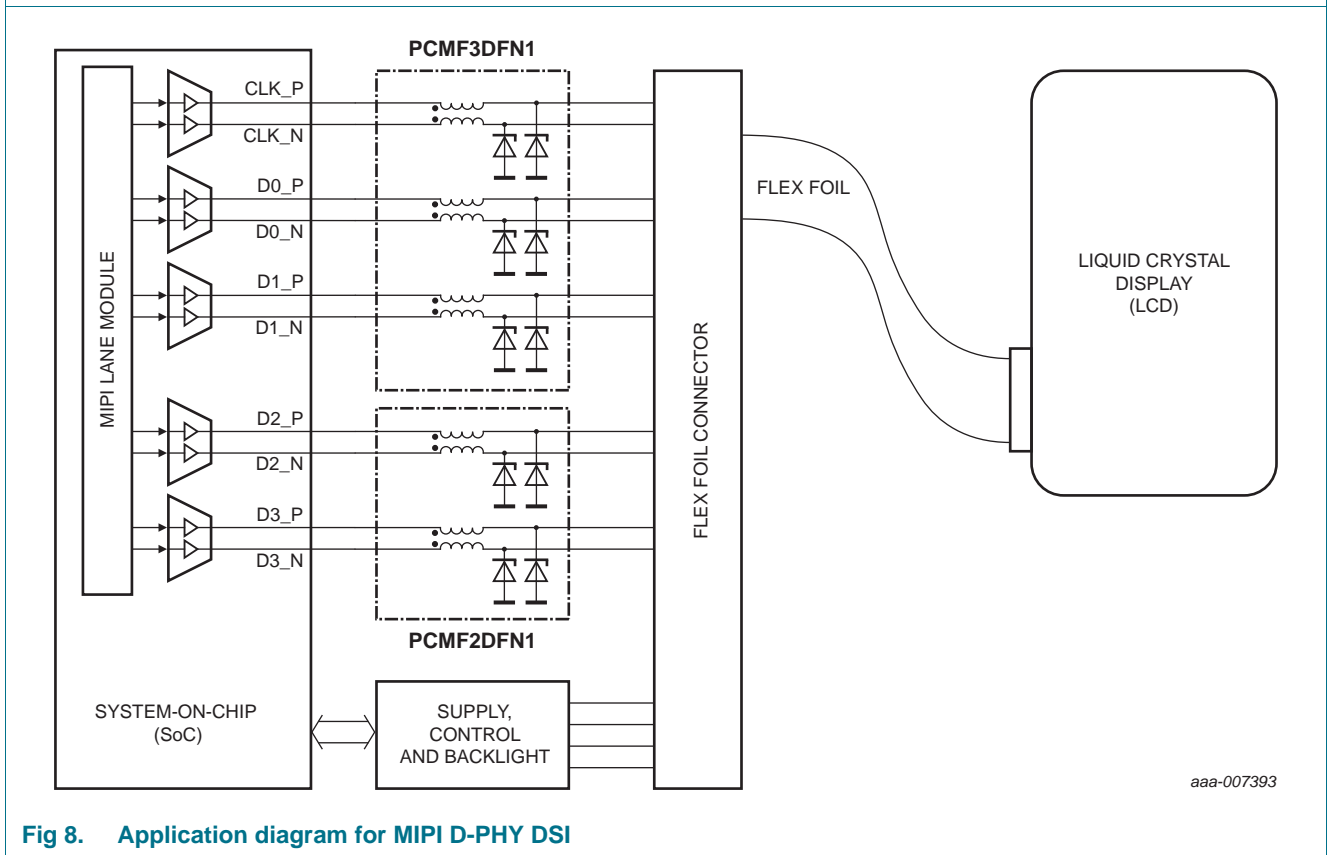
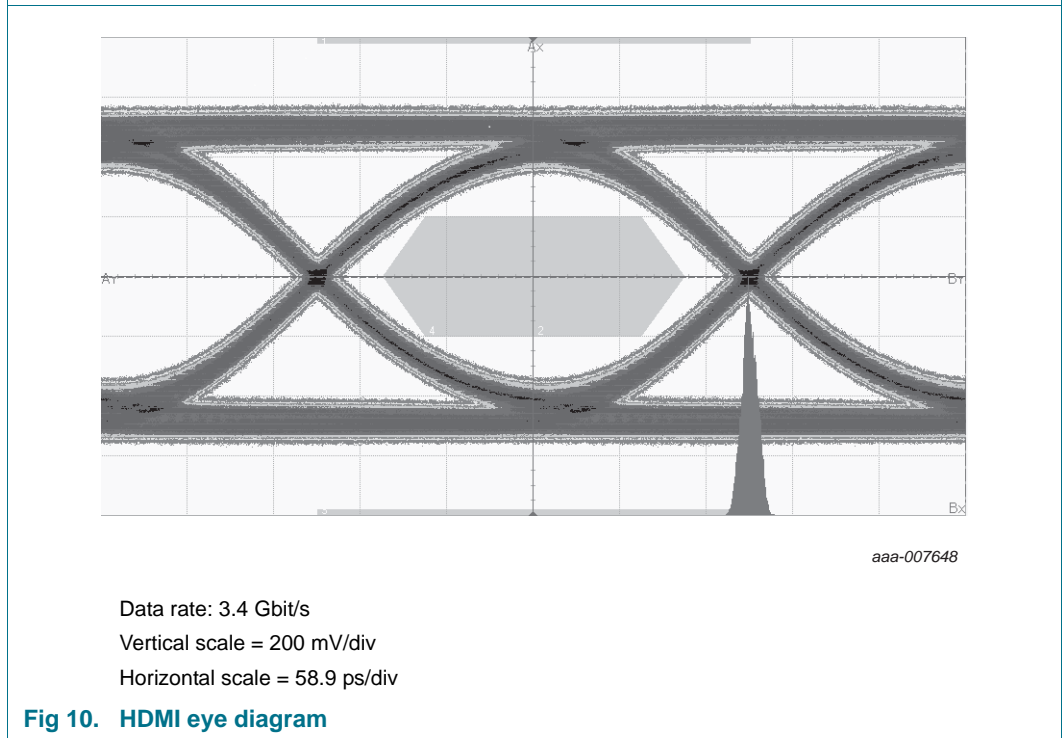
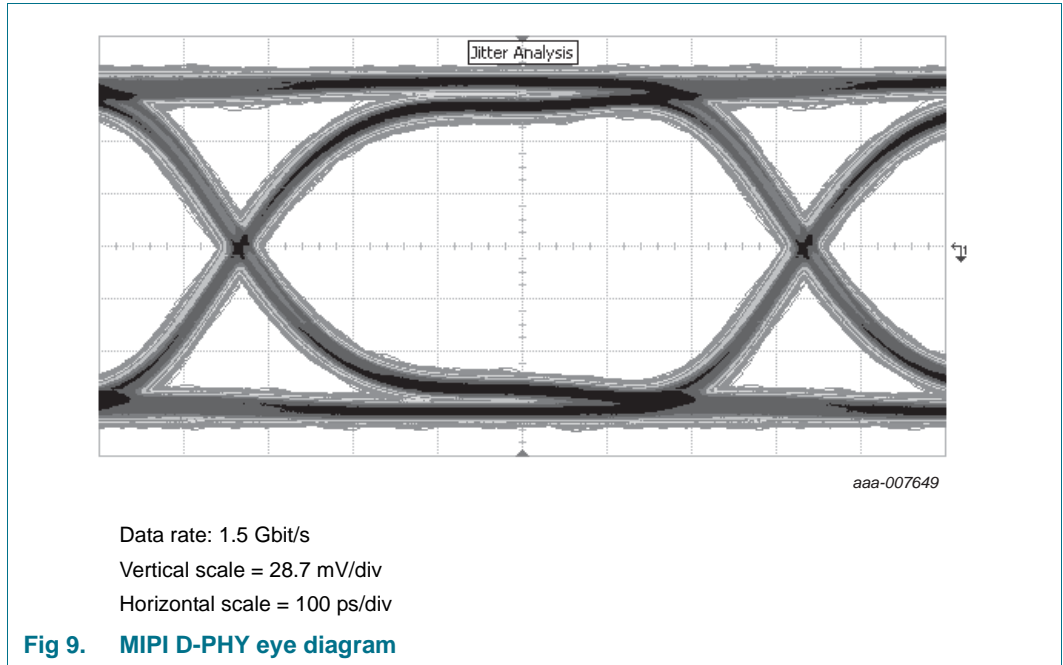


Fig 8. Application diagram for MIPI D-PHY DSI

7.2 Eye diagram



8. Package outline

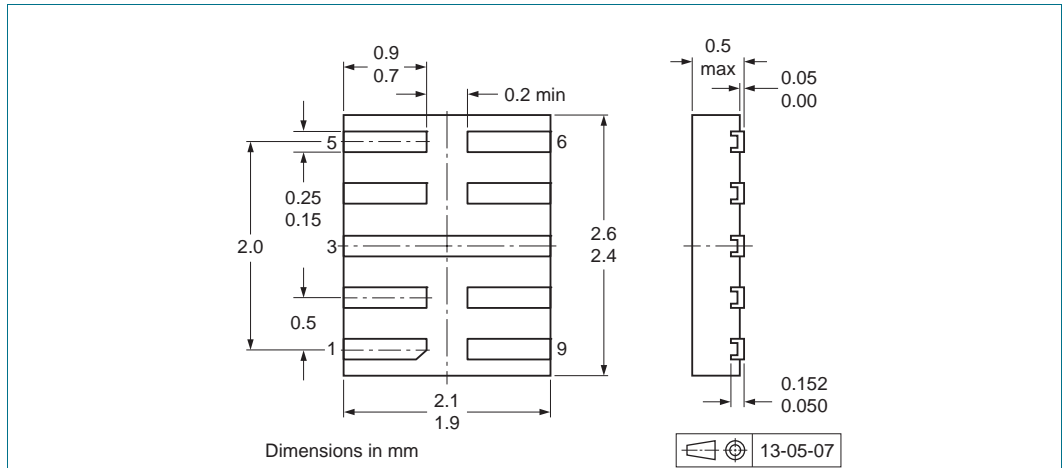


Fig 11. Package outline DFN2520-9 (SOT1333-1)

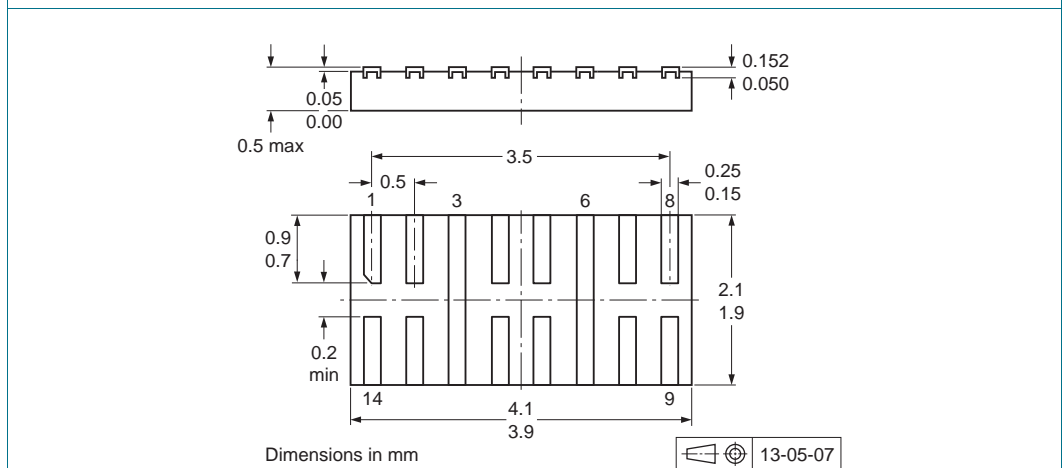


Fig 12. Package outline DFN4020-14 (SOT1334-1)

9. Soldering

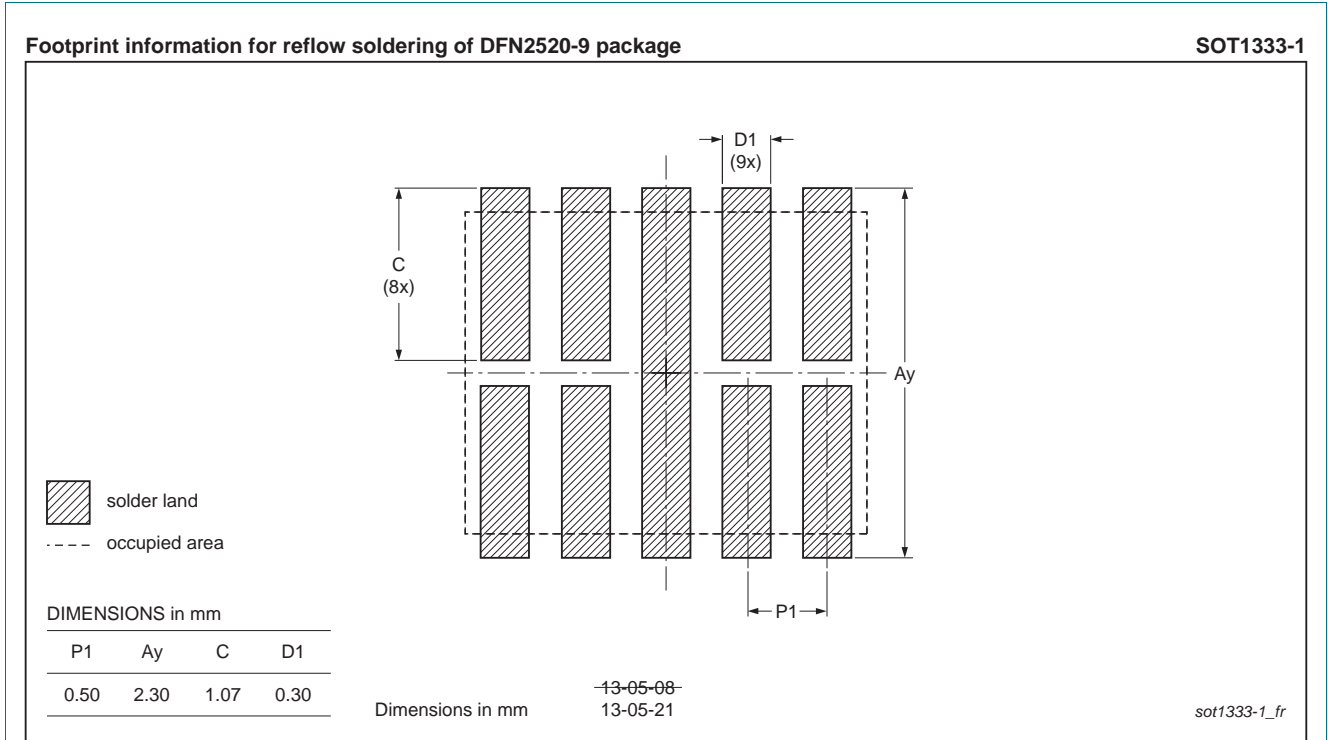


Fig 13. Reflow soldering footprint DFN2520-9 (SOT1333-1)

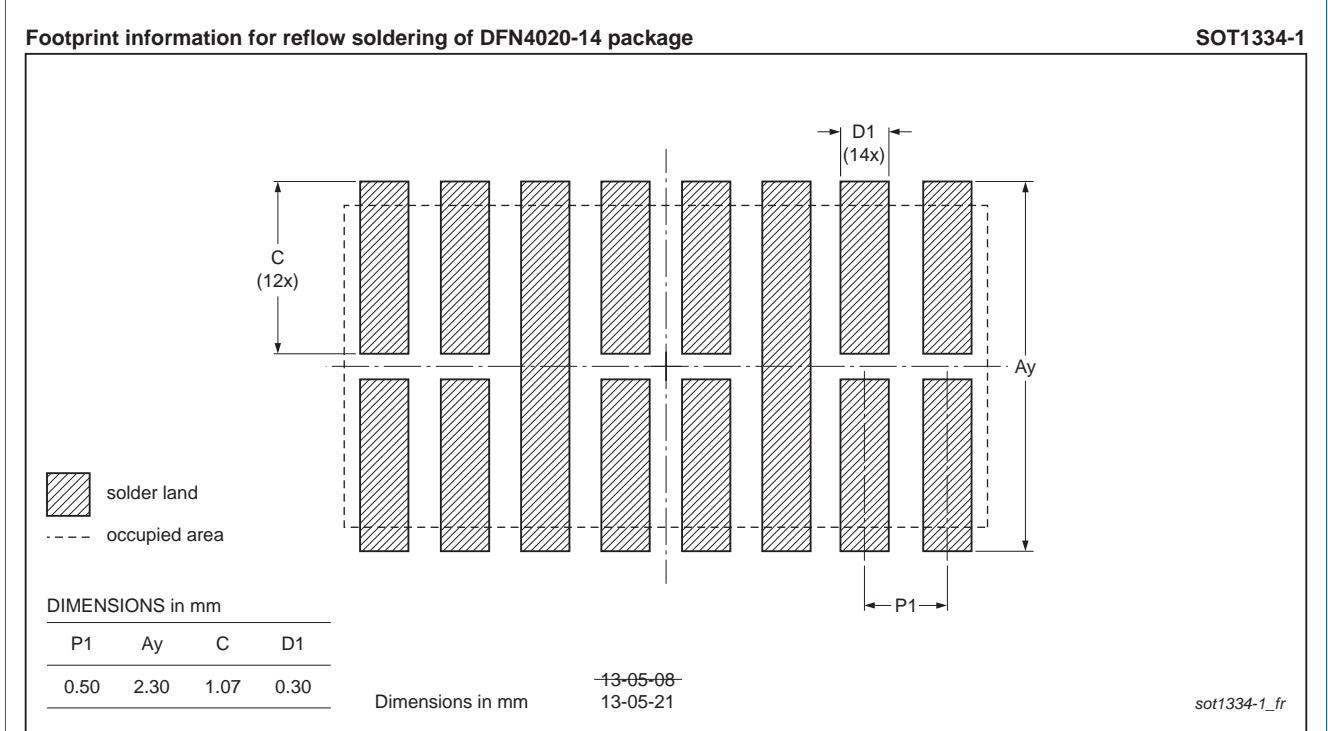


Fig 14. Reflow soldering footprint DFN4020-14 (SOT1334-1)

10. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCMF2DFN1_PCMF3DFN1 v.2	20140428	Product data sheet	-	PCMF2DFN1_PCMF3DFN1 v.1
Modification:	• Surge rating adapted			
PCMF2DFN1_PCMF3DFN1 v.1	20130606	Product data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

11.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

11.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the

product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

11.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

12. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

13. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
2	Pinning information	2
3	Ordering information	3
4	Marking	3
5	Limiting values	3
6	Characteristics	4
6.1	Channel characteristics	4
6.2	Frequency characteristics	6
7	Application information	7
7.1	Application diagram	7
7.2	Eye diagram	8
8	Package outline	9
9	Soldering	10
10	Revision history	11
11	Legal information	12
11.1	Data sheet status	12
11.2	Definitions	12
11.3	Disclaimers	12
11.4	Trademarks	13
12	Contact information	13
13	Contents	14

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2014. All rights reserved.

For more information, please visit: <http://www.nxp.com>
 For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 28 April 2014

Document identifier: PCMF2DFN1_PCMF3DFN1