



# BUK98180-100A

## N-channel TrenchMOS logic level FET

16 March 2016

Product data sheet

### 1. General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

### 2. Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant
- Suitable for logic level gate drive sources

### 3. Applications

- 12 V, 24 V and 42 V loads
- Automotive and general purpose power switching
- Motors, lamps and solenoids

### 4. Quick reference data

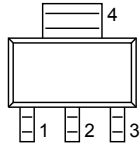
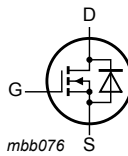
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	-	100	V
$I_D$	drain current	$V_{GS} = 5\text{ V}$ ; $T_{sp} = 25\text{ °C}$ ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	-	4.6	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	8	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 5\text{ A}$ ; $T_j = 25\text{ °C}$	-	147	173	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ ; $I_D = 5\text{ A}$ ; $T_j = 25\text{ °C}$	-	-	201	m $\Omega$
		$V_{GS} = 5\text{ V}$ ; $I_D = 5\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	153	180	m $\Omega$
<b>Avalanche ruggedness</b>						
$E_{DS(AL)}$	non-repetitive drain-source avalanche energy	$I_D = 4\text{ A}$ ; $V_{sup} \leq 100\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 5\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped	-	-	16	mJ



## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>SC-73 (SOT223)</p>	 <p>mbb076</p>
2	D	drain		
3	S	source		
4	D	drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK98180-100A	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223
BUK98180-100A/CU	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK98180-100A	918010
BUK98180-100A/CU	918010

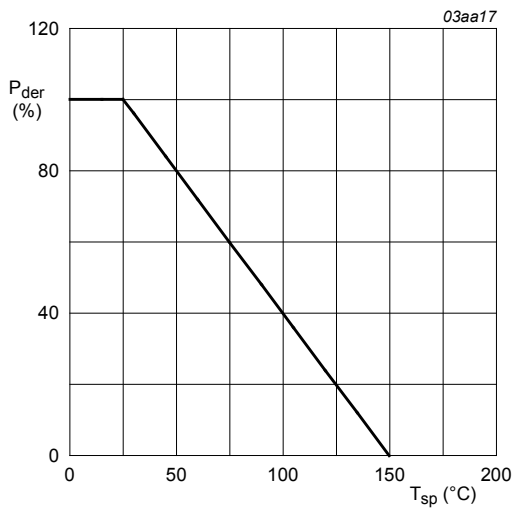
## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

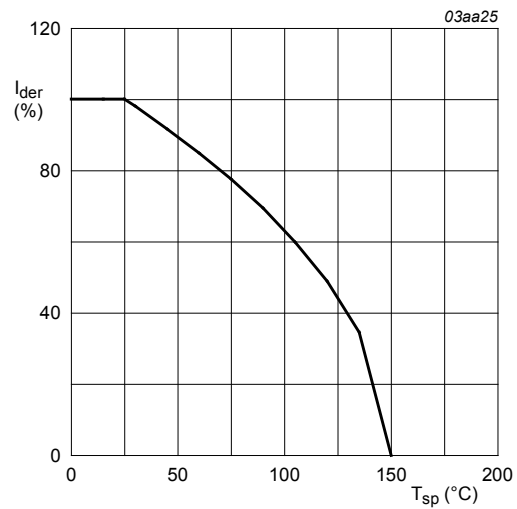
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	100	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	100	V
$V_{GS}$	gate-source voltage		-10	10	V
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	8	W
$I_D$	drain current	$T_{sp} = 25\text{ °C}$ ; $V_{GS} = 5\text{ V}$ ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	4.6	A
		$T_{sp} = 100\text{ °C}$ ; $V_{GS} = 5\text{ V}$ ; <a href="#">Fig. 2</a>	-	3	A
$I_{DM}$	peak drain current	$T_{sp} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; <a href="#">Fig. 3</a>	-	18	A

Symbol	Parameter	Conditions	Min	Max	Unit
T <sub>stg</sub>	storage temperature		-55	150	°C
T <sub>j</sub>	junction temperature		-55	150	°C
V <sub>GSM</sub>	peak gate-source voltage	pulsed; t <sub>p</sub> ≤ 50 μs	-15	15	V
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>sp</sub> = 25 °C	-	4.6	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>sp</sub> = 25 °C	-	18	A
<b>Avalanche ruggedness</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 4 A; V <sub>sup</sub> ≤ 100 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 5 V; T <sub>j(init)</sub> = 25 °C; unclamped	-	16	mJ



**Fig. 1. Normalized total power dissipation as a function of solder point temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$



**Fig. 2. Normalized continuous drain current as a function of solder point temperature**

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

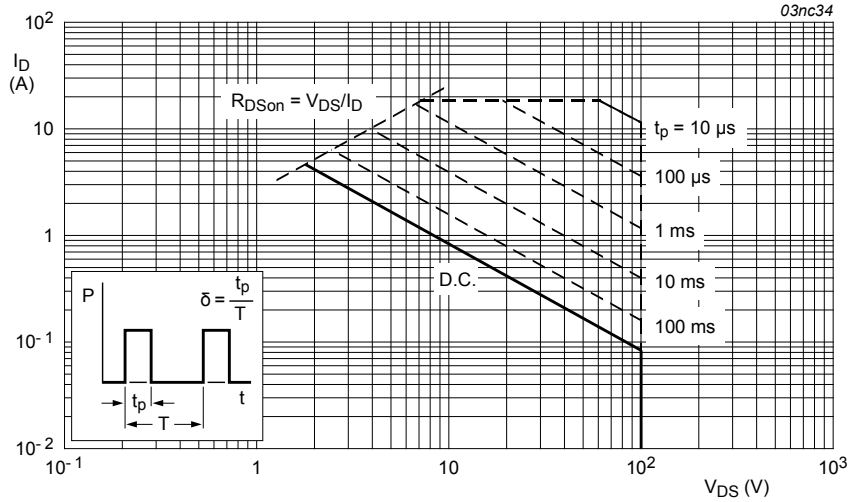


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{amb} = 25^\circ C; I_{DM}$  is single pulse

### 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Fig. 4	-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	120	-	K/W

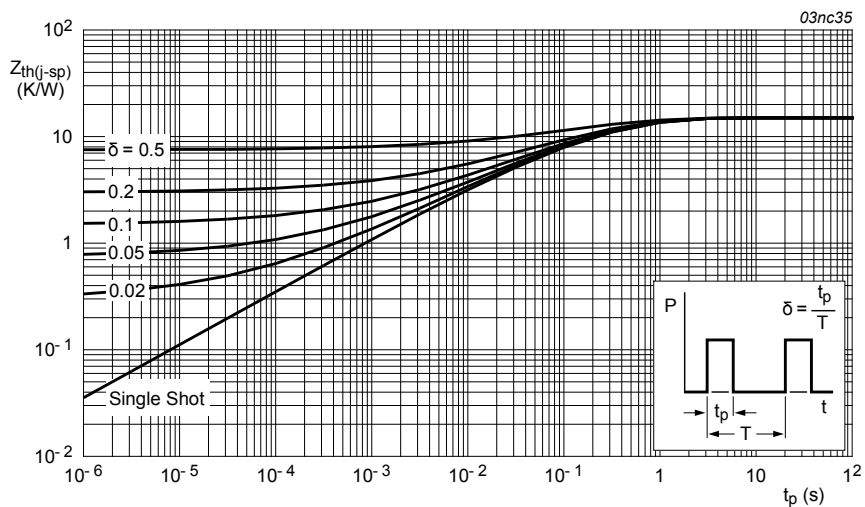
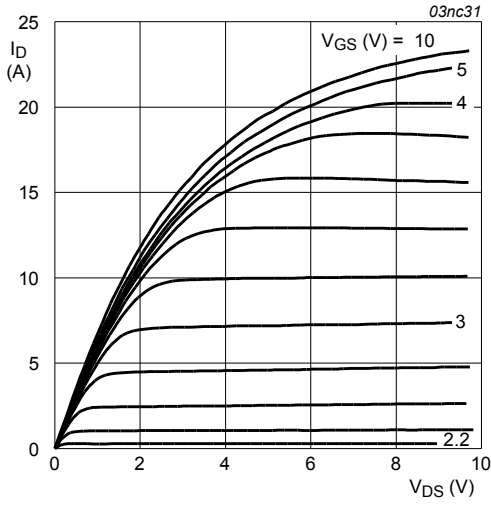


Fig. 4. Transient thermal impedance from junction to solder point as a function of pulse duration

## 10. Characteristics

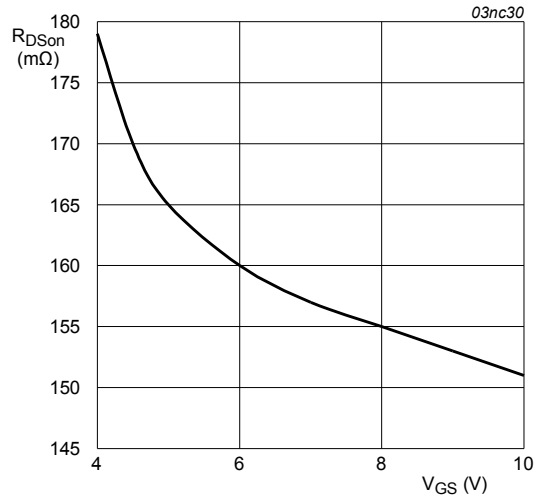
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	100	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	89	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 11</a>	1	1.5	2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ <a href="#">Fig. 11</a>	-	-	2.3	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C};$ <a href="#">Fig. 11</a>	0.6	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.05	10	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	147	173	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	-	201	m $\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 12;</a> <a href="#">Fig. 13</a>	-	153	180	m $\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ <a href="#">Fig. 12;</a> <a href="#">Fig. 13</a>	-	-	389	m $\Omega$
<b>Dynamic characteristics</b>						
$C_{iss}$	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 14</a>	-	464	619	pF
$C_{oss}$	output capacitance		-	60	72	pF
$C_{rss}$	reverse transfer capacitance		-	36	50	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \text{ } \Omega; V_{GS} = 5 \text{ V};$ $R_{G(ext)} = 10 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	7	-	ns
$t_r$	rise time		-	89	-	ns
$t_{d(off)}$	turn-off delay time		-	18	-	ns
$t_f$	fall time		-	25	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 5 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 15</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s};$	-	49	-	ns
$Q_r$	recovered charge	$V_{GS} = -10 \text{ V}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	130	-	nC



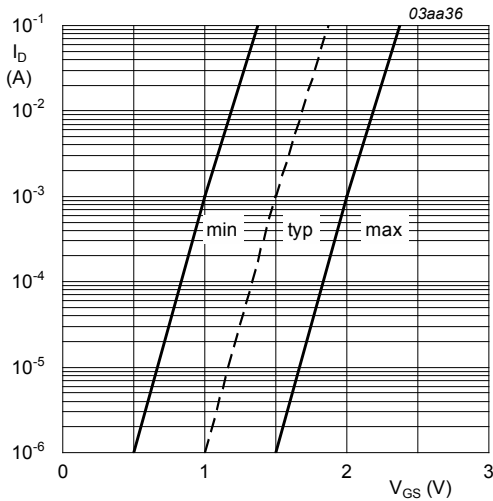
**Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values**

$T_j = 25^\circ\text{C}$



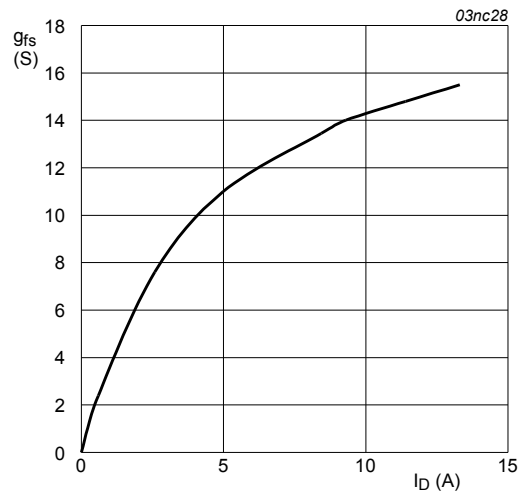
**Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values**

$T_j = 25^\circ\text{C}; I_D = 5\text{A}$



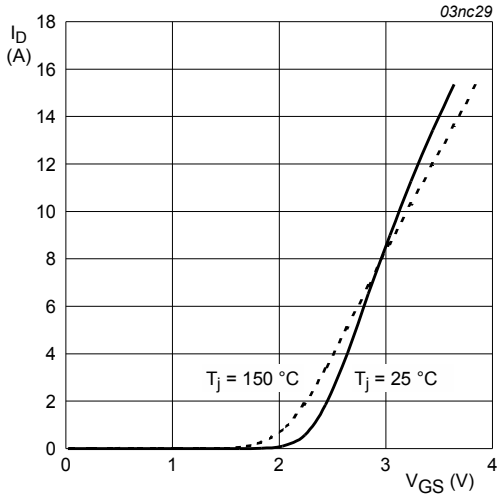
**Fig. 7. Sub-threshold drain current as a function of gate-source voltage**

$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$



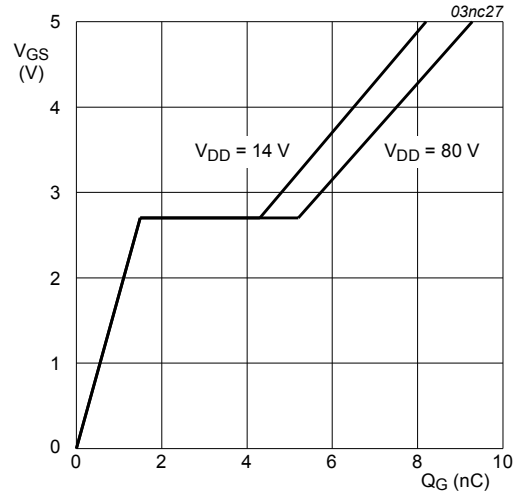
**Fig. 8. Forward transconductance as a function of drain current; typical values**

$T_j = 25^\circ\text{C}; V_{DS} = 25\text{V}$



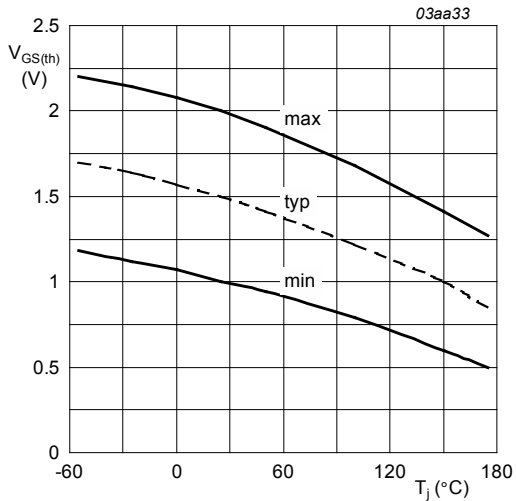
**Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values**

$V_{DS} = 25V$



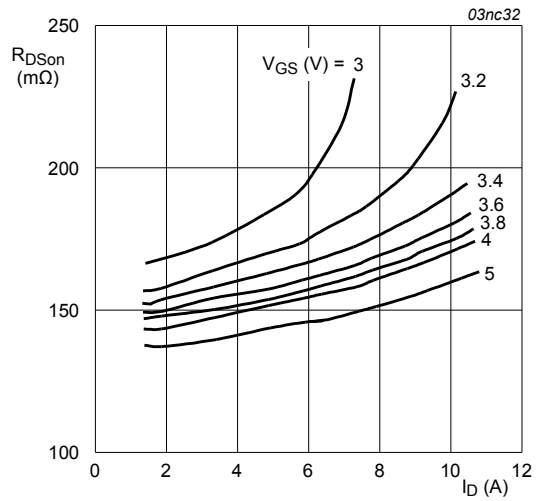
**Fig. 10. Gate-source voltage as a function of turn-on gate charge; typical values**

$T_j = 25^\circ C; I_D = 5A$



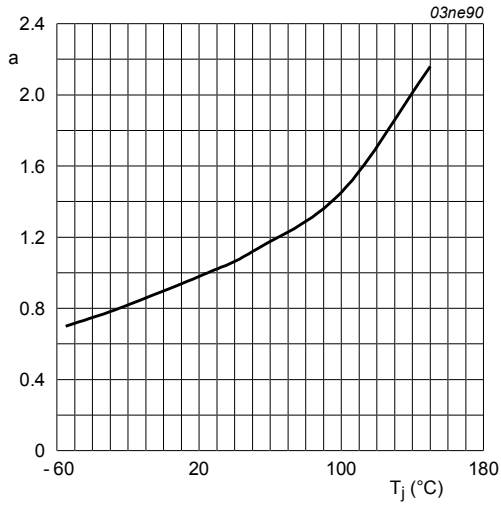
**Fig. 11. Gate-source threshold voltage as a function of junction temperature**

$I_D = 1mA; V_{DS} = V_{GS}$



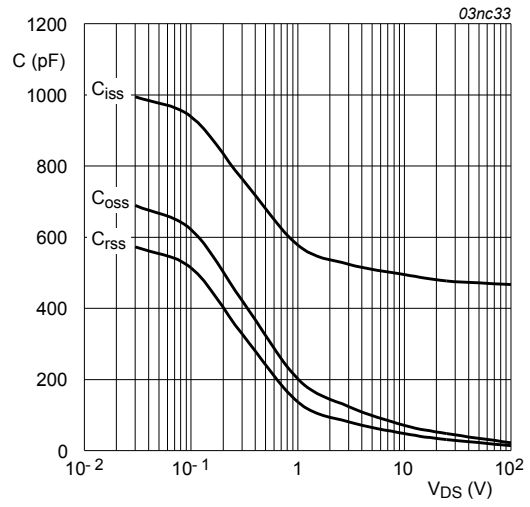
**Fig. 12. Drain-source on-state resistance as a function of drain current; typical values**

$T_j = 25^\circ C$



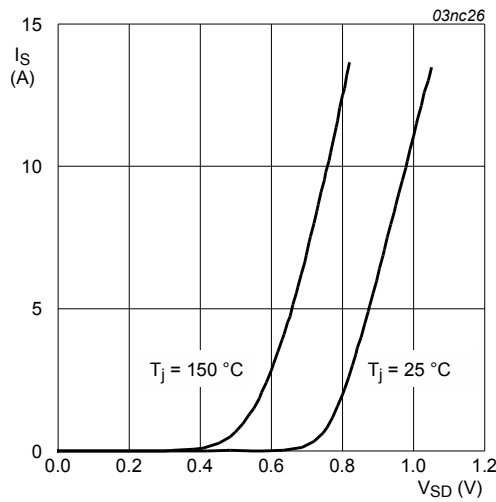
**Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature**

$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}C)}$$



**Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

$V_{GS} = 0V; f = 1MHz$



**Fig. 15. Reverse diode current as a function of reverse diode voltage; typical value**

$V_{GS} = 0V$



### 11. Package outline

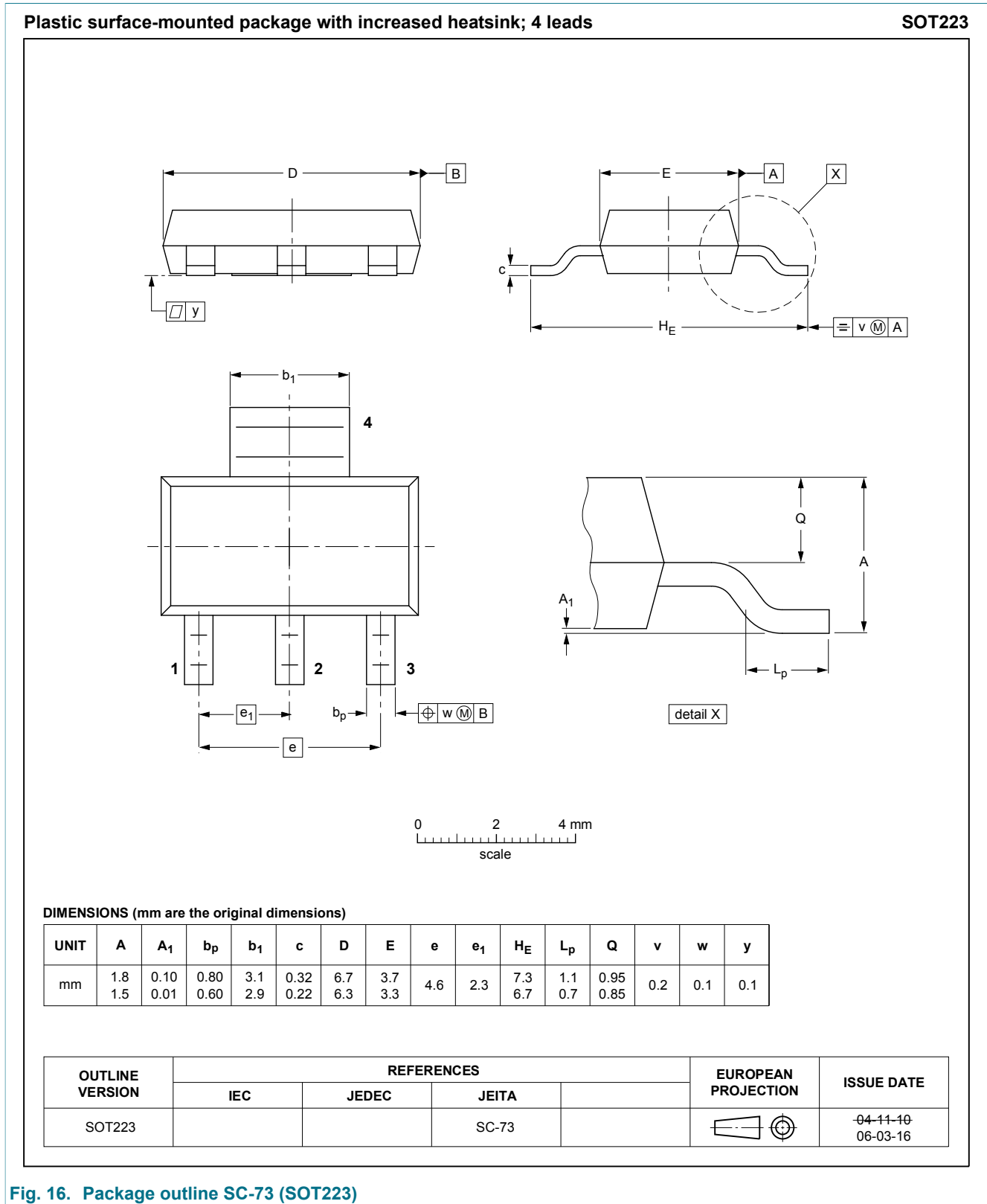


Fig. 16. Package outline SC-73 (SOT223)

## 12. Legal information

### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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