3.5A Synchronous Buck Li-ion Charger With Intelligent Path Management and Adapter Adaptive

General Description

The LP28501 is a 3.5A Li-Ion battery charger intended for 4.4V~14V wall adapters. It utilizes a high efficiency synchronous buck converter topology to reduce power dissipation during charging. The LP28501 includes complete charge termination circuitry, automatic recharge and a ±1% 4.2V/4.3V /4.35V float voltage.

The LP28501 could manage the power supply for system intelligently. The adapter would satisfy the system`s demand firstly, then charge battery with extra current output capacity from adapter. If the current capacity of adapter could not meet the system demand, the adapter and battery would supply power for system together. When the adapter`s current capacity is low than the set charge current, the LP28501 would decrease the charge current automatically to keep the output of adapter would not be pull down by the chip.

Additional features include shorted cell detection; temperature qualified charging and overvoltage protection. The LP28501 is available in a low profile QFN-28 package.

Order Information

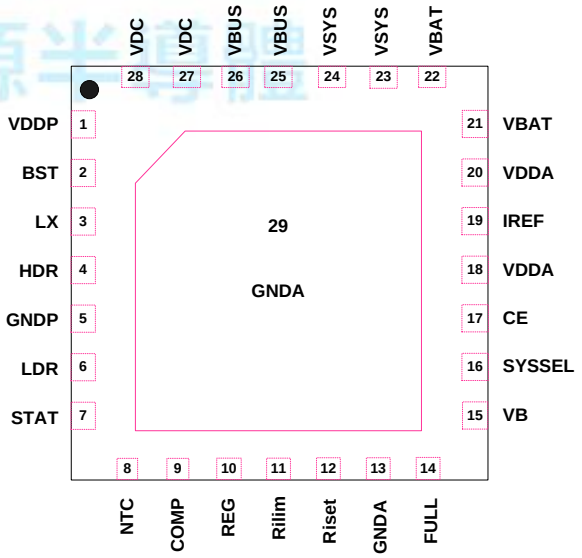
LP28501 □ □ □

- F: Pb-Free
- Package Type
  - QV: QFN-28

Features

- Power Path Management Intelligently
- Adapter Adaptive
- CHARGE:
  - Very Low Power Dissipation
  - 3.5A Maximum Charge Current
  - Efficiency up to 90%
  - Input voltage: 4.4V~14V
  - Programmable charge complete voltage: 4.2V /4.3V /4.35V
  - Operation with Thermal Regulation to Maximize Charge Rate Without Risk of Overheating
  - Charges Single Cell Li-Ion Batteries Directly from USB Port
- Available in QFN28(4*4mm) Package
- RoHS Compliant and 100% Lead (Pb)-Free

Functional Pin Description



TOP VIEW

Applications

- Quick charge 2.0/3.0 (QC2.0 / QC3.0)
- Portable Media Players
- Cellular and Smart mobile phone
- PDA/DSC
- Handheld Battery-Powered Devices
- Handheld Computers
- Charging Docks and Cradles

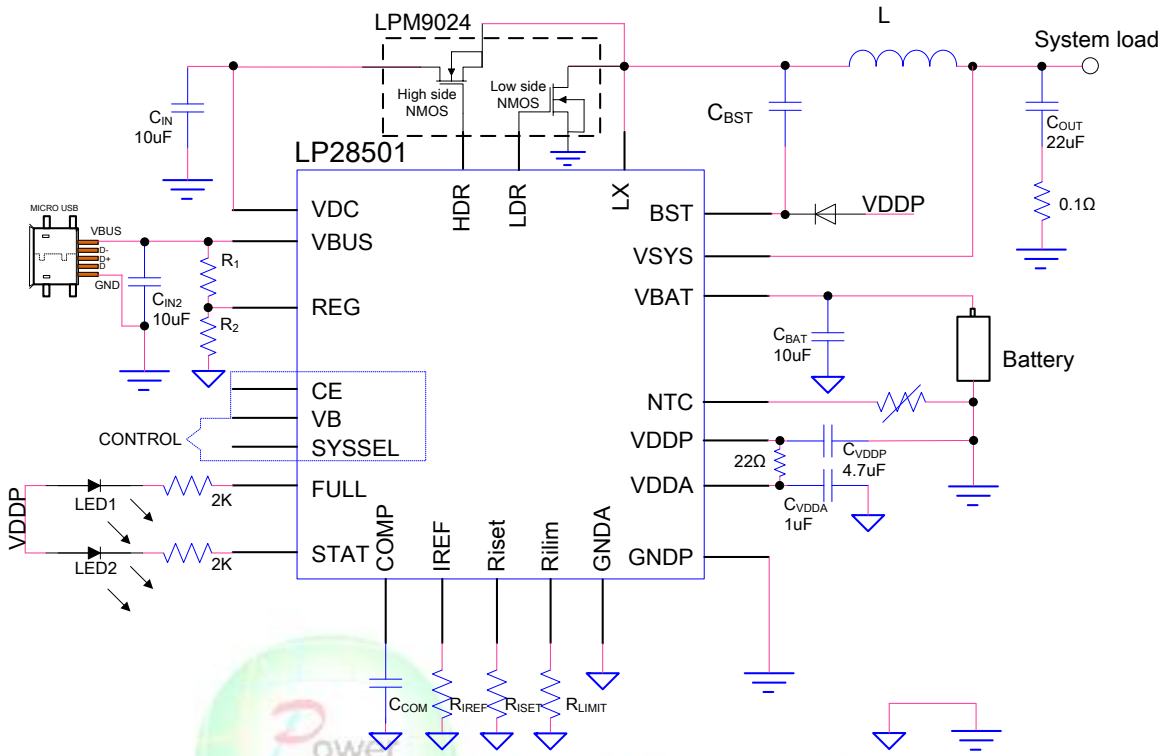
Marking Information

Device	Marking	Package	Shipping
LP28501QVF	LPS LP28501 YWX	QFN-28	3K/REEL
Y: Year code. W: Week code. X: Batch numbers.			

Pin Description

Pin	Name	Description
1	**VDDP**	Internal LDO output. Connect a decoupling 4.7uF capacitor to GNDP.
2	**BST**	Positive supply for the high side driver. A 0.22μF capacitor should be placed between BST and LX.
3	**LX**	Switching Node Connection.
4	**HDR**	High side drive gate.
5	**GNDP**	Ground for Power section.
6	**LDR**	Low side drive gate.
7	**STAT**	Indicates charge status. Active low when charging is on. STAT will blink with timeout, vsysovp, NTC fault.
8	**NTC**	Connect a 10K NTC resistor to GNDA, 100uA(constant current source) current output from NTC pin.
9	**COMP**	Compensation pin, a 2.2nF ceramic capacitor is needed from COMP to GNDA.
10	**REG**	Input voltage feedback for the input voltage regulation loop. Connect to tap of an external resistor divider from VBUS to GNDA to program the input voltage regulation. Once the voltage at REG pin drops to the inner threshold, the charge current is reduced to maintain the input voltage at the regulation value.
11	**Rilim**	Adapter current limit setting pin. A resistor RLIMT is needed from Rilim to GNDA. Adapter current is programmed by $I_{LIMT}(A) = 550 \times \frac{2V}{Rilim(\Omega)}$. This pin could not be floating. Recommend: 40K> R_{ilim} >0.37K. The chip would set the max input current limit when 0.37K> $R_{ilim.}$
12	**Riset**	Charging current setting pin, a resistor RISET is needed from Riset to GNDA. CC current is programmed by $I_{CHG}(A) = \frac{1500V}{R_{ISET}(\Omega)}$. The internal reference for Riset comparator is 1.5V when Vbat > VTRIKL. Recommend： 6.8K> R_{ISET} >0.43K.
13,29	**GNDA**	Ground for the analog circuits.
14	**FULL**	Battery full indication pin, active low.
15	**VB**	Programmable battery-full voltage. Connect to GND for 4.35V,leave floating to 4.2V, and connect to VDDA for 4.3V.
16	**SYSSEL**	Programmable VSYS minimum voltage. Connect to GND for 3V,leave floating to 3.3V, and connect to VDDA for3.5V.
17	**CE**	Charge enable pin. Active high or floating.
19	**IREF**	Current reference generator. A 100k resistor connect to GNDA, internal voltage reference is 1V.
18,20	**VDDA**	Power supply for the internal analog circuit.
21,22	**VBAT**	Battery charger output and battery voltage sense pin. Connect to battery cell.
23,24	**VSYS**	System voltage output.
25,26	**VBUS**	USB or adapter input.
27,28	**VDC**	A capacitor is needed from this pin to GNDP.

Typical Application Circuit



Absolute Maximum Ratings Note 1

- ✧ Input and Vout to GND(VDC,VBUS) ---------- -0.3V to 18V
- ✧ Other Pin to GND---------- -0.3V to 6.5V
- ✧ LX voltage to GND---------- -0.3V to 18V
- ✧ HDR,BST voltage to GND---------- -0.3V to 23V
- ✧ BST referred to LX---------- -0.3V to 6.5V
- ✧ BAT Short-circuit Duration---------- Continuous
- ✧ Maximum Junction Temperature ---------- 150°C
- ✧ Storage Temperature ---------- -45℃ to 165℃
- ✧ Operating Junction Temperature Range (TJ) ---------- -40℃ to 85°C
- ✧ Maximum Soldering Temperature (at leads, 10 sec) ---------- 260°C

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- ✧ Maximum Power Dissipation (QFN-28, PD,TA=25°C) ---------- 2.5W
- ✧ Thermal Resistance (QFN-28, JA) ---------- 50℃/W

ESD Susceptibility

- ✧ HBM(Human Body Mode) Note 2 ---------- 2KV
- ✧ MM(Machine Mode) Note 3 ---------- 200V

Note 2. The Human body model (HBM) is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. The testing is done according JEDEC.

Note 3. Machine Model (MM) is a 200pF capacitor discharged through a 500nH inductor with no series resistor into each pin. The testing is done according JEDEC.

Electrical Characteristics

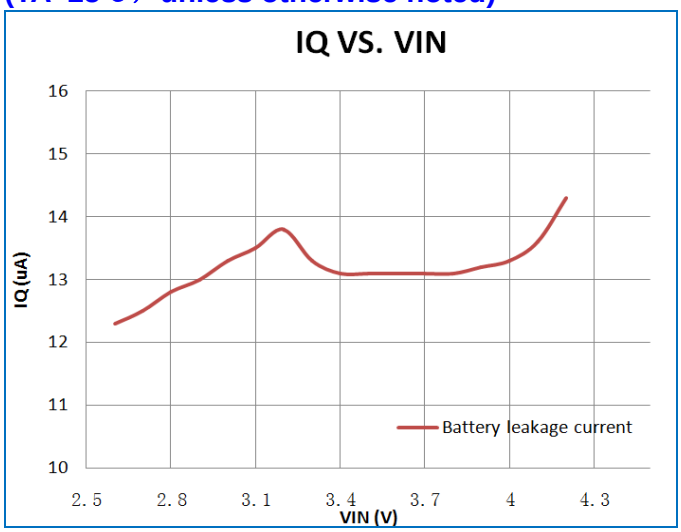
(The specifications which apply over the full operating temperature range, otherwise specifications are at TA = 25°C. Vin = 5V, unless otherwise noted.)

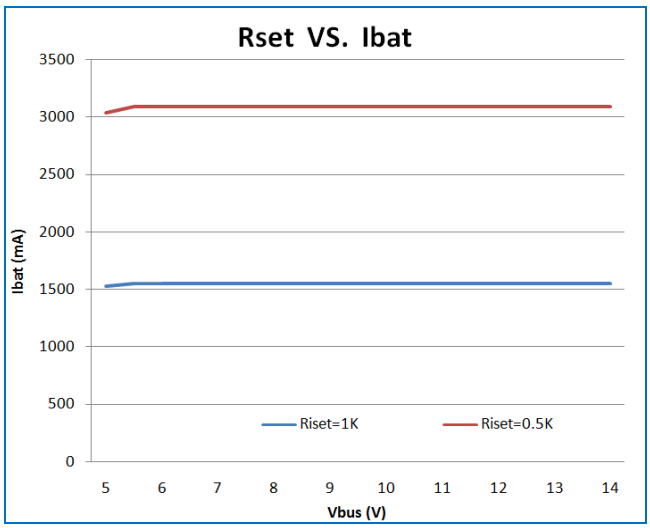
Parameter	Test Conditions	Measured	Limits			Units
			Min	Typ	Max	
VBUS, VSYS,VDD						
Input voltage		Vbus	4.4		14	V
VBUS port protection threshold	VBUS Rising	UVLO	4.15	4.25	4.35	V
	VBUS Falling		3.95	4.05	4.15	
Input voltage regulation reference		V_{REG}	2.3	2.4	2.5	V
VSYS over voltage protection	SYSSEL = float, Vbat=2V			3.3		V
	SYSSEL = high, Vbat=2V			3.5		V
	SYSSEL = low, Vbat=2V			3.0		V
VDDP/VDDA				5		V
POWER PATH MANAGEMENT						
VDC Power by USB/Adapter MOSFET Rdson	1A current Load	R(VBUS,VDC)		50		mΩ
Switch between VSYS and VBAT	Vbat=4.2V, VBUS absent, Ibat=3A	R(VSYS, VBAT)	-	40		mΩ
QUIESCENT CURRENTS						
VBUS Current	VBUS=4V	Ibus		80		uA
Battery Discharge Current in Standby mode	VBAT=4.2V, VBUS absent	I_{BAT}	-	15	-	μA
Charger Controller						
Trickle charge Condition	Vbat<1.4V	V_{Riset}		0.04		V
	1.4V<Vbat<VTRICKL			0.2		
Vbat voltage	VB=float, RSET=1K,Ibat=100mA		4.158	4.2	4.242	V
	VB=high, RSET=1K,Ibat=100mA			4.3		
	VB=low, RSET=1K,Ibat=100mA			4.35		
Charge Current in CC Mode	RSET=1K,VBAT=3.6V	Ibat		1500		mA
	RSET=0.5K,VBAT=3.6V			3000		
Current Mode (CC)		V_{Riset}	1.45	1.5	1.55	V
Trickle charge voltage threshold	Vbat rising	V_{trikl}	2.8	2.9	3.0	V
Trickle charge voltage threshold hysteresis		V_{trhys}	-	200	-	mV
Charge Current in Trickle charge Condition	Vbat＜1.4V	Itrikl		15		mA
	1.4V＜Vbat＜VTRIKL,Rset=1K			200		
	1.4V＜Vbat＜VTRIKL,Rset=0.5K			400		
End of charger current				13.3%*Icc		mA
Adapter Current Limit		V_{Rilim}	1.9	2	2.1	V
Current limit through VBUS	RILIMIT=1K	I_{LIMIT}		1.1		A
	RILIMIT=0.5K			2.2		
Switch frequency	Vbus=5V,Vbat=3.6V,Rset=0.5K			1.2		MHz
Trickle Charge Timer	Default REGister, wake-up mode			90		min
Charge Timer	Default REGister, CC+CV mode			10		hr
Recharge threshold	Vbat falling		-	150	-	mV
STAT low level	Open drain pulled up with 5mA	STAT	-	-	0.2	V
Leakage Current to STAT	Vbat=4.3V, Ibat=0			0.6	1	uA
FULL low level	Open drain pulled up with 5mA	FULL			0.2	V
Leakage Current to FULL	Vbat=4.3V, Ibat=0			0.4	1	uA
CE threshold	Enable charge, CE rising	V_{CER}	3.5			V
	Disable charge, CE falling	V_{CEF}			2	
Temperature sense comparators						

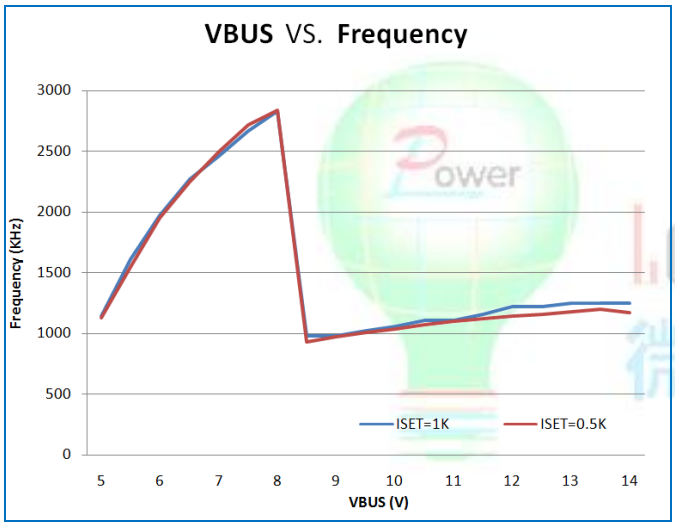
V_{LTF}	High voltage threshold	Temp fault at V(NTC)> V_{LTF}	2.45	2.50	2.55	V
V_{HTF}	Low voltage threshold	Temp fault at V(NTC)< V_{HTF}	0.48	0.50	0.52	V
I_{NTC}	Temperature sense current sense, R_{IREF}=100K		94	100	106	uA
Charging Temperature Shutdown	Temperature rising	Not tested in production	-	145	-	℃
	Hysteresis falling		-	25	-	℃

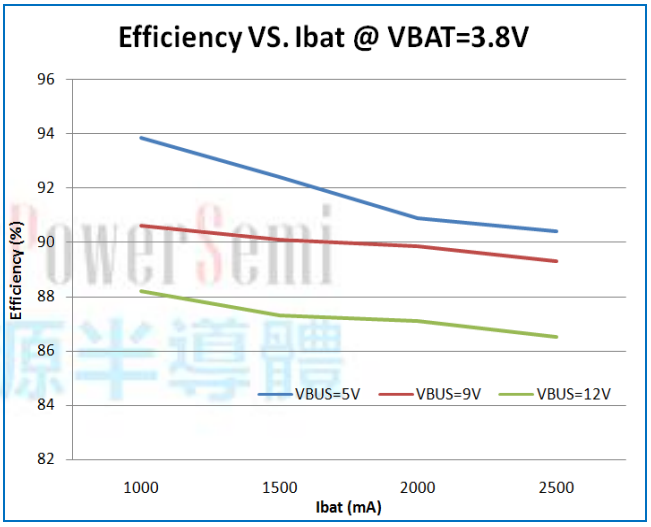
Typical Operating Characteristics

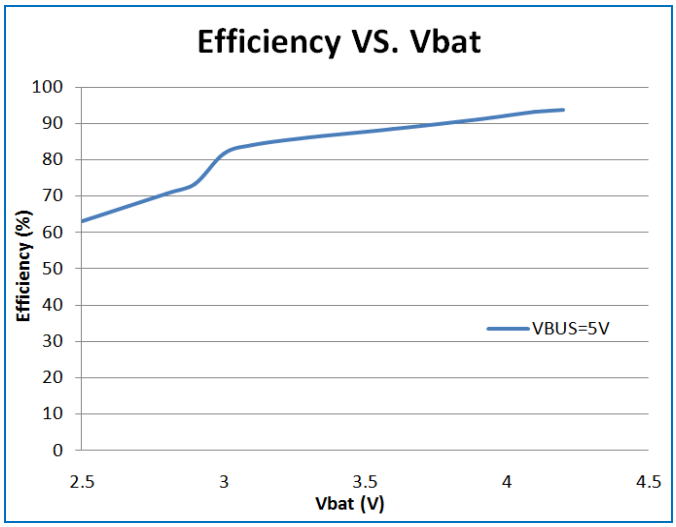
(TA=25℃，unless otherwise noted)

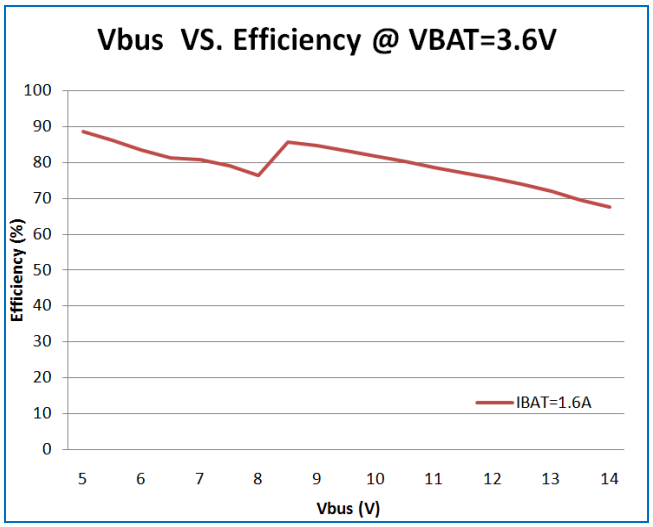


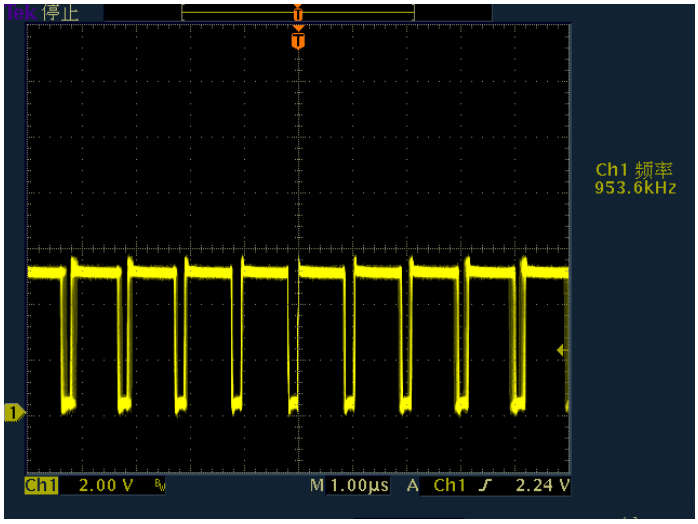




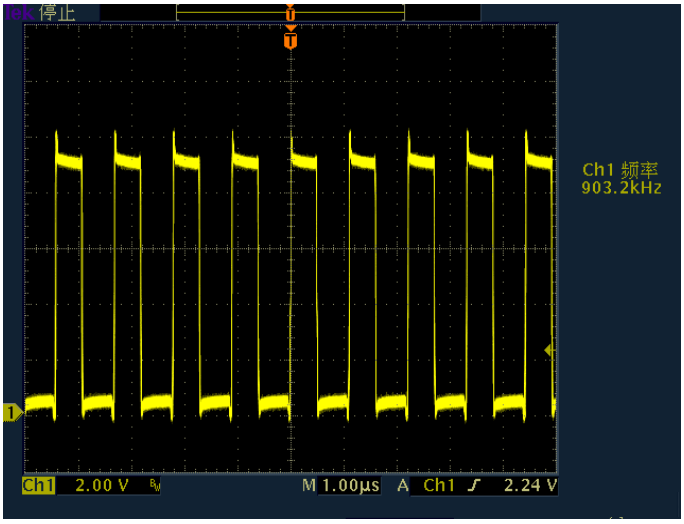




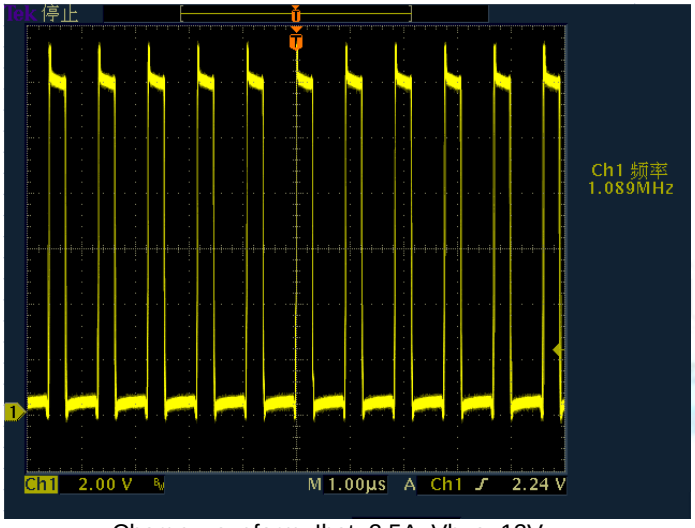




Charge waveform: Ibat=2.5A, Vbus=5V



Charge waveform: Ibat=2.5A, Vbus=9V



Charge waveform: Ibat=2.5A, Vbus=12V

Application Information

The LP28501 is an easy controlled power path management device and a single cell Li-Ion battery charger. It integrates the input reverse-blocking FET, high-side switching FET, lowside switching FET, and BATFET between system and battery. The device also integrates the bootstrap diode for the high-side gate drive.

Device Power Up

Power Up from Battery without DC Source

If only battery is present and the voltage is above depletion threshold, the BATFET turns on and connects battery to system. The REG LDO stays off to minimize the quiescent current. The low R_{DSON} in BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

Power Up from DC Source

When the DC source plugs in, the LP28501 checks the input source voltage to turn on REG LDO and all the bias circuits. It also checks the input current limit before starts the buck converter.

Input Source Qualification

After REG LDO powers up, the LP28501 checks the current capability of the input source. The input source has to meet the following requirements to start the buck converter.

1. VBUS voltage below 16V
2. VREG voltage above 2.43V

Once the input source passes all the conditions above, the a permit signal is asserted to the chip.

Input Current Limit Detection

The USB ports on personal computers are convenient charging source for portable devices (PDs). If the portable device is attached to a USB host, the USB specification requires the portable device to draw limited current (100mA/500mA in USB 2.0, and 150mA/900mA in USB 3.0). If the portable device is attached to a charging port, it is allowed to draw up to the maximum current form the USB host by two parts limit：

1. VREG voltage above 2.43V
2. The maximum input current < I_{LIMIT}

VSYS and Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by battery voltage. With a not fully depleted battery, the system is regulated (R_{BATFET} * $I_{BAT\ TO\ SYS}$)V less than the battery voltage. And a selectable VSYS could be set by SYSSEL when battery is fully depleted and adapter is applied to VBUS.

Charge state indication

As showed below, the STAT and FULL LED respond to this six STATES.

STATE	STAT	FULL
Without Battery	Flicker	Light On
Charging	Light On	Light Off
Charge complete	Light Off	Light On
Battery overheat	Flicker	Light Off
Time out	Flicker	Light Off
V_{REG} < $V_{REG(th)}$	Light On	Light Off

Dynamic Power Management

To meet maximum current limit in USB spec and avoid over loading the adapter, the LP28501 features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage. When input source is over-loaded because the charge current is too large, either the current exceeds the input current limit or the voltage falls below the input voltage limit by detection from REG. The device then reduces the charge current until the REG voltage rises above the threshold voltage and the input current is less than the current limit.

Power Path Management

The LP28501 accommodates a wide range of input sources from USB to wall adapter. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT), or both.

If the system current and the input current limit is large than the adapter current limit, the adapter voltage would be pulled down by this large system current.

Battery Charging Management

The LP28501 charges 1-cell Li-Ion battery with up to 3.5A charge current for high capacity tablet battery. The low dissipation BATFET improves charging efficiency and minimizes the voltage drop during discharging.

Autonomous Charging Cycle

With battery charging enabled, the LP28501 can complete a charging cycle. The charger device automatically terminates the charging cycle when the charging current is below termination threshold and charge voltage is above recharge threshold. When a full battery voltage is discharged below recharge threshold 0.15V, the LP28501 automatically starts another charging cycle. The STAT output indicates the charging status of charging (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking). The three state indicates the different charging phases: low-charging, high-charge complete, blink-charge fault. Another charge down indication is FULL(low when charge complete or without battery).

Battery Charging Profile

The device charges the battery in three phases: preconditioning, constant current and constant voltage. At the beginning of a charging cycle, the device checks the battery voltage and applies current.

If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted.

Battery Temperature Detection

The LP28501 continuously monitors battery temperature by measuring the voltage between the NTC pins and ground, typically determined by a negative temperature coefficient thermistor and an external voltage divider. The device compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the battery temperature must be within the V_{LTF} to V_{HTF} thresholds. There is a constant current source in NTC which is 100uA（I_{NTC}） flowing out form this pin. So V_{NTC} is I_{NTC}*R_{NTC}.

When the NTC fault occurs, the STAT pin will blink to indicate the fault.

Input Current Limit on Rilim and Iiset

For safe operation, the LP28501 has an additional hardware pin on ILIM to limit maximum input current on ILIM pin. The input maximum current is set by a resistor from ILIM pin to ground as:

$$I_{ALMT}(A) = 550 \times \frac{2V}{Rilim(\Omega)}$$

ISET ramming Charge Current

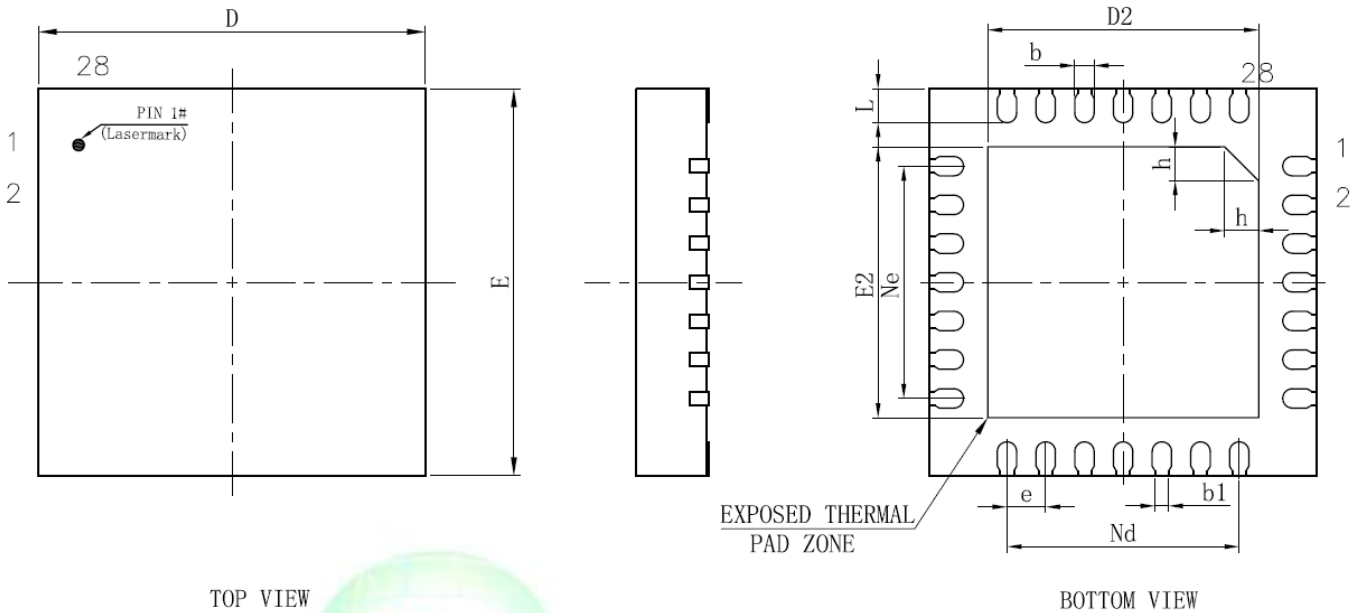
The charge current is R_{ISET} rammed using a single resistor from the R_{ISET} pin to ground. The battery charge current is 1000 times the current out of the R_{ISET} pin. The R_{ISET} ram resistor and the charge current are calculated using the following equations:

$$I_{CHG}(A) = 1000 \times \frac{1.5V}{R_{ISET}(\Omega)}$$

Note: V_{RISET} is 1.5Volts when VBAT>VTRIKL.

Packaging Information

QFN-28



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e	0.40BSC		
Ne	2.40BSC		
Nd	2.40BSC		
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.30	0.35	0.40
h	0.30	0.35	0.40