FPA-640x512 InGaAs Imager

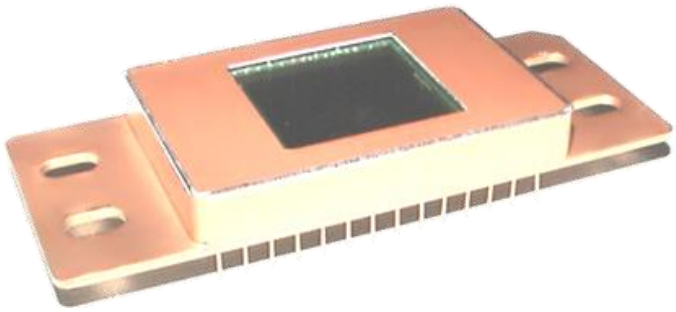
NEAR INFRARED (0.9um-1.7um) IMAGE SENSOR

FEATURES

- 640x512 Array Format
- 28-pin Metal DIP Package
- Embedded Thermoelectric Cooler
- Typical Pixel Operability >99.5%
- Quantum Efficiency >70%
- 12 months warranty after delivery will be provided

APPLICATIONS

- Near-infrared Imaging
- Imaging Spectroscopy
- Covert Surveillance
- Semiconductor Inspection
- Medical Science and Biology
- Fiberoptic Telecommunication
- Astronomy and Scientific
- Industrial Thermal Imaging
- Moisture Mapping



GENERAL DESCRIPTIONS

PARAMETER	VALUE
Sensor Technology	Standard InGaAs/InP
Spectral Range	0.9um-1.7um
Image Format	640(H)x512(V)
Pixel Size	25umx25um (>99% Fill Factor)
Image Size	16mm(H)x12.8mm(V)
Package Type	28-pin Metal DIP Package
Weight	24.6g

FPA CHARACTERISTICS (T_a=25°C)

PARAMETER	TYPICAL	CONDITIONS
Dark Current	≤ 0.2 pA	Pixel bias =0.1 volt
Quantum Efficiency	≥ 70%	λ=1.0um-1.6um
Fill Factor	>99%	
Adjacent pixel crosstalk	<1%	
Detectivity	≥ $5x10^{12}$ Jones	T_{int}=16ms, High Gain, λ=1.55um
Response Nonuniformity	≤ 10%	Under 50% Saturation
Nonlinearity (Max. Deviation)	≤ 2%	Over 15%-85% Full Well Capacity
Max. Pixel Rate	10MHz	
Gain	High gain*: 23.6uV/e^- Low gain: 1.26 uV/e^-	
Full Well	High gain* : 118K e^- Low gain: 1.9M e^-	
Pixel Operability**	> 99%(Minimum)	Dark Current ≤ 20% Full Well Response Nonuniformity ≤ 20%

* Gain and full well under high gain mode may vary from lot to lot.

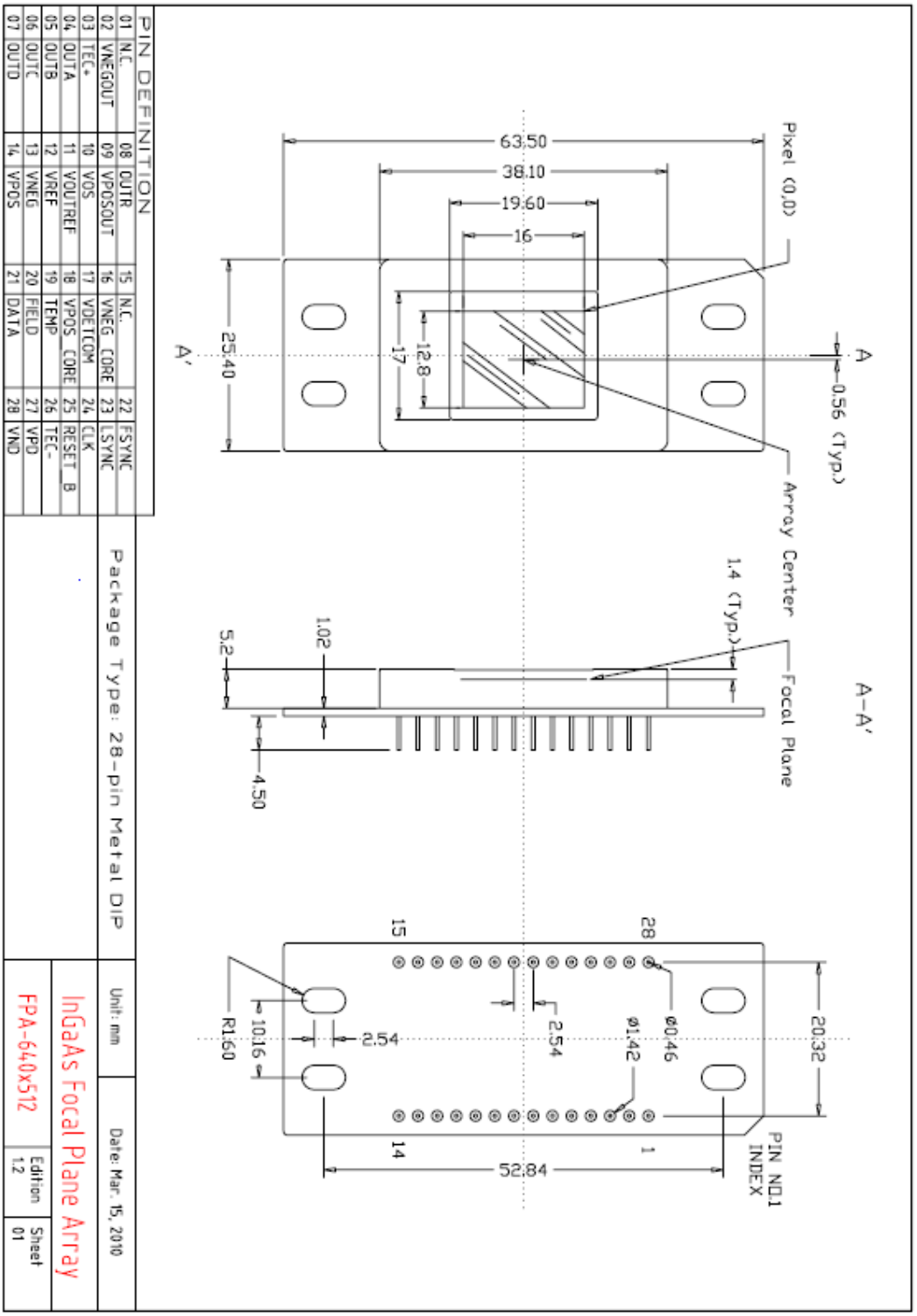
** Pixel Operability is defined within the center 636x508 regions

ABSOLUTE MAXIMUM RATINGS

PARAMETER	UNIT	MIN	MAX
Operation Temperature	°C	-20	85
Storage Temperature	°C	-40	85
Power Consumption	mW	---	325***

*** without driving the cooler

PACKAGE OUTLINE



Note : ID number of the imager is printed on the flank of the package

OPERATING CONDITIONS

Bias Input

Pin #	Bias	Voltage	Current	Remark
27	VPD	5.5V	<15mA	Logic positive supply
28	VND	0V	<15mA	Logic negative supply
9	VPOSOUT	5.5V	<25mA	Output driver positive supply
2	VNEGOUT	0V	<25mA	Output driver negative supply
14	VPOS	5.5V	<15mA	Positive analog supply
13	VNEG	0V	<15mA	Negative analog supply and substrate
18	VPOS_CORE	5.5V	<80mA	Positive analog supply
16	VNEG_CORE	0V	<80mA	Negative analog supply
11	VOUTREF	1.6V	<1mA	Output reference level
12	VREF	2.2V – 3.2V	<1mA	CTIA amplifier reference supply
17	VDETCOM	2.7V - 5.5V	<20mA	Detector common voltage Detector bias = VREF-VDETCOM*

*VDETCOM lower than VREF will forward bias the detector pixels.

Digital Pattern Input

Pin #	Clocks	Levels	Rise/Fall	Remark
25	RESET_B	0V - 5.5V	<10ns	Resets digital registers and latches when logic “0” is applied, normally pull up to logic “1”
24	CLK	0V - 5.5V	<10ns	Master clock Max. Freq.=5MHz
23	LSYNC	0V - 5.5V	<10ns	Line sync - controls line readout timing
22	FSYNC	0V - 5.5V	<10ns	Frame sync - controls frame start and integration time
21	DATA	0V - 5.5V	<10ns	Data code input - programs chip function registers
20	FIELD	0V - 5.5V	<10ns	Field sync – controls interlaced field readout

Clocks	Synchronization
FSYNC	Rising and falling when CLK is falling
LSYNC	Rising and falling when CLK is falling
DATA	Rising and falling when CLK is rising
FIELD	Rising and falling when CLK is falling

Video Output

Pin #	Outputs	Levels	Settle	Remark
4	OUTA	2.3V to 4.7V*	<70ns to 0.1%	Output A used in single output mode
5	OUTB	2.3V to 4.7V*	<70ns to 0.1%	Output A and B used in two output mode
6	OUTC	2.3V to 4.7V*	<70ns to 0.1%	Output A, B, C, and D used in four output mode
7	OUTD	2.3V to 4.7V*	<70ns to 0.1%	Output A, B, C, and D used in four output mode
8	OUTR	1.6V	-	Reference for common mode output

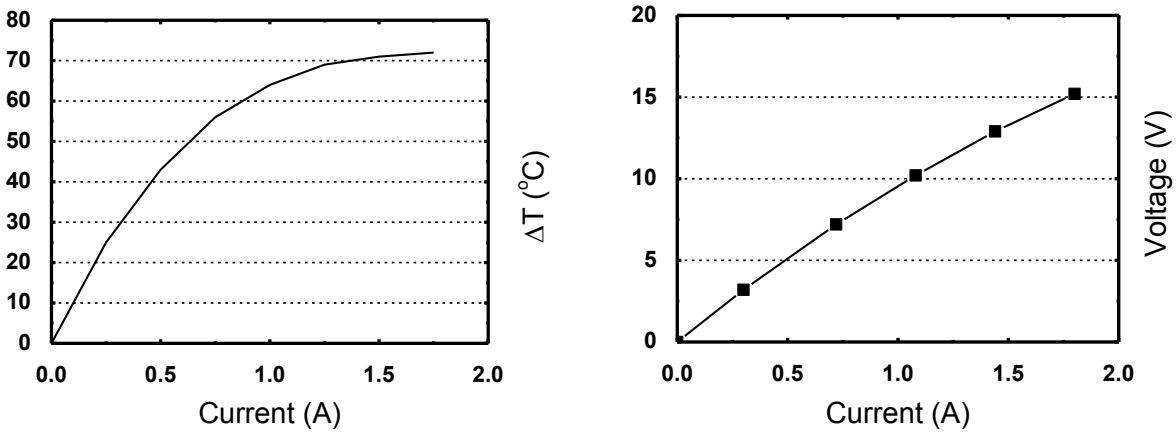
* Low gain mode, the swing under high gain mode is 2.3V~5.1V

Advanced Function

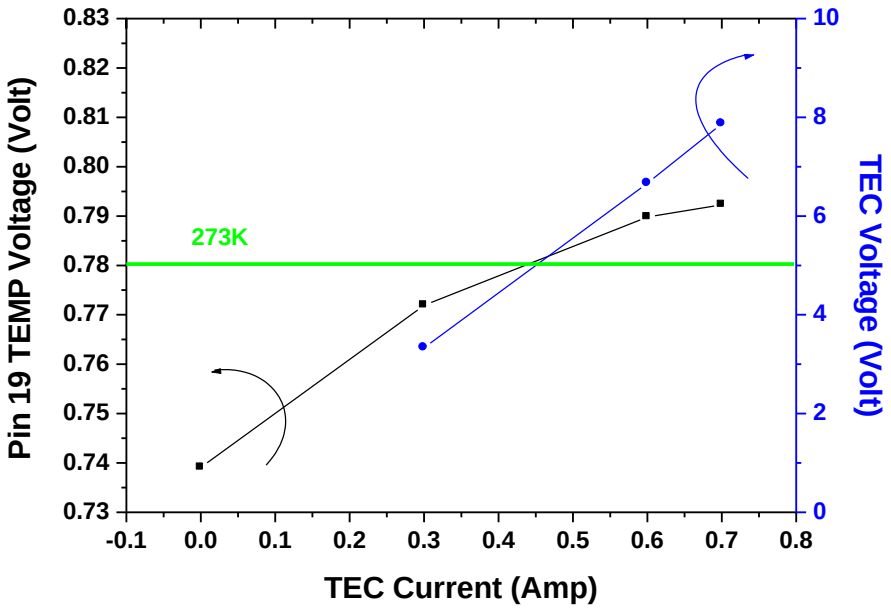
Pin #	Functions	Voltages	Remark
10	VOS	1.6V - 5.5V	Variable Offset/Skimming Control Voltage
19	TEMP	0V - 5.5V	On chip temperature monitor 0.74V at 300K, **Slope=-14.8mV/10K in 50-300K**

THERMOELECTRIC COOLER DATA (without thermal loading)

$\triangle T_{max}$	I_{max}	V_{max}
> 70℃	1.80A	15.40V

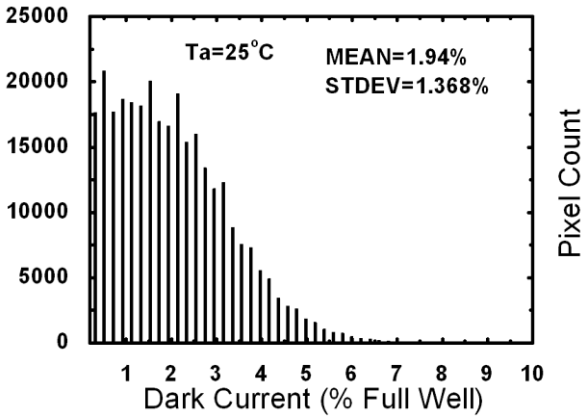


Cooling Performance with sensor loading and operating



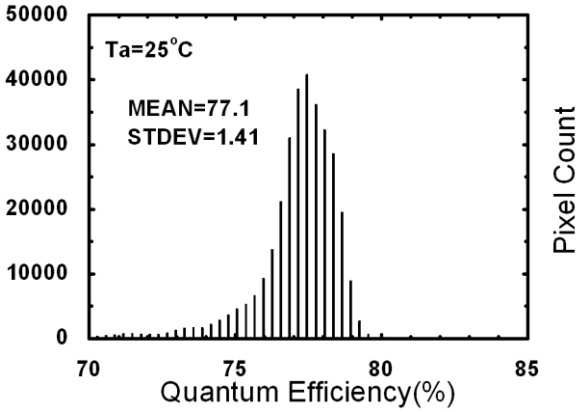
EXAMPLE CURVES

Statistical Histogram of Dark Current



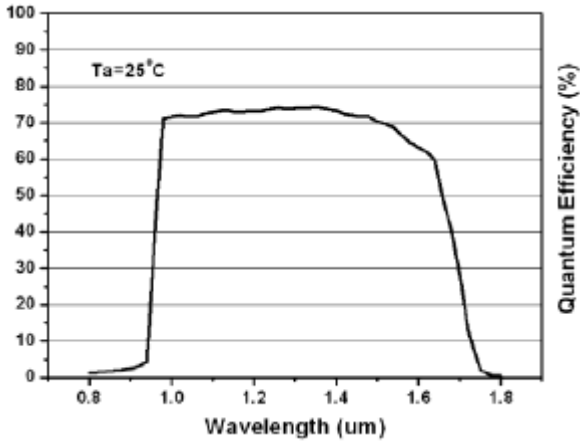
Test Conditions:	
Illumination	Dark
Wavelength	---
Gain	Low
Integration Time	16ms
Remark	Effective Screen

Statistical Histogram of Quantum Efficiency



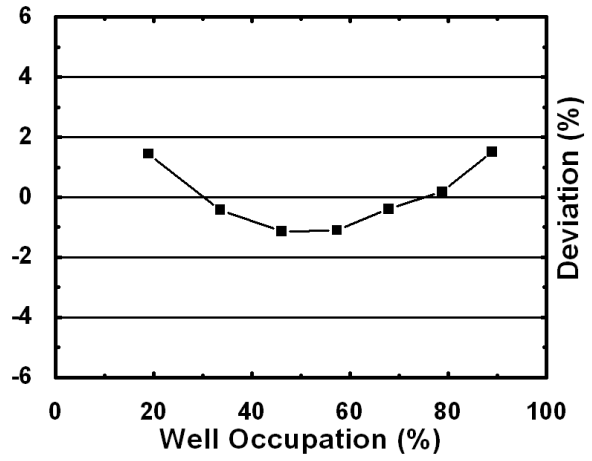
Test Conditions:	
Illumination	Nonuniformity≤± 0.15%
Wavelength	1310nm
Gain	Low
Integration Time	5msec, 50% saturation
Remark	Effective Screen

Quantum Efficiency



Test Conditions:	
Illumination	Nonuniformity≤± 0.15%
Wavelength	Broadband
Gain	Low
Integration Time	5msec, 50% saturation
Remark	Effective Screen Array Average

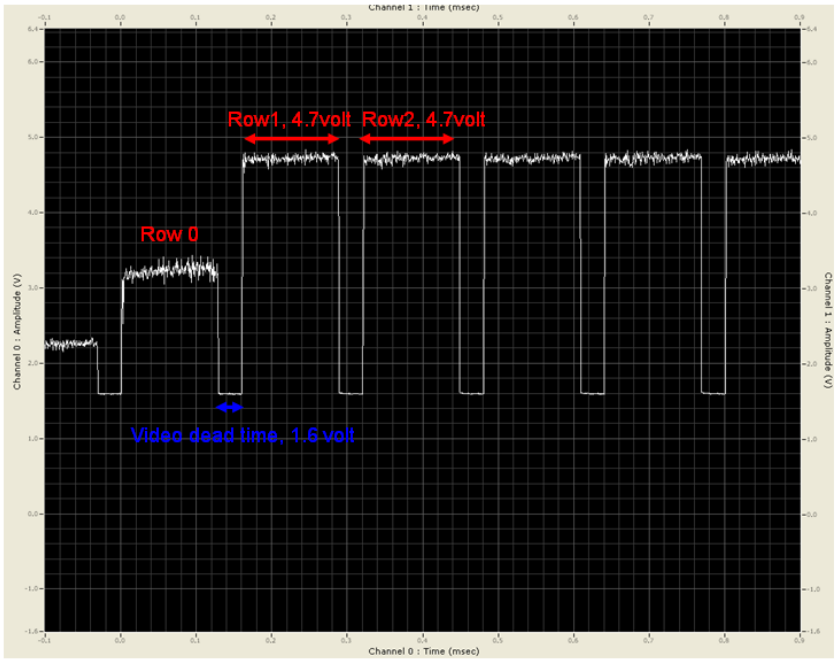
Linearity



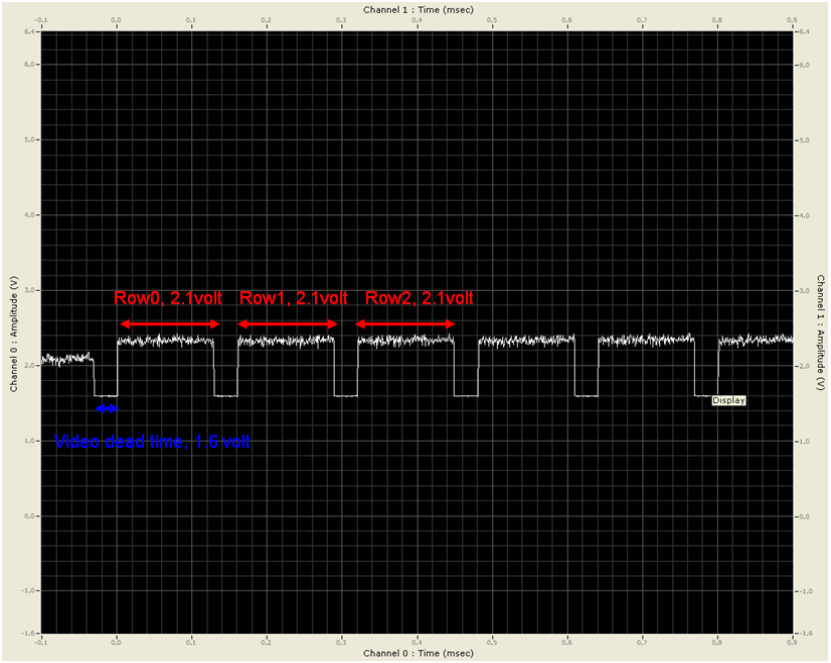
Test Conditions:	
Illumination	Nonuniformity≤± 0.15%
Wavelength	1310nm
Gain	Low
Integration Time	---
Remark	Effective Screen Array Average

OUTA WAVEFROM(LOW GAIN MODE)

Waveform under dark*



Waveform under saturation



* The dark level under high gain mode is 5.1volt.

Waveform under near saturation