2.9 nV/sqrt(Hz) Low Noise, RRIO Amplifier

Check for Samples: LMP7732

FEATURES

- **(Typical Values, T_A = 25°C, V_S = 5V)**
- **Input Voltage Noise**
  - **f = 3 Hz 3.3 nV/√Hz**
  - **f = 1 kHz 2.9 nV/√Hz**
- **CMRR 130 dB**
- **Open Loop Gain 130 dB**
- **GBW 22 MHz**
- **Slew Rate 2.4 V/µs**
- **THD 0.001% @ f = 10 kHz, AV = 1, RL = 2 kΩ**
- **Supply Current 4.4 mA**
- **Supply Voltage Range 1.8V to 5.5V**
- **Operating Temperature Range −40°C to 125°C**
- **Input Bias Current ±1.5 nA**
- **RRIO**

APPLICATIONS

- **Gas Analysis Instruments**
- **Photometric Instrumentation**
- **Medical Instrumentation**

DESCRIPTION

The LMP7732 is a dual low noise, rail-to-rail input and output, low voltage amplifier. The LMP7732 is part of the LMP™ amplifier family and is ideal for precision and low noise applications with low voltage requirements.

This operational amplifier offers low voltage noise of 2.9 nV/√Hz with a 1/f corner of only 3 Hz. The LMP7732 has bipolar junction input stages with a bias current of only 1.5 nA. This low input bias current, complemented by the very low level of voltage noise, makes the LMP7732 an excellent choice for photometry applications.

The LMP7732 provides a wide GBW of 22 MHz while consuming only 4 mA of current. This high gain bandwidth along with the high open loop gain of 130 dB enables accurate signal conditioning in applications with high closed loop gain requirements.

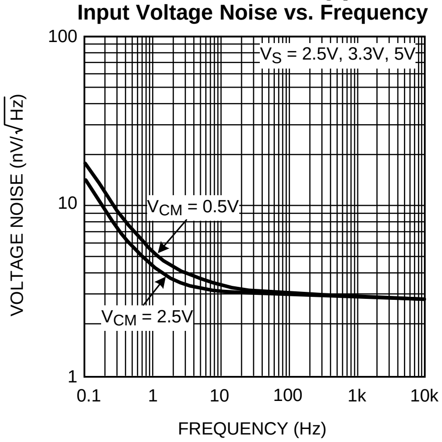
The LMP7732 has a supply voltage range of 1.8V to 5.5V, making it an ideal choice for battery operated portable applications.

The LMP7732 is offered in the 8-Pin SOIC and VSSOP packages.

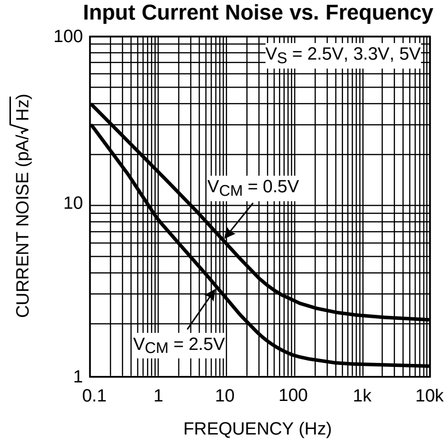
The LMP7731 is the single version of this product and is offered in the 5-Pin SOT-23 and 8-Pin SOIC packages.

Typical Performance Characteristics

Input Voltage Noise vs. Frequency



Input Current Noise vs. Frequency



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance(3)	Human Body Model	For inputs pins only	2000V
		For all other pins	2000V
	Machine Model		200V
	Charge Device Model		1000V
V_{IN} Differential			±2V
Supply Voltage ($V_S = V^+ – V^−$)			6.0V
Storage Temperature Range			−65°C to 150°C
Junction Temperature(4)			+150°C max
Soldering Information		Infrared or Convection (20 sec)	235°C
		Wave Soldering Lead Temp. (10 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $θ_{JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ θJ_A$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings(1)

Temperature Range		−40°C to 125°C
Supply Voltage ($V_S = V^+ – V^−$)		1.8V to 5.5V
Package Thermal Resistance ($θ_{JA}$)	8-Pin SOIC	190 °C/W
	8-Pin VSSOP	235°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.

2.5V Electrical Characteristics[1]

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 2.5V, V^- = 0V, V_{CM} = V^+/2, R_L >10 kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min[2]	Typ[3]	Max[2]	Units
V_{OS}	Input Offset Voltage[4]	V_{CM} = 2.0V		±9	±500 **±600**	μV
		V_{CM} = 0.5V		±9	±500 **±600**	
TCV_{OS}	Input Offset Voltage Temperature Drift	V_{CM} = 2.0V		±0.5	±5.5	μV/°C
		V_{CM} = 0.5V		±0.2	±5.5	
I_B	Input Bias Current	V_{CM} = 2.0V		±1	±30 **±45**	nA
		V_{CM} = 0.5V		±12	±50 **±75**	
I_{OS}	Input Offset Current	V_{CM} = 2.0V		±1	±50 **±75**	nA
		V_{CM} = 0.5V		±11	±60 **±80**	
TCI_{OS}	Input Offset Current Drift	V_{CM} = 0.5V and V_{CM} = 2.0V		0.0474		nA/°C
CMRR	Common Mode Rejection Ratio	0.15V ≤ V_{CM} ≤ 0.7V 0.23V ≤ V_{CM} ≤ 0.7V	101 **89**	120		dB
		1.5V ≤ V_{CM} ≤ 2.35V 1.5V ≤ V_{CM} ≤ 2.27V	105 **99**	129		
PSRR	Power Supply Rejection Ratio	2.5V ≤ V^+ ≤ 5V	105 **101**	113		dB
		1.8V ≤ V^+ ≤ 5.5V		111		
CMVR	Common Mode Voltage Range	Large Signal CMRR ≥ 80 dB	0		2.5	V
A_{VOL}	Open Loop Voltage Gain	R_L = 10 kΩ to V^+/2 V_{OUT} = 0.5V to 2.0V	112 **104**	130		dB
		R_L = 2 kΩ to V^+/2 V_{OUT} = 0.5V to 2.0V	109 **90**	119		
V_{OUT}	Output Voltage Swing High	R_L = 10 kΩ to V^+/2		4	50 **75**	mV from either rail
		R_L = 2 kΩ to V^+/2		13	50 **75**	
	Output Voltage Swing Low	R_L = 10 kΩ to V^+/2		6	50 **75**	
		R_L = 2 kΩ to V^+/2		9	50 **75**	
I_{OUT}	Output Current	Sourcing, V_{OUT} = V^+/2 V_{IN} (diff) = 100 mV	22 **12**	31		mA
		Sinking, V_{OUT} = V^+/2 V_{IN} (diff) = −100 mV	15 **10**	44		
I_S	Supply Current	V_{CM} = 2.0V		4.0	5.4 **6.8**	mA
		V_{CM} = 0.5V		4.6	6.2 **7.8**	
SR	Slew Rate	A_V = +1, C_L = 10 pF, R_L = 10 kΩ to V^+/2 V_{OUT} = 2 V_{PP}		2.4		V/μs

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. Absolute maximum Ratings indicate junction temperature limits beyond which the device maybe permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing, statistical analysis or design.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Ambient production test is performed at 25°C with a variance of ±3°C.

2.5V Electrical Characteristics[(1)] (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 2.5V, V^- = 0V, V_{CM} = V^+/2, R_L >10 kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min[(2)]	Typ[(3)]	Max[(2)]	Units
GBW	Gain Bandwidth	C_L = 20 pF, R_L = 10 kΩ to V^+/2		21		MHz
G_M	Gain Margin	C_L = 20 pF, R_L = 10 kΩ to V^+/2		14		dB
Φ_M	Phase Margin	C_L = 20 pF, R_L = 10 kΩ to V^+/2		60		deg
R_{IN}	Input Resistance	Differential Mode		38		kΩ
		Common Mode		151		MΩ
THD+N	Total Harmonic Distortion + Noise	A_V = 1, f_O = 1 kHz, Amplitude = 1V		0.002		%
e_n	Input Referred Voltage Noise Density	f = 1 kHz, V_{CM} = 2.0V		3.0		$nV/\sqrt{Hz}$
		f = 1 kHz, V_{CM} = 0.5V		3.0		
	Input Voltage Noise	0.1 Hz to 10 Hz		75		nV_{PP}
i_n	Input Referred Current Noise Density	f = 1 kHz, V_{CM} = 2.0V		1.1		$pA/\sqrt{Hz}$
		f = 1 kHz, V_{CM} = 0.5V		2.3		

3.3V Electrical Characteristics (1)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 3.3V, V^- = 0V, V_{CM} = V^+/2, R_L > 10 kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage (4)	V_{CM} = 2.5V		±6	±500 **±600**	μV
		V_{CM} = 0.5V		±6	±500 **±600**	
TCV_{OS}	Input Offset Voltage Temperature Drift	V_{CM} = 2.5V		±0.5	±5.5	μV/°C
		V_{CM} = 0.5V		±0.2	±5.5	
I_B	Input Bias Current	V_{CM} = 2.5V		±1.5	±30 **±45**	nA
		V_{CM} = 0.5V		±13	±50 **±77**	
I_{OS}	Input Offset Current	V_{CM} = 2.5V		±1	±50 **±70**	nA
		V_{CM} = 0.5V		±11	±60 **±80**	
TCI_{OS}	Input Offset Current Drift	V_{CM} = 0.5V and V_{CM} = 2.5V		0.048		nA/°C
CMRR	Common Mode Rejection Ratio	0.15V ≤ V_{CM} ≤ 0.7V 0.23V ≤ V_{CM} ≤ 0.7V	101 **89**	120		dB
		1.5V ≤ V_{CM} ≤ 3.15V 1.5V ≤ V_{CM} ≤ 3.07V	105 **99**	130		
PSRR	Power Supply Rejection Ratio	2.5V ≤ V^+ ≤ 5.0V	105 **101**	113		dB
		1.8V ≤ V^+ ≤ 5.5V		111		
CMVR	Common Mode Voltage Range	Large Signal CMRR ≥ 80 dB	0		3.3	V
A_{VOL}	Open Loop Voltage Gain	R_L = 10 kΩ to V^+/2 V_{OUT} = 0.5V to 2.8V	112 **104**	130		dB
		R_L = 2 kΩ to V^+/2 V_{OUT} = 0.5V to 2.8V	110 **92**	119		
V_{OUT}	Output Voltage Swing High	R_L = 10 kΩ to V^+/2		5	50 **75**	mV from either rail
		R_L = 2 kΩ to V^+/2		14	50 **75**	
	Output Voltage Swing Low	R_L = 10 kΩ to V^+/2		9	50 **75**	
		R_L = 2 kΩ to V^+/2		13	50 **75**	
I_{OUT}	Output Current	Sourcing, V_{OUT} = V^+/2 V_{IN} (diff) = 100 mV	28 **22**	45		mA
		Sinking, V_{OUT} = V^+/2 V_{IN} (diff) = −100 mV	25 **20**	48		
I_S	Supply Current	V_{CM} = 2.5V		4.2	5.6 **7.0**	mA
		V_{CM} = 0.5V		4.8	6.4 **8.0**	
SR	Slew Rate	A_V = +1, C_L = 10 pF, R_L = 10 kΩ to V^+/2 V_{OUT} = 2 V_{PP}		2.4		V/μs

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. Absolute maximum Ratings indicate junction temperature limits beyond which the device maybe permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing, statistical analysis or design.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Ambient production test is performed at 25°C with a variance of ±3°C.

3.3V Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 3.3V, V^- = 0V, V_{CM} = V^+/2, R_L > 10 kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min[2]	Typ[3]	Max[2]	Units
GBW	Gain Bandwidth	C_L = 20 pF, R_L = 10 kΩ to V^+/2		22		MHz
G_M	Gain Margin	C_L = 20 pF, R_L = 10 kΩ to V^+/2		14		dB
Φ_M	Phase Margin	C_L = 20 pF, R_L = 10 kΩ to V^+/2		62		deg
THD+N	Total Harmonic Distortion + Noise	A_V = 1, f_O = 1 kHz, Amplitude = 1V		0.002		%
R_{IN}	Input Resistance	Differential Mode		38		kΩ
		Common Mode		151		MΩ
e_n	Input Referred Voltage Noise Density	f = 1 kHz, V_{CM} = 2.5V		2.9		nV/√Hz
		f = 1 kHz, V_{CM} = 0.5V		2.9		
	Input Voltage Noise	0.1 Hz to 10 Hz		75		nV_{PP}
i_n	Input Referred Current Noise Density	f = 1 kHz, V_{CM} = 2.5V		1.1		pA/√Hz
		f = 1 kHz, V_{CM} = 0.5V		2.1		

5V Electrical Characteristics[1]

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, R_L > 10 kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min[2]	Typ[3]	Max[2]	Units
V_{OS}	Input Offset Voltage[4]	V_{CM} = 4.5V		±6	±500 **±600**	μV
		V_{CM} = 0.5V		±6	±500 **±600**	
TCV_{OS}	Input Offset Voltage Temperature Drift	V_{CM} = 4.5V		±0.5	±5.5	μV/°C
		V_{CM} = 0.5V		±0.2	±5.5	
I_B	Input Bias Current	V_{CM} = 4.5V		±1.5	±30 **±50**	nA
		V_{CM} = 0.5V		±14	±50 **±85**	
I_{OS}	Input Offset Current	V_{CM} = 4.5V		±1	±50 **±70**	nA
		V_{CM} = 0.5V		±11	±65 **±80**	
TCI_{OS}	Input Offset Current Drift	V_{CM} = 0.5V and V_{CM} = 4.5V		0.0482		nA/°C
CMRR	Common Mode Rejection Ratio	0.15V ≤ V_{CM} ≤ 0.7V 0.23V ≤ V_{CM} ≤ 0.7V	101 **89**	120		dB
		1.5V ≤ V_{CM} ≤ 4.85V 1.5V ≤ V_{CM} ≤ 4.77V	105 **99**	130		
PSRR	Power Supply Rejection Ratio	2.5V ≤ V^+ ≤ 5V	105 **101**	113		dB
		1.8V ≤ V^+ ≤ 5.5V		111		
CMVR	Common Mode Voltage Range	Large Signal CMRR ≥ 80 dB	0		5	V
A_{VOL}	Open Loop Voltage Gain	R_L = 10 kΩ to V^+/2 V_{OUT} = 0.5V to 4.5V	112 **104**	130		dB
		R_L = 2 kΩ to V^+/2 V_{OUT} = 0.5V to 4.5V	110 **94**	119		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. Absolute maximum Ratings indicate junction temperature limits beyond which the device maybe permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing, statistical analysis or design.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Ambient production test is performed at 25°C with a variance of ±3°C.

5V Electrical Characteristics(1) (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, R_L > 10 kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min(2)	Typ(3)	Max(2)	Units
V_{OUT}	Output Voltage Swing High	R_L = 10 kΩ to V^+/2		8	50 **75**	mV from either rail
		R_L = 2 kΩ to V^+/2		24	50 **75**	
	Output Voltage Swing Low	R_L = 10 kΩ to V^+/2		9	50 **75**	
		R_L = 2 kΩ to V^+/2		23	50 **75**	
I_{OUT}	Output Current	Sourcing, V_{OUT} = V^+/2 V_{IN} (diff) = 100 mV	33 **27**	47		mA
		Sinking, V_{OUT} = V^+/2 V_{IN} (diff) = −100 mV	30 **25**	49		
I_S	Supply Current	V_{CM} = 4.5V		4.4	6.0 **7.4**	mA
		V_{CM} = 0.5V		5.0	6.8 **8.4**	
SR	Slew Rate	A_V = +1, C_L = 10 pF, R_L = 10 kΩ to V^+/2 V_{OUT} = 2 V_{PP}		2.4		V/μs
GBW	Gain Bandwidth	C_L = 20 pF, R_L = 10 kΩ to V^+/2		22		MHz
G_M	Gain Margin	C_L = 20 pF, R_L = 10 kΩ to V^+/2		12		dB
Φ_M	Phase Margin	C_L = 20 pF, R_L = 10 kΩ to V^+/2		65		deg
R_{IN}	Input Resistance	Differential Mode		38		kΩ
		Common Mode		151		MΩ
THD+ N	Total Harmonic Distortion + Noise	A_V = 1, f_O = 1 kHz, Amplitude = 1V		0.001		%
e_n	Input Referred Voltage Noise Density	f = 1 kHz, V_{CM} = 4.5V		2.9		nV/√Hz
		f = 1 kHz, V_{CM} = 0.5V		2.9		
	Input Voltage Noise	0.1 Hz to 10 Hz		75		nV_{PP}
i_n	Input Referred Current Noise Density	f = 1 kHz, V_{CM} = 4.5V		1.1		pA/√Hz
		f = 1 kHz, V_{CM} = 0.5V		2.2		

Connection Diagram

8-Pin SOIC/VSSOP

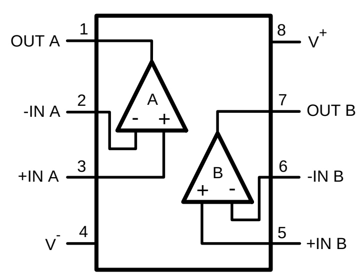


Figure 1. Top View

Typical Performance Characteristics

Unless otherwise noted: T_A = 25°C, R_L > 10 kΩ, V_{CM} = V_S/2.

Offset Voltage Distribution

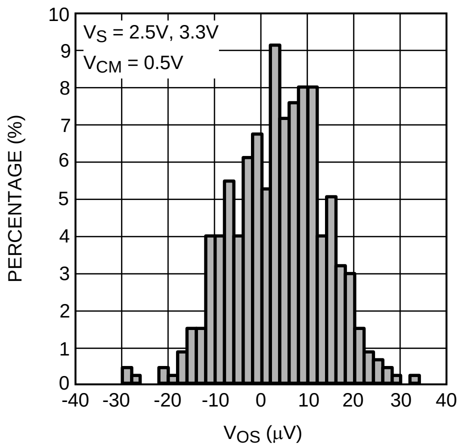


Figure 2.

TCV$_{OS}$ Distribution

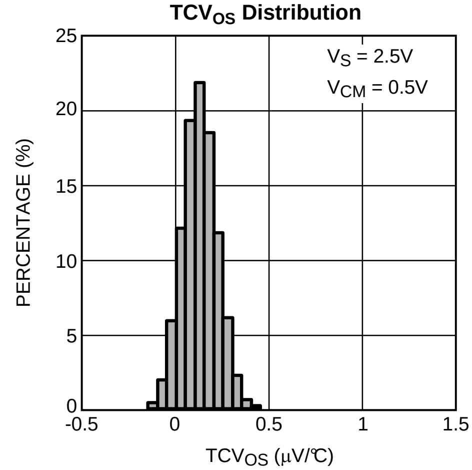


Figure 3.

Offset Voltage Distribution

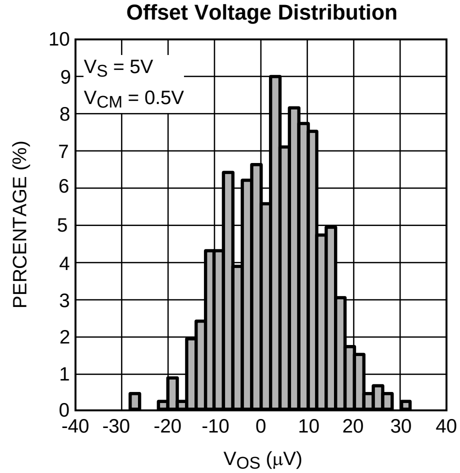


Figure 4.

TCV$_{OS}$ Distribution

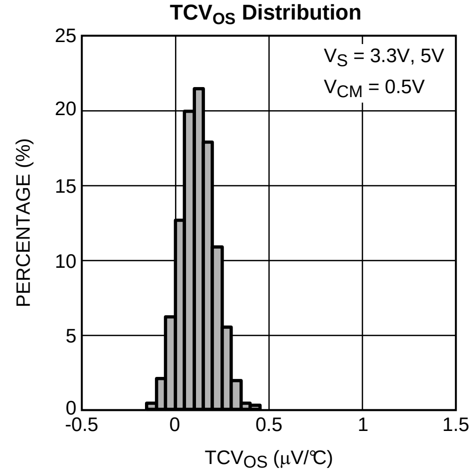


Figure 5.

Offset Voltage Distribution

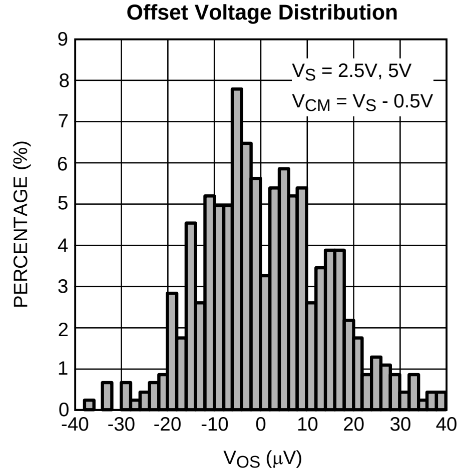


Figure 6.

TCV$_{OS}$ Distribution

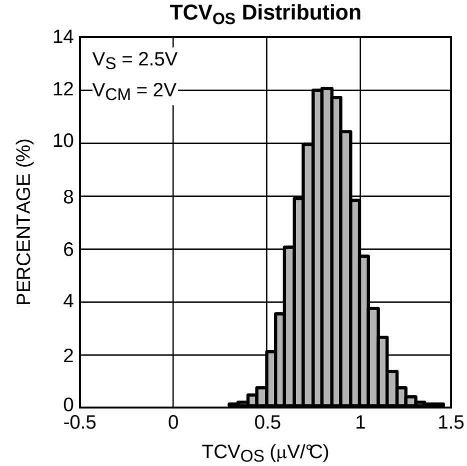


Figure 7.

Typical Performance Characteristics (continued)

Unless otherwise noted: T_A = 25°C, R_L > 10 kΩ, V_{CM} = V_S/2.

Offset Voltage Distribution

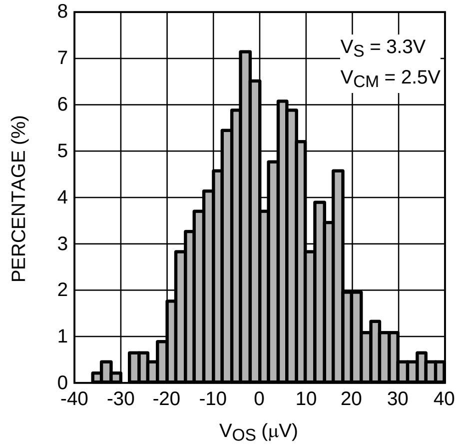


Figure 8.

TCV_{OS} Distribution

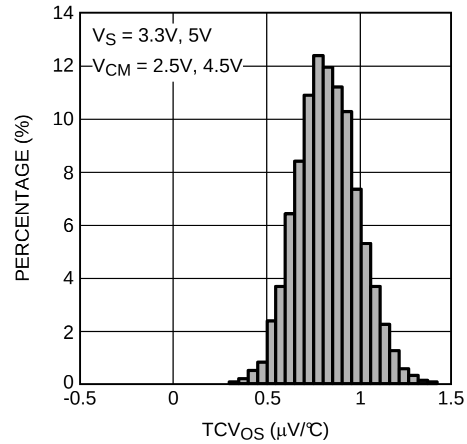


Figure 9.

Offset Voltage vs. Temperature

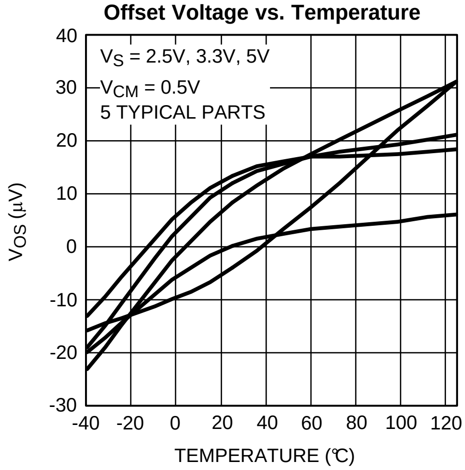


Figure 10.

Offset Voltage vs. Temperature

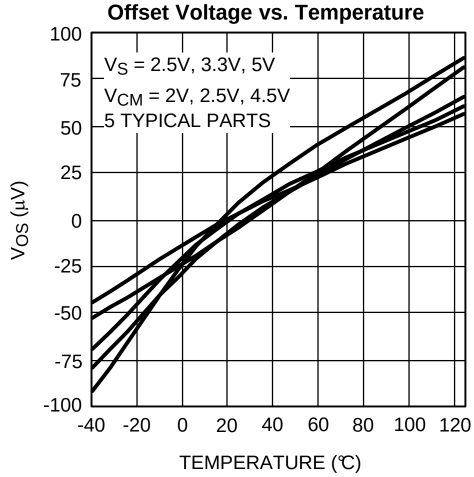


Figure 11.

PSRR vs. Frequency

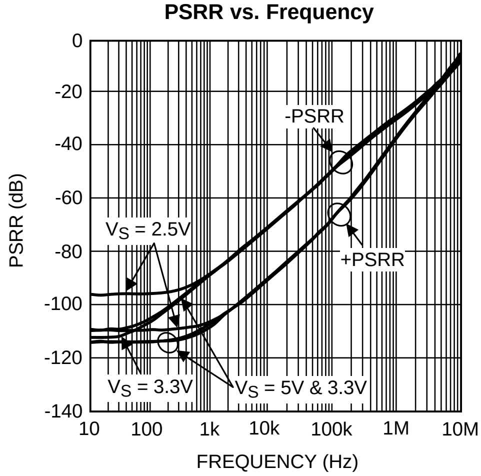


Figure 12.

CMRR vs. Frequency

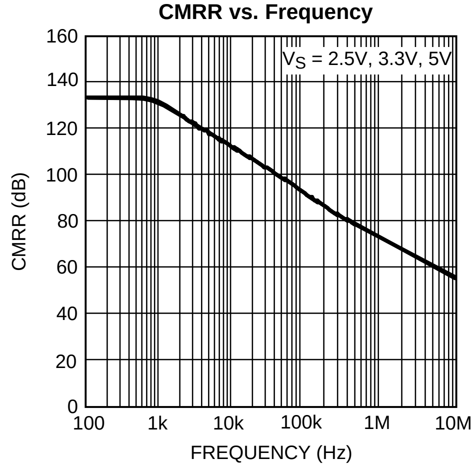


Figure 13.

Typical Performance Characteristics (continued)

Unless otherwise noted: T_A = 25°C, R_L > 10 kΩ, V_{CM} = V_S/2.

Offset Voltage vs. Supply Voltage

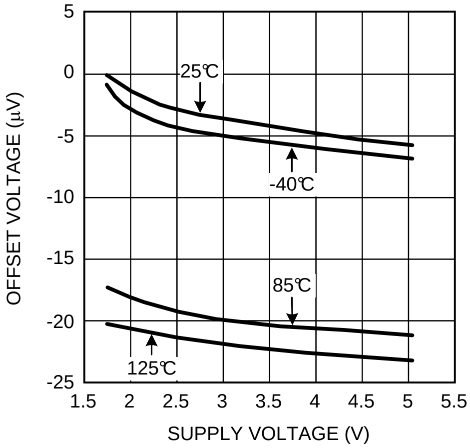


Figure 14.

Offset Voltage vs. V_{CM}

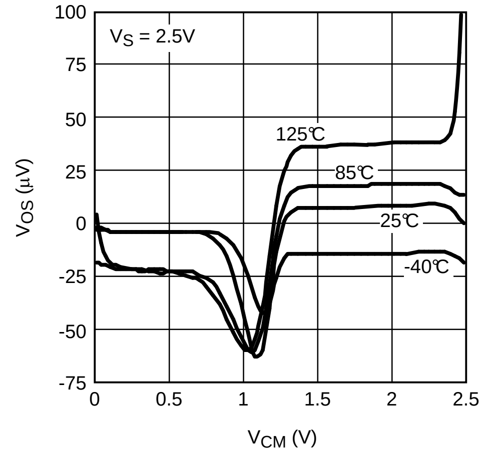


Figure 15.

Offset Voltage vs. V_{CM}

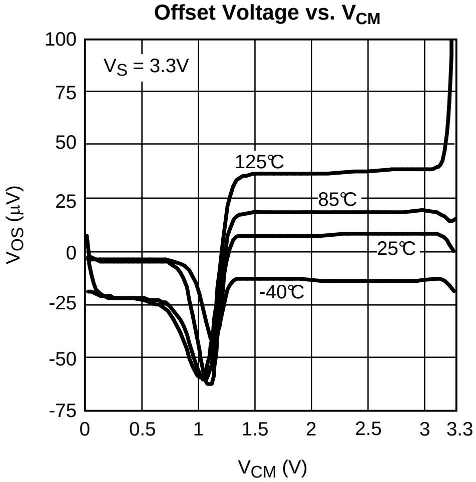


Figure 16.

Offset Voltage vs. V_{CM}

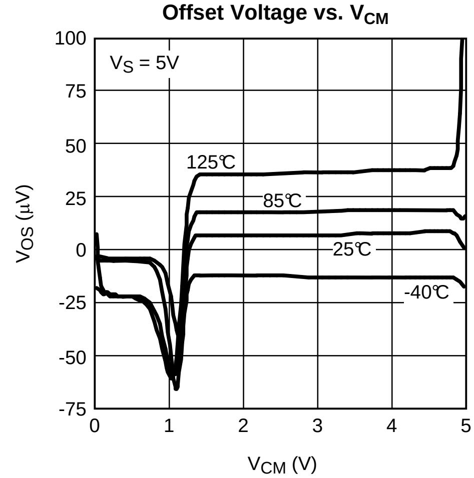


Figure 17.

Input Offset Voltage Time Drift

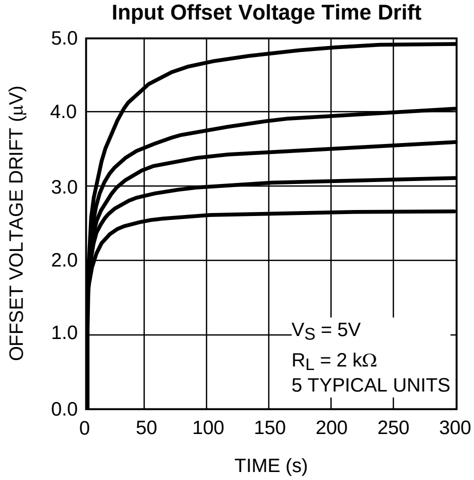


Figure 18.

Slew Rate vs. Supply Voltage

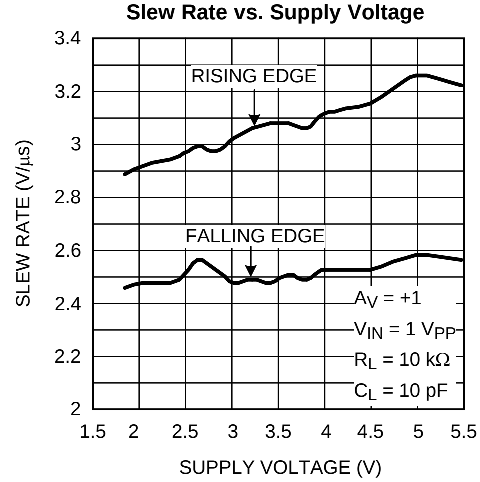


Figure 19.

Typical Performance Characteristics (continued)

Unless otherwise noted: T_A = 25°C, R_L > 10 kΩ, V_{CM} = V_S/2.

Time Domain Voltage Noise

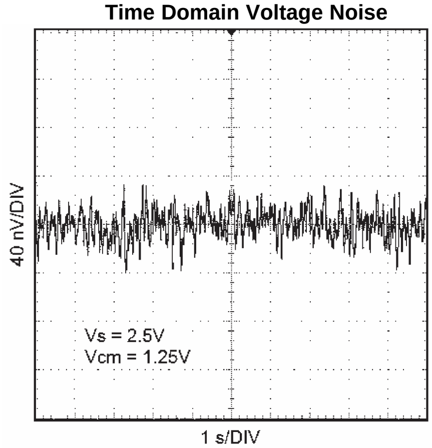


Figure 20.

Time Domain Voltage Noise

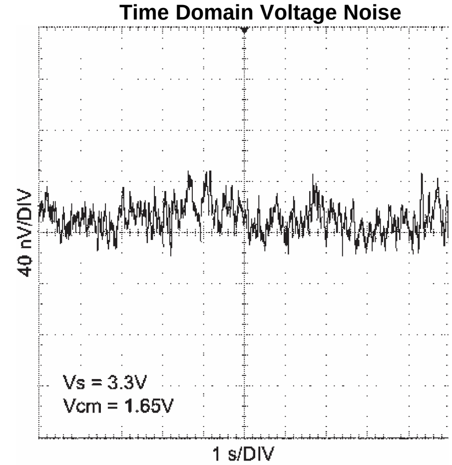


Figure 21.

Time Domain Voltage Noise

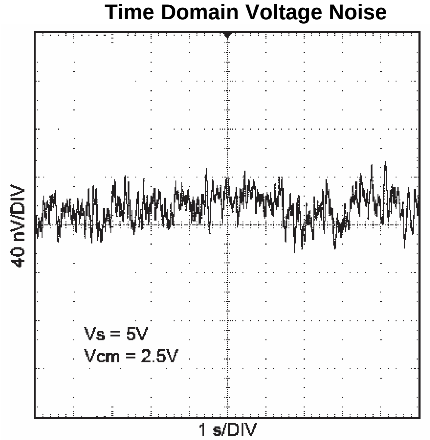


Figure 22.

Output Voltage vs. Output Current

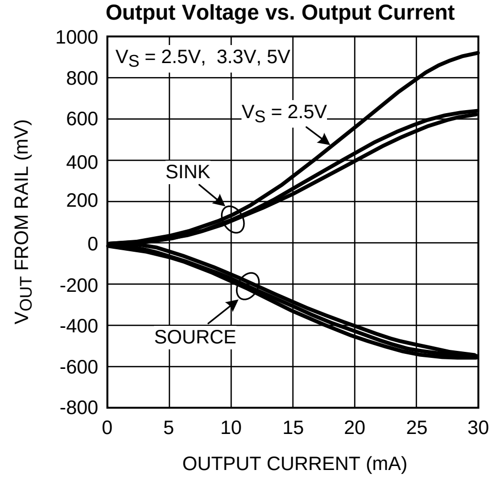


Figure 23.

Input Bias Current vs. V_{CM}

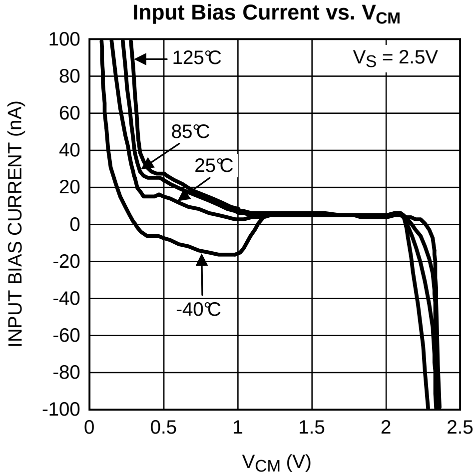


Figure 24.

Input Bias Current vs. V_{CM}

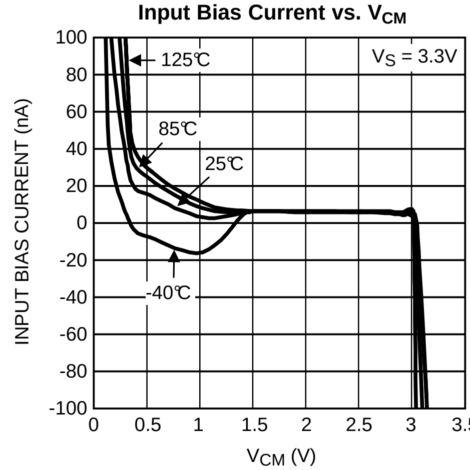


Figure 25.

Typical Performance Characteristics (continued)

Unless otherwise noted: T_A = 25°C, R_L > 10 kΩ, V_{CM} = V_S/2.

Input Bias Current vs. V_{CM}

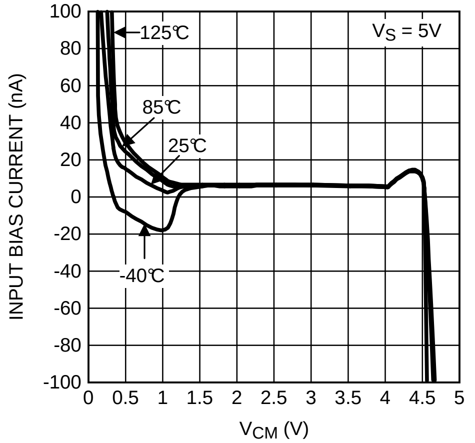


Figure 26.

Open Loop Frequency Response Over Temperature

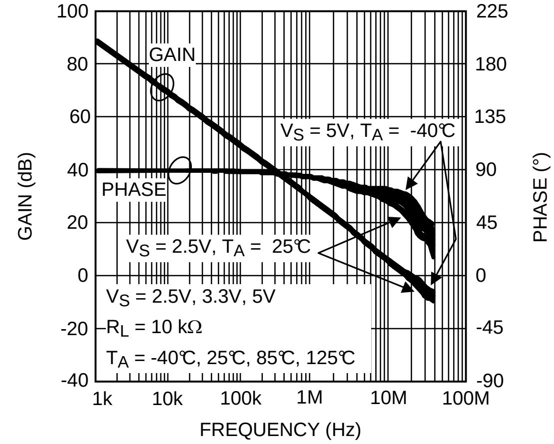


Figure 27.

Open Loop Frequency Response

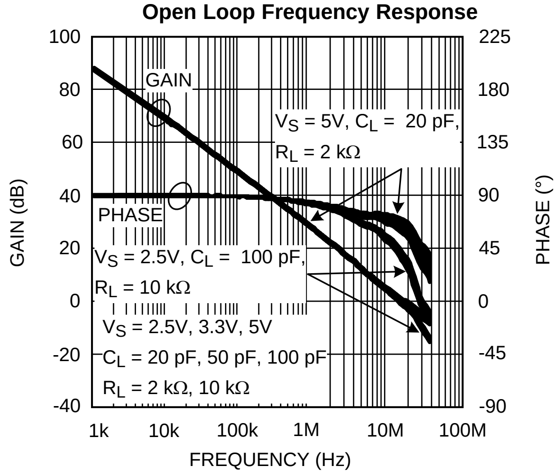


Figure 28.

Open Loop Frequency Response

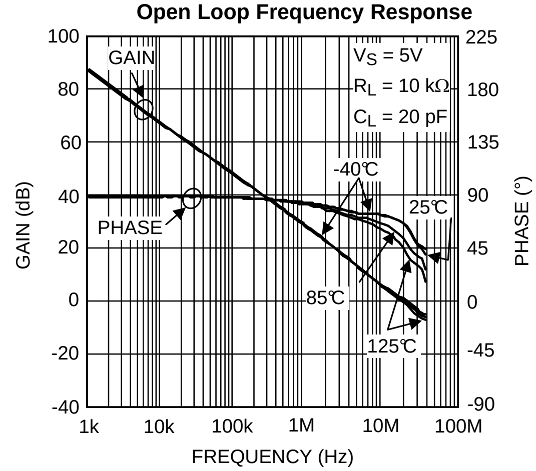


Figure 29.

THD+N vs. Frequency

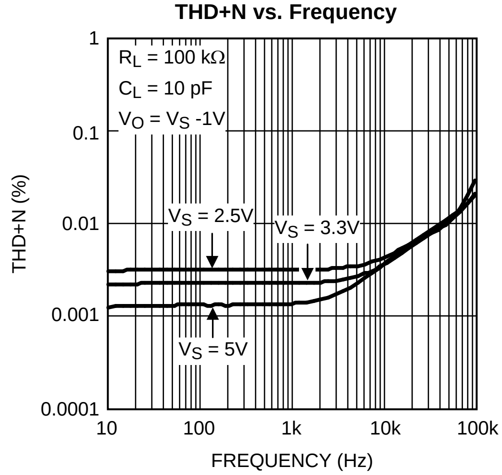


Figure 30.

THD+N vs. Output Voltage

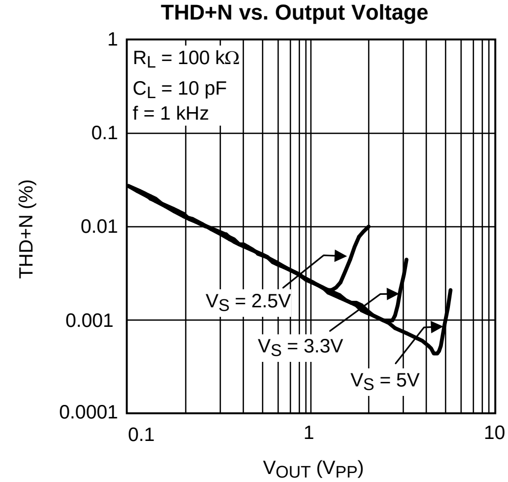


Figure 31.

Typical Performance Characteristics (continued)

Unless otherwise noted: T_A = 25°C, R_L > 10 kΩ, V_{CM} = V_S/2.

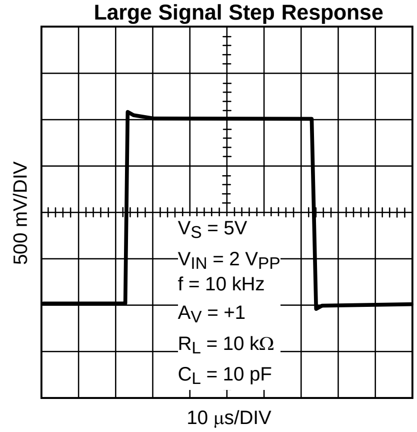


Figure 32.

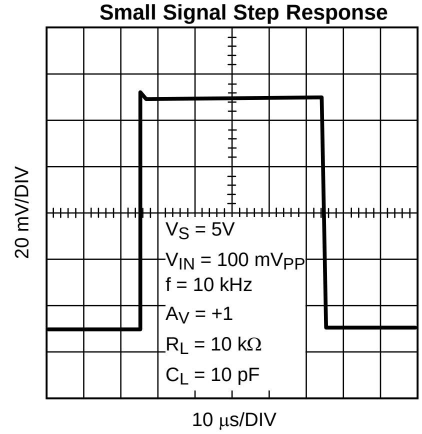


Figure 33.

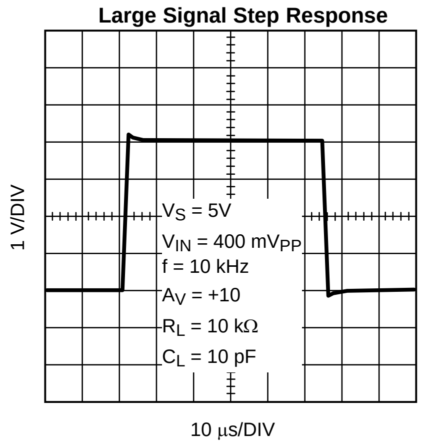


Figure 34.

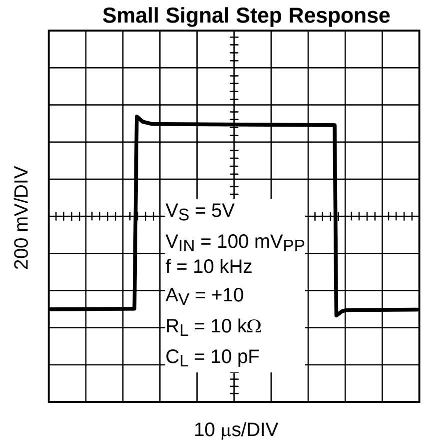


Figure 35.

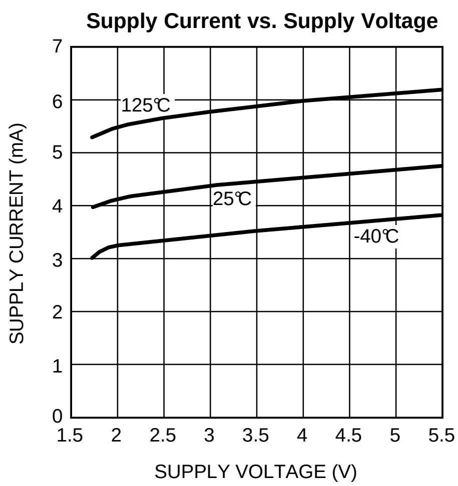


Figure 36.

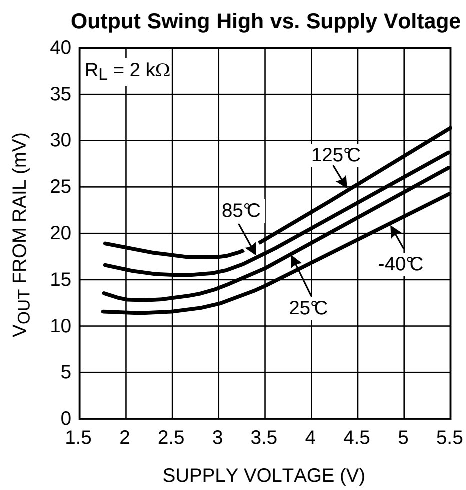


Figure 37.

Typical Performance Characteristics (continued)

Unless otherwise noted: T_A = 25°C, R_L > 10 kΩ, V_{CM} = V_S/2.

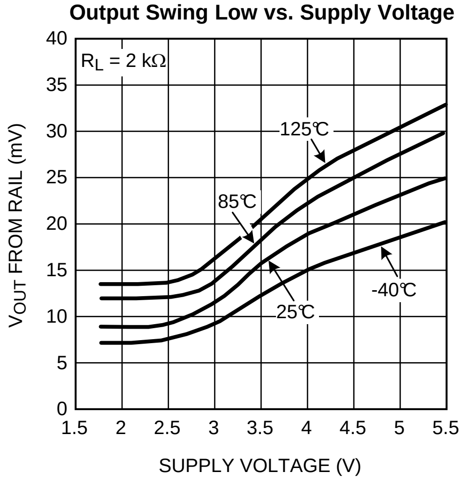


Figure 38.

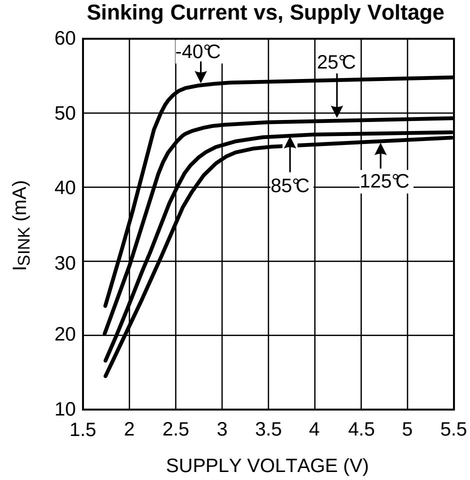


Figure 39.

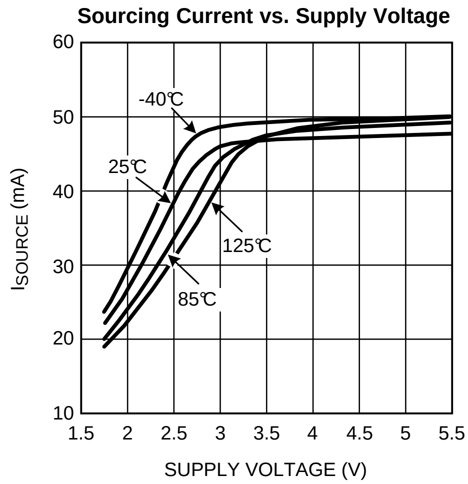


Figure 40.

APPLICATION NOTES

LMP7732

The LMP7732 is a dual low noise, rail-to-rail input and output, low voltage amplifier.

The low input voltage noise of only 2.9 nV/√Hz with a 1/f corner at 3 Hz makes the LMP7732 ideal for sensor applications where DC accuracy is of importance.

The LMP7732 has high gain bandwidth of 22 MHz. This wide bandwidth enables the use of the amplifier at higher gain settings while retaining ample usable bandwidth for the application. This is particularly beneficial when system designers need to use sensors with very limited output voltage range as it allows larger gains in one stage which in turn increases signal to noise ratio.

The LMP7732 has a proprietary input bias cancellation circuitry on the input stages. This allows the LMP7732 to have only about 1.5 nA bias current with a bipolar input stage. This low input bias current, paired with the inherent lower input voltage noise of bipolar input stages makes the LMP7732 an excellent choice for precision applications. The combination of low input bias current, low input offset voltage, and low input voltage noise enables the user to achieve unprecedented accuracy and higher signal integrity.

Texas Instruments is heavily committed to precision amplifiers and the market segment they serve. Technical support and extensive characterization data is available for sensitive applications or applications with a constrained error budget.

The LMP7732 comes in the 8-Pin SOIC and VSSOP packages. These small packages are ideal solutions for area constrained PC boards and portable electronics.

INPUT BIAS CURRENT CANCELLATION

The LMP7732 has proprietary input bias current cancellation circuitry on its input stage.

The LMP7732 has rail-to-rail input. This is achieved by having a p-input and n-input stage in parallel. Figure 41 only shows one of the input stages as the circuitry is symmetrical for both stages.

Figure 41 shows that as the common mode voltage gets closer to one of the extreme ends, current I_1 significantly increases. This increased current shows as an increase in voltage drop across resistor R_1 equal to I_1*R_1 on IN+ of the amplifier. This voltage contributes to the offset voltage of the amplifier. When common mode voltage is in the mid-range, the transistors are operating in the linear region and I_1 is significantly small. The voltage drop due to I_1 across R_1 can be ignored as it is orders of magnitude smaller than the amplifier's input offset voltage. As the common mode voltage gets closer to one of the rails, the offset voltage generated due to I_1 increases and becomes comparable to the amplifiers offset voltage.

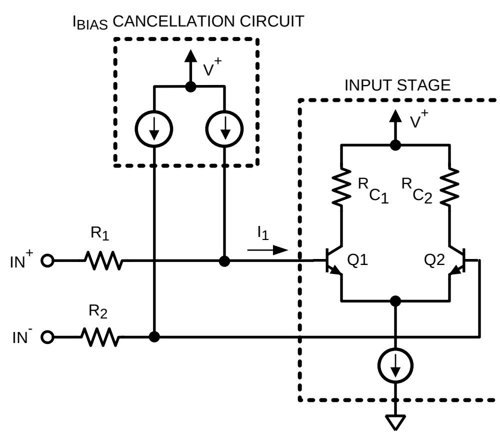


Figure 41. Input Bias Current Cancellation

INPUT VOLTAGE NOISE MEASUREMENT

The LMP7732 has very low input voltage noise. The peak-to-peak input voltage noise of the LMP7732 can be measured using the test circuit shown in Figure 42.

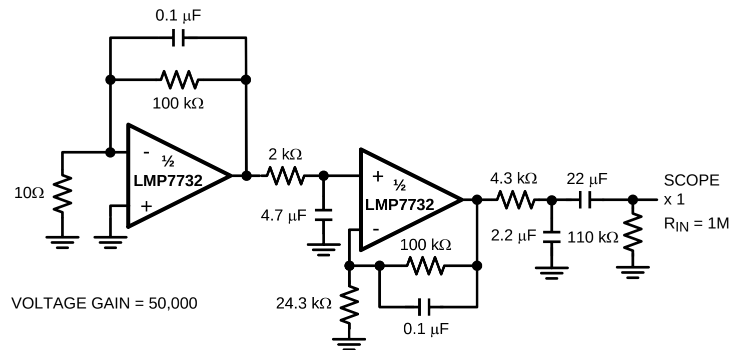


Figure 42. 0.1 Hz to 10 Hz Noise Test Circuit

The frequency response of this noise test circuit at the 0.1 Hz corner is defined by only one zero. The test time for the 0.1 Hz to 10 Hz noise measurement using this configuration should not exceed 10 seconds, as this time limit acts as an additional zero to reduce or eliminate the contributions of noise from frequencies below 0.1 Hz.

Figure 43 shows typical peak-to-peak noise for the LMP7732 measured with the circuit in Figure 42.

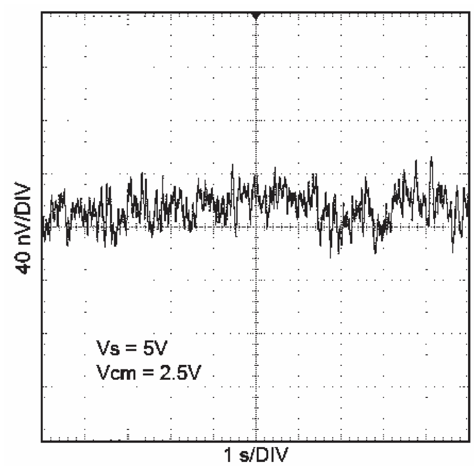


Figure 43. 0.1 Hz to 10 Hz Input Voltage Noise

Measuring the very low peak-to-peak noise performance of the LMP7732, requires special testing attention. In order to achieve accurate results, the device should be warmed up for at least five minutes. This is so that the input offset voltage of the op amp settles to a value. During this warm up period, the offset can typically change by a few µV because the chip temperature increases by about 30°C. If the 10 seconds of the measurement is selected to include this warm up time, some of this temperature change might show up as the measured noise. Figure 44 shows the start-up drift of five typical LMP7732 units.

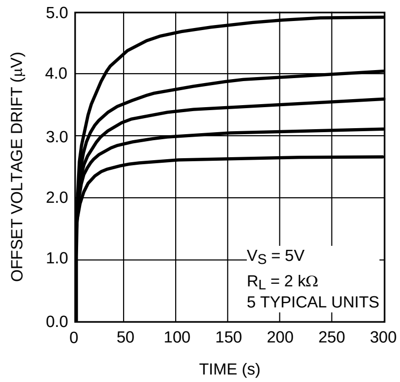


Figure 44. Start-Up Input Offset Voltage Drift

During the peak-to-peak noise measurement, the LMP7732 must be shielded. This prevents offset variations due to airflow. Offset can vary by a few nV due to this airflow and that can invalidate measurements of input voltage noise with a magnitude which is in the same range. For similar reasons, sudden motions must also be restricted in the vicinity of the test area. The feed-through which results from this motion could increase the observed noise value which in turn would invalidate the measurement.

DIODES BETWEEN THE INPUTS

The LMP7732 has a set of anti-parallel diodes between their input pins, as shown in Figure 45. These diodes are present to protect the input stage of the amplifiers. At the same time, they limit the amount of differential input voltage that is allowed on the input pins. A differential signal larger than the voltage needed to turn on the diodes might cause damage to the diodes. The differential voltage between the input pins should be limited to ±3 diode drops or the input current needs to be limited to ±20 mA.

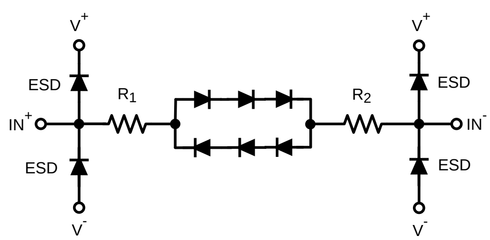


Figure 45. Anti-Parallel Diodes between Inputs

DRIVING AN ADC

Analog to Digital Converters, ADCs, usually have a sampling capacitor on their input. When the ADC's input is directly connected to the output of the amplifier a charging current flows from the amplifier to the ADC. This charging current causes a momentary glitch that can take some time to settle. There are different ways to minimize this effect. One way is to slow down the sampling rate. This method gives the amplifier sufficient time to stabilize its output. Another way to minimize the glitch, caused by the switch capacitor, is to have an external capacitor connected to the input of the ADC. This capacitor is chosen so that its value is much larger than the internal switching capacitor and it will hence provide the charge needed to quickly and smoothly charge the ADC's sampling capacitor. Since this large capacitor will be loading the output of the amplifier as well, an isolation resistor is needed between the output of the amplifier and this capacitor. The isolation resistor, R_{ISO}, separates the additional load capacitance from the output of the amplifier and will also form a low-pass filter and can be designed to provide noise reduction as well as anti-aliasing. The draw back of having R_{ISO} is that it reduces signal swing since there is some voltage drop across it.

Figure 46 (a) shows the ADC directly connected to the amplifier. To minimize the glitch in this setting, a slower sample rate needs to be used. Figure 46 (b) shows R_{ISO} and an external capacitor used to minimize the glitch.

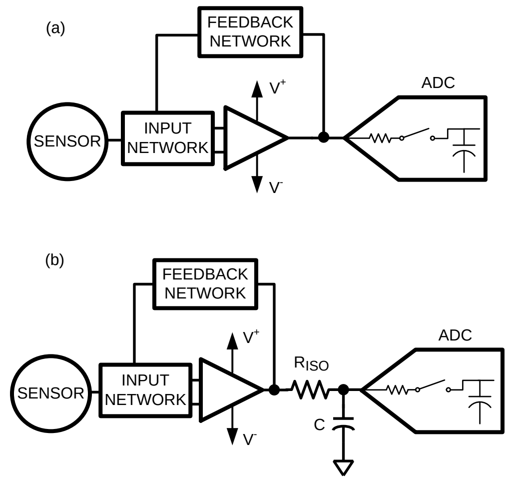


Figure 46. Driving An ADC

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMP7732MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP77 32MA	Samples
LMP7732MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP77 32MA	Samples
LMP7732MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		AZ3A	Samples
LMP7732MME/NOPB	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		AZ3A	Samples
LMP7732MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		AZ3A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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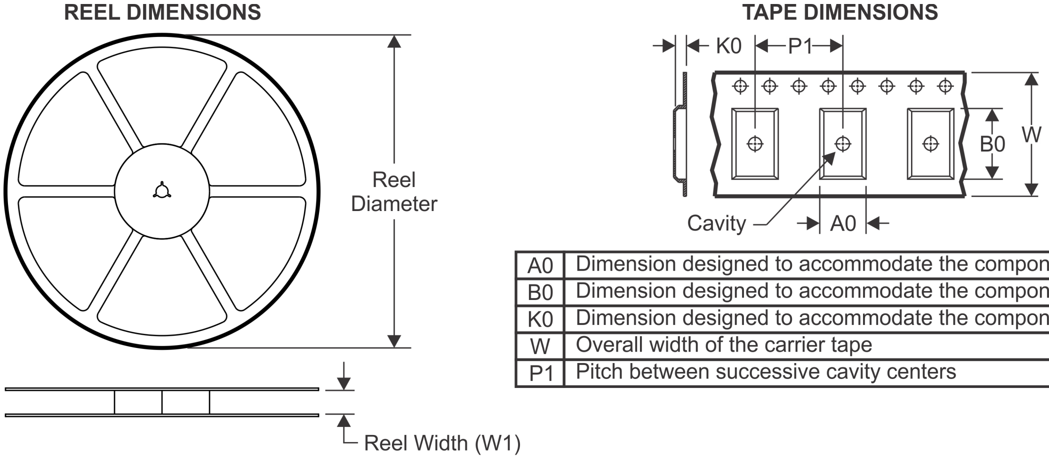
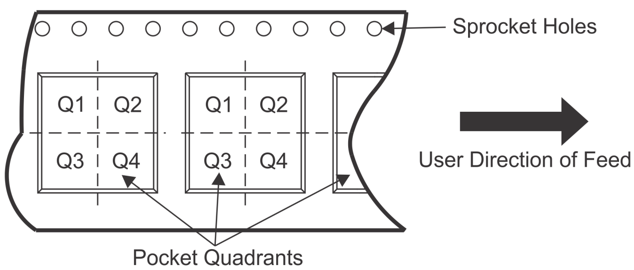
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



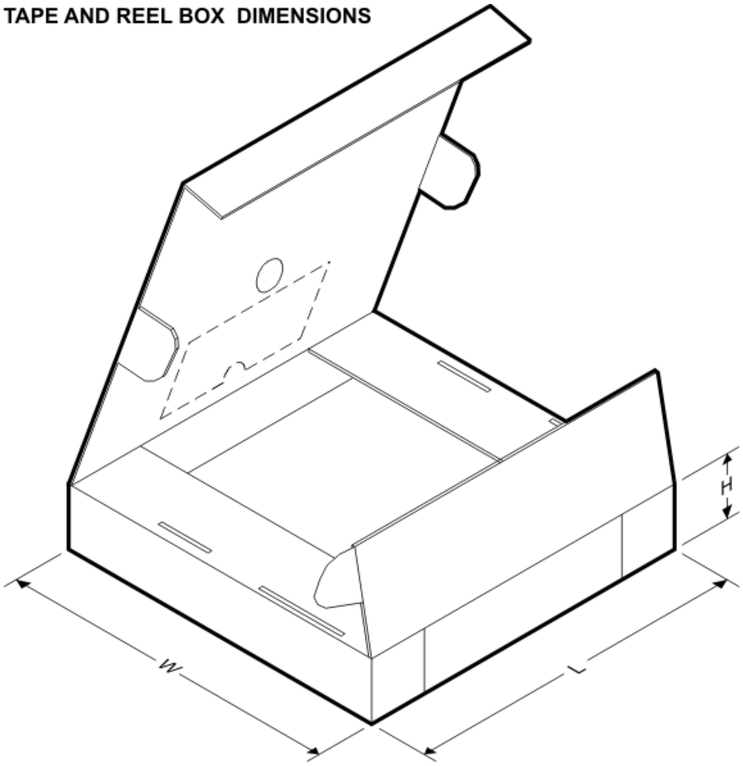
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP7732MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP7732MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP7732MME/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP7732MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

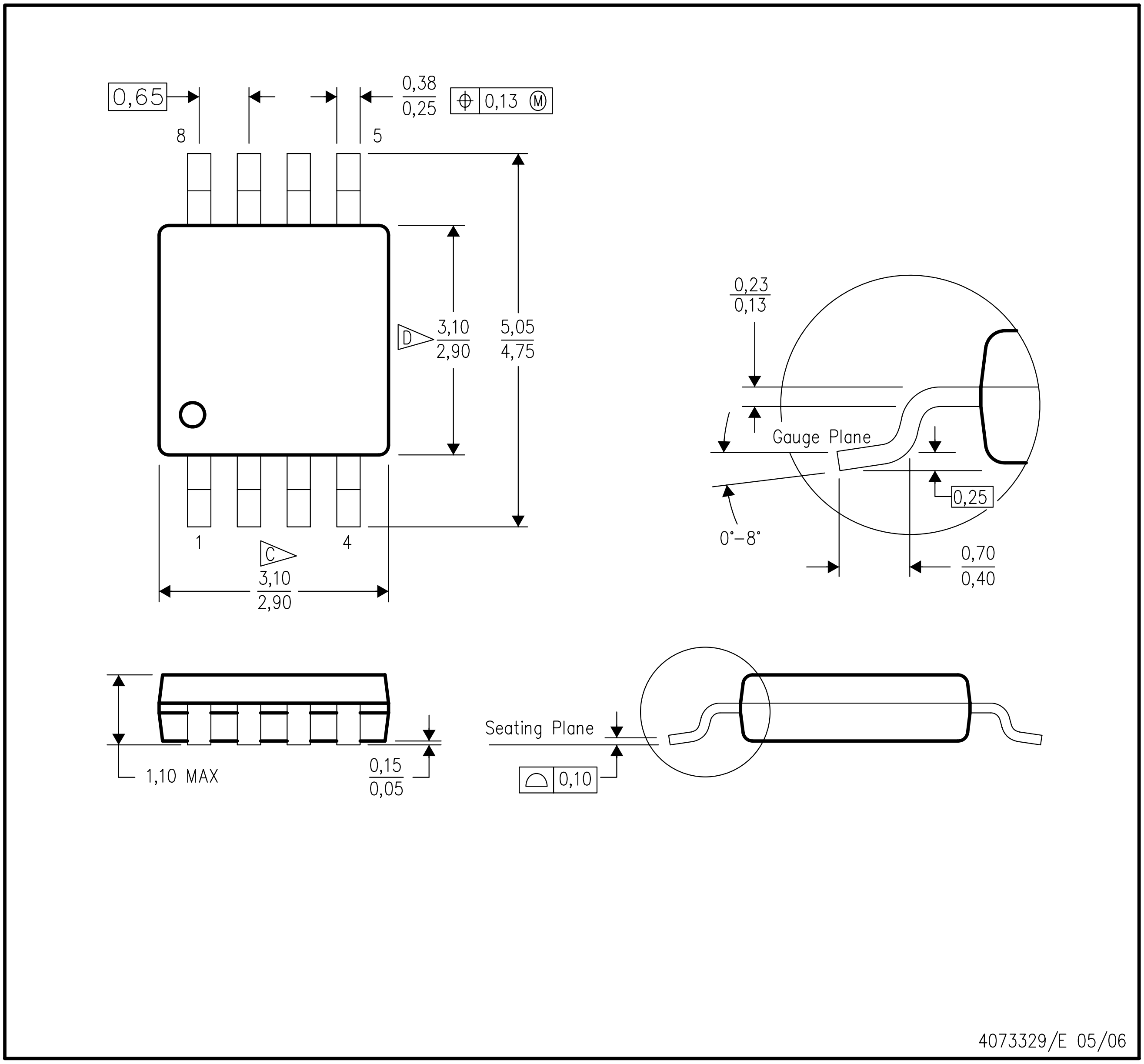
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

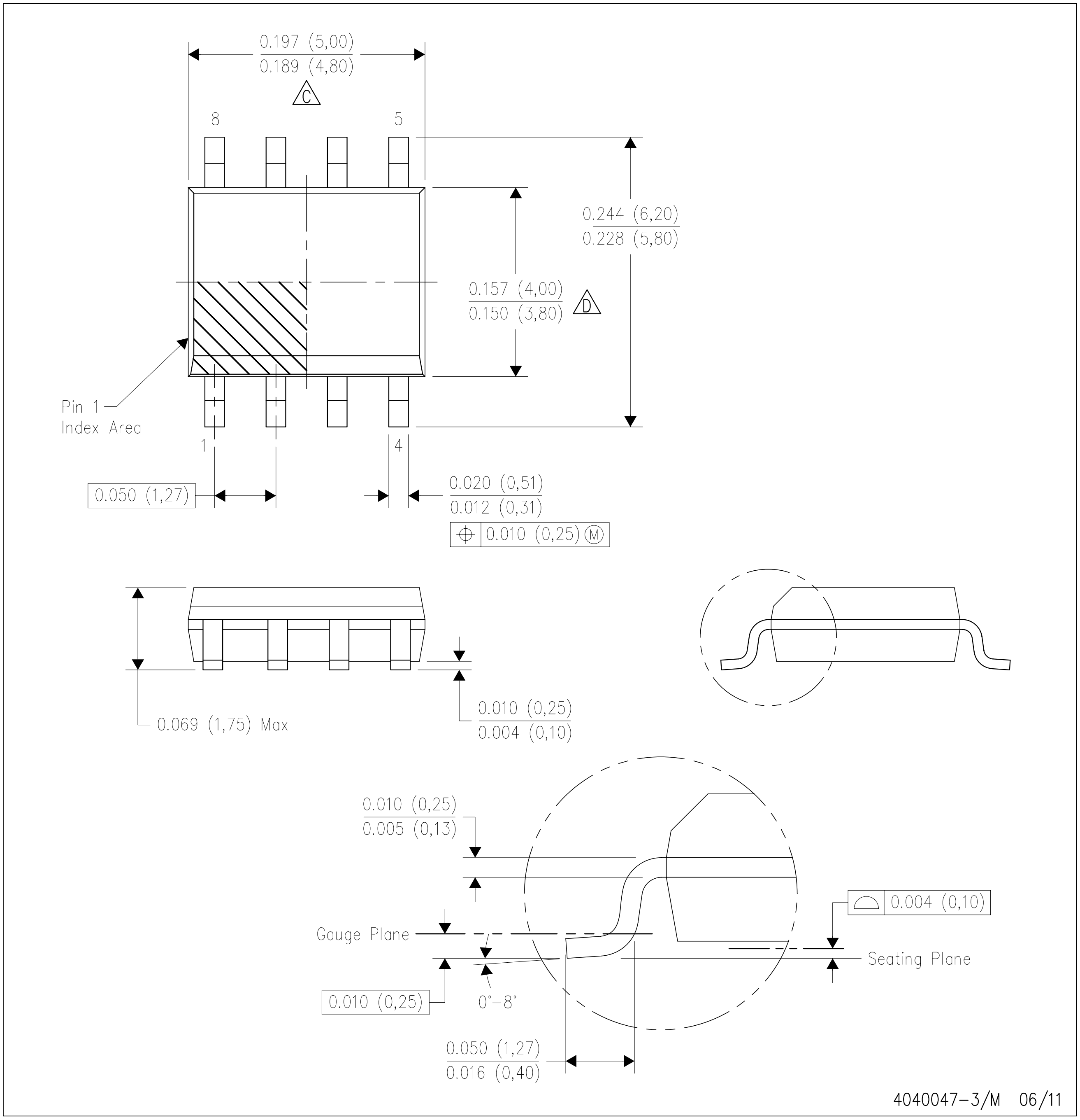
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP7732MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMP7732MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMP7732MME/NOPB	VSSOP	DGK	8	250	210.0	185.0	35.0
LMP7732MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.