

Description

The G12N10 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

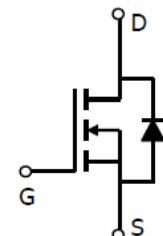
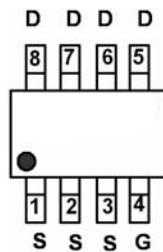
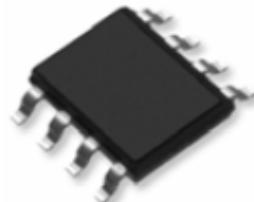
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V _{DSS}	R _{DS(ON)} @4.5V(Typ)	R _{DS(ON)} @10V(Typ)	I _D
100V	15.5 mΩ	14.5 mΩ	12A

- Special process technology for high ESD capability
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current

Application

- DC/DC Primary Side Switch
- Telecom/Server
- Synchronous Rectification

**Schematic diagram****Marking and pin assignment****SOP-8****Absolute Maximum Ratings (T_A=25°C unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	100	V
Gate-Source Voltage	V _{GS}	±20	V
Drain Current-Continuous	I _D	12	A
Drain Current-Continuous(T _C =100°C)	I _D (100°C)	8.4	A
Pulsed Drain Current	I _{DM}	70	A
Maximum Power Dissipation	P _D	3.1	W
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient ^(Note 2)	R _{θJA}	40	°C/W
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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

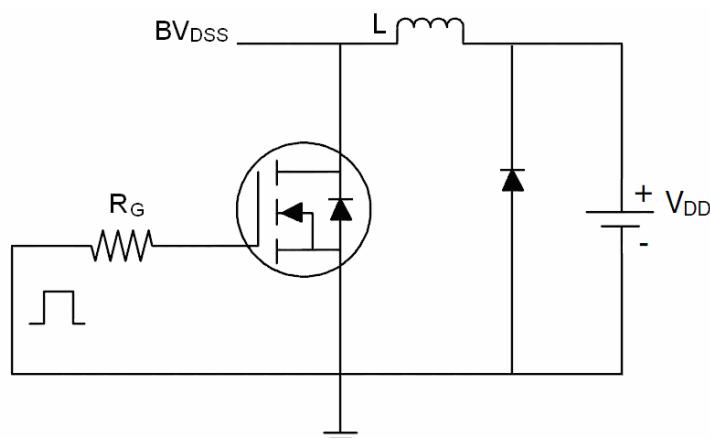
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	100	110	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=100\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1.2	1.7	2.2	V
Drain-Source On-State Resistance	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=6\text{A}$	-	14.5	17	$\text{m}\Omega$
Drain-Source On-State Resistance	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=6\text{A}$	-	15.5	20	$\text{m}\Omega$
Forward Transconductance	g_{FS}	$V_{\text{DS}}=10\text{V}, I_{\text{D}}=6\text{A}$	-	26	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{\text{DS}}=50\text{V}, V_{\text{GS}}=0\text{V}, F=1.0\text{MHz}$	-	3800	-	PF
Output Capacitance	C_{oss}		-	690	-	PF
Reverse Transfer Capacitance	C_{rss}		-	291	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}}=50\text{V}, I_{\text{D}}=6\text{A}, R_L=5\Omega, R_G=1\Omega, V_{\text{GS}}=10\text{V}$	-	13	-	nS
Turn-on Rise Time	t_r		-	14	-	nS
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$		-	25	-	nS
Turn-Off Fall Time	t_f		-	10	-	nS
Total Gate Charge	Q_g	$I_{\text{D}}=6\text{A}, V_{\text{DD}}=50\text{V}, V_{\text{GS}}=10\text{V}$	-	95	-	nC
Gate-Source Charge	Q_{gs}		-	16	-	nC
Gate-Drain Charge	Q_{gd}		-	24	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{\text{GS}}=0\text{V}, I_{\text{S}}=12\text{A}$	-	0.85	1.2	V
Diode Forward Current ^(Note 2)	I_{S}		-	-	10	A
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}, I_F = 12\text{A}$ $dI/dt = 100\text{A}/\mu\text{s}$ ^(Note 3)	-	33		nS
Reverse Recovery Charge	Q_{rr}		-	54		nC

Notes:

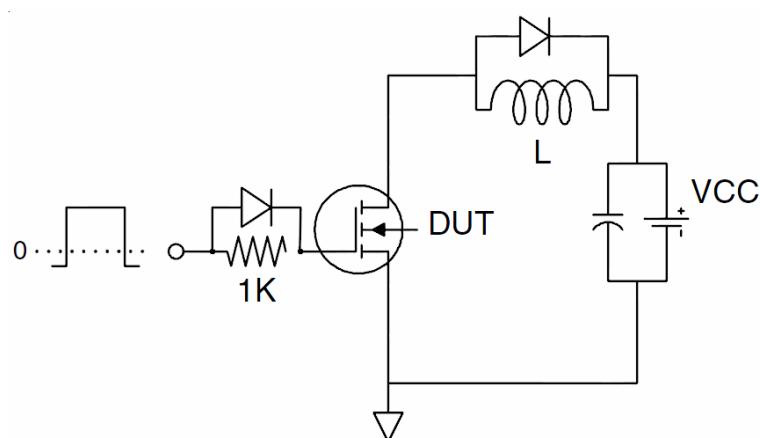
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

Test Circuit

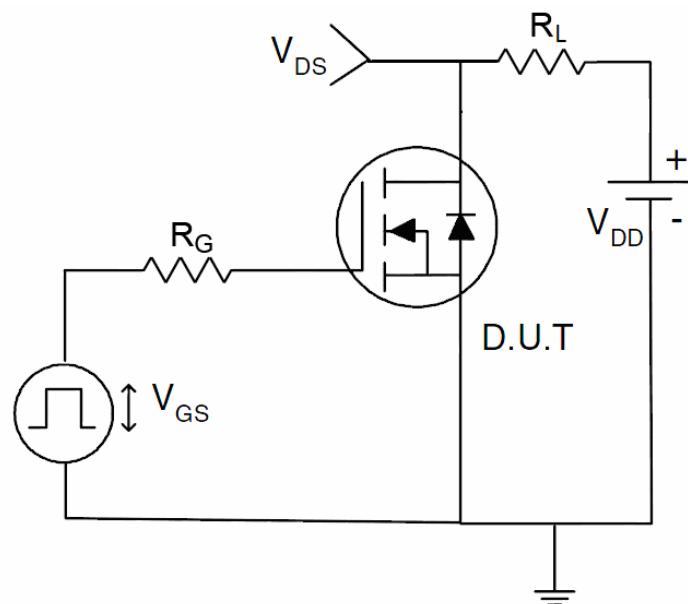
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

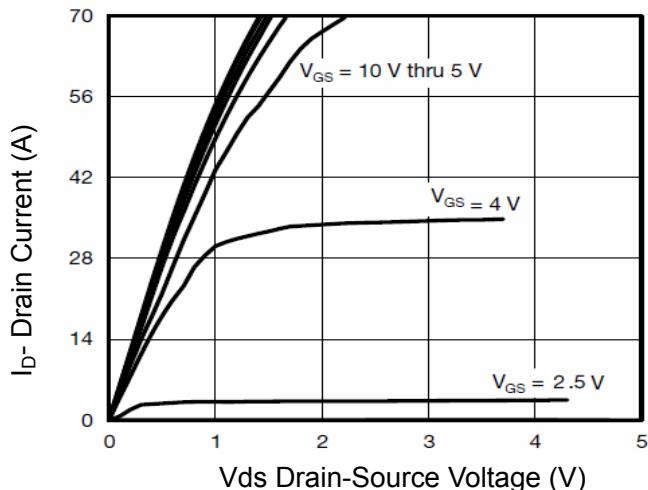


Figure 1 Output Characteristics

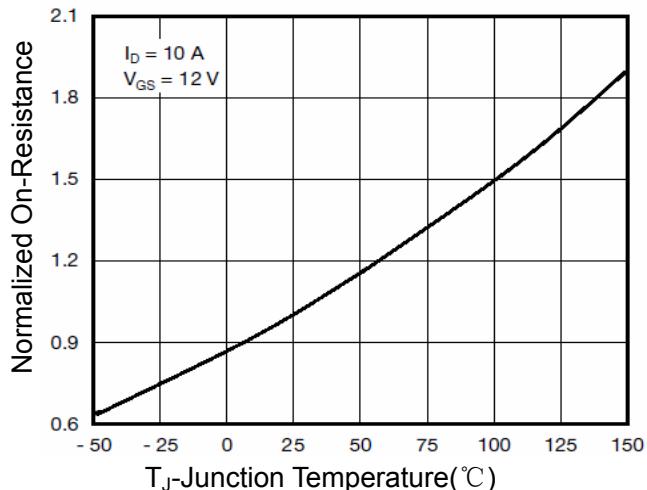


Figure 4 Rdson-JunctionTemperature

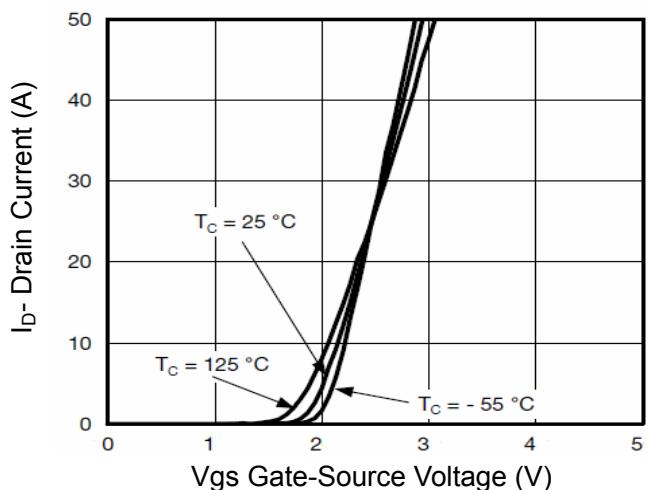


Figure 2 Transfer Characteristics

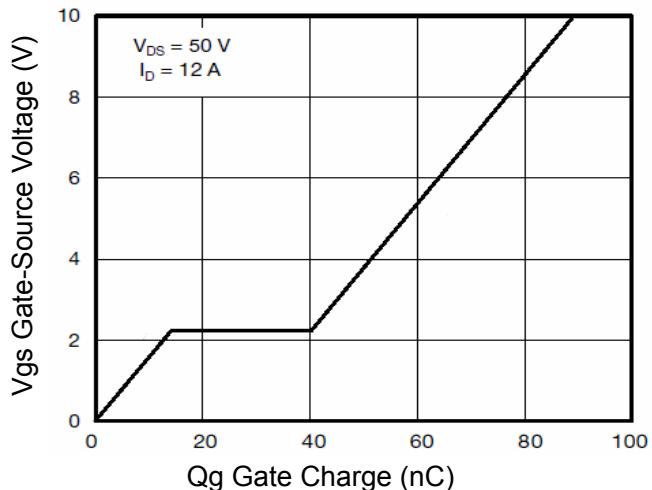


Figure 5 Gate Charge

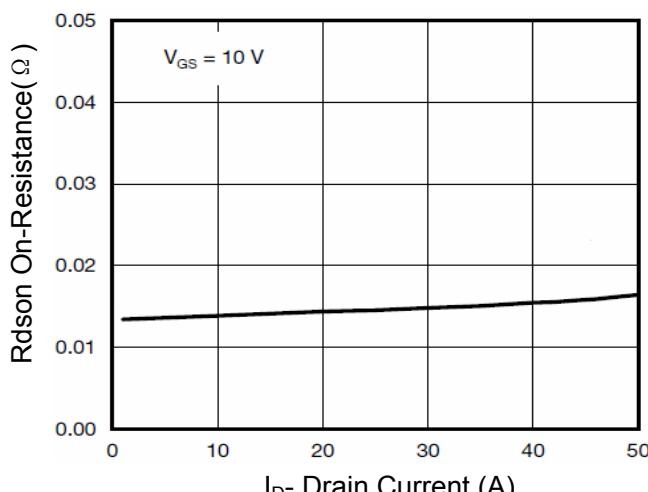


Figure 3 Rdson- Drain Current

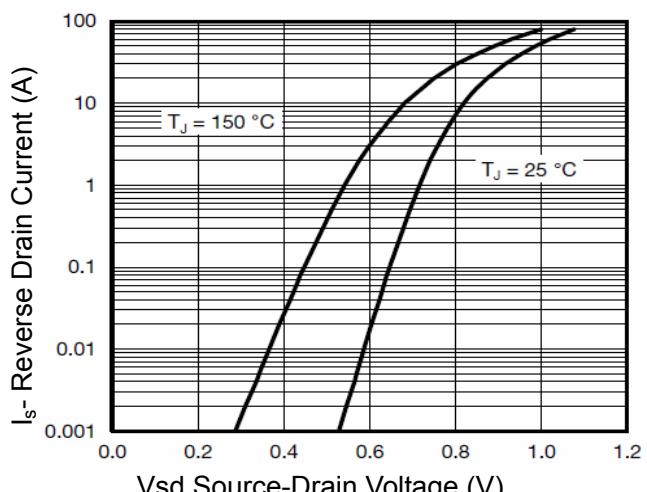


Figure 6 Source- Drain Diode Forward

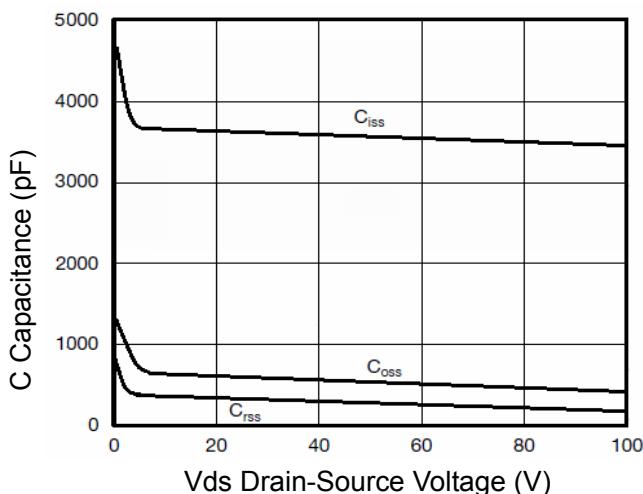


Figure 7 Capacitance vs Vds

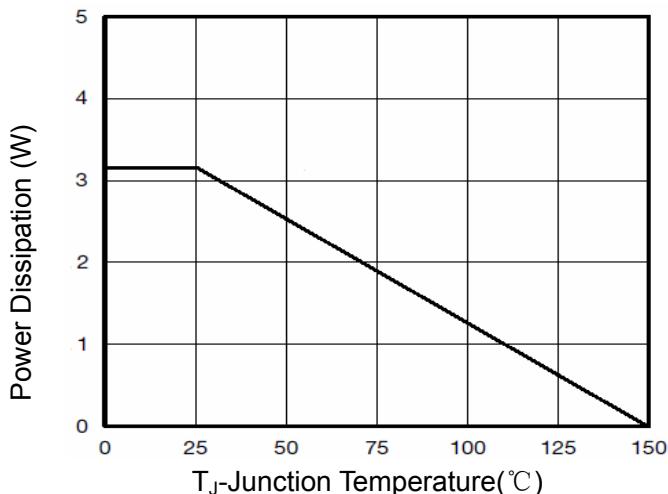


Figure 9 Power De-rating

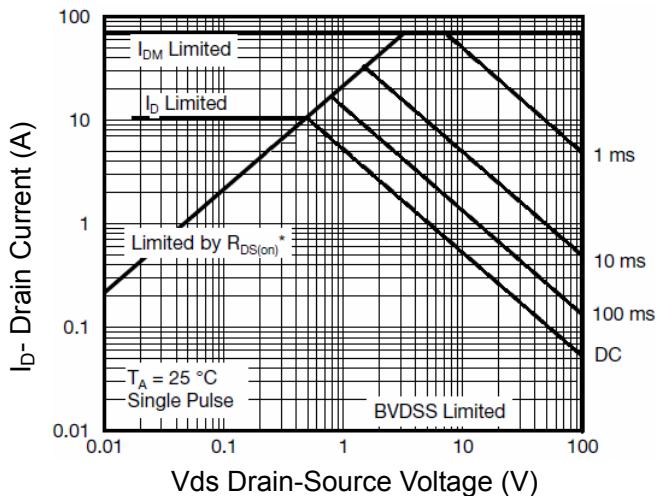


Figure 8 Safe Operation Area

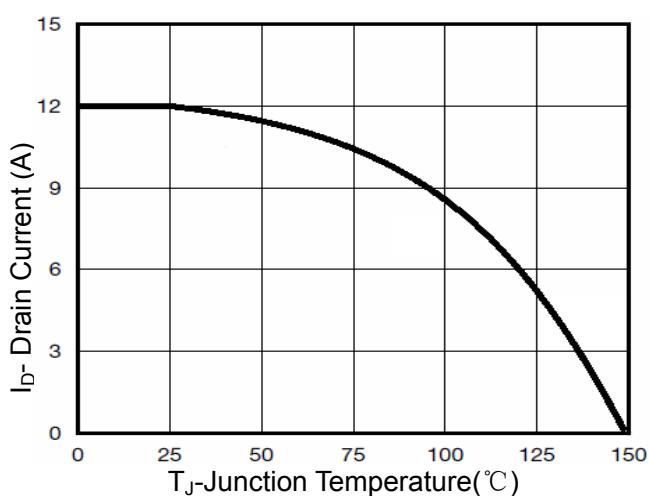


Figure 10 Current De-rating

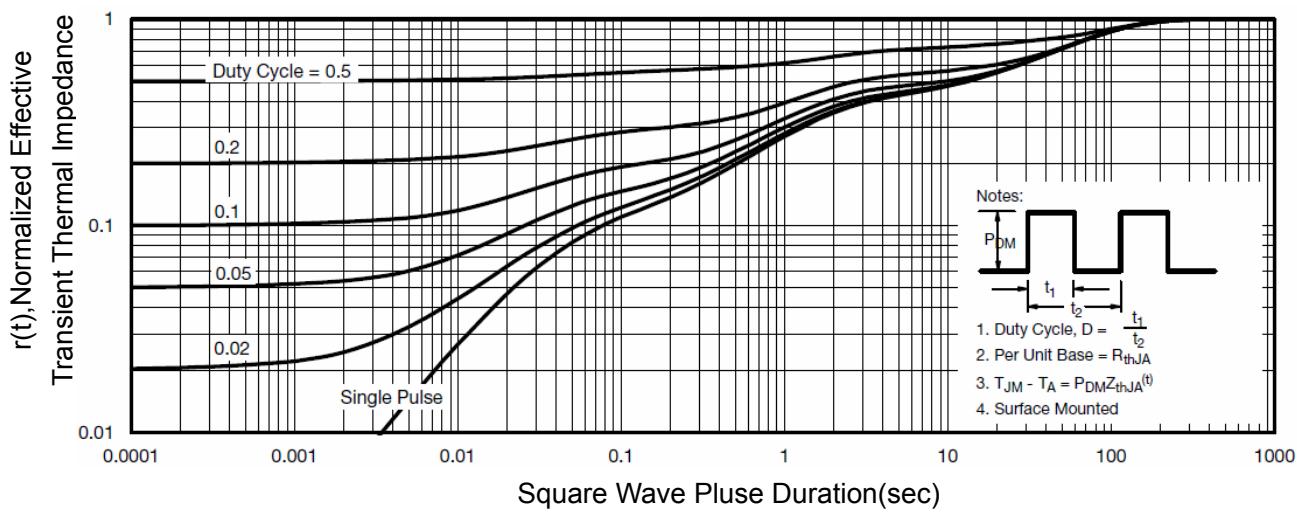


Figure 11 Normalized Maximum Transient Thermal Impedance