Description

· Trench Power MV MOSFET technology
· Low $R_{DS(ON)}$
· Low Gate Charge
· Optimized for fast-switching applications

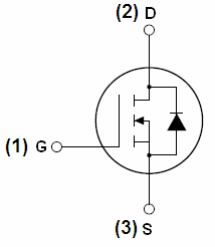
General Features

VDSS	RDS(ON) @10V (typ)	RDS(ON) @4.5V (typ)	ID
100V	6.2mΩ	8.5 mΩ	48A

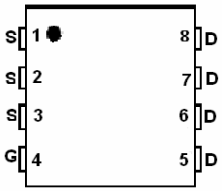
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

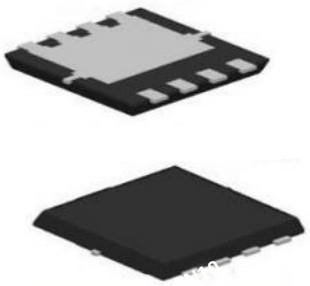
· Synchronus Rectification in DC/DC and AC/DC Converters
· Industrial and Motor Drive applications



Schematic diagram



Marking and pin assignment



DFN 5x6

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [G]	T_C=25°C (Package Limited)	I_D	48	A
	T_C=100°C		43	
Pulsed Drain Current [C]		I_{DM}	105	A
Continuous Drain Current	T_A=25°C	I_{DSM}	22	A
	T_A=100°C		18	
Avalanche energy L=0.3mH [C]		E_{AS}	105	mJ
Power Dissipation [B]	T_C=25°C	P_D	75	W
	T_C=100°C		30	
Power Dissipation [A]	T_A=25°C	P_{DSM}	8.3	W
	T_A=70°C		6.6	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Maximum		Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	12	15	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		32	40	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	1.4	1.67	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0V	100	115		V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=100V, V_{GS}=0V			1	μA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.3	1.9	2.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=24A		6.2	7.3	mΩ
		T_J=125°C		10.9	12.8	
		V_{GS}=4.5V, I_D=24A		8.5	10.0	
g_{FS}	Diode Forward Voltage	V_{DS}=5V, I_D=20A	30			S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.7	0.95	V
I_S	Maximum Body-Diode Continuous Current [G]				48	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		2808		pF
C_{oss}	Output Capacitance			961		pF
C_{rss}	Reverse Transfer Capacitance			23		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		2		Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=50V, I_D=24A		50		nC
Q_g(4.5V)	Total Gate Charge			33		nC
Q_{gs}	Gate Source Charge			17		nC
Q_{gd}	Gate Drain Charge			11		nC
$t_{D(on)}$	Turn-on Delay Time	V_{GS}=10V, V_{DS}=50V, R_L=2.5Ω, R_{GEN}=3Ω		15		ns
t_r	Turn-on Rise Time			12		ns
$t_{D(off)}$	Turn-off Delay Time			25		ns
t_f	Turn-off Fall Time			13		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A,di/dt=500A/μs		45		ns
Q_{rr}	Body Diode Reverse Recovery charge	I_F=20A,di/dt=500A/μs		140		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature TJ(MAX)=150° C.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

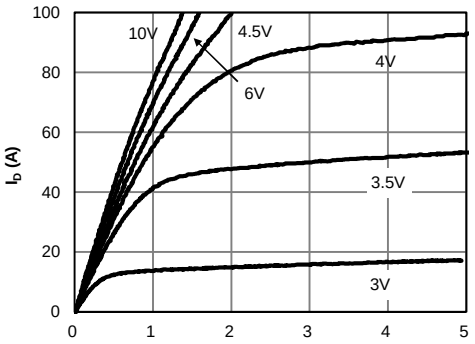


Figure 1: On-Region Characteristics (Note E)

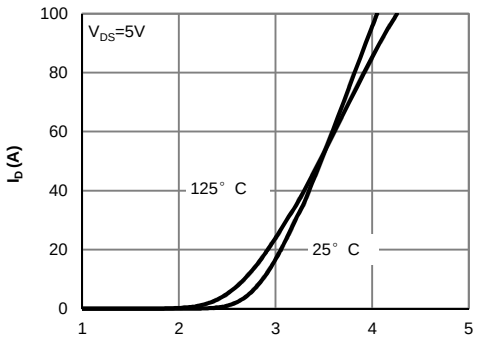


Figure 2: Transfer Characteristics (Note E)

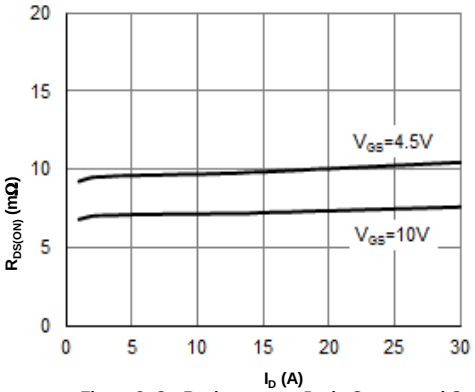


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

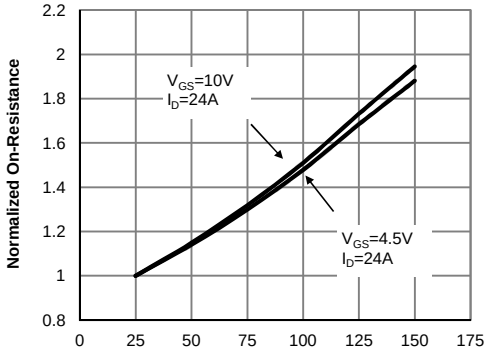


Figure 4: On-Resistance vs. Junction Temperature (Note E)

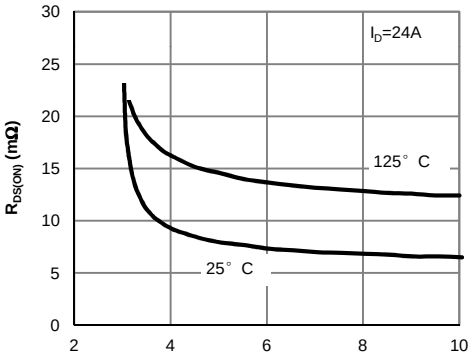


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

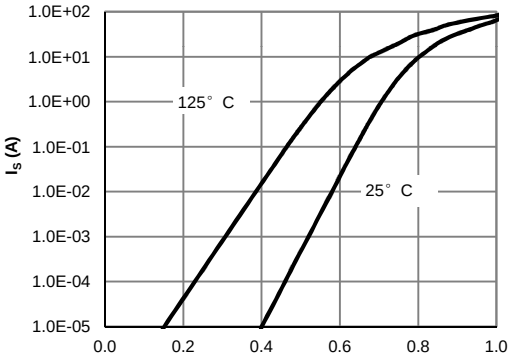


Figure 6: Body-Diode Characteristics (Note E)

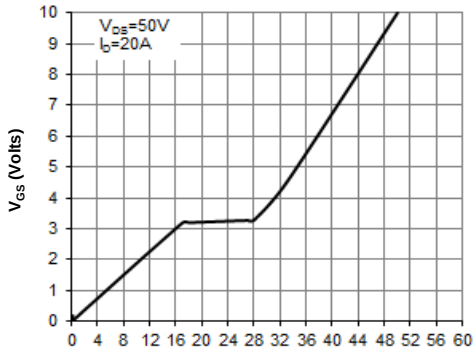


Figure 7: Gate-Charge Characteristics

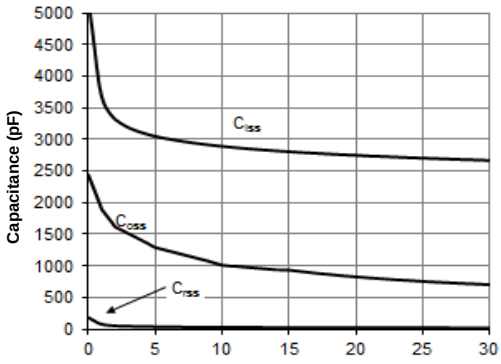
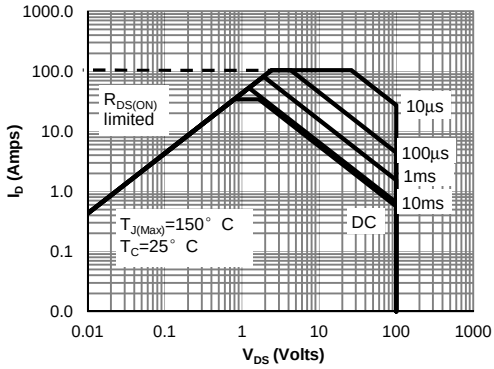


Figure 8: Capacitance Characteristics



V_{GS}> or equal to 4.5V

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

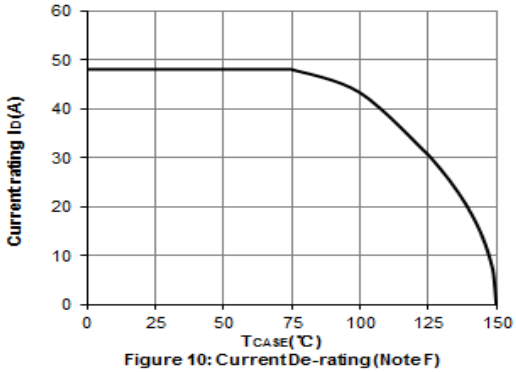


Figure 10: Current De-rating (Note F)

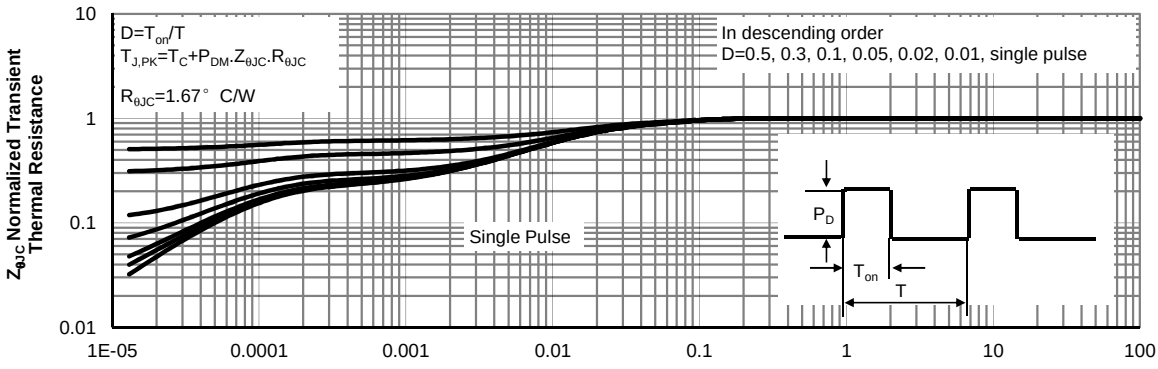


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Figure A: Gate Charge Test Circuit & Waveforms

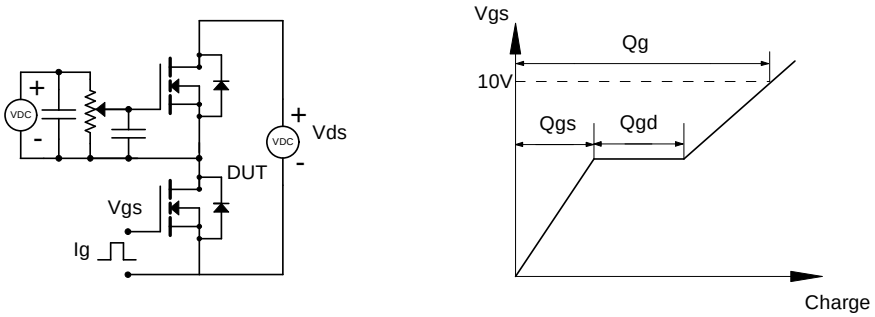


Figure B: Resistive Switching Test Circuit & Waveforms

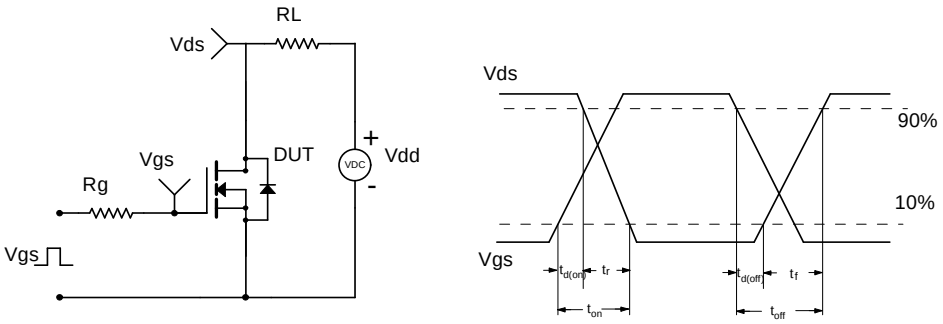


Figure C: Unclamped Inductive Switching (UIS) Test

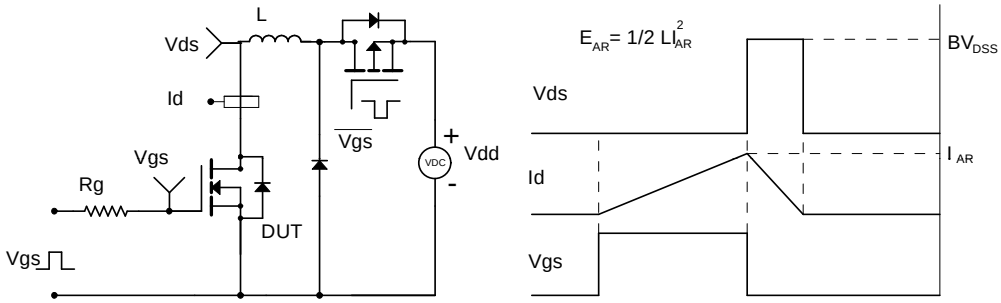


Figure D: Diode Recovery Test Circuit & Waveforms