DESCRIPTION

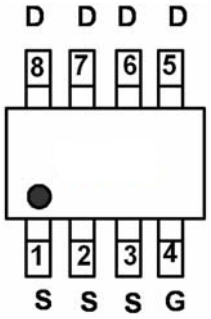
The 10N03 uses advanced trench technology

And design to provide excellent RDS (ON) with

Low gate charge . It can be used in a wide

Vanety of applications .

V_{DS}	$R_{DS(ON)}$	I_D
30V	--	10A

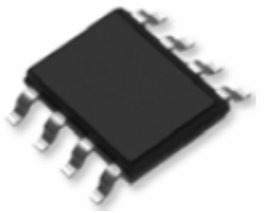


Marking and pin Assignment

GENERAL FEATURES

- V_{DS} = 30 V, I_D = 10 A

  $R_{DS(ON)}$ < 13.5 mΩ @ V_{GS} = 10 V
- High density cell design for ultra low Rdson
- Fully characterized Avalanche voltage and current
- Good stabilty and unifomity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability



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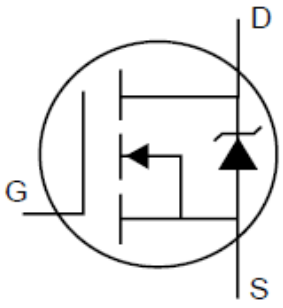
Application

- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



Absolute Maximum Ratings (TC=25℃, unless otherwise noted)

Symbol	Parameter	10N03	Units
V_{DS}	Drain-to-Source Voltage	30	V
I_D	Continuous Drain Current	10	A
	Drain Current-Continuous(Tc=100℃)	6	
I_{DM}	Pulsed Drain Current	50	
P_D	Power Dissipation	2.5	W
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single PulseAvalanche Energy	--	--
T_J and T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	℃

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	--	--	50	℃/W	Water cooled heatsink, PD adjusted for a peak junction temperature of +150℃.

OFF Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
B_{VDSS}	Drain-to-Source Breakdown Voltage	30	33	--	V	V_{GS}=0, I_D=250μA
I_{GSS}	Gate-to-Source Forward Leakage	--	--	±100	nA	V_{DS}=0V, V_{GS}=±20V
I_{DSS}	Zero Gate Voltage Drain Current	--	--	1	μA	V_{DS}=30V, V_{GS}=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max	Units	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	7.5	13.5	mΩ	V_{GS}=10V,I_D=10A
$V_{GS(TH)}$	Gate Threshold Voltage, Figure 12.	1.0	1.5	3.0	V	V_{DS}= V_{GS}, I_D=250μA
G_{fs}	Forward Transconductance	15	---	--	S	V_{DS}=15V, I_D=10A

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C_{iss}	Input Capacitance	--	1550	--	pF	V_{DS}=15V,V_{GS}=0V, f=1.0MHZ
C_{oss}	Output Capacitance	--	300	--		
C_{rss}	Reverse Transfer Capacitance	--	180	--		
Q_g	Total Gate Charge	--	13	--	nC	V_{DS}=15V, V_{GS}=5V, I_D=10A
Q_{gs}	Gate-to-Source Charge	--	5.5	--		
Q_{gd}	Gate-to-Drain (“Miller”) Charge	--	3.5	--		

Drain-Source Diode Characteristics

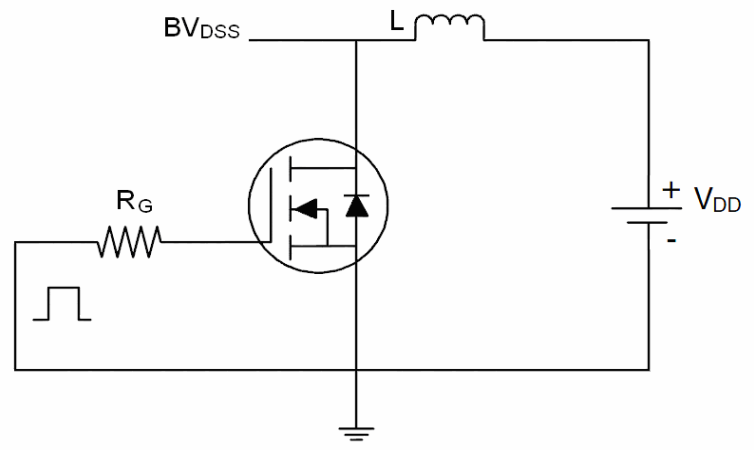
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=10A	--	--	1.2	V
Diode Forward Current	I_S	--	--	--	10	A
Reverse Recovery Time	t_{rr}	--	--	--	--	nS
Reverse Recovery Charge	Q_{rr}		--	--	--	nC
Forword Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD				

Notes:

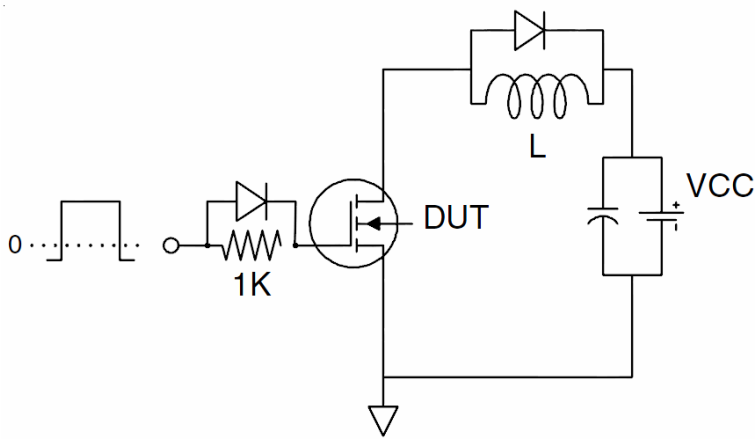
1. Repetitive Rating:Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤10 sec.
3. Pulse Test:Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production.

Test circuit

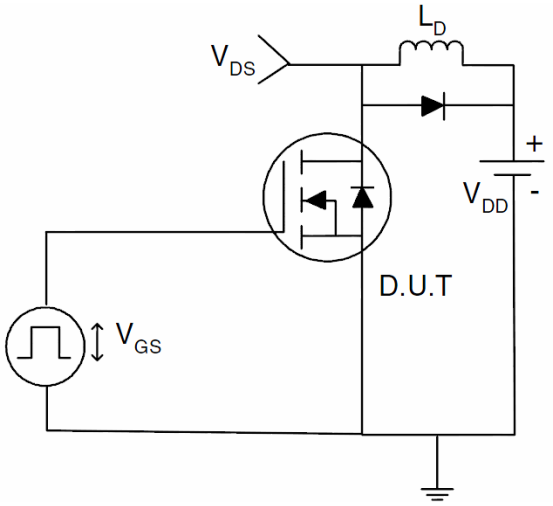
1）E_{AS} test Circuits



2）Gate charge test Circuit:



3）Switch Time Test Circuit：



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

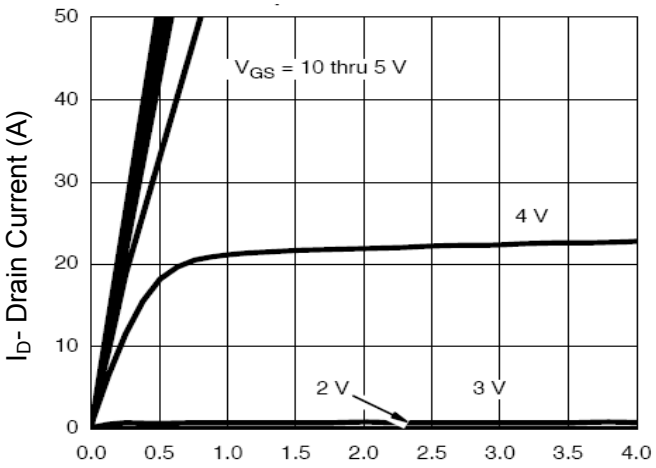


Figure 1 Output Characteristics

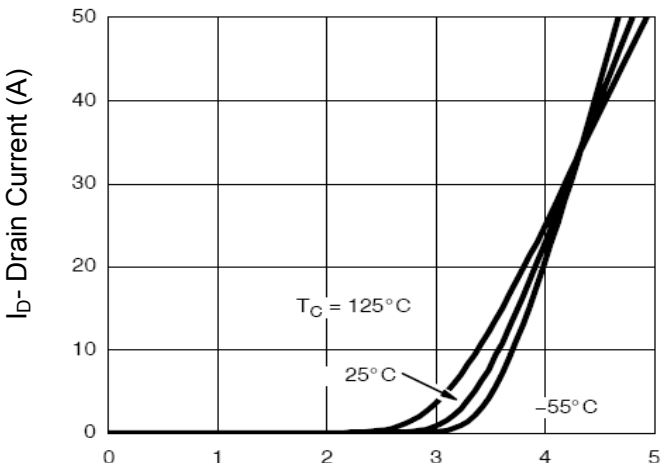


Figure 2 Transfer Characteristics

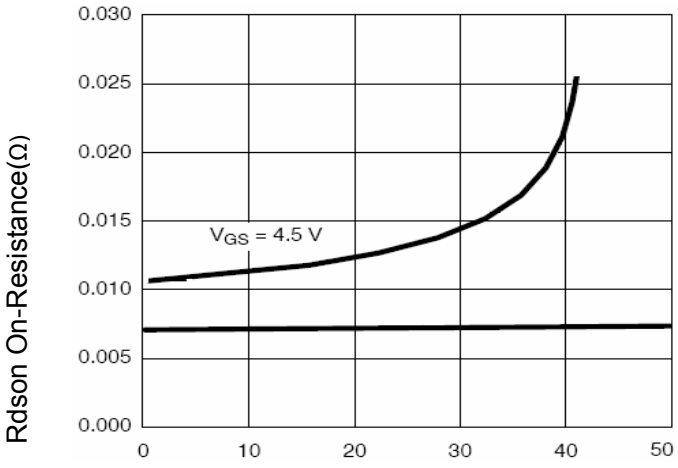


Figure 3 Rdson- Drain Current

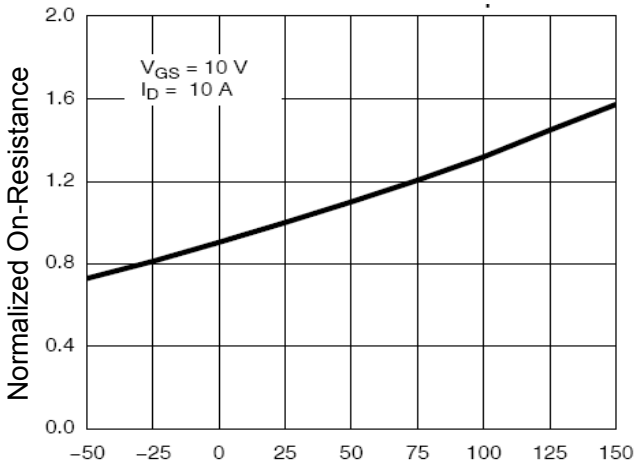


Figure 4 Rdson-JunctionTemperature

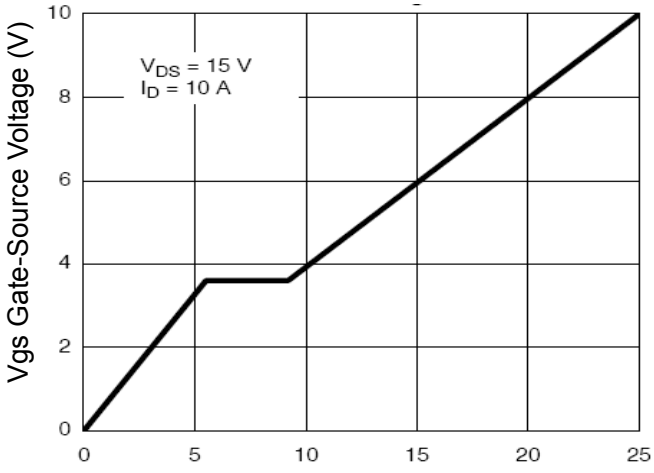


Figure 5 Gate Charge

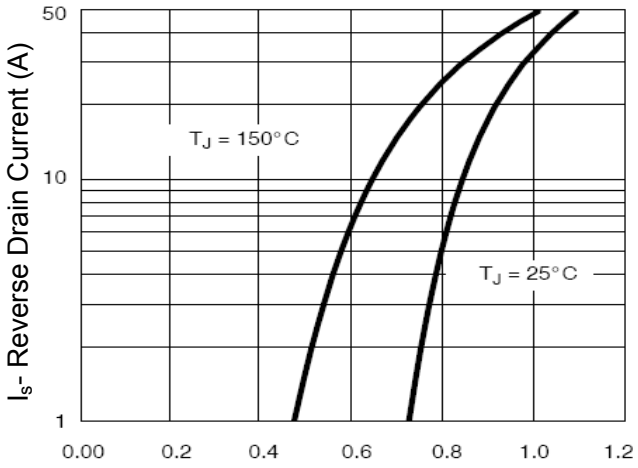


Figure 6 Source- Drain Diode Forward

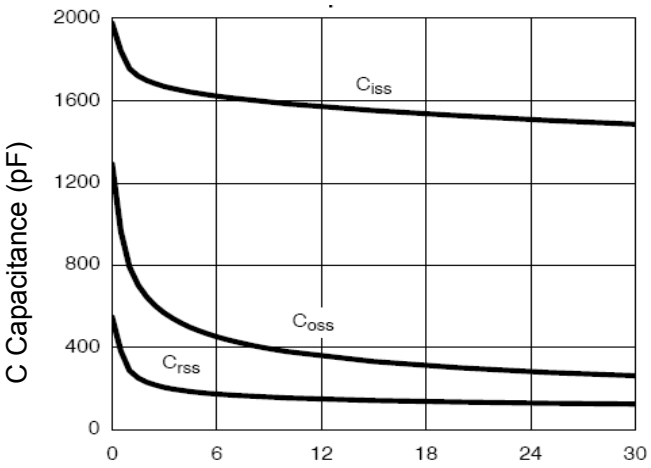


Figure 7 Capacitance vs Vds

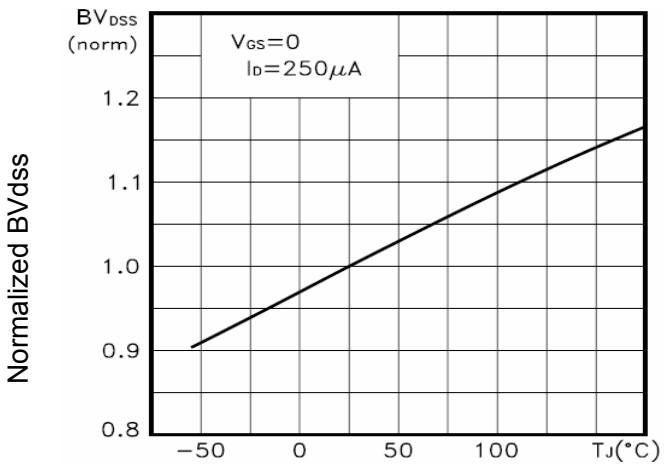


Figure 9 BV_{DSS} vs Junction Temperature

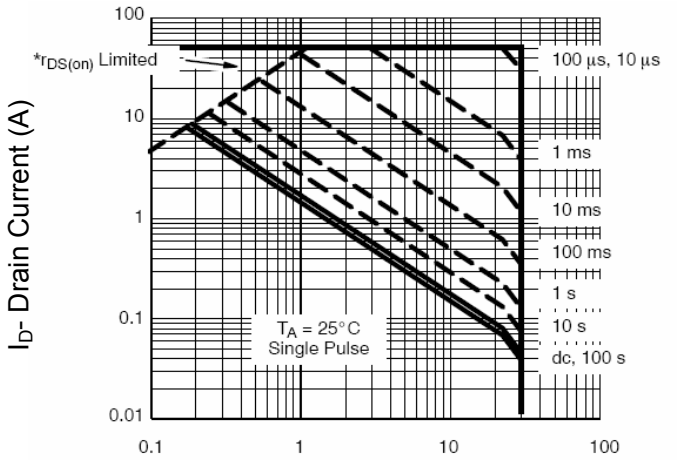


Figure 8 Safe Operation Area

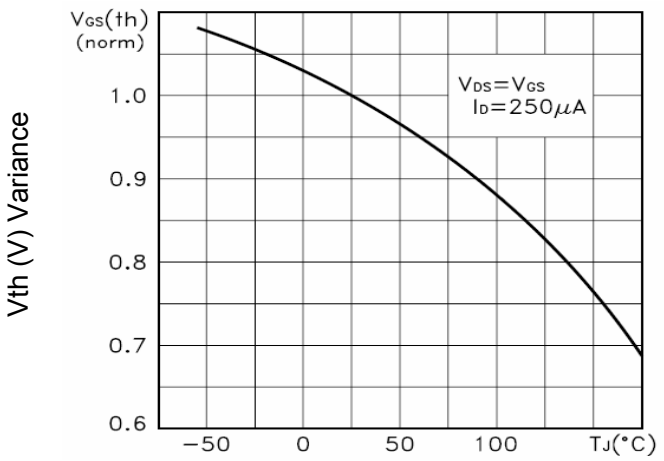


Figure 10 $V_{GS(th)}$ vs Junction Temperatur

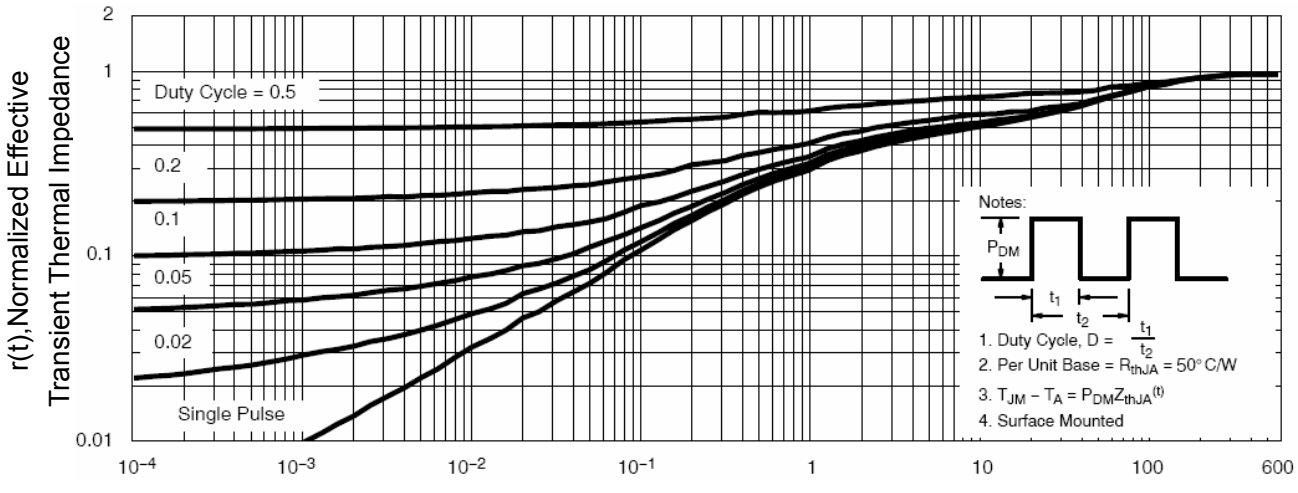


Figure 11 Normalized Maximum Transient Thermal Impedance