General Description

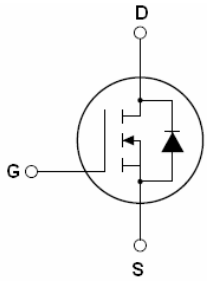
The 18N10 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for power switching application.

Features

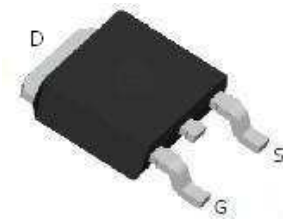
V_{DSS}	$R_{DS(ON)}$ @10V (typ)	I_D
100V	35mΩ	18A

Application

- Power switching application
- LED backlighting



Schematic Diagram



To-252

Table 1. Absolute Maximum Ratings (TA=25℃)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage (V_{GS}=0V)	100	V
V_{GS}	Gate-Source Voltage (V_{DS}=0V)	±20	V
$I_{D\ (DC)}$	Drain Current (DC) at Tc=25℃	18	A
$I_{D\ (DC)}$	Drain Current (DC) at Tc=100℃	12.6	A
$I_{DM\ (pluse)}$	Drain Current-Continuous@ Current-Pulsed **(Note 1)**	72	A
P_D	Maximum Power Dissipation(Tc=25℃)	47	W
E_{AS}	Single Pulse Avalanche Energy **(Note 2)**	20	mJ
T_J,T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	℃

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2.E_{AS} condition:T_J=25℃,V_{DD}=50V,V_G=10V, R_G=25Ω

Table 2. Thermal Characteristic

Symbol	Parameter	Value	Max	Unit
$R_{\theta JC}$	Thermal Resistance,Junction-to-Case	---	3.2	℃/W

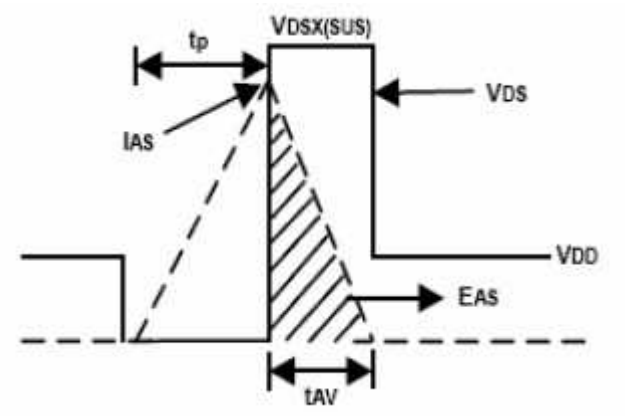
Table 3. Electrical Characteristics (TA=25℃unless otherwise noted)

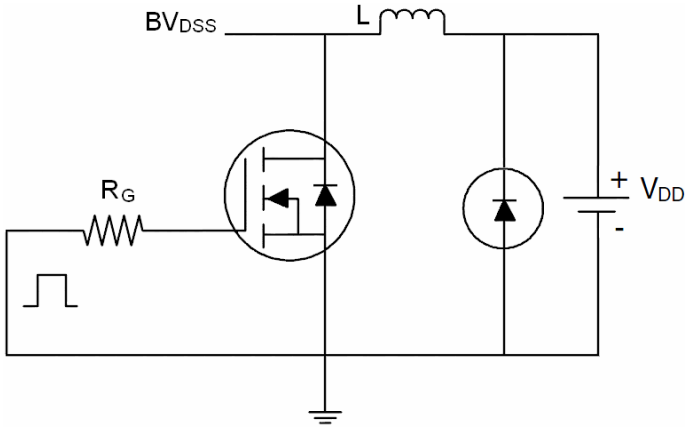
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=250μA	100			V
I_{DSS}	Zero Gate Voltage Drain Current(Tc=25℃)	V_{DS}=100V,V_{GS}=0V			1	μA
I_{DSS}	Zero Gate Voltage Drain Current(Tc=100℃)	V_{DS}=100V,V_{GS}=0V			5	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.0	2.0	3.0	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V, I_D=4.5A		35	46	mΩ
Dynamic Characteristics						
g_{FS}	Forward Transconductance	V_{DS}=5V,I_D=4.5A	5			S
C_{iss}	Input Capacitance	V_{DS}=50V,V_{GS}=0V f=1.0MHz		1380		PF
C_{oss}	Output Capacitance			88		PF
C_{rss}	Reverse Transfer Capacitance			60		PF
Q_g	Total Gate Charge	V_{DS}=50V,I_D=4.5A V_{GS}=10V		26.8		nC
Q_{gs}	Gate-Source Charge			6.4		nC
Q_{gd}	Gate-Drain Charge			12.4		nC
Switching Times						
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=50V,R_L=8.6Ω V_{GS}=10V,R_G=3Ω		7		nS
t_r	Turn-on Rise Time			12		nS
$t_{d(off)}$	Turn-Off Delay Time			24		nS
t_f	Turn-Off Fall Time			11		nS
Source-Drain Diode Characteristics						
I_{SD}	Source-Drain Current(Body Diode)			18		A
I_{SDM}	Pulsed Source-Drain Current(Body Diode)			72		A
V_{SD}	Forward On Voltage**(Note 1)**	T_J=25℃,I_{SD}=1A,V_{GS}=0V		0.75	1	V
t_{rr}	Reverse Recovery Time**(Note 1)**	T_J=25℃,I_F=4.5A di/dt=500A/μs		22		nS
Q_{rr}	Reverse Recovery Charge**(Note 1)**			28		nC
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible(turn-on is dominated by L_S+L_D)				

Notes 1.Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 1.5%, Starting T_J=25℃

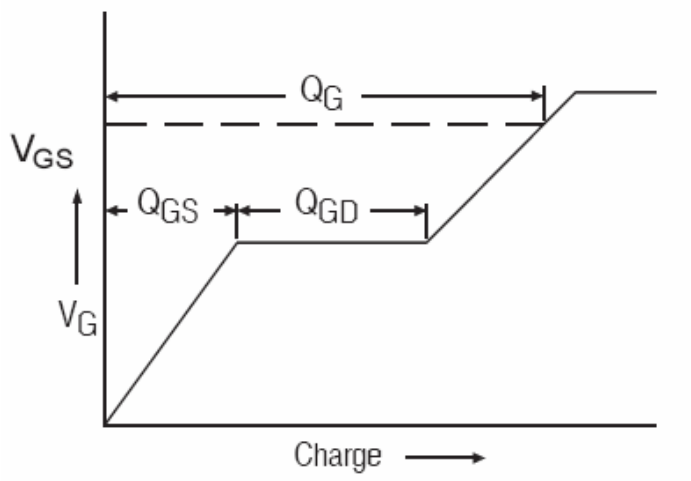
Test Circuit

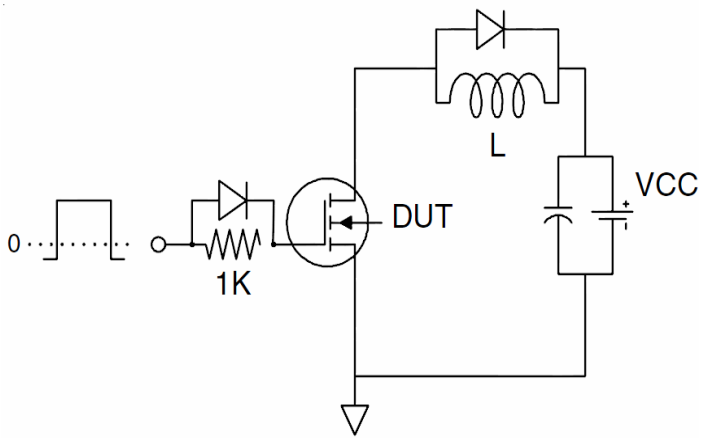
1) E_{AS} Test Circuits



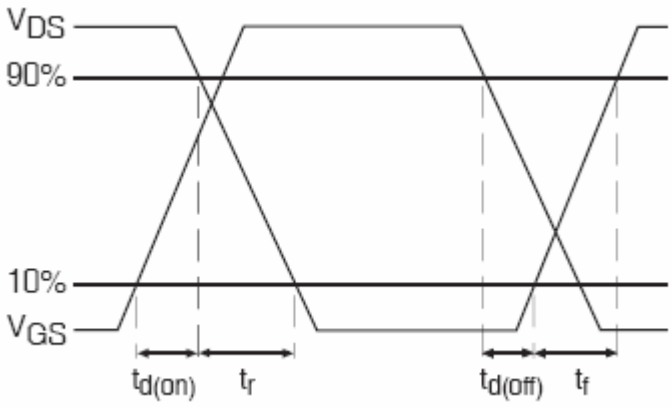


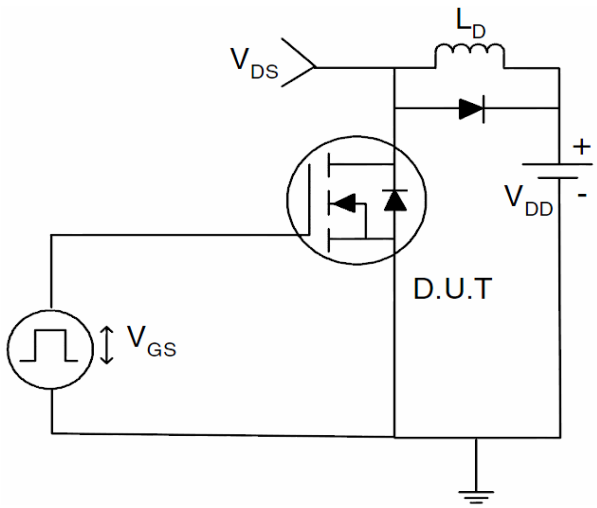
2) Gate Charge Test Circuit:





3) Switch Time Test Circuit:





TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

Figure1. On-Region Characteristics

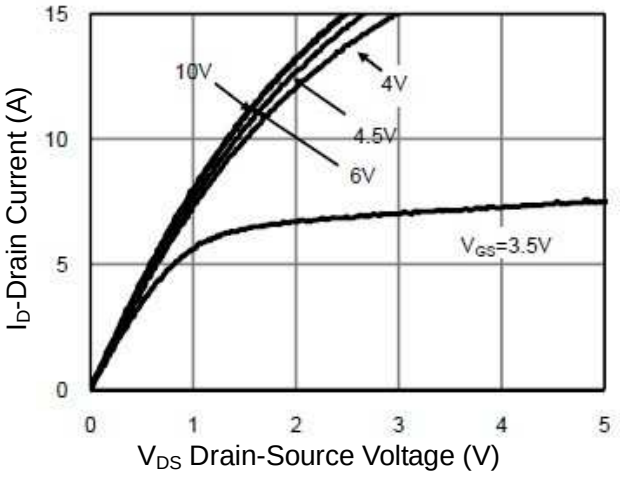


Figure 2: Transfer Characteristics

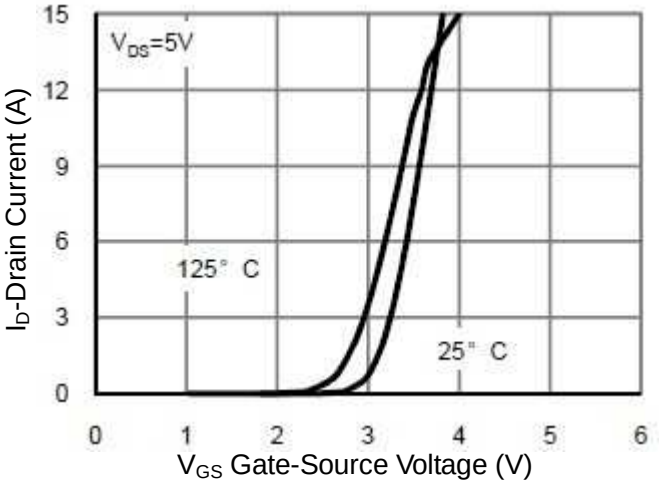


Figure3. ID vs Junction Temperature

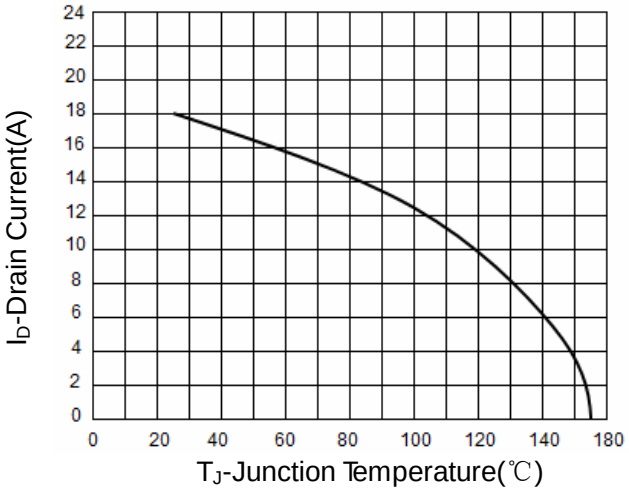


Figure4. On-Resistance vs. Junction Temperature

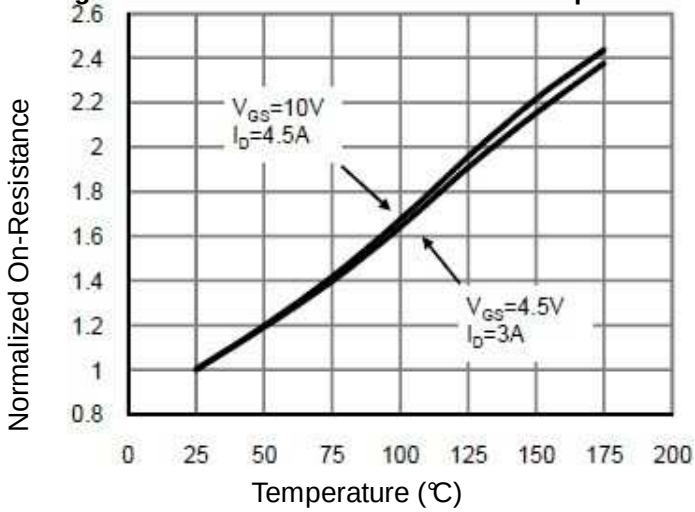


Figure5. On-Resistance vs. Gate-Source Voltage

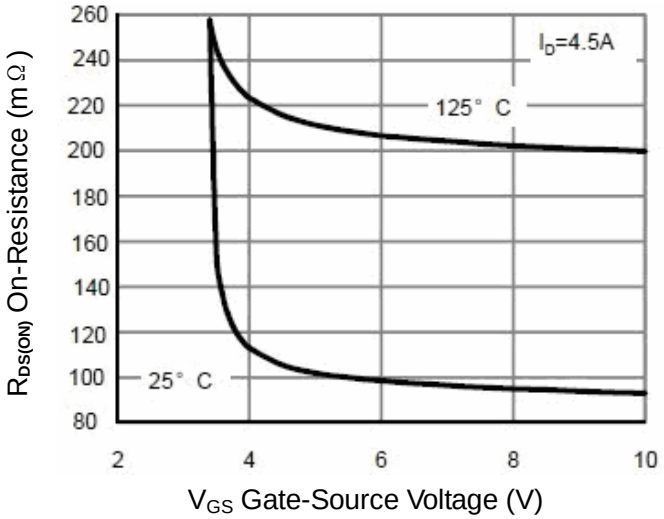


Figure6. Body-Diode Characteristics

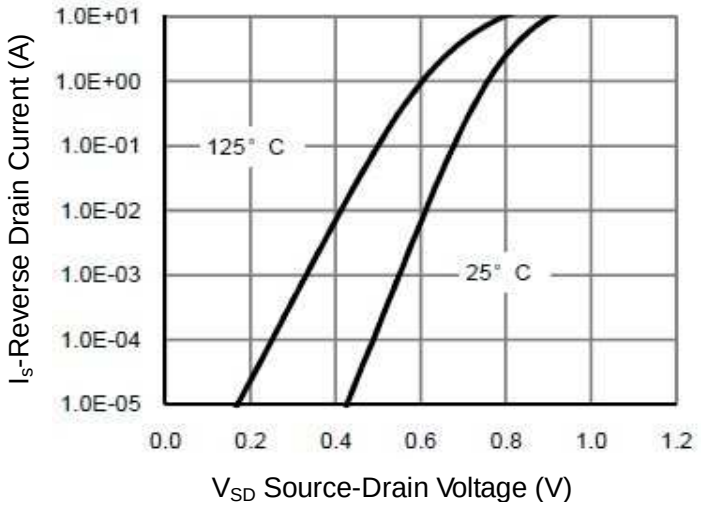


Figure7. Gate-Charge Characteristics

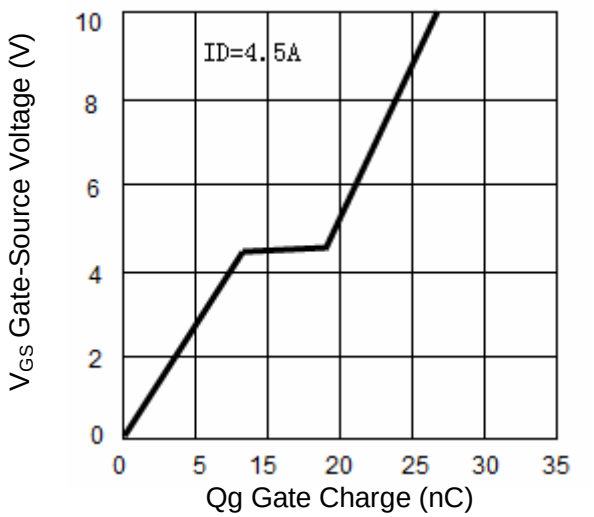


Figure 8. Capacitance Characteristics

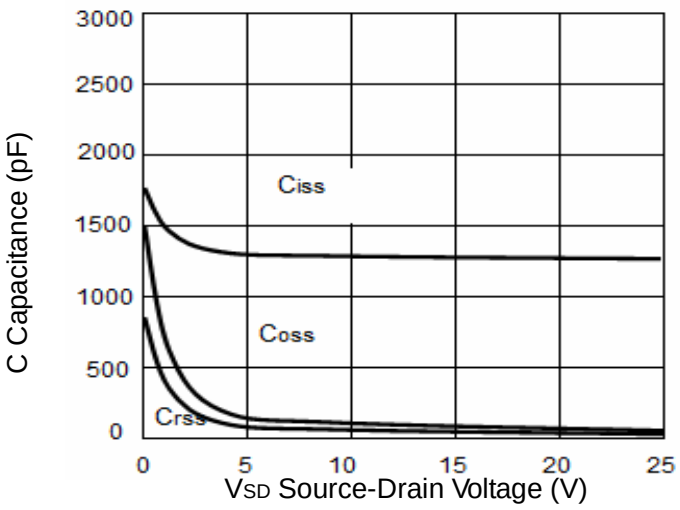


Figure 9. Maximum Forward Biased Safe Operating Area

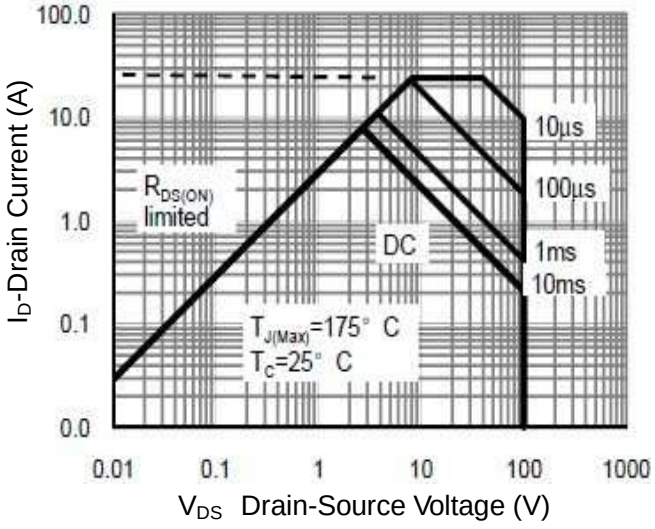


Figure10. Single Pulse Power Rating Junction-to-Case

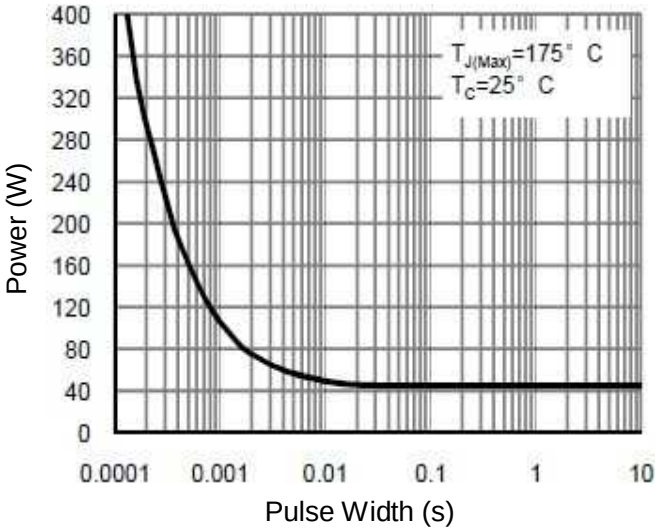


Figure11. Normalized Maximum Transient Thermal Impedance