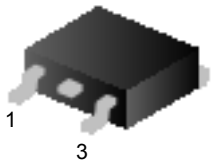
FIR7N65LG

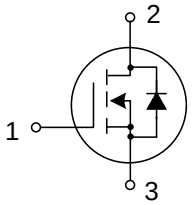
Advanced N-Ch Power MOSFET

General Description

FIR7N65LG , the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-252 , which accords with the RoHS standard.

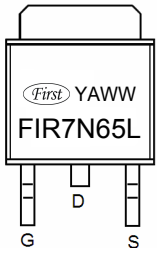
PIN Connection TO-252(D-PAK)





Features

- **Fast Switching**
- **Low ON Resistance(Rdson≤1.4)**
- **Low Gate Charge (Typical Data:24nC)**
- **Low Reverse transfer capacitances(Typical:5.5pF)**
- **100% Single Pulse avalanche energy Test**



Marking Diagram

Y = Year
A = Assembly Location
WW = Work Week
FIR7N65L = Specific Device Code

Absolute Maximum Ratings (Ta = 25°C unless otherwise noted; reference only)

Characteristics		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	±30	V
Drain Current	T_C=25°C	I_D	7.0	A
	T_C=100°C		4.4	
Drain Current Pulsed		I_{DM}	28	A
Power Dissipation(T_C=25°C)		P_D	100	W
-Derate above 25°C			0.8	W/°C
Single Pulsed Avalanche Energy(Note 1)		E_{AS}	350	mJ
Operation Junction Temperature Range		T_J	-55～+150	°C
Storage Temperature Range		T_{stg}	-55～+150	°C

Thermal Characteristics

Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.25	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	100	°C/W

Electrical Characteristics (Ta = 25°C unless otherwise noted; reference only)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B_{VDSS}	25 °C, V_{GS}=0V, I_D=250μA	650	--	--	V
		125°C, V_{GS}=0V, I_D=250μA	650	--	--	V
Drain-Source Leakage Current	I_{DSS}	25 °C, V_{DS}=650V, V_{GS}=0V	--	--	1	uA
		125°C, V_{DS}=520V, V_{GS}=0V	--	--	100	uA
		150°C, V_{DS}=520V, V_{GS}=0V	--	--	100	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=2A	--	1.2	1.4	Ω
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1.0MHZ		1130		pF
Output Capacitance	C_{oss}		--	93	--	
Reverse Transfer Capacitance	C_{rss}		--	5.5	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=325V,I_D=4.0A, R_G=10Ω (Note 2,3)	--	19	--	ns
Turn-on Rise Time	t_r		--	21	--	
Turn-off Delay Time	$t_{d(off)}$		--	42	--	
Turn-off Fall Time	t_f		--	19	--	
Total Gate Charge	Q_g	V_{DS}=520V,I_D=4.0A, V_{GS}=10V (Note 2,3)	--	24	--	nC
Gate-Source Charge	Q_{gs}		--	5.1	--	
Gate-Drain Charge	Q_{gd}		--	9.5	--	

Source-Drain Diode Ratings And Characteristics

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	7.0	A
Pulsed Source Current	I_{SM}		--	--	28	
Diode Forward Voltage	V_{SD}	I_S=4.0A,V_{GS}=0V	--	--	1.5	V
Reverse Recovery Time	T_{rr}	I_S=4.0A,V_{GS}=0V, dI_F/dt=100A/μs	--	382	--	ns
Reverse Recovery Charge	Q_{rr}		--	1980	--	nC

Notes:

1. L=10mH,I_{AS}= 8.4A,V_{DD}=100V, R_G=10Ω, starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

Characteristics Curve:

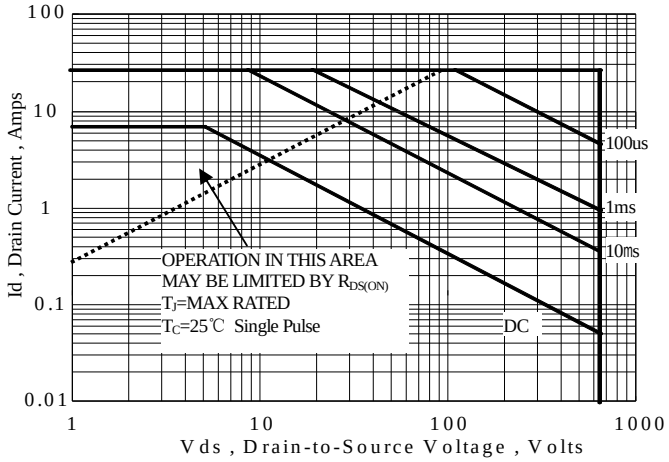


Figure 1 Maximum Forward Bias Safe Operating Area

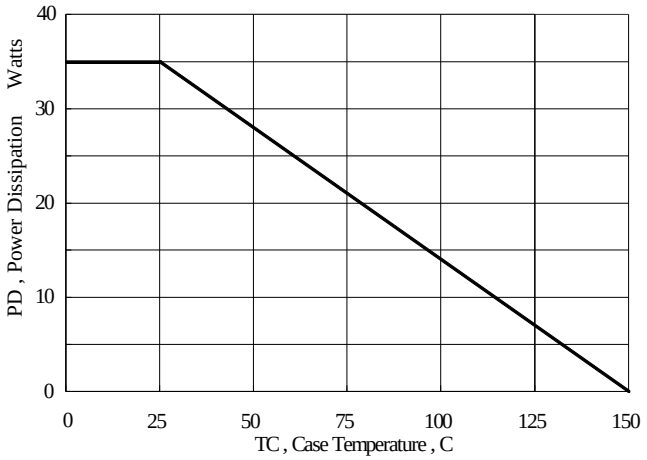


Figure 2 Maximum Power Dissipation vs Case Temperature

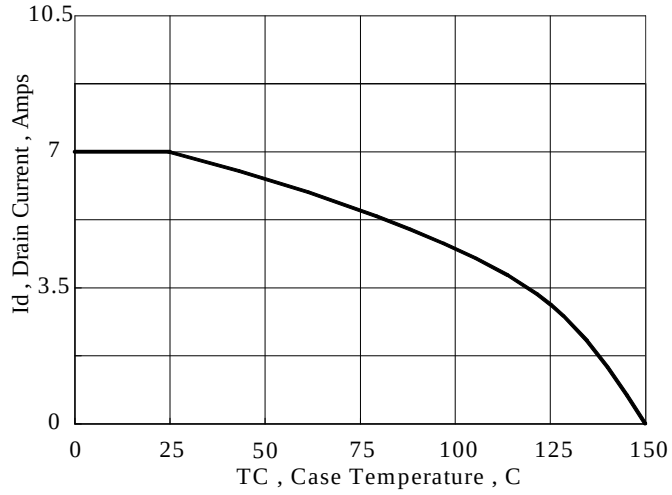


Figure 3 Maximum Continuous Drain Current vs Case Temperature

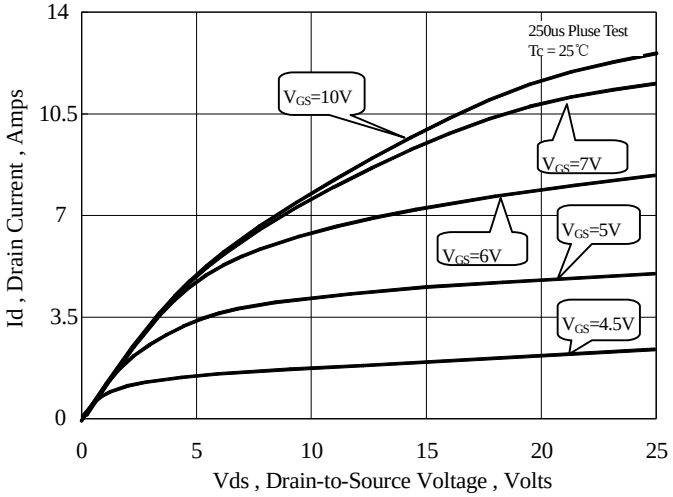
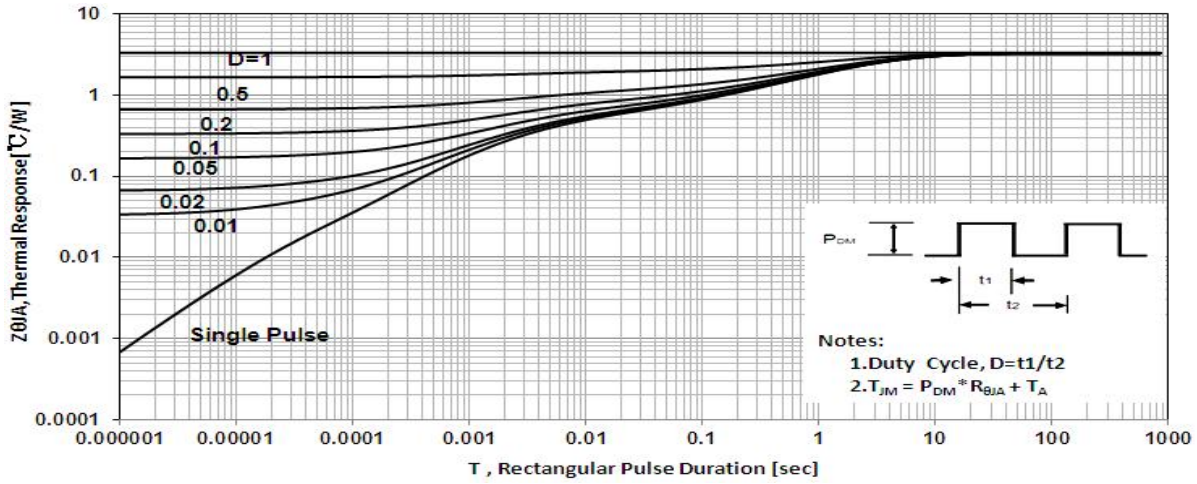


Figure 4 Typical Output Characteristics



Fi e 5 Maximum Effective Thermal Im endance unction to Case

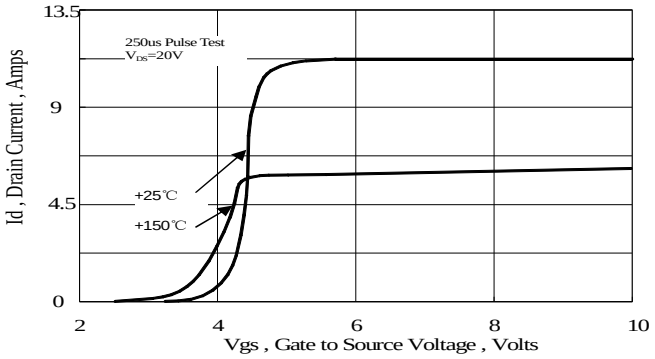


Figure 6 Typical Transfer Characteristics

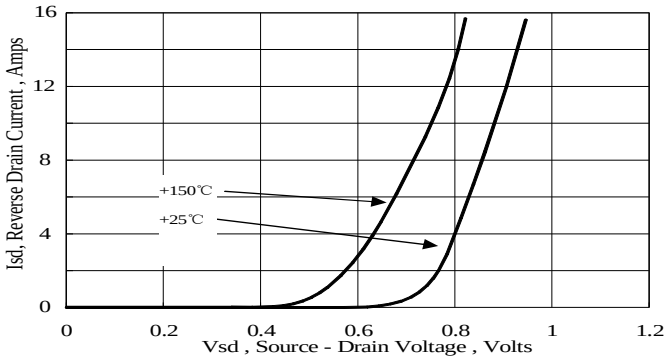


Figure 7 Typical Body Diode Transfer Characteristics

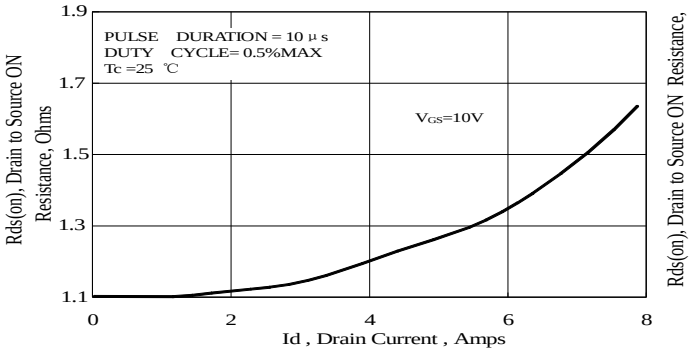


Figure 8 Typical Drain to Source ON Resistance vs Drain Current

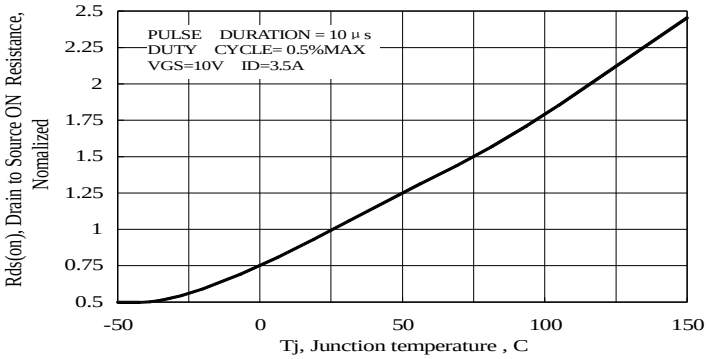


Figure 9 Typical Drian to Source on Resistance vs Junction Temperature

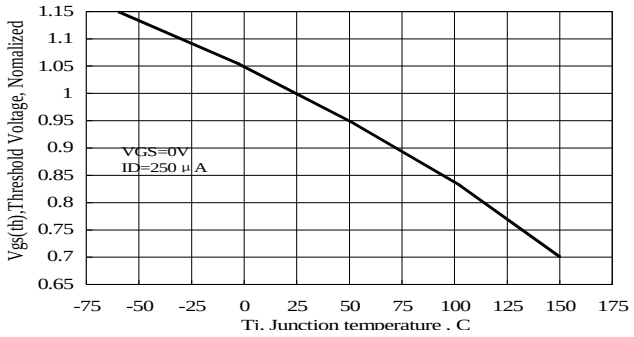


Figure 10 Typical Theshold Voltage vs Junction Temperature

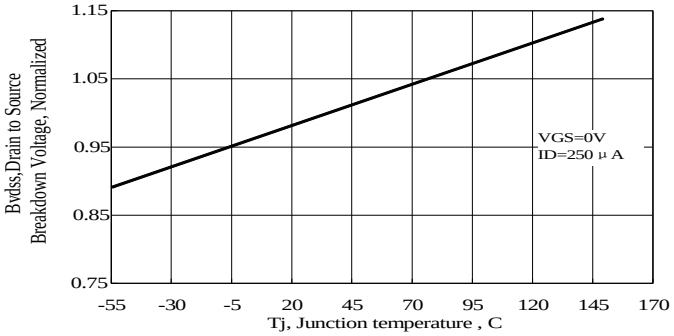


Figure 11 Typical Breakdown Voltage vs Junction Temperature

Figure 12 Typical Capacitance vs Drain to Source Voltage

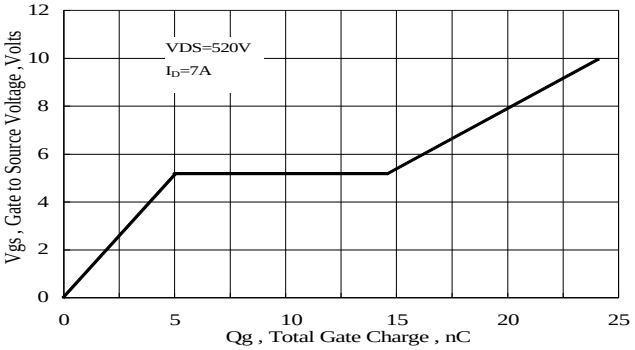


Figure 13 Typical Gate Charge vs Gate to Source Voltage

Test Circuit and Waveform

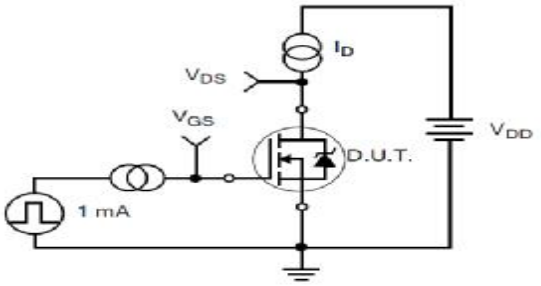


Figure 17. Gate Charge Test Circuit

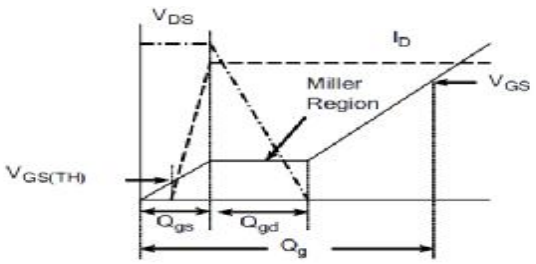


Figure 18. Gate Charge Waveform

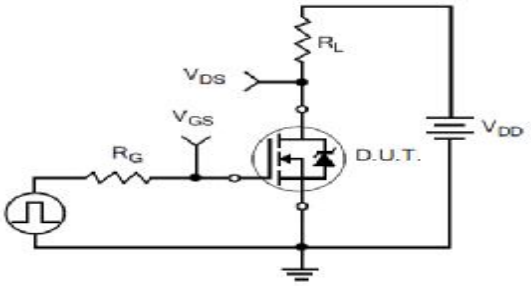


Figure 19. Resistive Switching Test Circuit

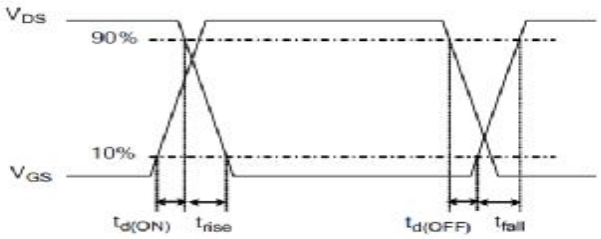


Figure 20. Resistive Switching Waveforms

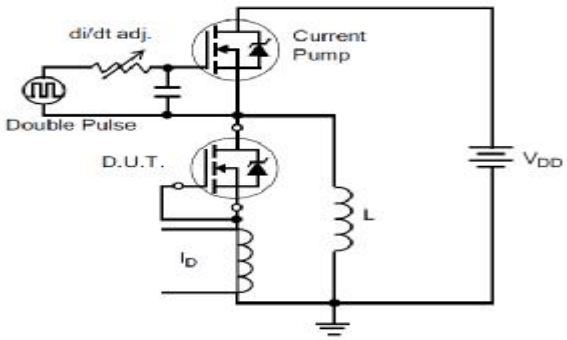


Figure 21. Diode Reverse Recovery Test Circuit

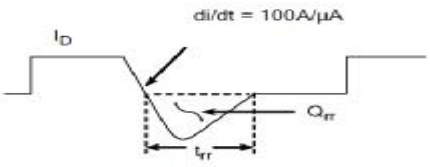


Figure 22. Diode Reverse Recovery Waveform

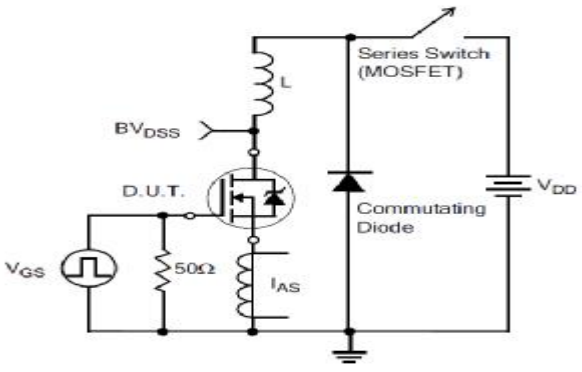
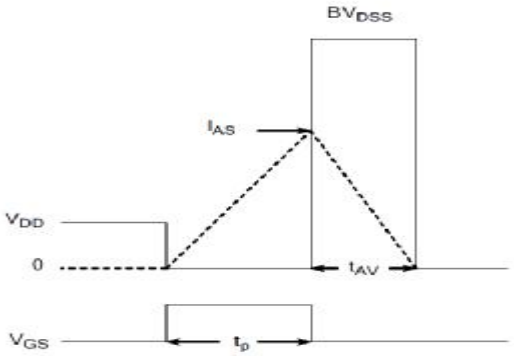


Figure 23. Unclamped Inductive Switching Test Circuit

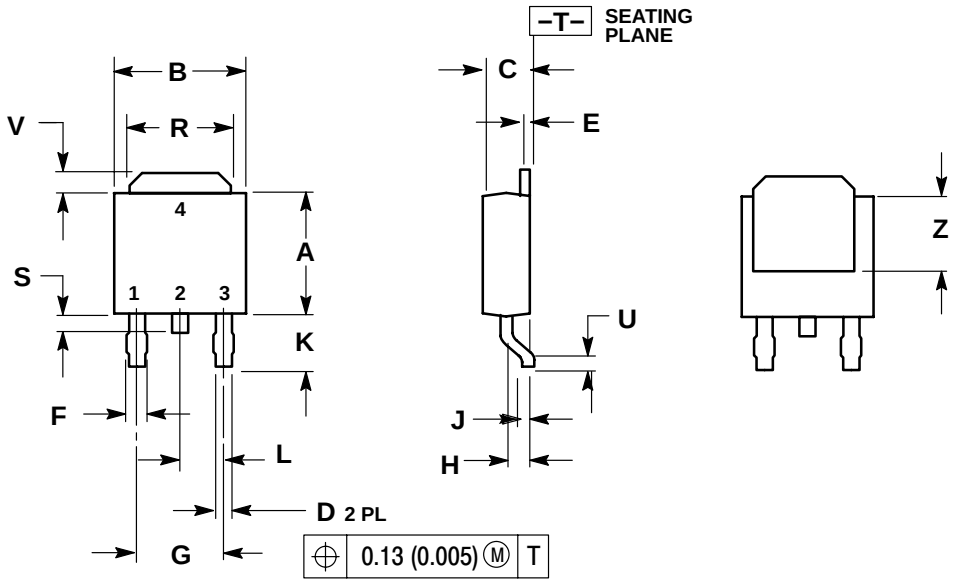


$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

Figure 24. Unclamped Inductive Switching Waveforms

Package Dimensions

TO-252



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---