

Description

Features

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V _{DSS}	R _{DS(ON)} @ 10V (typ)	I _D
650V	1.95Ω	4.5 A

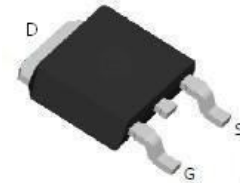
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

Application

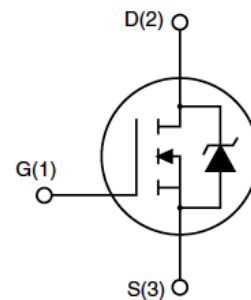
- DC Motor Control and Class D Amplifier
- Uninterruptible Power Supply (UPS)
- Automotive



To-251



To-252



Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter		Max.	Units
			TO-251/TO-252	
V _{DSS}	Drain-Source Voltage		650	V
V _{GSS}	Gate-Source Voltage		± 30	V
I _D	Continuous Drain Current	T _C = 25°C	4.5	A
		T _C = 100°C	2.7	A
I _{DM}	Pulsed Drain Current ^{note1}		18	A
E _{AS}	Single Pulsed Avalanche Energy ^{note2}		101	mJ
dv/dt	Peak Diode Recovery Energy ^{note3}		4.5	V/ns
P _D	Power Dissipation	T _C = 25°C	100	W
	Linear Derating Factor	T _C > 25°C	0.48	W/°C
R _{θJC}	Thermal Resistance, Junction to Case		1.25	°C/W
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C

*Drain current limited by maximum junction temperature

Electrical Characteristics $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	650	-	-	V
$\Delta V_{(BR)DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	Reference to 25°C , $I_D = 250\mu A$	-	0.5	-	$V/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 650V, V_{GS} = 0V$	-	-	1	μA
		$V_{DS} = 520V, T_C = 125^\circ\text{C}$	-	-	10	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 30V$	-	-	± 100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage ^{note4}	$V_{DS} = V_{GS}, I_D = 250\mu A$	2	-	4	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10V, I_D = 2.25A$	-	1.95	2.3	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 30V, I_D = 2.25A$	-	2.0	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0\text{MHz}$	-	605.6	-	pF
C_{oss}	Output Capacitance		-	65.2	-	pF
C_{riss}	Reverse Transfer Capacitance		-	6.57	-	pF
Q_g	Total Gate Charge	$V_{DD} = 520V, I_D = 4.5A,$ $V_{GS} = 10V$	-	17.8	-	nC
Q_{gs}	Gate-Source Charge		-	2.87	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	7.78	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 325V, I_D = 4.5A,$ $R_G = 10\Omega, V_{GS} = 10V$	-	12.3	-	ns
t_r	Turn-On Rise Time		-	15.33	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	36.7	-	ns
t_f	Turn-Off Fall Time		-	11.33	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	4.5	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	18	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0V, I_S = 4.5A$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0V, I_F = 4.5A,$ $di/dt = 100A/\mu s$	-	363	-	ns
Q_{rr}	Reverse Recovery Charge		-	1.071	-	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $L = 10\text{mH}, I_{AS} = 4.5A, V_{DD} = 50V, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 4.5A, di/dt \leq 200A/\mu s, V_{DD} \leq V_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

Typical Performance Characteristics

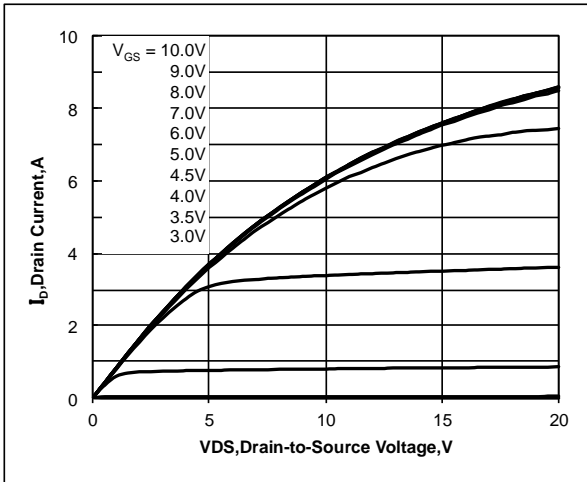


Figure 1. Output Characteristics

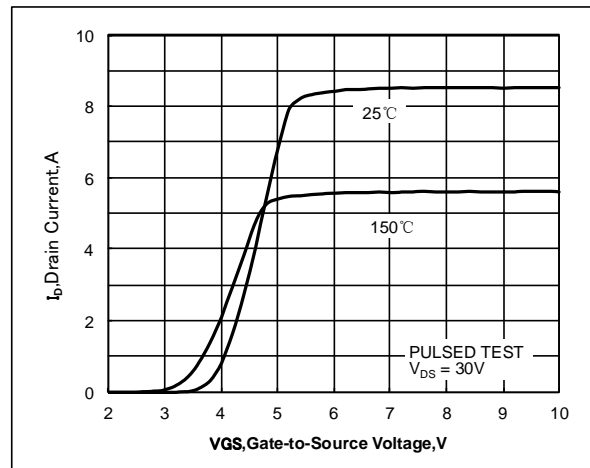


Figure 2. Transfer Characteristics

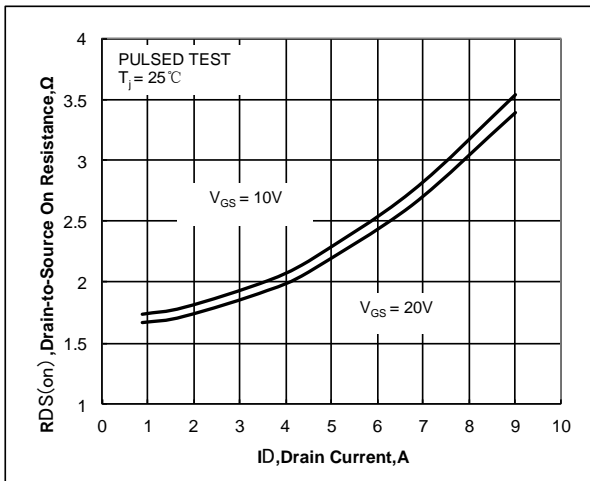


Figure 3. Drain-to-Source On Resistance vs. Drain Current and Gate Voltage

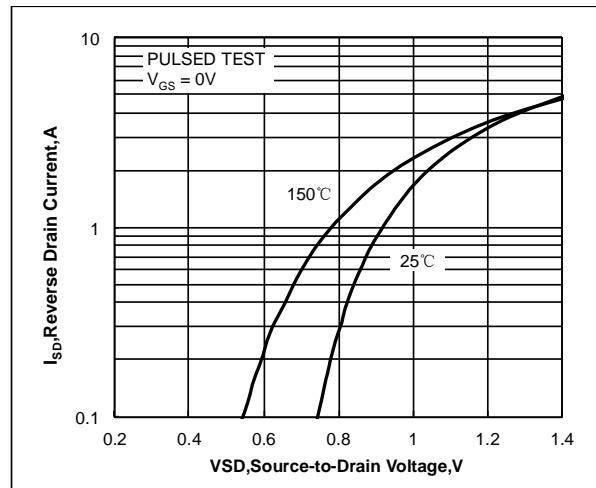
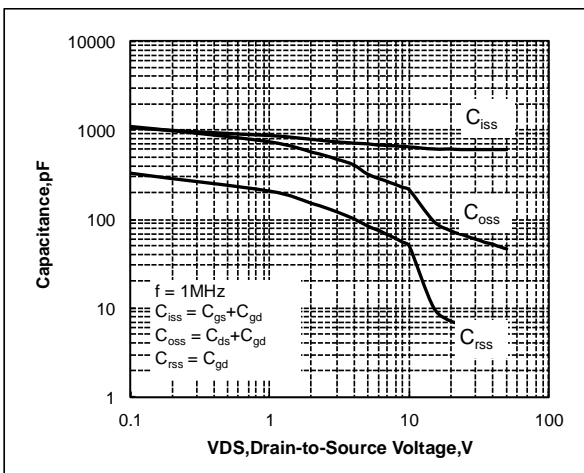


Figure 4. Body Diode Forward Voltage vs. Source Current and Temperature



Typical Performance Characteristics

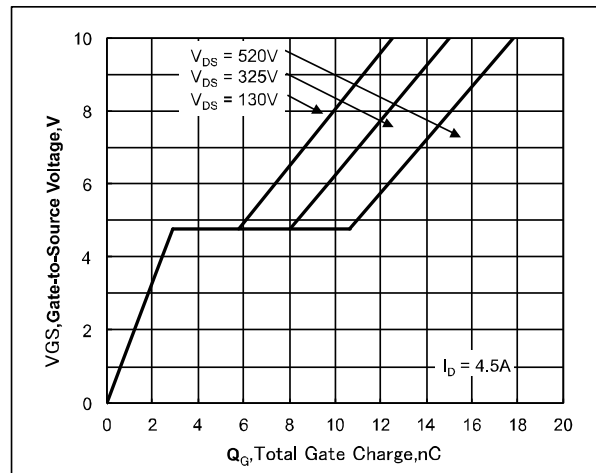


Figure 6. Gate Charge Characteristics

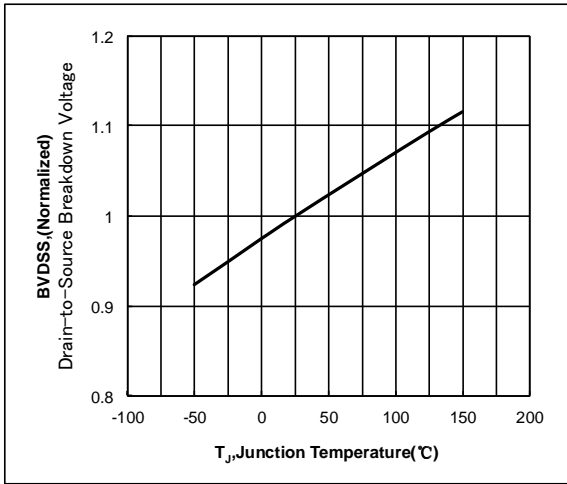


Figure 7. Normalized Breakdown Voltage vs. Junction Temperature

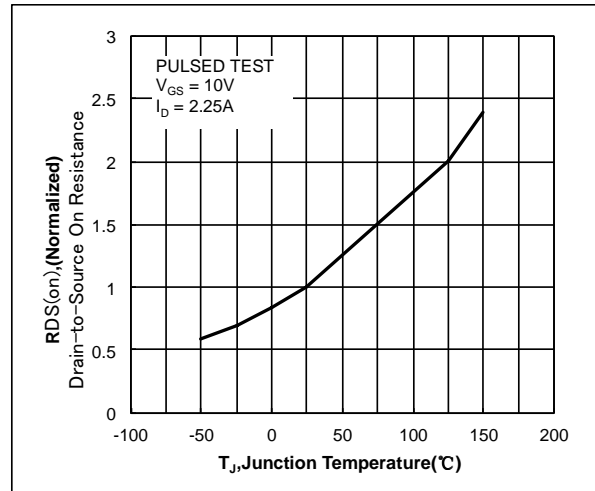


Figure 8. Normalized On Resistance vs. Junction Temperature

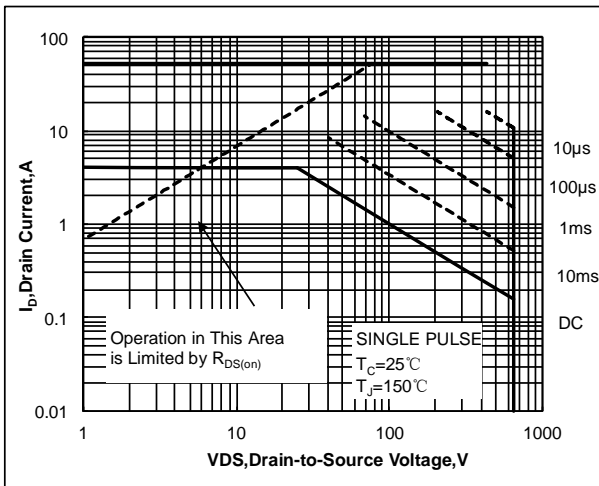


Figure 9. Maximum Safe Operating Area

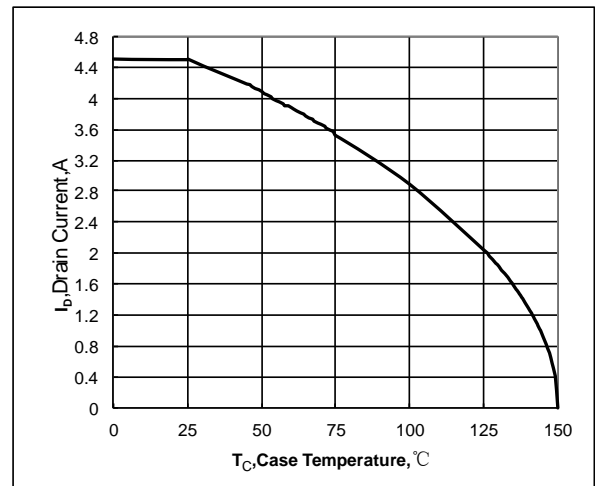


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

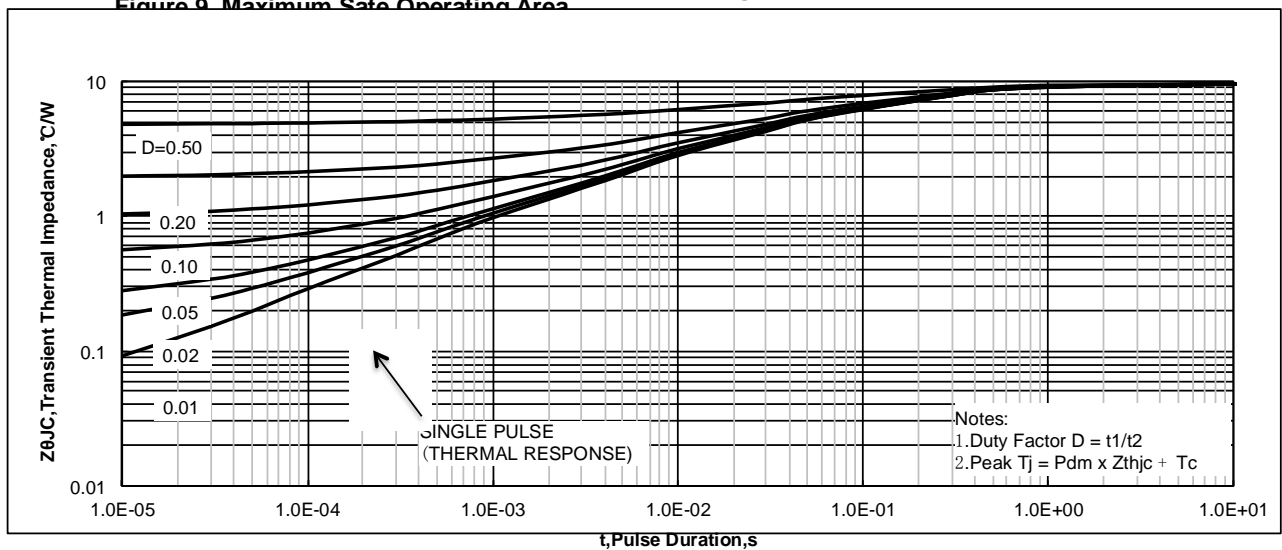


Figure 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

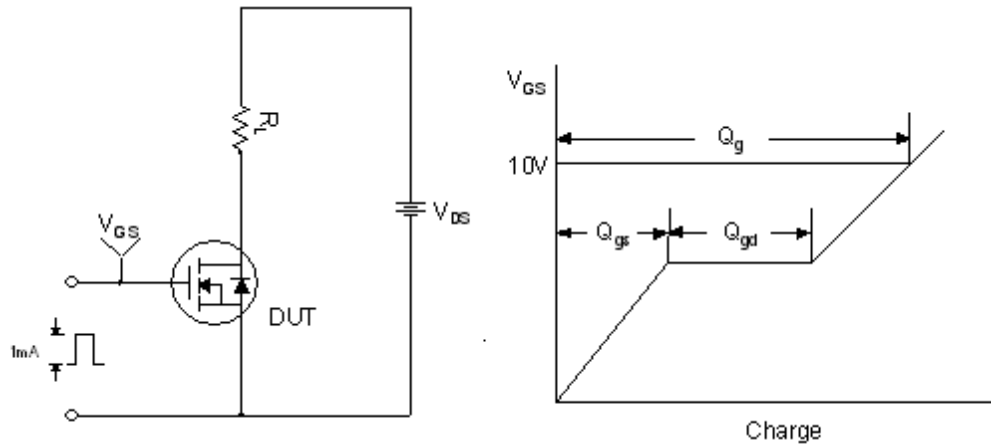


Figure 12. Gate Charge Test Circuit & Waveform

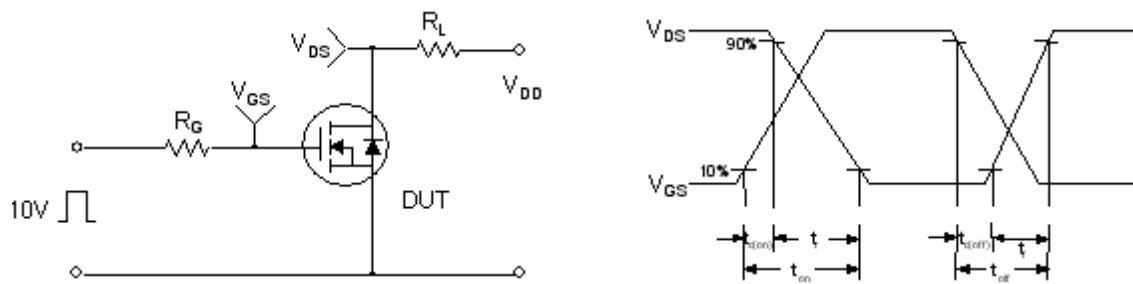


Figure 13. Resistive Switching Test Circuit & Waveforms

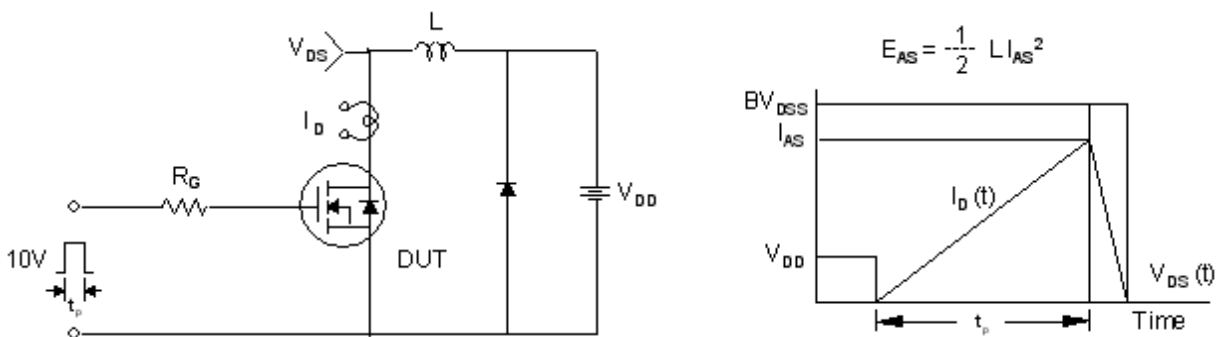


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

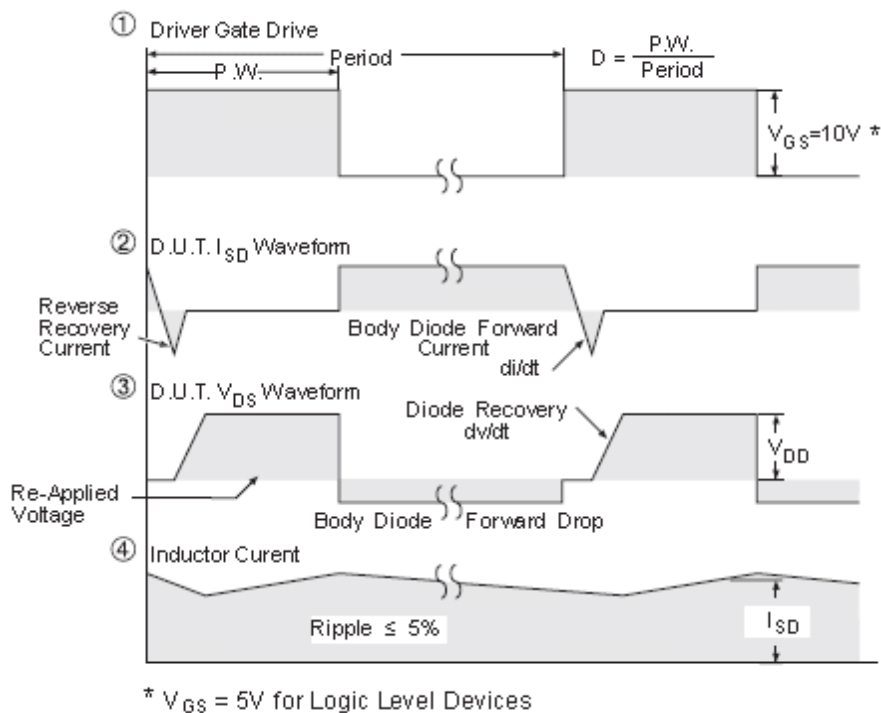
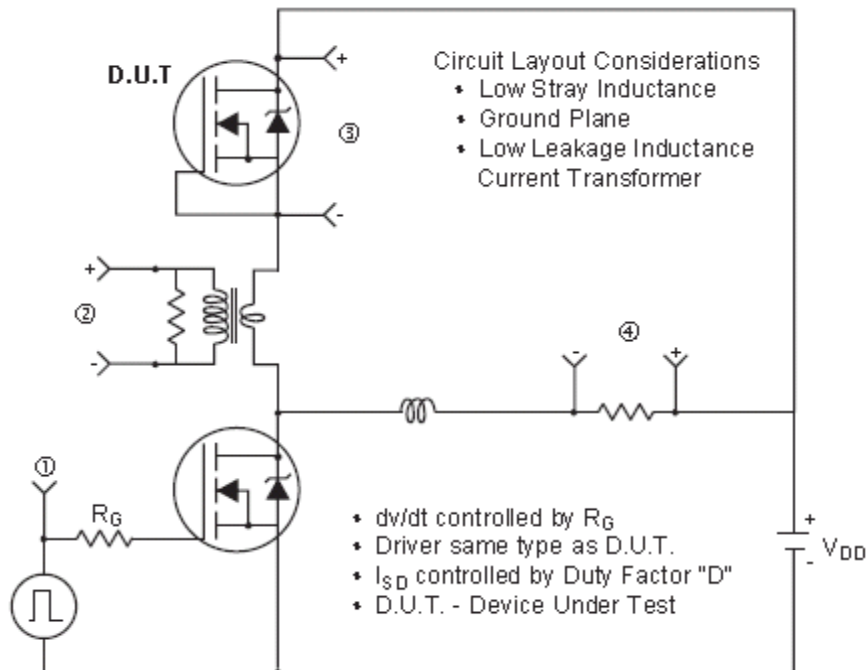


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)