

LM1086 1.5A Low Dropout Positive Regulators

FEATURES

- Available in 1.8V, 2.5V, 2.85V, 3.3V, 3.45V, 5V and Adjustable Versions
- Current Limiting and Thermal Protection
- Output Current 1.5A
- Line Regulation 0.015% (typical)
- Load Regulation 0.1% (typical)

APPLICATIONS

- SCSI-2 Active Terminator
- High Efficiency Linear Regulators
- Battery Charger
- Post Regulation for Switching Supplies
- Constant Current Regulator
- Microprocessor Supply

DESCRIPTION

The LM1086 is a series of low dropout positive voltage regulators with a maximum dropout of 1.5V at 1.5A of load current. It has the same pin-out as TI's industry standard LM317.

The LM1086 is available in an adjustable version, which can set the output voltage with only two external resistors. It is also available in six fixed voltages: 1.8V, 2.5V, 2.85V, 3.3V, 3.45V and 5.0V. The fixed versions integrate the adjust resistors.

The LM1086 circuit includes a zener trimmed bandgap reference, current limiting and thermal shutdown.

Connection Diagram

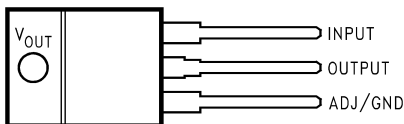


Figure 1. TO-220 Top View

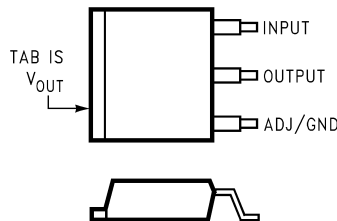
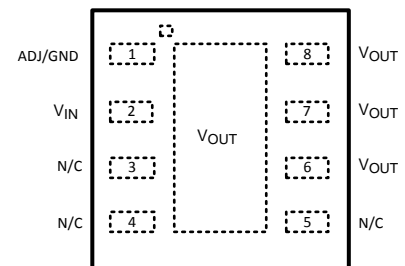


Figure 2. DPAK/TO-263 Top View



Pins 6, 7, and 8 must be tied together.

Figure 3. WSON Top View

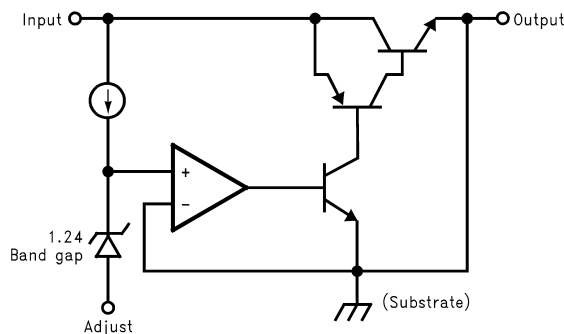
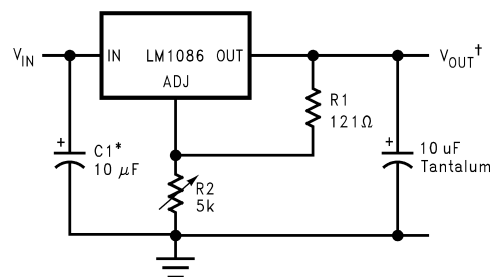


Figure 4. Basic Functional Diagram, Adjustable Version

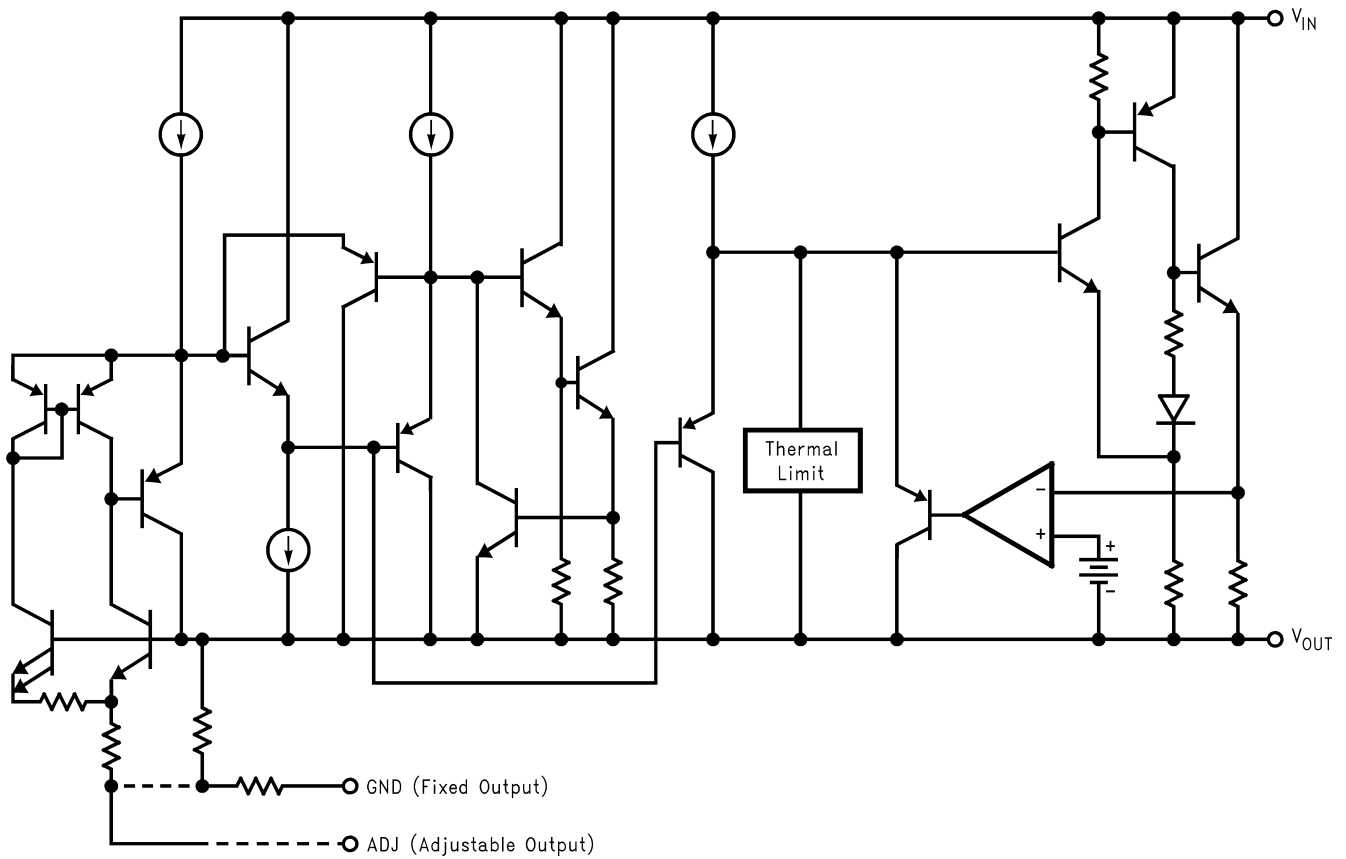


*NEEDED IF DEVICE IS FAR FROM FILTER CAPACITORS

$$V_{OUT}^{\dagger} = 1.25V \left(1 + \frac{R2}{R1}\right)$$

Figure 5. Application Circuit 1.2V to 15V Adjustable Regulator

Simplified Schematic





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

Maximum Input-to-Output Voltage Differential	
LM1086-ADJ	29V
LM1086-1.8	27V
LM1086-2.5	27V
LM1086-2.85	27V
LM1086-3.3	27V
LM1086-3.45	27V
LM1086-5.0	25V
Power Dissipation ⁽³⁾	Internally Limited
Junction Temperature (T_J) ⁽⁴⁾	150°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature	260°C, to 10 sec
ESD Tolerance ⁽⁵⁾	2000V

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) Power dissipation is kept in a safe range by current limiting circuitry. Refer to [OVERLOAD RECOVERY](#) in [Application Note](#). The value θ_{JA} for the WSON package is specifically dependent on PCB trace area, trace material, and the number of thermal vias. For improved thermal resistance and power dissipation for the WSON package, refer to Application Note AN-1187 (literature number [SNOA401](#)).
- (4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly into a PC board. Refer to Thermal Considerations in the Application Notes.
- (5) For testing purposes, ESD was applied using human body model, 1.5k Ω in series with 100pF.

Operating Ratings⁽¹⁾

Junction Temperature Range (T_J) ⁽²⁾		
"C" Grade	Control Section	0°C to 125°C
	Output Section	0°C to 150°C
"I" Grade	Control Section	-40°C to 125°C
	Output Section	-40°C to 150°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
- (2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly into a PC board. Refer to Thermal Considerations in the Application Notes.

Electrical Characteristics

Typicals and limits appearing in normal type apply for $T_j = 25^\circ\text{C}$. Limits appearing in **Boldface** type apply over the entire junction temperature range for operation.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{REF}	Reference Voltage	LM1086-ADJ $I_{OUT} = 10\text{mA}$, $V_{IN} - V_{OUT} = 3\text{V}$ $10\text{mA} \leq I_{OUT} \leq I_{FULL\ LOAD}$, $1.5\text{V} \leq V_{IN} - V_{OUT} \leq 15\text{V}$ (3)	1.238 1.225	1.250 1.250	1.262 1.270	V V
V_{OUT}	Output Voltage (3)	LM1086-1.8 $I_{OUT} = 0\text{mA}$, $V_{IN} = 5\text{V}$ $0 \leq I_{OUT} \leq I_{FULL\ LOAD}$, $3.3\text{V} \leq V_{IN} \leq 18\text{V}$	1.782 1.764	1.8 1.8	1.818 1.836	V
		LM1086-2.5 $I_{OUT} = 0\text{mA}$, $V_{IN} = 5\text{V}$ $0 \leq I_{OUT} \leq I_{FULL\ LOAD}$, $4.0\text{V} \leq V_{IN} \leq 18\text{V}$	2.475 2.450	2.50 2.50	2.525 2.55	V
		LM1086-2.85 $I_{OUT} = 0\text{mA}$, $V_{IN} = 5\text{V}$ $0 \leq I_{OUT} \leq I_{FULL\ LOAD}$, $4.35\text{V} \leq V_{IN} \leq 18\text{V}$	2.82 2.79	2.85 2.85	2.88 2.91	V V
		LM1086-3.3 $I_{OUT} = 0\text{mA}$, $V_{IN} = 5\text{V}$ $0 \leq I_{OUT} \leq I_{FULL\ LOAD}$, $4.75\text{V} \leq V_{IN} \leq 18\text{V}$	3.267 3.235	3.300 3.300	3.333 3.365	V V
		LM1086-3.45 $I_{OUT} = 0\text{mA}$, $V_{IN} = 5\text{V}$ $0 \leq I_{OUT} \leq I_{FULL\ LOAD}$, $4.95\text{V} \leq V_{IN} \leq 18\text{V}$	3.415 3.381	3.45 3.45	3.484 3.519	V V
		LM1086-5.0 $I_{OUT} = 0\text{mA}$, $V_{IN} = 8\text{V}$ $0 \leq I_{OUT} \leq I_{FULL\ LOAD}$, $6.5\text{V} \leq V_{IN} \leq 20\text{V}$	4.950 4.900	5.000 5.000	5.050 5.100	V V
ΔV_{OUT}	Line Regulation (4)	LM1086-ADJ $I_{OUT} = 10\text{mA}$, $1.5\text{V} \leq (V_{IN} - V_{OUT}) \leq 15\text{V}$		0.015 0.035	0.2 0.2	% %
		LM1086-1.8 $I_{OUT} = 0\text{mA}$, $3.3\text{V} \leq V_{IN} \leq 18\text{V}$		0.3 0.6	6 6	mV
		LM1086-2.5 $I_{OUT} = 0\text{mA}$, $4.0\text{V} \leq V_{IN} \leq 18\text{V}$		0.3 0.6	6 6	mV
		LM1086-2.85 $I_{OUT} = 0\text{mA}$, $4.35\text{V} \leq V_{IN} \leq 18\text{V}$		0.3 0.6	6 6	mV mV
		LM1086-3.3 $I_{OUT} = 0\text{mA}$, $4.5\text{V} \leq V_{IN} \leq 18\text{V}$		0.5 1.0	10 10	mV mV
		LM1086-3.45 $I_{OUT} = 0\text{mA}$, $4.95\text{V} \leq V_{IN} \leq 18\text{V}$		0.5 1.0	10 10	mV mV
		LM1086-5.0 $I_{OUT} = 0\text{mA}$, $6.5\text{V} \leq V_{IN} \leq 20\text{V}$		0.5 1.0	10 10	mV mV
ΔV_{OUT}	Load Regulation (4)	LM1086-ADJ $(V_{IN} - V_{OUT}) = 3\text{V}$, $10\text{mA} \leq I_{OUT} \leq I_{FULL\ LOAD}$		0.1 0.2	0.3 0.4	% %
		LM1086-1.8, 2.5, 2.85 $V_{IN} = 5\text{V}$, $0 \leq I_{OUT} \leq I_{FULL\ LOAD}$		3 6	12 20	mV mV
		LM1086-3.3, 3.45 $V_{IN} = 5\text{V}$, $0 \leq I_{OUT} \leq I_{FULL\ LOAD}$		3 7	15 25	mV mV
		LM1086-5.0 $V_{IN} = 8\text{V}$, $0 \leq I_{OUT} \leq I_{FULL\ LOAD}$		5 10	20 35	mV mV
	Dropout Voltage (5)	LM1086-ADJ, 1.8, 2.5, 2.85, 3.3, 3.45, 5 ΔV_{REF} , $\Delta V_{OUT} = 1\%$, $I_{OUT} = 1.5\text{A}$		1.3	1.5	V

(1) All limits are specified by testing or statistical analysis.

(2) Typical Values represent the most likely parametric norm.

(3) $I_{FULL\ LOAD}$ is defined in the current limit curves. The $I_{FULL\ LOAD}$ Curve defines current limit as a function of input-to-output voltage. Note that 15W power dissipation for the LM1086 is only achievable over a limited range of input-to-output voltage.

(4) Load and line regulation are measured at constant junction temperature, and are specified up to the maximum power dissipation of 15W. Power dissipation is determined by the input/output differential and the output current. Ensured maximum power dissipation will not be available over the full input/output range.

(5) Dropout voltage is specified over the full output current range of the device.

Electrical Characteristics (continued)

Typicals and limits appearing in normal type apply for $T_J = 25^\circ\text{C}$. Limits appearing in **Boldface** type apply over the entire junction temperature range for operation.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
I_{LIMIT}	Current Limit	LM1086-ADJ $V_{IN}-V_{OUT} = 5V$ $V_{IN}-V_{OUT} = 25V$	1.50 0.05	2.7 0.15		A A
		LM1086-1.8, 2.5, 2.85, 3.3, 3.45, $V_{IN} = 8V$	1.5	2.7		A
		LM1086-5.0, $V_{IN} = 10V$	1.5	2.7		A
	Minimum Load Current ⁽⁶⁾	LM1086-ADJ $V_{IN} - V_{OUT} = 25V$		5.0	10.0	mA
	Quiescent Current	LM1086-1.8, 2.5, 2.85, $V_{IN} \leq 18V$		5.0	10.0	mA
		LM1086-3.3, $V_{IN} \leq 18V$		5.0	10.0	mA
		LM1086-3.45, $V_{IN} \leq 18V$		5.0	10.0	mA
		LM1086-5.0, $V_{IN} \leq 20V$		5.0	10.0	mA
	Thermal Regulation	$T_A = 25^\circ\text{C}$, 30ms Pulse		0.008	0.04	%/W
	Ripple Rejection	$f_{RIPPLE} = 120\text{Hz}$, $C_{OUT} = 25\mu\text{F}$ Tantalum, $I_{OUT} = 1.5A$				
		LM1086-ADJ, $C_{ADJ} = 25\mu\text{F}$, $(V_{IN}-V_O) = 3V$	60	75		dB
		LM1086-1.8, 2.5, 2.85, $V_{IN} = 6V$	60	72		dB
		LM1086-3.3, $V_{IN} = 6.3V$	60	72		dB
		LM1086-3.45, $V_{IN} = 6.3V$	60	72		dB
		LM1086-5.0 $V_{IN} = 8V$	60	68		dB
	Adjust Pin Current	LM1086		55	120	μA
	Adjust Pin Current Change	$10\text{mA} \leq I_{OUT} \leq I_{FULL\ LOAD}$, $1.5V \leq (V_{IN}-V_{OUT}) \leq 15V$		0.2	5	μA
	Temperature Stability			0.5		%
	Long Term Stability	$T_A = 125^\circ\text{C}$, 1000Hrs		0.3	1.0	%
	RMS Noise (% of V_{OUT})	$10\text{Hz} \leq f \leq 10\text{kHz}$		0.003		%
θ_{JC}	Thermal Resistance Junction-to-Case	3-Lead DDPAK/TO-263: Control Section/Output Section			1.5/4.0	$^\circ\text{C/W}$
		3-Lead TO-220: Control Section/Output Section			1.5/4.0	$^\circ\text{C/W}$

(6) The minimum output current required to maintain regulation.

Typical Performance Characteristics

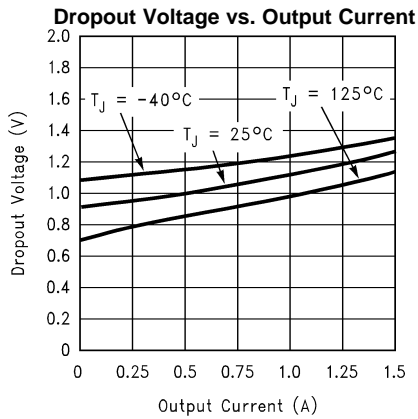


Figure 6.

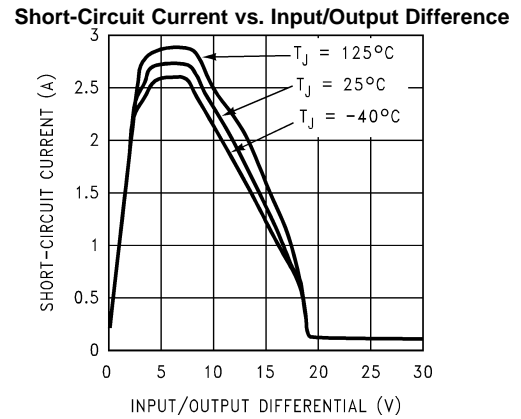


Figure 7.

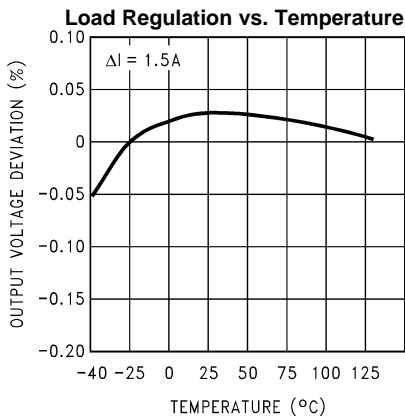


Figure 8.

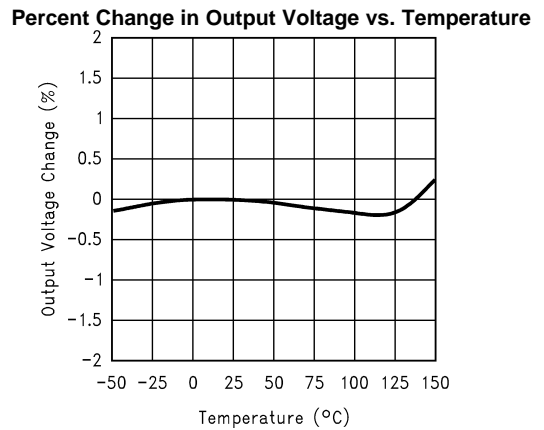


Figure 9.

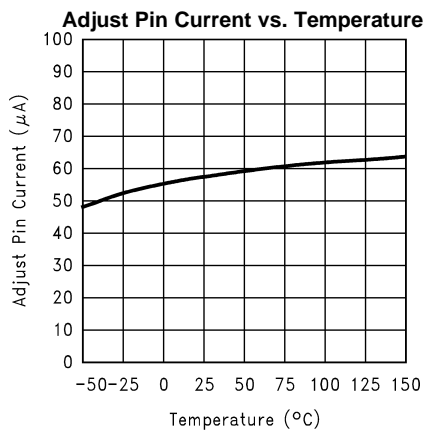


Figure 10.

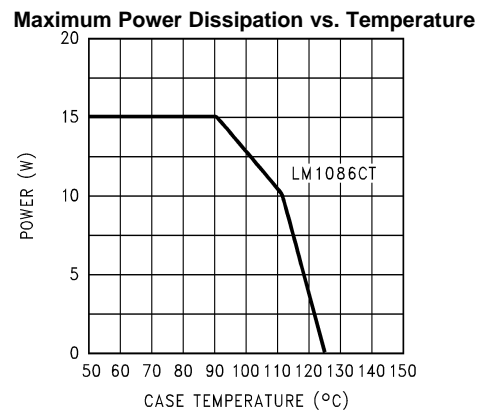


Figure 11.

Typical Performance Characteristics (continued)

Ripple Rejection vs. Frequency (LM1086-Adj.)

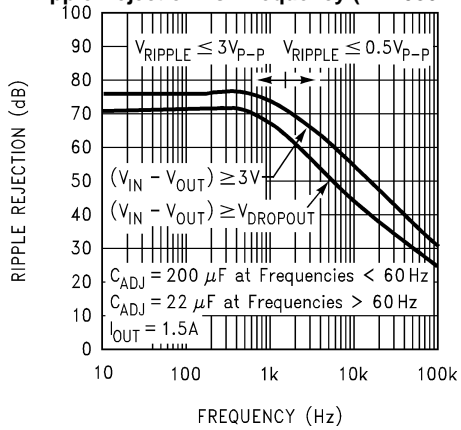


Figure 12.

Ripple Rejection vs. Output Current (LM1086-Adj.)

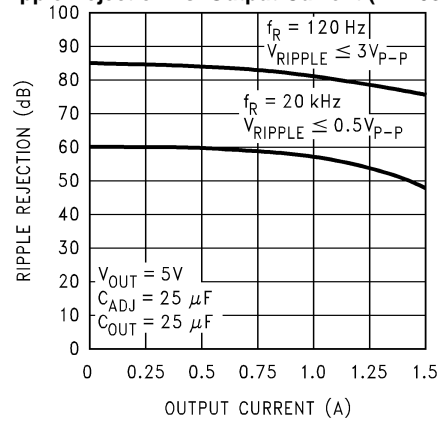


Figure 13.

Ripple Rejection vs. Frequency (LM1086-5)

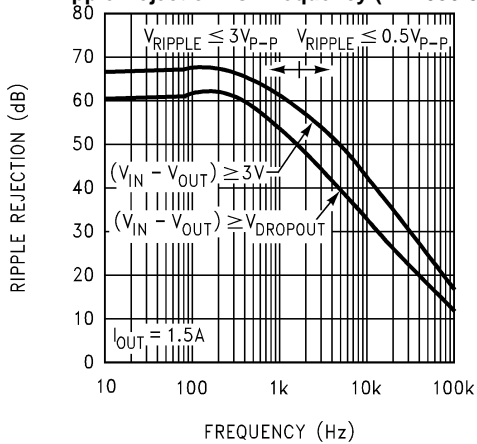


Figure 14.

Ripple Rejection vs. Output Current (LM1086-5)

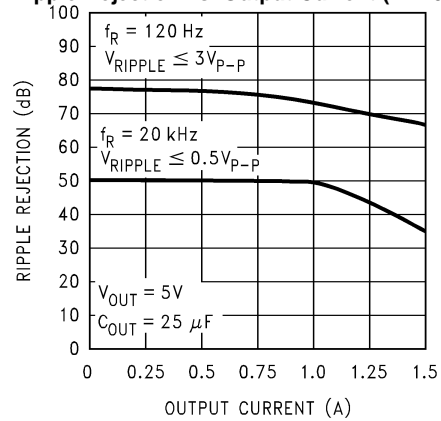


Figure 15.

Line Transient Response

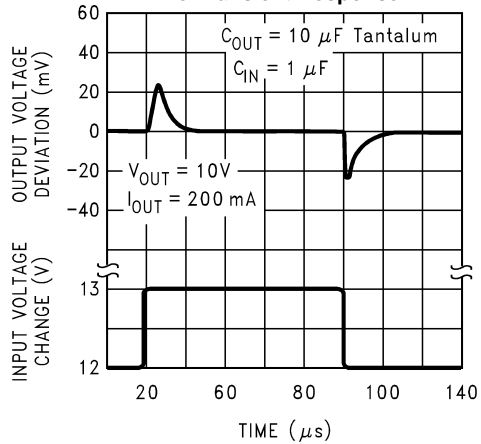


Figure 16.

Load Transient Response

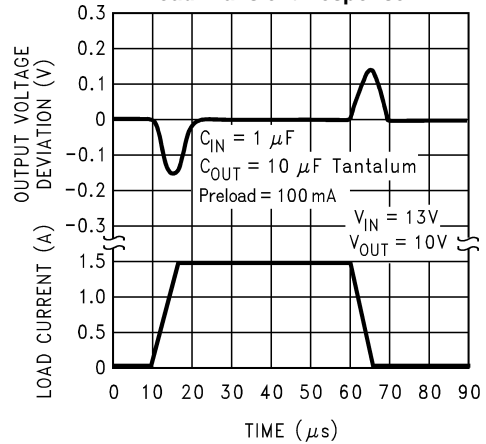


Figure 17.

GENERAL

Figure 18 shows a basic functional diagram for the LM1086-Adj (excluding protection circuitry). The topology is basically that of the LM317 except for the pass transistor. Instead of a Darlington NPN with its two diode voltage drop, the LM1086 uses a single NPN. This results in a lower dropout voltage. The structure of the pass transistor is also known as a quasi LDO. The advantage a quasi LDO over a PNP LDO is its inherently lower quiescent current. The LM1086 is specified to provide a minimum dropout voltage 1.5V over temperature, at full load.

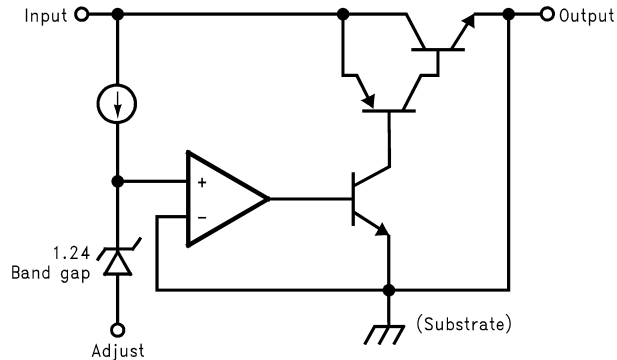


Figure 18. Basic Functional Diagram for the LM1086, excluding Protection circuitry

OUTPUT VOLTAGE

The LM1086 adjustable version develops at 1.25V reference voltage, (V_{REF}), between the output and the adjust terminal. As shown in figure 2, this voltage is applied across resistor R1 to generate a constant current I1. This constant current then flows through R2. The resulting voltage drop across R2 adds to the reference voltage to sets the desired output voltage.

The current I_{ADJ} from the adjustment terminal introduces an output error. But since it is small (120uA max), it becomes negligible when R1 is in the 100Ω range.

For fixed voltage devices, R1 and R2 are integrated inside the devices.

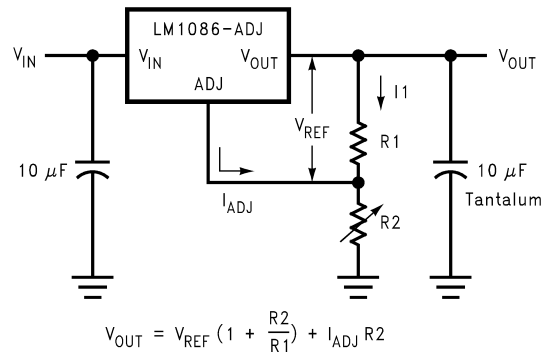


Figure 19. Basic Adjustable Regulator

STABILITY CONSIDERATION

Stability consideration primarily concern the phase response of the feedback loop. In order for stable operation, the loop must maintain negative feedback. The LM1086 requires a certain amount series resistance with capacitive loads. This series resistance introduces a zero within the loop to increase phase margin and thus increase stability. The equivalent series resistance (ESR) of solid tantalum or aluminum electrolytic capacitors is used to provide the appropriate zero (approximately 500 kHz).

The Aluminum electrolytic are less expensive than tantalums, but their ESR varies exponentially at cold temperatures; therefore requiring close examination when choosing the desired transient response over temperature. Tantalums are a convenient choice because their ESR varies less than 2:1 over temperature.

The recommended load/decoupling capacitance is a 10uF tantalum or a 50uF aluminum. These values will assure stability for the majority of applications.

The adjustable versions allows an additional capacitor to be used at the ADJ pin to increase ripple rejection. If this is done the output capacitor should be increased to 22uF for tantalums or to 150uF for aluminum.

Capacitors other than tantalum or aluminum can be used at the adjust pin and the input pin. A 10uF capacitor is a reasonable value at the input. See [RIPPLE REJECTION](#) section regarding the value for the adjust pin capacitor.

It is desirable to have large output capacitance for applications that entail large changes in load current (microprocessors for example). The higher the capacitance, the larger the available charge per demand. It is also desirable to provide low ESR to reduce the change in output voltage:

$$\Delta V = \Delta I \times \text{ESR}$$

It is common practice to use several tantalum and ceramic capacitors in parallel to reduce this change in the output voltage by reducing the overall ESR.

Output capacitance can be increased indefinitely to improve transient response and stability.

RIPPLE REJECTION

Ripple rejection is a function of the open loop gain within the feed-back loop (refer to [Figure 18](#) and [Figure 19](#)). The LM1086 exhibits 75dB of ripple rejection (typ.). When adjusted for voltages higher than V_{REF} , the ripple rejection decreases as function of adjustment gain: $(1+R1/R2)$ or V_O/V_{REF} . Therefore a 5V adjustment decreases ripple rejection by a factor of four (-12dB); Output ripple increases as adjustment voltage increases.

However, the adjustable version allows this degradation of ripple rejection to be compensated. The adjust terminal can be bypassed to ground with a capacitor (C_{ADJ}). The impedance of the C_{ADJ} should be equal to or less than $R1$ at the desired ripple frequency. This bypass capacitor prevents ripple from being amplified as the output voltage is increased.

$$1/(2\pi * f_{RIPPLE} * C_{ADJ}) \leq R1$$

LOAD REGULATION

The LM1086 regulates the voltage that appears between its output and ground pins, or between its output and adjust pins. In some cases, line resistances can introduce errors to the voltage across the load. To obtain the best load regulation, a few precautions are needed.

[Figure 20](#) shows a typical application using a fixed output regulator. $Rt1$ and $Rt2$ are the line resistances. V_{LOAD} is less than the V_{OUT} by the sum of the voltage drops along the line resistances. In this case, the load regulation seen at the R_{LOAD} would be degraded from the data sheet specification. To improve this, the load should be tied directly to the output terminal on the positive side and directly tied to the ground terminal on the negative side.

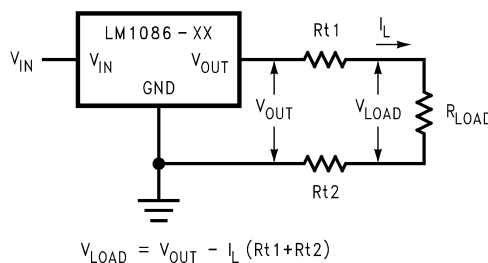


Figure 20. Typical Application using Fixed Output Regulator

When the adjustable regulator is used (Figure 21), the best performance is obtained with the positive side of the resistor R1 tied directly to the output terminal of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 5V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of 0.05Ω × I_L. If R1 (=125Ω) is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, it is 4 times worse. In addition, the ground side of the resistor R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

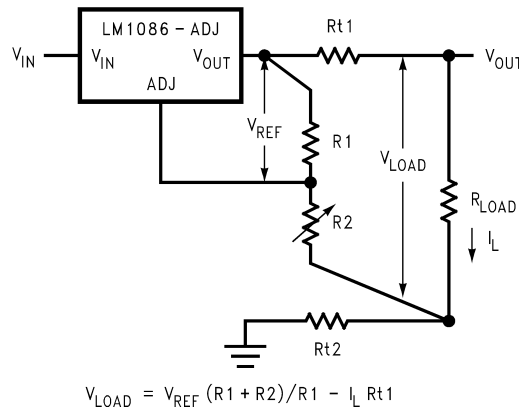


Figure 21. Best Load Regulation using Adjustable Output Regulator

PROTECTION DIODES

Under normal operation, the LM1086 regulator does not need any protection diode. With the adjustable device, the internal resistance between the adjustment and output terminals limits the current. No diode is needed to divert the current around the regulator even with a capacitor on the adjustment terminal. The adjust pin can take a transient signal of ±25V with respect to the output voltage without damaging the device.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and rate of decrease of V_{IN}. In the LM1086 regulator, the internal diode between the output and input pins can withstand microsecond surge currents of 10A to 20A. With an extremely large output capacitor (≥1000 μf), and with input instantaneously shorted to ground, the regulator could be damaged. In this case, an external diode is recommended between the output and input pins to protect the regulator, shown in Figure 22.

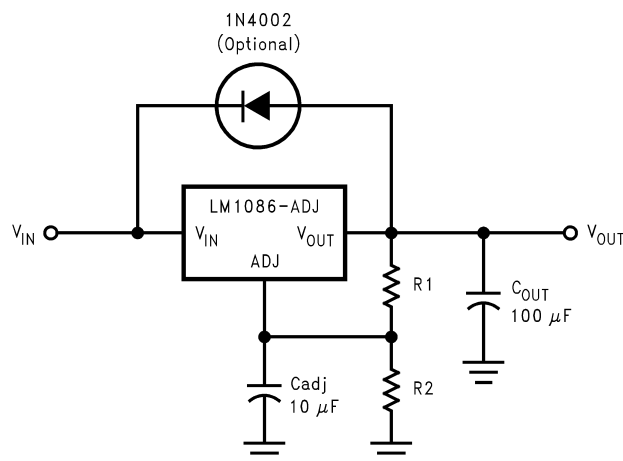


Figure 22. Regulator with Protection Diode

OVERLOAD RECOVERY

Overload recovery refers to regulator's ability to recover from a short circuited output. A key factor in the recovery process is the current limiting used to protect the output from drawing too much power. The current limiting circuit reduces the output current as the input to output differential increases. Refer to short circuit curve in the [Typical Performance Characteristics](#) section.

During normal start-up, the input to output differential is small since the output follows the input. But, if the output is shorted, then the recovery involves a large input to output differential. Sometimes during this condition the current limiting circuit is slow in recovering. If the limited current is too low to develop a voltage at the output, the voltage will stabilize at a lower level. Under these conditions it may be necessary to recycle the power of the regulator in order to get the smaller differential voltage and thus adequate start up conditions. Refer to [Typical Performance Characteristics](#) section for the short circuit current vs. input differential voltage.

THERMAL CONSIDERATIONS

ICs heats up when in operation, and power consumption is one factor in how hot it gets. The other factor is how well the heat is dissipated. Heat dissipation is predictable by knowing the thermal resistance between the IC and ambient (θ_{JA}). Thermal resistance has units of temperature per power (C/W). The higher the thermal resistance, the hotter the IC.

The LM1086 specifies the thermal resistance for each package as junction to case (θ_{JC}). In order to get the total resistance to ambient (θ_{JA}), two other thermal resistance must be added, one for case to heat-sink (θ_{CH}) and one for heatsink to ambient (θ_{HA}). The junction temperature can be predicted as follows:

$$T_J = T_A + P_D (\theta_{JC} + \theta_{CH} + \theta_{HA}) = T_A + P_D \theta_{JA}$$

where

- T_J is junction temperature
- T_A is ambient temperature
- P_D is the power consumption of the device

Device power consumption is calculated as follows:

$$I_{IN} = I_L + I_G$$

$$P_D = (V_{IN} - V_{OUT}) I_L + V_{IN} I_G$$

Figure 23 shows the voltages and currents which are present in the circuit.

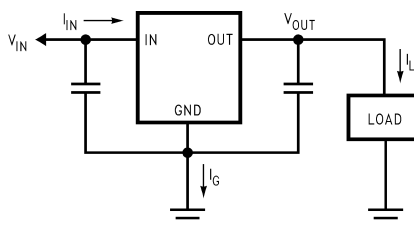


Figure 23. Power Dissipation Diagram

Once the device power is determined, the maximum allowable ($\theta_{JA(max)}$) is calculated as:

$$\theta_{JA(max)} = T_{R(max)} / P_D = T_{J(max)} - T_{A(max)} / P_D$$

The LM1086 has different temperature specifications for two different sections of the IC: the control section and the output section. The [Electrical Characteristics](#) table shows the junction to case thermal resistances for each of these sections, while the maximum junction temperatures ($T_{J(max)}$) for each section is listed in the [Absolute Maximum](#) section of the datasheet. $T_{J(max)}$ is 125°C for the control section, while $T_{J(max)}$ is 150°C for the output section.

$\theta_{JA(max)}$ should be calculated separately for each section as follows:

$$\theta_{JA(max, CONTROL SECTION)} = (125^\circ\text{C for } T_{A(max)}) / P_D$$

$$\theta_{JA(max, OUTPUT SECTION)} = (150^\circ\text{C for } T_{A(max)}) / P_D$$

The required heat sink is determined by calculating its required thermal resistance ($\theta_{HA(max)}$).

$$\theta_{HA(max)} = \theta_{JA(max)} - (\theta_{JC} + \theta_{CH})$$

$\theta_{HA(max)}$ should be calculated twice as follows:

$$\theta_{HA(max)} = \theta_{JA(max, CONTROL SECTION)} - (\theta_{JC (CONTROL SECTION)} + \theta_{CH})$$

$$\theta_{HA(max)} = \theta_{JA(max, OUTPUT SECTION)} - (\theta_{JC(OUTPUT SECTION)} + \theta_{CH})$$

If thermal compound is used, θ_{CH} can be estimated at 0.2 C/W. If the case is soldered to the heat sink, then a θ_{CH} can be estimated as 0 C/W.

After, $\theta_{HA(max)}$ is calculated for each section, choose the lower of the two $\theta_{HA(max)}$ values to determine the appropriate heat sink.

If PC board copper is going to be used as a heat sink, then [Figure 24](#) can be used to determine the appropriate area (size) of copper foil required.

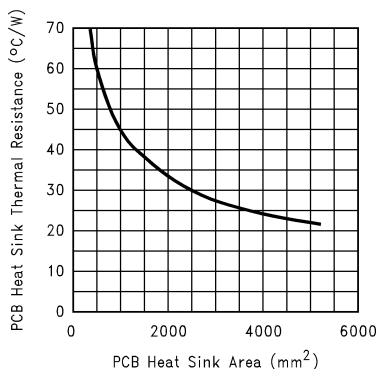


Figure 24. Heat sink thermal Resistance vs. Area

Typical Applications

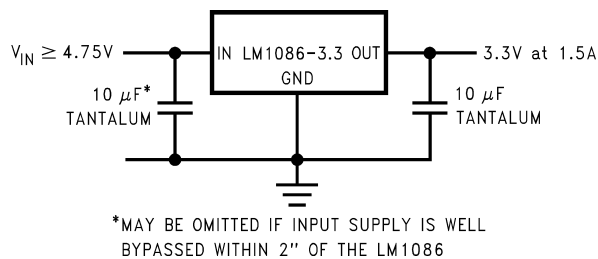


Figure 25. 5V to 3.3V, 1.5A Regulator

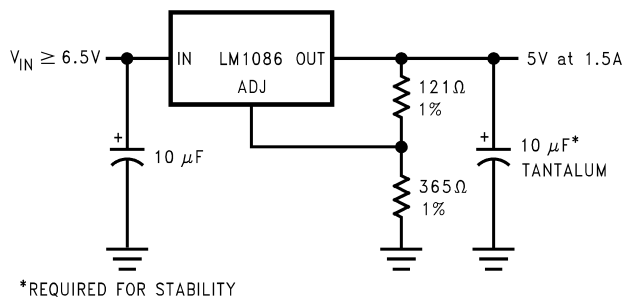
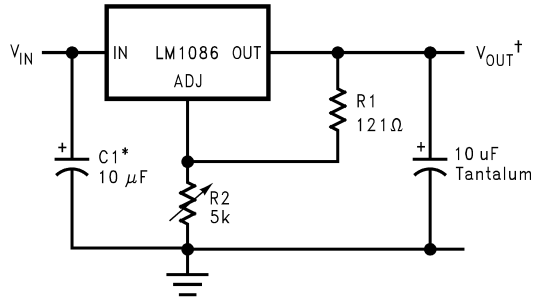


Figure 26. Adjustable @ 5V



*NEEDED IF DEVICE IS FAR FROM FILTER CAPACITORS

$$V_{OUT} = 1.25V \left(1 + \frac{R2}{R1}\right)$$

Figure 27. 1.2V to 15V Adjustable Regulator

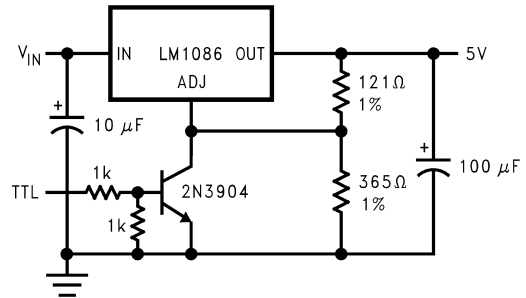


Figure 28. 5V Regulator with Shutdown

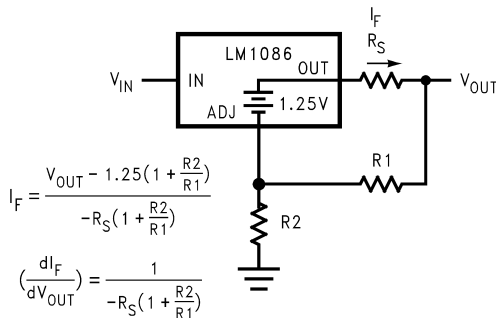


Figure 29. Battery Charger

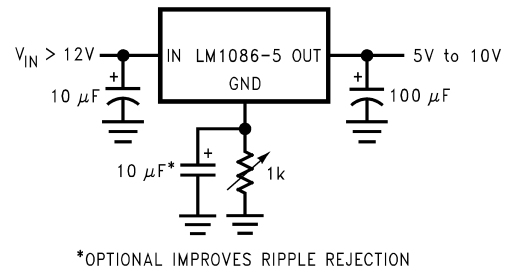


Figure 30. Adjustable Fixed Regulator

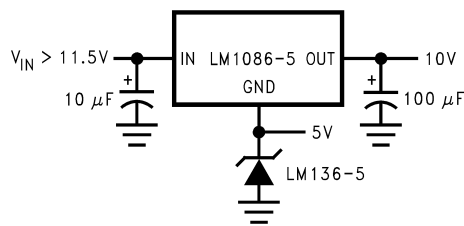


Figure 31. Regulator with Reference

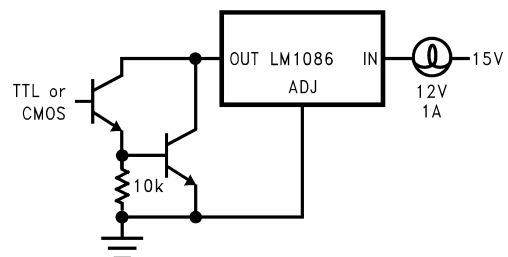


Figure 32. High Current Lamp Driver Protection

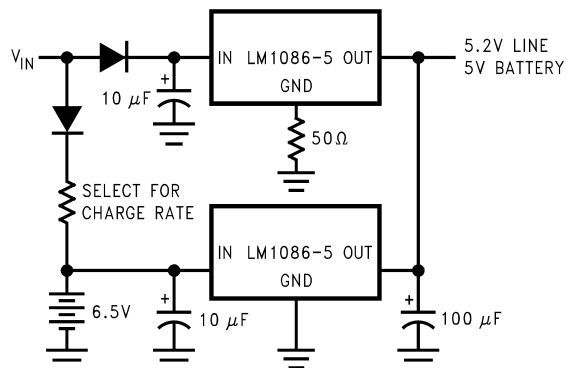
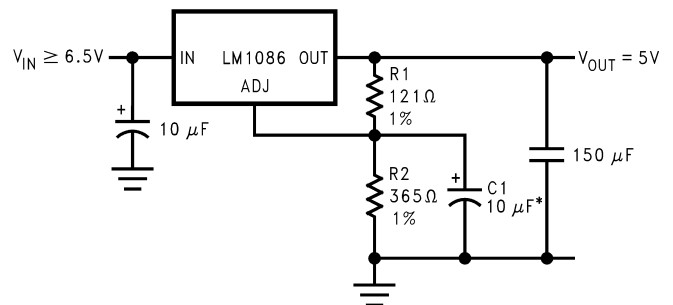


Figure 33. Battery Backup Regulated Supply



*C1 IMPROVES RIPPLE REJECTION.
XC SHOULD BE ≈ R1 AT RIPPLE FREQUENCY

Figure 34. Ripple Rejection Enhancement

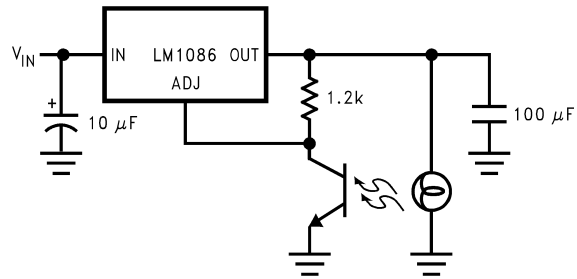


Figure 35. Automatic Light control

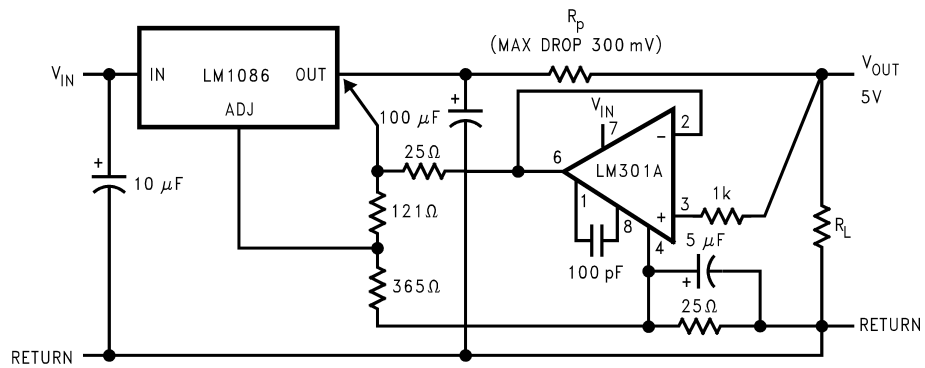


Figure 36. Remote Sensing

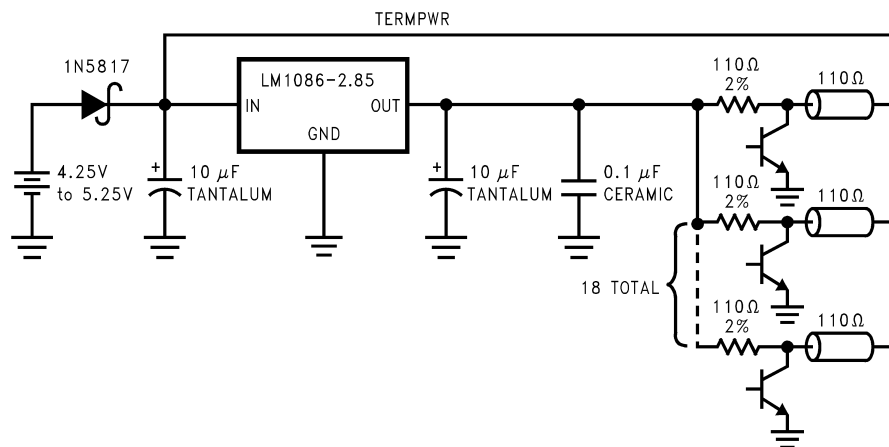


Figure 37. SCSI-2 Active termination