

Description

The 30P10A uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

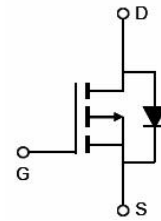
General Features

V_{DSS}	$R_{DS(ON)}$ @ -4.5V(Typ)	$R_{DS(ON)}$ @ -10V(Typ)	I_D
-100V	39 m Ω	33 m Ω	-30A

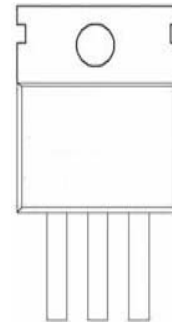
- Super high dense cell design
- Advanced trench process technology
- Reliable and rugged
- High density cell design for ultra low On-Resistance

Application

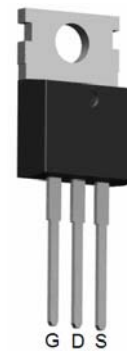
- Portable equipment and battery powered systems



Schematic diagram



Marking and pin assignment



TO-220

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-30	A
Drain Current-Continuous($T_C=100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	-21	A
Pulsed Drain Current	I_{DM}	-140	A
Maximum Power Dissipation	P_D	120	W
Derating factor		0.8	W/ $^\circ\text{C}$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta Jc}$	1.25	°C/W
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Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

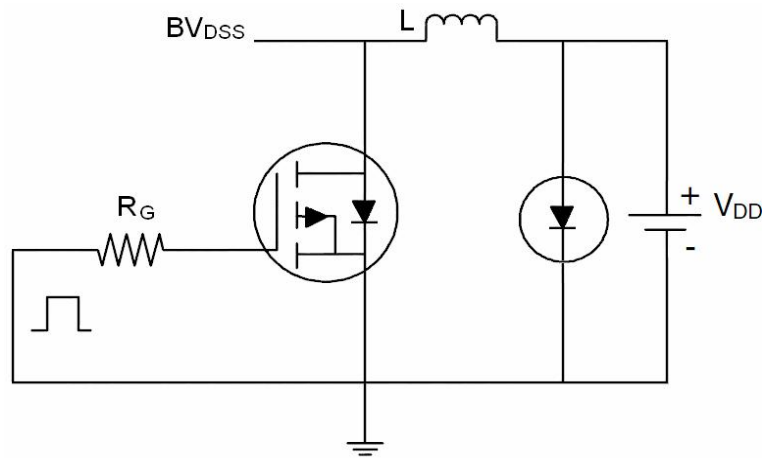
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-100V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.5	-2.2	-3	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-10A$	-	33	45	$m\Omega$
		$V_{GS}=-4.5V, I_D=-8A$	-	39	55	$m\Omega$
Forward Transconductance	g_{FS}	$V_{DS}=-50V, I_D=-10A$	5	-	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=-25V, V_{GS}=0V,$ $F=1.0MHz$	-	2700	-	PF
Output Capacitance	C_{oss}		-	790	-	PF
Reverse Transfer Capacitance	C_{rss}		-	450	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-50V, I_D=-15A$ $V_{GS}=-10V, R_{GEN}=9.1\Omega$	-	17	-	nS
Turn-on Rise Time	t_r		-	80	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	45	-	nS
Turn-Off Fall Time	t_f		-	65	-	nS
Total Gate Charge	Q_g	$V_{DS}=-50V, I_D=-15A,$ $V_{GS}=-10V$	-	90	-	nC
Gate-Source Charge	Q_{gs}		-	15	-	nC
Gate-Drain Charge	Q_{gd}		-	35	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_S=-10A$	-	-	-1.2	V
Diode Forward Current ^(Note 2)	I_S	-	-	-	-30	A
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ C, I_F = -15A$	-	90	-	nS
Reverse Recovery Charge	Q_{rr}	$di/dt = 100A/\mu s$ (Note 3)	-	70	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

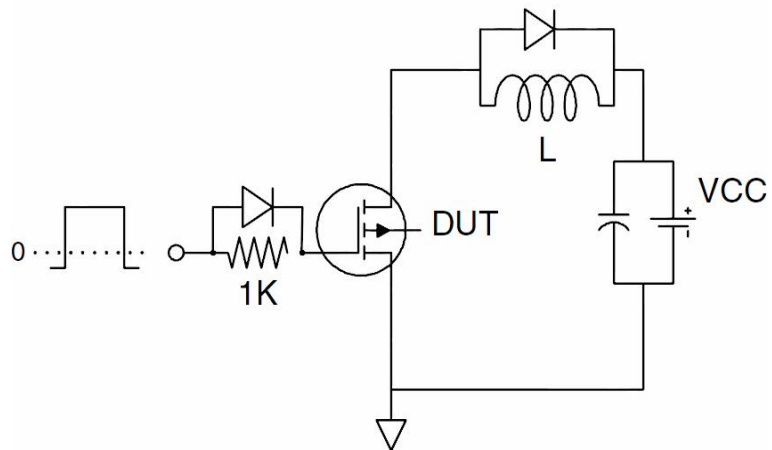
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^\circ C, V_{DD}=-50V, V_G=-10V, L=0.5mH, R_g=25\Omega$

Test Circuit

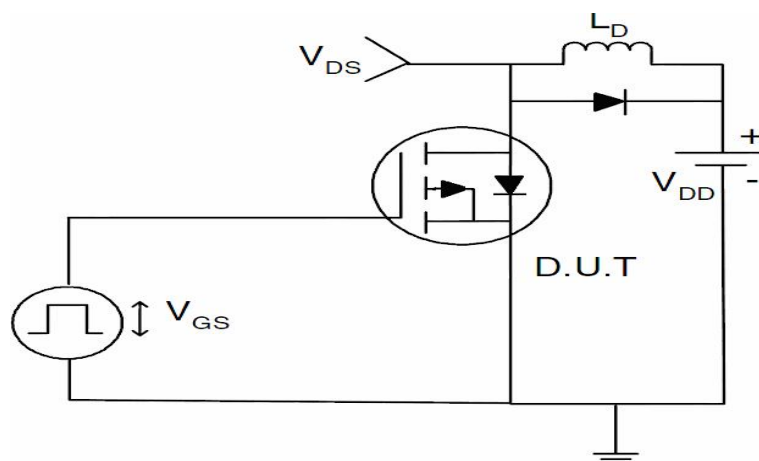
1) EAS Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

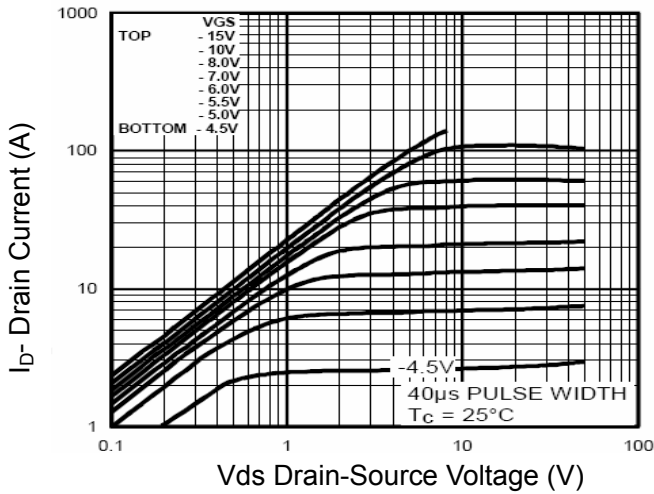


Figure 1 Output Characteristics

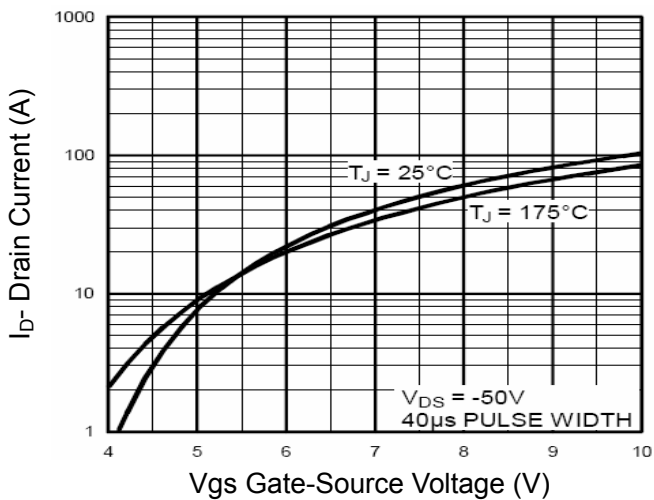


Figure 2 Transfer Characteristics

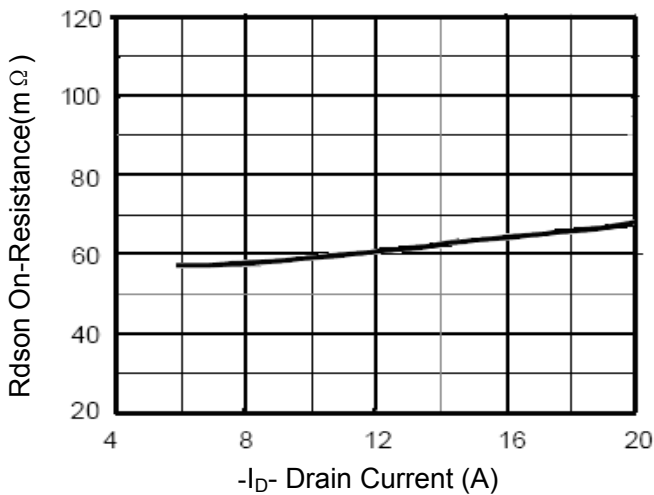


Figure 3 Rdson- Drain Current

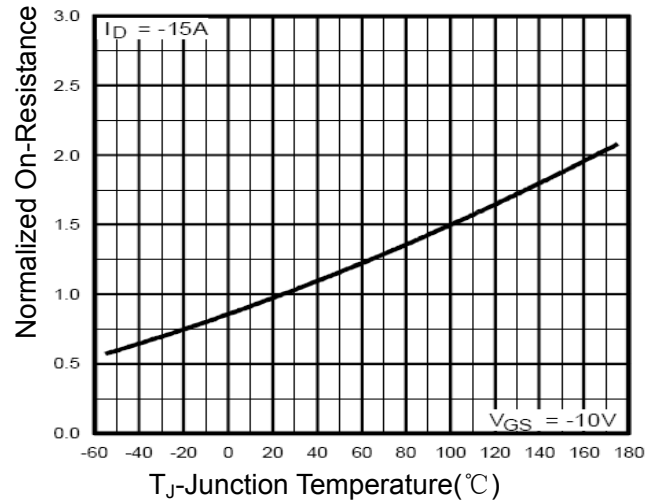


Figure 4 Rdson-Junction Temperature

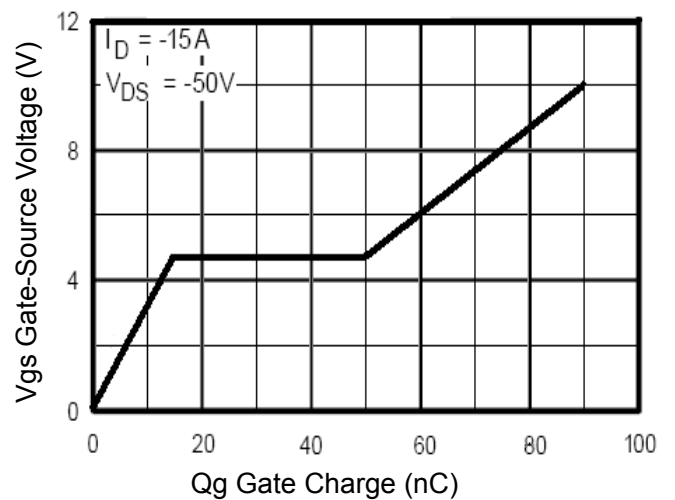


Figure 5 Gate Charge

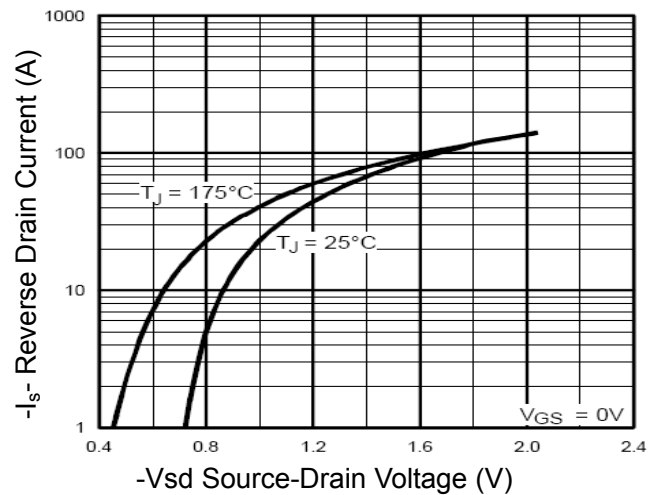


Figure 6 Source- Drain Diode Forward

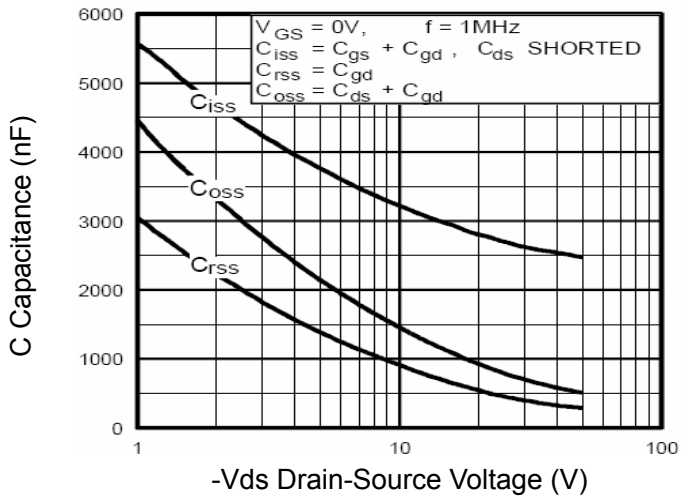


Figure 7 Capacitance vs Vds

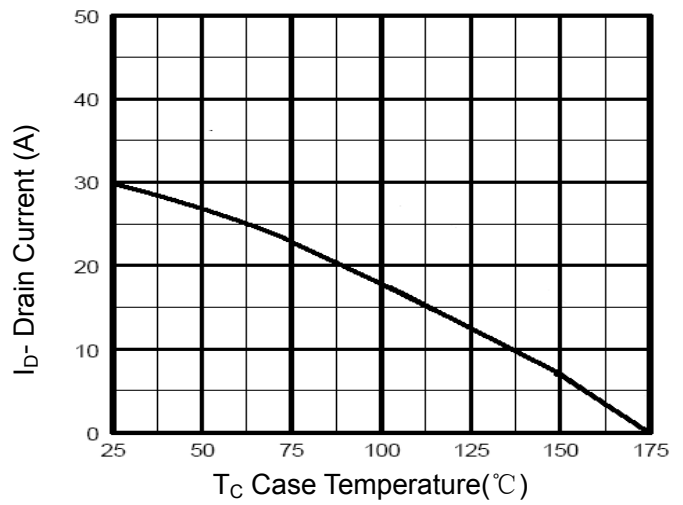


Figure 9 Drain Current vs Case Temperature

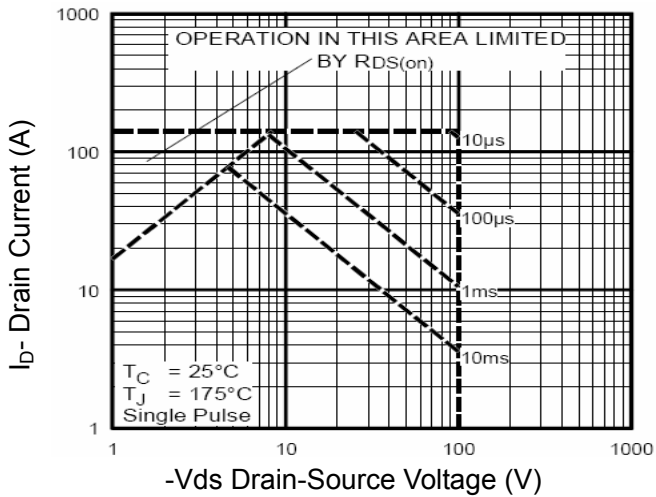


Figure 8 Safe Operation Area

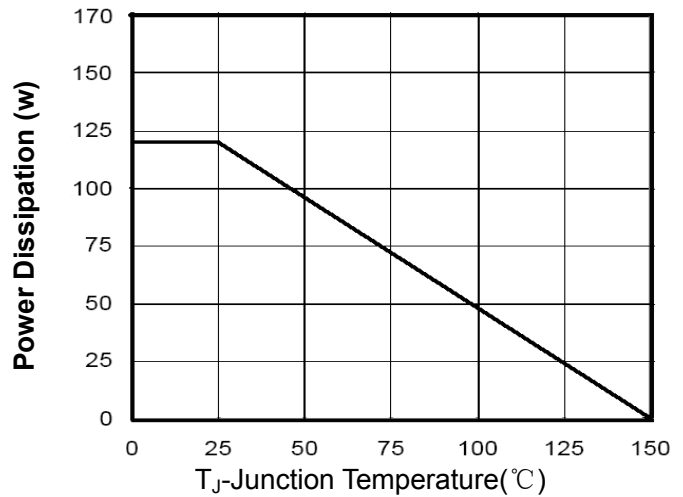


Figure 10 Power De-rating

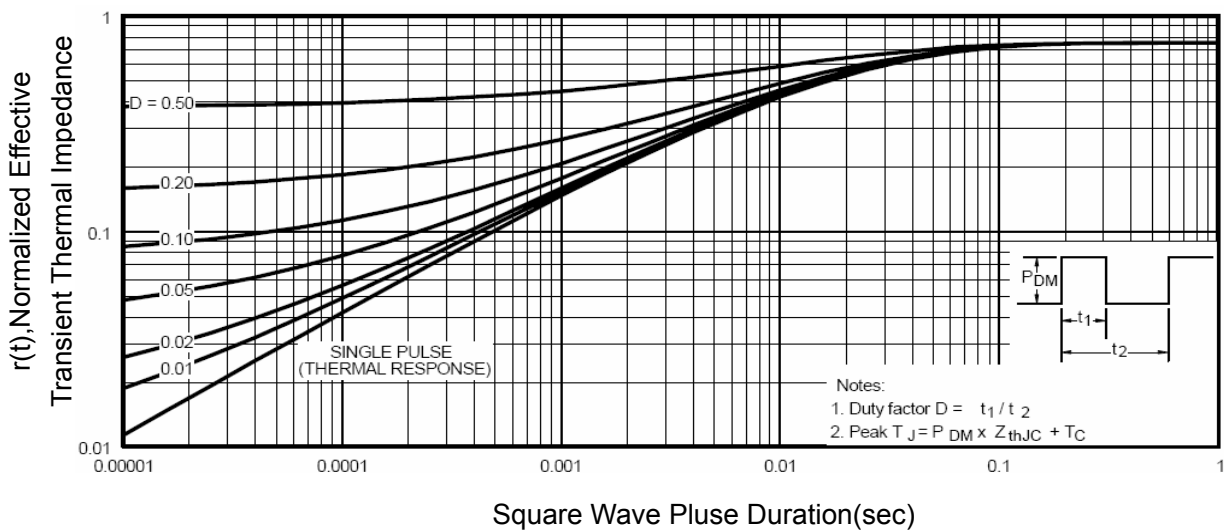


Figure 11 Normalized Maximum Transient Thermal Impedance