

# bq24314A Overvoltage and Overcurrent Protection IC and Li+ Charger Front-End Protection IC

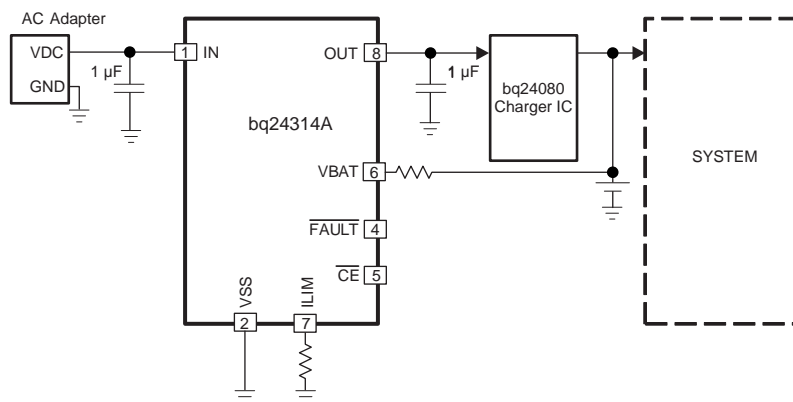
## 1 Features

- Provides Protection for Three Variables:
  - Input Overvoltage, With Rapid Response in  $< 1 \mu\text{s}$
  - User-Programmable Overcurrent With Current Limiting
  - Battery Overvoltage
- Maximum Input Voltage of 30 V
- Supports up to 1.5-A Input Current
- Robust Against False Triggering Due to Current Transients
- Thermal Shutdown
- Enable Input
- Status Indication – Fault Condition
- Available in Space-Saving Small 8 Lead 2 x 2 WSON

## 2 Applications

- Mobile Phones and Smart Phones
- PDAs
- MP3 Players
- Low-Power Handheld Devices
- Bluetooth™ Headsets

## 4 Simplified Schematic



## 3 Description

The bq24314A device is a highly integrated circuit (IC) designed to provide protection to Li-ion batteries from failures of the charging circuit. The device continuously monitors the input voltage, the input current, and the battery voltage. In case of an input overvoltage condition, the device immediately removes power from the charging circuit by turning off an internal switch. In the case of an overcurrent condition, it limits the system current at the threshold value, and if the overcurrent persists, switches the pass element OFF after a blanking period. Additionally, the device also monitors its own die temperature and switches off if it exceeds 140°C. The input overcurrent threshold is user-programmable.

The device can be controlled by a processor and also provides status information about fault conditions to the host.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq24314A	WSON (8)	2.00 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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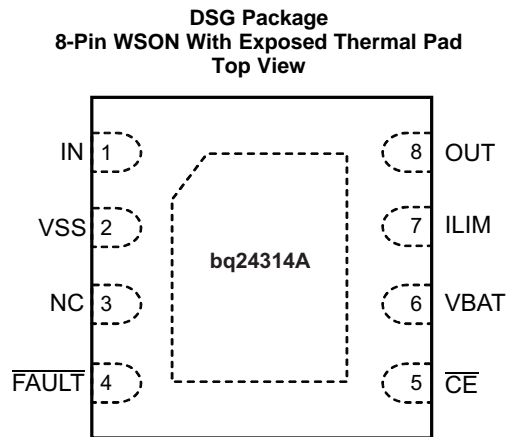
## 5 Revision History

### Changes from Original (November 2008) to Revision A

Page

• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	<b>1</b>
• Changed SON to WSON throughout document .....	<b>1</b>
• Changed $R_{LIM}$ from 25k to 24.9k throughout document.....	<b>5</b>
• Changed $A\Omega$ to $Ak\Omega$ .....	<b>5</b>
• Moved Figures 2 through 11 from <i>Typical Characteristics</i> to <i>Application Curves</i> section .....	<b>15</b>

## 6 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{CE}}$	5	I	Chip enable input. Active low. When $\overline{\text{CE}}$ = High, the input FET is off. Internally pulled down.
$\overline{\text{FAULT}}$	4	O	Open-drain output, device status. $\overline{\text{FAULT}}$ = Low indicates that the input FET Q1 has been turned off due to input overvoltage, input overcurrent, battery overvoltage, or thermal shutdown.
ILIM	7	I/O	Input overcurrent threshold programming. Connect a resistor to VSS to set the overcurrent threshold.
IN	1	I	Input power, connect to external DC supply. Connect external 1 $\mu\text{F}$ ceramic capacitor (minimum) to VSS.
NC	3	—	These pins may have internal circuits used for test purposes. Do not make any external connections at these pins for normal operation.
OUT	8	O	Output terminal to the charging system. Connect external 1 $\mu\text{F}$ ceramic capacitor (minimum) to VSS.
VBAT	6	I	Battery voltage sense input. Connect to pack positive terminal through a resistor.
VSS	2	—	Ground terminal
Thermal PAD		—	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. The VSS pin must be connected to ground at all times.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>I</sub>	Input voltage	IN (with respect to VSS)	-0.3	30	V
		OUT (with respect to VSS)	-0.3	12	
		ILIM, FAULT, CE, VBAT (with respect to VSS)	-0.3	7	
I <sub>I</sub>	Input current	IN		2	A
I <sub>O</sub>	Output current	OUT		2	A
	Output sink current	FAULT		15	mA
T <sub>J</sub>	Junction temperature		-40	150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

			VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500		
		IN(IEC 61000-4-2) <sup>(3)</sup>	Air Discharge		±15000
			Contact		±8000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.  
 (3) With IN bypassed to the VSS with a 1-μF low-ESR ceramic capacitor

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V <sub>IN</sub>	Input voltage range		3		30	V
I <sub>IN</sub>	Input current, IN pin				1.5	A
I <sub>OUT</sub>	Output current, OUT pin				1.5	A
R <sub>ILIM</sub>	OCP Programming resistor		15		90	kΩ
T <sub>J</sub>	Junction temperature		-40		125	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		bq24314A	UNIT
		DSG (WSON)	
		8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	64	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	84.1	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	33.9	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.9	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	34.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	5.6	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

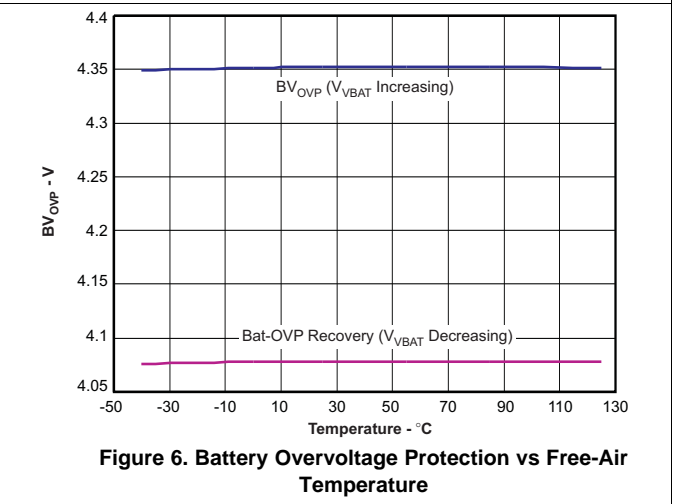
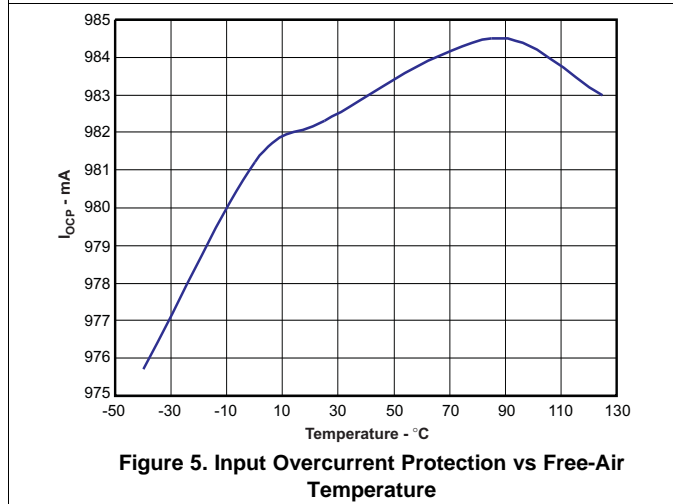
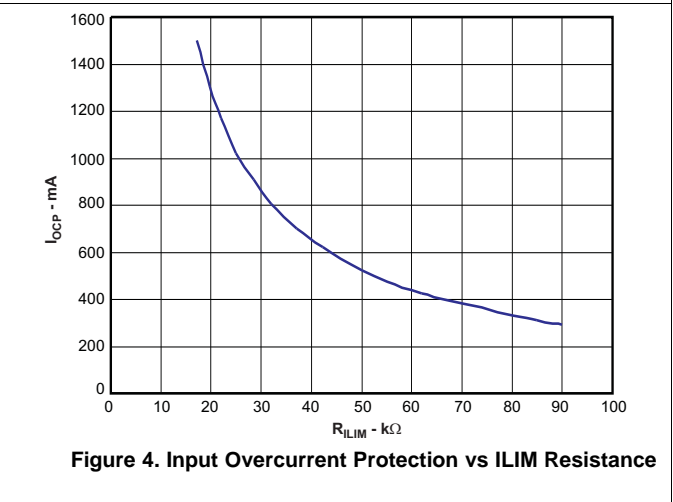
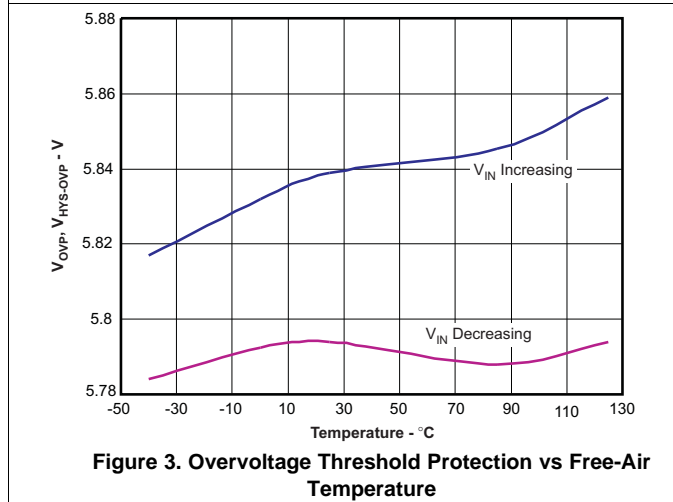
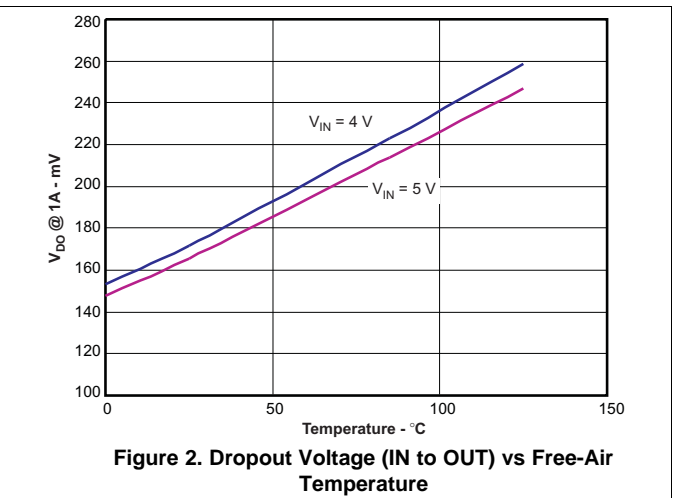
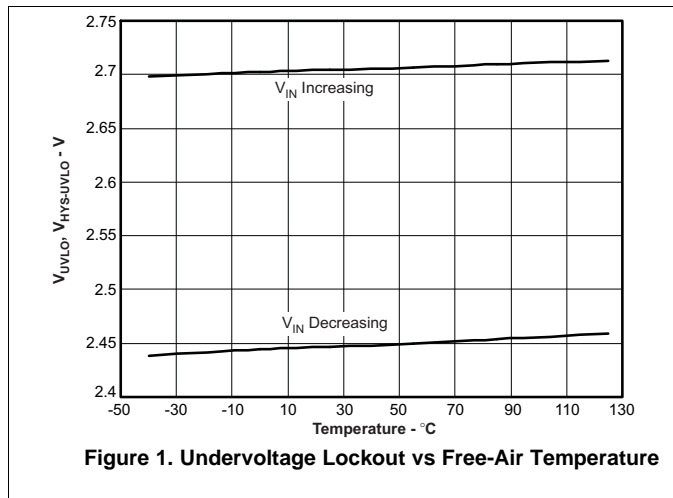
over junction temperature range  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>IN</b>						
UVLO	Undervoltage lock-out, input power detected threshold	$\overline{\text{CE}} = \text{Low}$ , $V_{\text{IN}}$ increasing from 0 V to 3 V	2.6	2.7	2.8	V
$V_{\text{hys}}(\text{UVLO})$	Hysteresis on UVLO	$\overline{\text{CE}} = \text{Low}$ , $V_{\text{IN}}$ decreasing from 3 V to 0 V	200	260	300	mV
$T_{\text{DGL}}(\text{PGOOD})$	Deglintch time, input power detected status	$\overline{\text{CE}} = \text{Low}$ . Time measured from $V_{\text{IN}}$ 0 V $\rightarrow$ 5 V 1 $\mu\text{s}$ rise-time, to output turning ON		8		ms
$I_{\text{DD}}$	Operating current	$\overline{\text{CE}} = \text{Low}$ , No load on OUT pin, $V_{\text{IN}} = 5\text{ V}$ , $R_{\text{ILIM}} = 24.9\text{ k}\Omega$		400	600	$\mu\text{A}$
$I_{\text{STDBY}}$	Standby current	$\overline{\text{CE}} = \text{High}$ , $V_{\text{IN}} = 5\text{ V}$		65	95	$\mu\text{A}$
<b>INPUT TO OUTPUT CHARACTERISTICS</b>						
VDO	Drop-out voltage IN to OUT	$\overline{\text{CE}} = \text{Low}$ , $V_{\text{IN}} = 5\text{ V}$ , $I_{\text{OUT}} = 1\text{ A}$		170	280	mV
<b>INPUT OVERVOLTAGE PROTECTION</b>						
$V_{\text{OVP}}$	Input overvoltage protection threshold	$\overline{\text{CE}} = \text{Low}$ , $V_{\text{IN}}$ increasing from 5 V to 7.5 V	5.71	5.85	6.00	V
$t_{\text{PD}}(\text{OVP})$	Input OV propagation delay <sup>(1)</sup>	$\overline{\text{CE}} = \text{Low}$		200		ns
$V_{\text{hys}}(\text{OVP})$	Hysteresis on OVP	$\overline{\text{CE}} = \text{Low}$ , $V_{\text{IN}}$ decreasing from 7.5 V to 5 V	20	60	110	mV
$t_{\text{ON}}(\text{OVP})$	Recovery time from input overvoltage condition	$\overline{\text{CE}} = \text{Low}$ , Time measured from $V_{\text{IN}} 7.5\text{ V} \rightarrow 5\text{ V}$ , 1 $\mu\text{s}$ fall-time		8		ms
<b>INPUT OVERCURRENT PROTECTION</b>						
$I_{\text{OCP}}$	Input overcurrent protection threshold range		300		1500	mA
$I_{\text{OCP}}$	Input overcurrent protection threshold	$\overline{\text{CE}} = \text{Low}$ , $R_{\text{ILIM}} = 24.9\text{ k}\Omega$ , $3\text{ V} \leq V_{\text{IN}} < V_{\text{OVP}} - V_{\text{hys}}(\text{OVP})$	900	1000	1100	mA
$K_{\text{ILIM}}$	Programmable current limit factor			25		Ak $\Omega$
$t_{\text{BLANK}}(\text{OCP})$	Blanking time, input overcurrent detected			176		$\mu\text{s}$
$t_{\text{REC}}(\text{OCP})$	Recovery time from input overcurrent condition			64		ms
<b>BATTERY OVERVOLTAGE PROTECTION</b>						
$BV_{\text{OVP}}$	Battery overvoltage protection threshold	$\overline{\text{CE}} = \text{Low}$ , $V_{\text{IN}} > 4.4\text{ V}$	4.30	4.35	4.4	V
$V_{\text{hys}}(\text{Bovp})$	Hysteresis on $BV_{\text{OVP}}$	$\overline{\text{CE}} = \text{Low}$ , $V_{\text{IN}} > 4.4\text{ V}$	200	275	320	mV
$I_{\text{VBAT}}$	Input bias current on VBAT pin	$V_{\text{BAT}} = 4.4\text{ V}$ , $T_{\text{J}} = 25^{\circ}\text{C}$			10	nA
$T_{\text{DGL}}(\text{Bovp})$	Deglintch time, battery overvoltage detected	$\overline{\text{CE}} = \text{Low}$ , $V_{\text{IN}} > 4.4\text{ V}$ . Time measured from $V_{\text{VBAT}}$ rising from 4.1 V to 4.4 V to FAULT going low.		176		$\mu\text{s}$
<b>THERMAL PROTECTION</b>						
$T_{\text{J(OFF)}}$	Thermal shutdown temperature			140	150	$^{\circ}\text{C}$
$T_{\text{J(OFF-HYS)}}$	Thermal shutdown hysteresis			20		$^{\circ}\text{C}$
<b>LOGIC LEVELS ON <math>\overline{\text{CE}}</math></b>						
$V_{\text{IL}}$	Low-level input voltage		0		0.4	V
$V_{\text{IH}}$	High-level input voltage		1.4			V
$I_{\text{IL}}$	Low-level input current	$V_{\text{CE}} = 0\text{ V}$			1	$\mu\text{A}$
$I_{\text{IH}}$	High-level input current	$V_{\text{CE}} = 1.8\text{ V} \geq$			15	$\mu\text{A}$
<b>LOGIC LEVELS ON FAULT</b>						
$V_{\text{OL}}$	Output low voltage	$I_{\text{SINK}} = 5\text{ mA}$			0.2	V
$I_{\text{HI-Z}}$	Leakage current, FAULT pin HI-Z	$V_{\text{FAULT}} = 5\text{ V}$			10	$\mu\text{A}$

(1) Not tested in production. Specified by design.

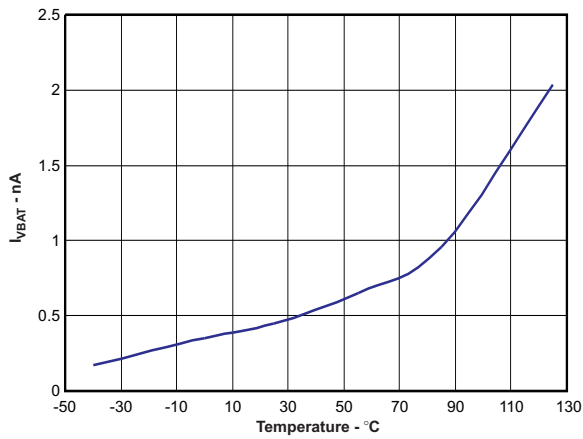
## 7.6 Typical Characteristics

Test conditions (unless otherwise noted) for typical operating performance:  $V_{IN} = 5\text{ V}$ ,  $C_{IN} = 1\ \mu\text{F}$ ,  $C_{OUT} = 1\ \mu\text{F}$ ,  $R_{LIM} = 24.9\ \text{k}\Omega$ ,  $R_{BAT} = 100\ \text{k}\Omega$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{PU} = 3.3\ \text{V}$  (see Figure 13 for the *Typical Application Circuit*)

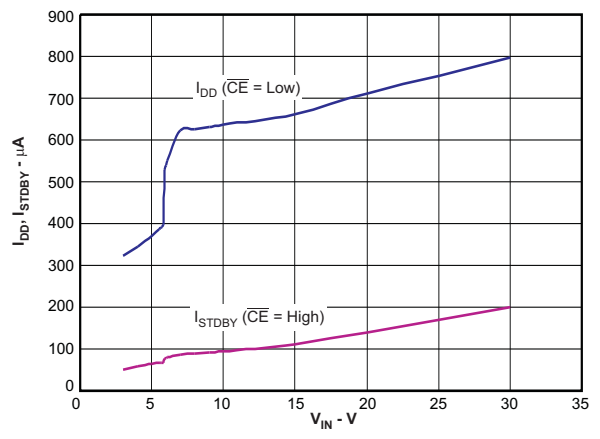


**Typical Characteristics (continued)**

Test conditions (unless otherwise noted) for typical operating performance:  $V_{IN} = 5\text{ V}$ ,  $C_{IN} = 1\ \mu\text{F}$ ,  $C_{OUT} = 1\ \mu\text{F}$ ,  $R_{ILIM} = 24.9\ \text{k}\Omega$ ,  $R_{BAT} = 100\ \text{k}\Omega$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{PU} = 3.3\ \text{V}$  (see [Figure 13](#) for the *Typical Application Circuit*)



**Figure 7. Leakage Current (VBAT Pin) vs Free-Air Temperature**



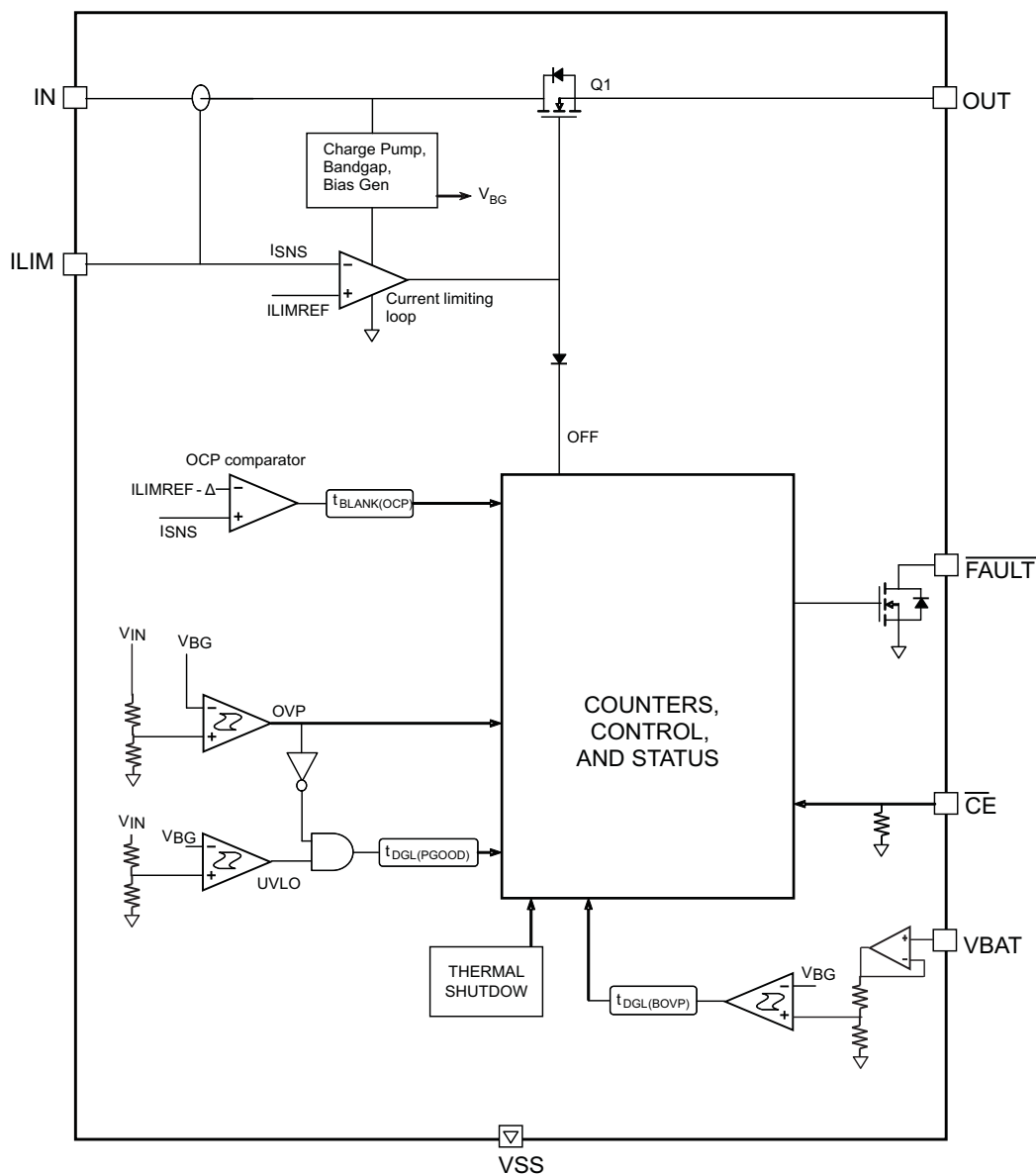
**Figure 8. Supply Current vs INPUT Voltage**

## 8 Detailed Description

### 8.1 Overview

The bq24314A device is a highly integrated circuit designed to provide protection to Li-ion batteries from failures of the charging circuit. The device continuously monitors the input voltage, the input current, and the battery voltage. In case of an input overvoltage condition, the device immediately removes power from the charging circuit by turning off an internal switch. In the case of an overcurrent condition, it limits the system current at the threshold value, and if the overcurrent persists, switches the pass element OFF after a blanking period. If the battery voltage rises to an unsafe level, the device disconnects power from the charging circuit until the battery voltage returns to an acceptable value. Additionally, the device also monitors its own die temperature and switches off if it exceeds 140°C. The input overcurrent threshold is user-programmable. The device can be controlled by a processor and also provides status information about fault conditions to the host.

### 8.2 Functional Block Diagram



**Figure 9. Simplified Block Diagram**



## 8.3 Feature Description

### 8.3.1 Input Overvoltage Protection

The bq24314A device integrates an input overvoltage protection feature to protect downstream devices from faulty input sources. If the input voltage rises above  $V_{OVP}$ , the internal FET Q1 is turned off, removing power from the circuit. As shown in [Figure 16](#) to [Figure 17](#), the response is very rapid, with the FET turning off in less than a microsecond. The  $\overline{\text{FAULT}}$  pin is driven low. When the input voltage returns below  $V_{OVP} - V_{hys(OVP)}$  (but is still above UVLO), the FET Q1 is turned on again after a deglitch time of  $t_{ON(OVP)}$  to ensure that the input supply has stabilized. [Figure 18](#) shows the recovery from input OVP.

### 8.3.2 Input Overcurrent Protection

The overcurrent threshold is programmed by a resistor  $R_{ILIM}$  connected from the ILIM pin to VSS. [Figure 4](#) shows the OCP threshold as a function of  $R_{ILIM}$ , and may be approximated by the following equation:

$$I_{OCP} = 25 \div R_{ILIM} \text{ (current in A, resistance in k}\Omega\text{)},$$

where

- $R_{ILIM}$  must be from between 15 k $\Omega$  to 90 k $\Omega$  (1)

If the load current tries to exceed the  $I_{OCP}$  threshold, the device limits the current for a blanking duration of  $t_{BLANK(OCP)}$ . If the load current returns to less than  $I_{OCP}$  before  $t_{BLANK(OCP)}$  times out, the device continues to operate. However, if the overcurrent situation persists for  $t_{BLANK(OCP)}$ , the FET Q1 is turned off for a duration of  $t_{REC(OCP)}$ , and the  $\overline{\text{FAULT}}$  pin is driven low. The FET is then turned on again after  $t_{REC(OCP)}$  and the current is monitored all over again. Each time an OCP fault occurs, an internal counter is incremented. If 15 OCP faults occur in one charge cycle, the FET is turned off permanently. The counter is cleared either by removing and re-applying input power, or by disabling and re-enabling the device with the  $\overline{\text{CE}}$  pin. [Figure 19](#) to [Figure 21](#) show what happens in an overcurrent fault.

To prevent the input voltage from spiking up due to the inductance of the input cable, Q1 is turned off slowly, resulting in a *soft-stop*, as shown in [Figure 21](#).

### 8.3.3 Battery Overvoltage Protection

The battery overvoltage threshold  $BV_{OVP}$  is internally set to 4.35 V. If the battery voltage exceeds the  $BV_{OVP}$  threshold, the FET Q1 is turned off, and the  $\overline{\text{FAULT}}$  pin is driven low. The FET is turned back on once the battery voltage drops to  $BV_{OVP} - V_{hys(Bovp)}$  (see [Figure 22](#) and [Figure 23](#)). Each time a battery overvoltage fault occurs, an internal counter is incremented. If 15 such faults occur in one charge cycle, the FET is turned off permanently. The counter is cleared either by removing and re-applying input power, or by disabling and re-enabling the device with the  $\overline{\text{CE}}$  pin. In the case of a battery overvoltage fault, Q1 is switched OFF gradually (see [Figure 22](#)).

### 8.3.4 Thermal Protection

If the junction temperature of the device exceeds  $T_{J(OFF)}$ , the FET Q1 is turned off, and the  $\overline{\text{FAULT}}$  pin is driven low. The FET is turned back on when the junction temperature falls below  $T_{J(OFF)} - T_{J(OFF-HYS)}$ .

### 8.3.5 Enable Function

The device has an enable pin which can be used to enable or disable the device. When the  $\overline{\text{CE}}$  pin is driven high, the internal FET is turned off. When the  $\overline{\text{CE}}$  pin is low, the FET is turned on if other conditions are safe. The OCP counter and the Bat-OVP counter are both reset when the device is disabled and re-enabled. The  $\overline{\text{CE}}$  pin has an internal pulldown resistor and can be left floating. Note that the  $\overline{\text{FAULT}}$  pin functionality is also disabled when the  $\overline{\text{CE}}$  pin is high.

## Feature Description (continued)

### 8.3.6 Fault Indication

The  $\overline{\text{FAULT}}$  pin is an active-low open-drain output. It is in a high-impedance state when operating conditions are safe, or when the device is disabled by setting  $\overline{\text{CE}}$  high. With  $\overline{\text{CE}}$  low, the  $\overline{\text{FAULT}}$  pin goes low whenever any of these events occurs:

- Input overvoltage
- Input overcurrent
- Battery overvoltage
- IC overtemperature

## 8.4 Device Functional Modes

### 8.4.1 OPERATION Mode

The device continuously monitors the input voltage, the input current, and the battery voltage. As long as the input voltage is less than VOVP, the output voltage tracks the input voltage (less the drop caused by RDSON of Q1). During fault conditions, the internal FET is turned off and the output is isolated from the input source.

### 8.4.2 POWER-DOWN Mode

The device remains in POWER-DOWN mode when the input voltage at the IN pin is below the undervoltage threshold UVLO. The FET Q1 connected between IN and OUT pins is off, and the status output,  $\overline{\text{FAULT}}$ , is set to Hi-Z. See [Figure 10](#).

### 8.4.3 POWER-ON RESET Mode

The device resets when the input voltage at the IN pin exceeds the UVLO threshold. All internal counters and other circuit blocks are reset. The device then waits for duration  $t_{\text{DGL(PGOOD)}}$  for the input voltage to stabilize. If, after  $t_{\text{DGL(PGOOD)}}$ , the input voltage and battery voltage are safe, FET Q1 is turned ON. The device has a soft-start feature to control the inrush current. The soft-start minimizes the ringing at the input (the ringing occurs because the parasitic inductance of the adapter cable and the input bypass capacitor form a resonant circuit). [Figure 14](#) shows the power-up behavior of the device. Because of the deglitch time at power-on, if the input voltage rises rapidly to beyond the OVP threshold, the device will not switch on at all, instead it will go into PROTECTION mode and indicate a fault on the  $\overline{\text{FAULT}}$  pin, as shown in [Figure 15](#).

Device Functional Modes (continued)

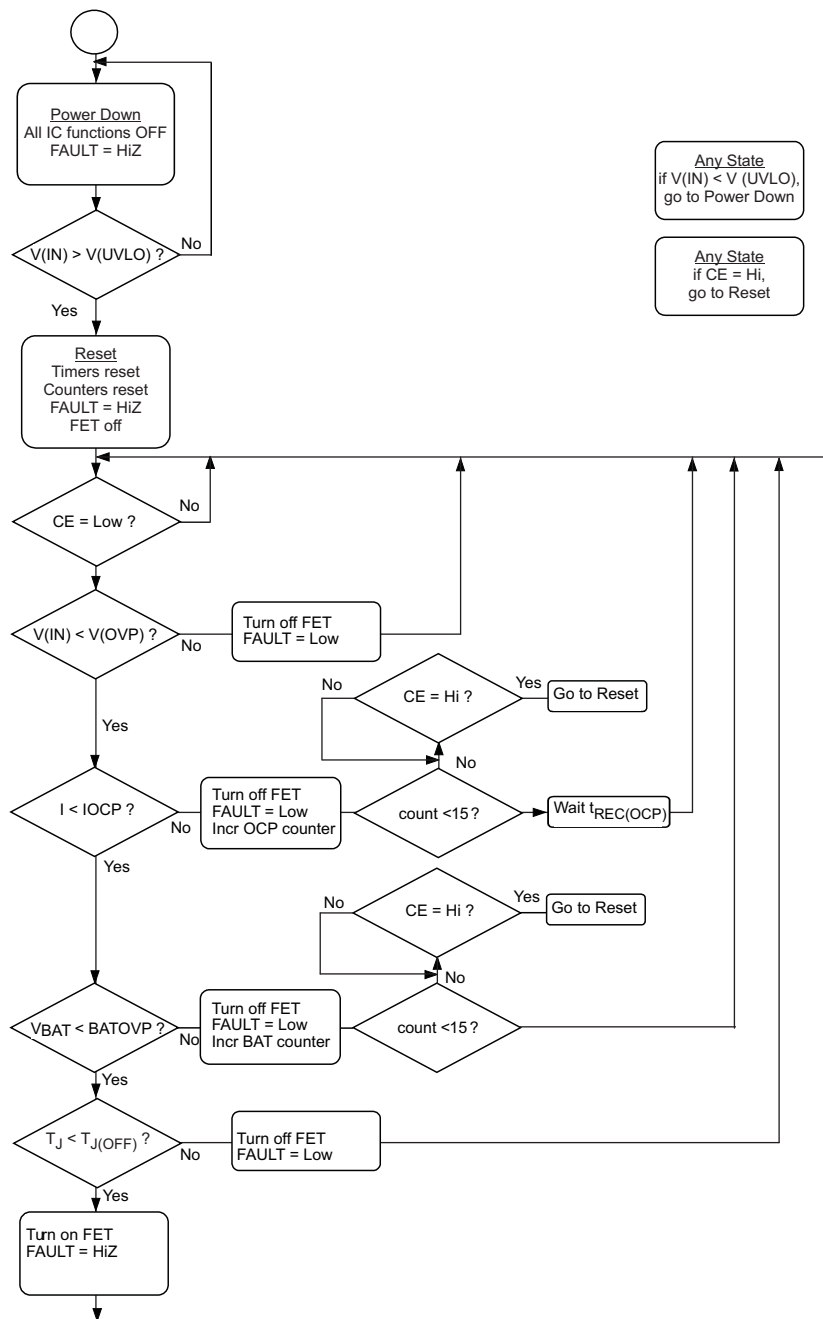


Figure 10. Flow Diagram

## 9 Application and Implementation

### NOTE

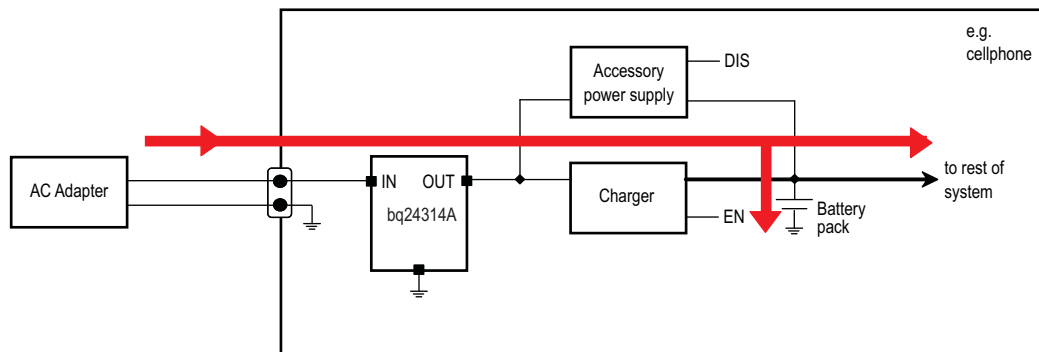
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

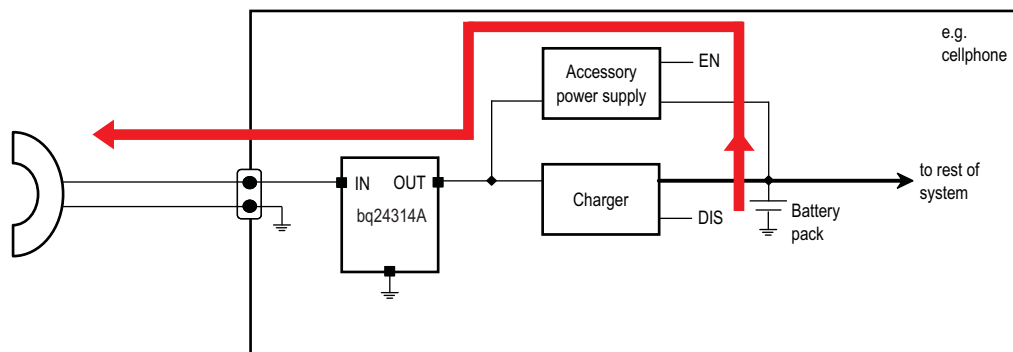
The bq24314A device protects against overvoltage, overcurrent, and battery overvoltage events that occur due to a faulty adapter or other input sources. If any of these faults occur, the bq24314A device isolates the downstream devices from the input source and alerts the host controller with the FAULT open-drain output.

#### 9.1.1 Powering Accessories

In some applications, the equipment that the protection IC resides in may be required to provide power to an accessory (for example, a cellphone may power a headset or an external memory card) through the same connector pins that are used by the adapter for charging. Figure 11 and Figure 12 illustrate typical charging and accessory-powering scenarios:



**Figure 11. Charging - Red Arrows Show Direction of Current Flow**



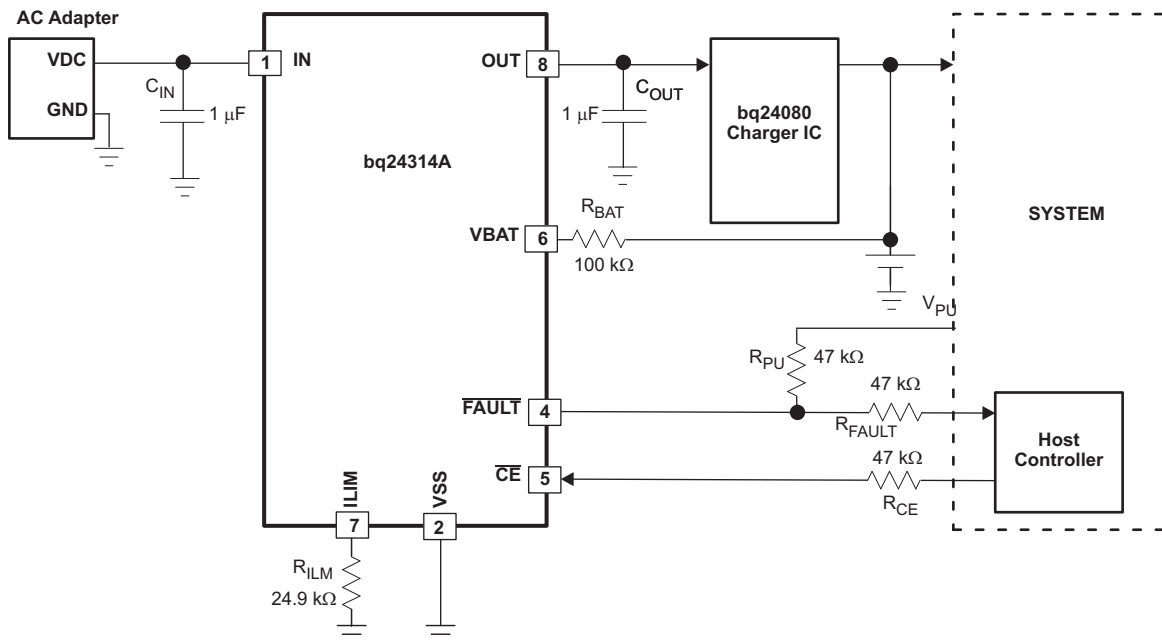
**Figure 12. Powering an Accessory - Red Arrows Show Direction of Current Flow**

In the second case, when power is being delivered to an accessory, the bq24314A device is required to support current flow from the OUT pin to the IN pin.

If  $V_{OUT} > UVLO + 0.7 \text{ V}$ , FET Q1 is turned on, and the reverse current does not flow through the diode but through Q1. Q1 will then remain ON as long as  $V_{OUT} > UVLO - V_{hys(UVLO)} + R_{DS(on)} \times I_{ACCESSORY}$ . Within this voltage range, the reverse current capability is the same as the forward capability, 1.5 A. It should be noted that there is no overcurrent protection in this direction.

## 9.2 Typical Application

The typical values for an application are  $V_{OVP} = 6.8\text{ V}$ ,  $I_{OCP} = 1000\text{ mA}$ , and  $BV_{OVP} = 4.35\text{ V}$ .



Terminal numbers shown are for the 2 x 2 DSG package.

Figure 13. Typical Application Circuit

### 9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Supply Voltage	5 V
INILIM	1 A

### 9.2.2 Detailed Design Procedure

#### 9.2.2.1 Selection of $R_{BAT}$

It is strongly recommended that the battery not be tied directly to the VBAT pin of the device, as under some failure modes of the device, the voltage at the IN pin may appear on the VBAT pin. This voltage can be as high as 30 V, and applying 30 V to the battery in case of the failure of the bq24314A device can be hazardous. Connecting the VBAT pin through  $R_{BAT}$  prevents a large current from flowing into the battery in case of a failure of the device. In the interests of safety,  $R_{BAT}$  should have a very high value. The problem with a large  $R_{BAT}$  is that the voltage drop across this resistor because of the VBAT bias current  $I_{VBAT}$  causes an error in the  $BV_{OVP}$  threshold. This error is over and above the tolerance on the nominal 4.35 V  $BV_{OVP}$  threshold.

Choosing  $R_{BAT}$  in the range from 100 kΩ to 470 kΩ is a good compromise. In the case of a device failure, with  $R_{BAT}$  equal to 100 kΩ, the maximum current flowing into the battery would be  $(30\text{ V} - 3\text{ V}) \div 100\text{ k}\Omega = 246\text{ }\mu\text{A}$ , which is low enough to be absorbed by the bias currents of the system components.  $R_{BAT}$  equal to 100 kΩ would result in a worst-case voltage drop of  $R_{BAT} \times I_{VBAT} = 1\text{ mV}$ . This is negligible to compared to the internal tolerance of 50 mV on  $BV_{OVP}$  threshold.

If the Bat-OVP function is not required, the VBAT pin should be connected to VSS.

### 9.2.2.2 Selection of $R_{CE}$ , $R_{FAULT}$ , and $R_{PU}$

The  $\overline{CE}$  pin can be used to enable and disable the IC. If host control is not required, the  $\overline{CE}$  pin can be tied to ground or left unconnected, permanently enabling the device.

In applications where external control is required, the  $\overline{CE}$  pin can be controlled by a host processor. As in the case of the VBAT pin (see above), the  $\overline{CE}$  pin should be connected to the host GPIO pin through as large a resistor as possible. The limitation on the resistor value is that the minimum  $V_{OH}$  of the host GPIO pin less the drop across the resistor should be greater than  $V_{IH}$  of the bq24314A device's  $\overline{CE}$  pin. The drop across the resistor is given by  $R_{CE} \times I_{IH}$ .

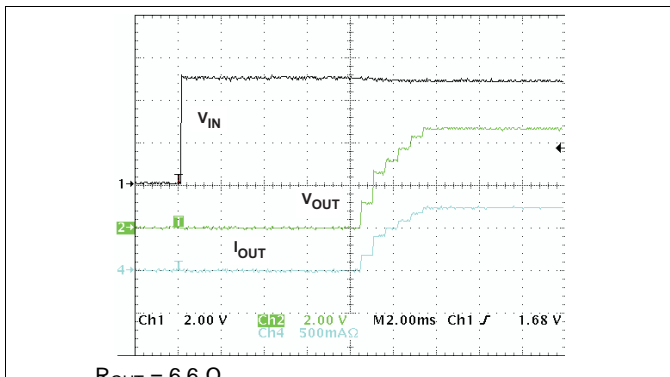
The FAULT pin is an open-drain output that goes low during OV, OC, battery-OV, and OT events. If the application does not require monitoring of the FAULT pin, it can be left unconnected. But if the FAULT pin has to be monitored, it should be pulled high externally through  $R_{PU}$ , and connected to the host through  $R_{FAULT}$ .  $R_{FAULT}$  prevents damage to the host controller if the bq24314A device fails (see above). The resistors should be of high value, in practice values between 22 k $\Omega$  and 100 k $\Omega$  should be sufficient.

### 9.2.2.3 Selection of Input and Output Bypass Capacitors

The input capacitor  $C_{IN}$  in Figure 13 is for decoupling, and serves an important purpose. Whenever there is a step change downwards in the system load current, the inductance of the input cable causes the input voltage to spike up.  $C_{IN}$  prevents the input voltage from overshooting to dangerous levels. It is strongly recommended that a ceramic capacitor of at least 1  $\mu$ F be used at the input of the device. It should be located in close proximity to the IN pin.

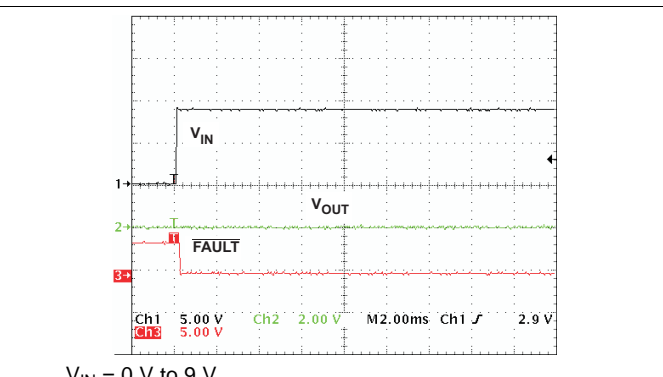
$C_{OUT}$  in Figure 13 is also important: If a very fast (< 1  $\mu$ s rise time) overvoltage transient occurs at the input, the current that charges  $C_{OUT}$  causes the device's current-limiting loop to kick in, reducing the gate-drive to FET Q1. This results in improved performance for input overvoltage protection.  $C_{OUT}$  should also be a ceramic capacitor of at least 1  $\mu$ F, located close to the OUT pin.  $C_{OUT}$  also serves as the input decoupling capacitor for the charging circuit downstream of the protection IC.

9.2.3 Application Curves



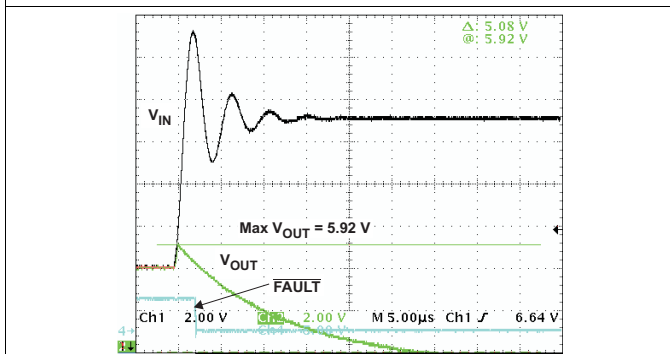
$R_{OUT} = 6.6 \Omega$

Figure 14. Normal Power-On Showing Soft-Start



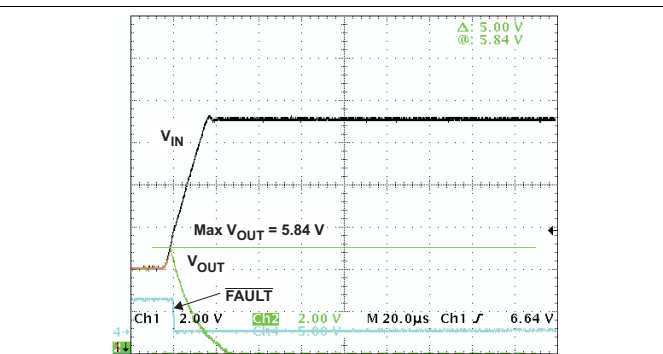
$V_{IN} = 0 \text{ V to } 9 \text{ V}$   
 $t_r = 50 \mu\text{s}$

Figure 15. OVP at Power-On



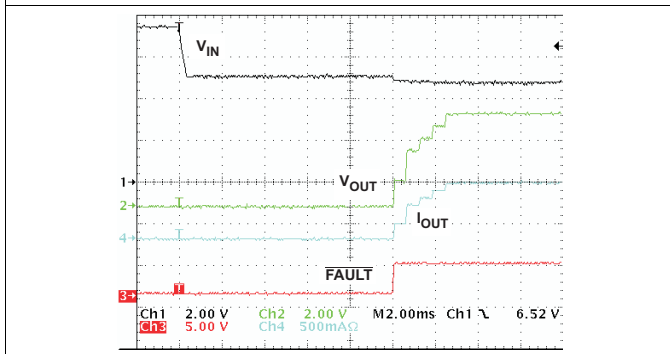
$V_{IN} = 5 \text{ V to } 12 \text{ V}$   
 $t_r = 1 \mu\text{s}$

Figure 16. OVP Response for Input Step



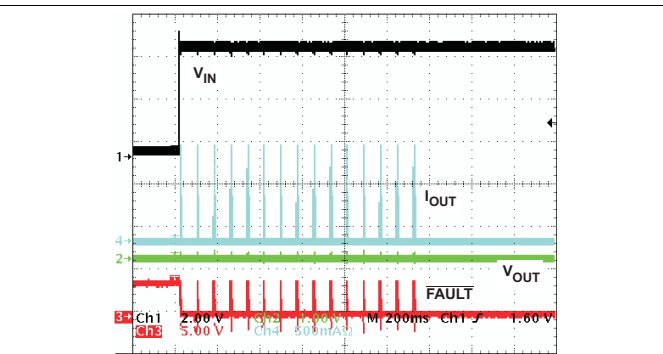
$V_{IN} = 5 \text{ V to } 12 \text{ V}$   
 $t_r = 20 \mu\text{s}$

Figure 17. OVP Response for Input Step



$V_{IN} = 7.5 \text{ V to } 5 \text{ V}$   
 $t_r = 400 \mu\text{s}$

Figure 18. Recovery from OVP



OCP Counter Counts to 15 Before Switching OFF the Device

Figure 19. Powering Up into a Short Circuit on OUT Pin

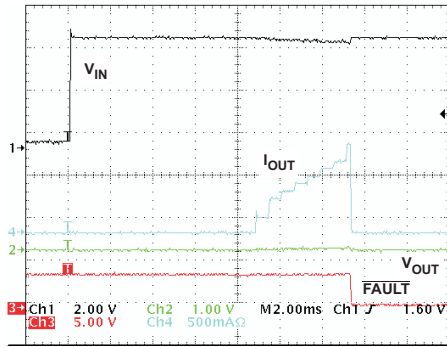
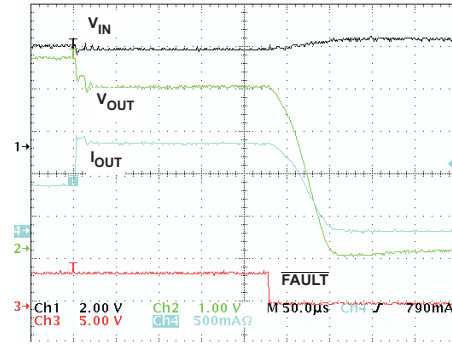
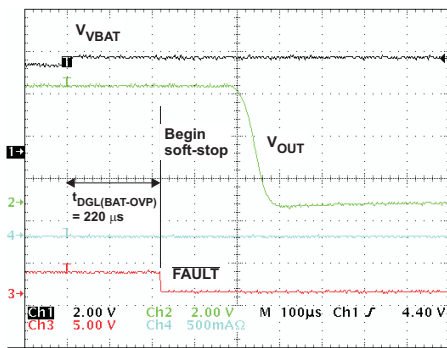


Figure 20. OCP, Zoom-in on First Cycle of Figure 19



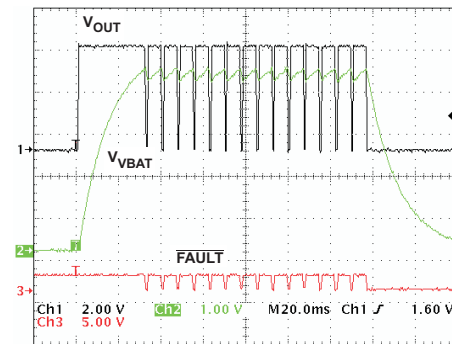
R<sub>OUT</sub> Switches from 6.6 Ω to 3.3 Ω

Figure 21. OCP, Current Limiting and Soft-Stop



V<sub>BAT</sub> Steps from 4.2 V to 4.4 V

Figure 22. BAT-OVP, t<sub>DGL(BAT-OVP)</sub> and Soft-Stop



V<sub>BAT</sub> Cycles Between 4.1 V and 4.4 V

Figure 23. BAT-OVP, BAT-OVP Counter



## 10 Power Supply Recommendations

The intention is for the bq24314A device to operate with 5-V adapters with a maximum current rating of 1.5 A. The device operates from sources from 3 V to 5.7 V. Outside of this range, the output is disconnected due to either UVLO or the OVP function.

## 11 Layout

### 11.1 Layout Guidelines

- This device is a protection device, and is meant to protect down-stream circuitry from hazardous voltages. Potentially, high voltages may be applied to this device. It has to be ensured that the edge-to-edge clearances of PCB traces satisfy the design rules for high voltages. See [Figure 24](#).
- The device uses WSON packages with a thermal pad. For good thermal performance, the thermal pad must be thermally coupled with the PCB ground plane (GND). This requires a copper pad directly under the device. This copper pad must be connected to the ground plane with an array of thermal vias.
- Ensure that external  $C_{IN}$  and  $C_{OUT}$  are located close to the device. Other external components like  $R_{ILIM}$  and  $R_{BAT}$  must also be located close to the device. See [Figure 13](#) for additional information.

### 11.2 Layout Example

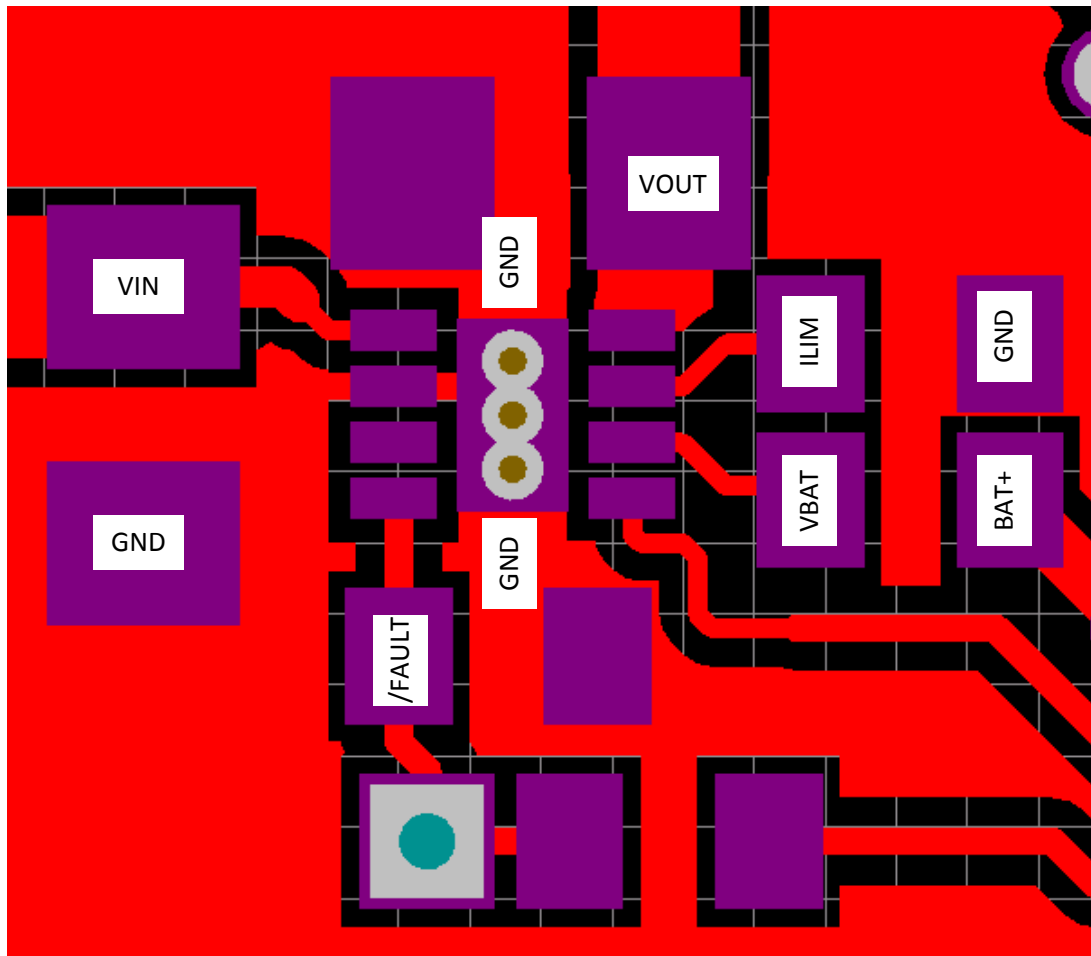


Figure 24. Layout Example

## 12 Device and Documentation Support

### 12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.2 Trademarks

E2E is a trademark of Texas Instruments.

Bluetooth is a trademark of Bluetooth SIG, Inc.

All other trademarks are the property of their respective owners.

### 12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24314ADSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CGG	<a href="#">Samples</a>
BQ24314ADSGRG4	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CGG	<a href="#">Samples</a>
BQ24314ADSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CGG	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

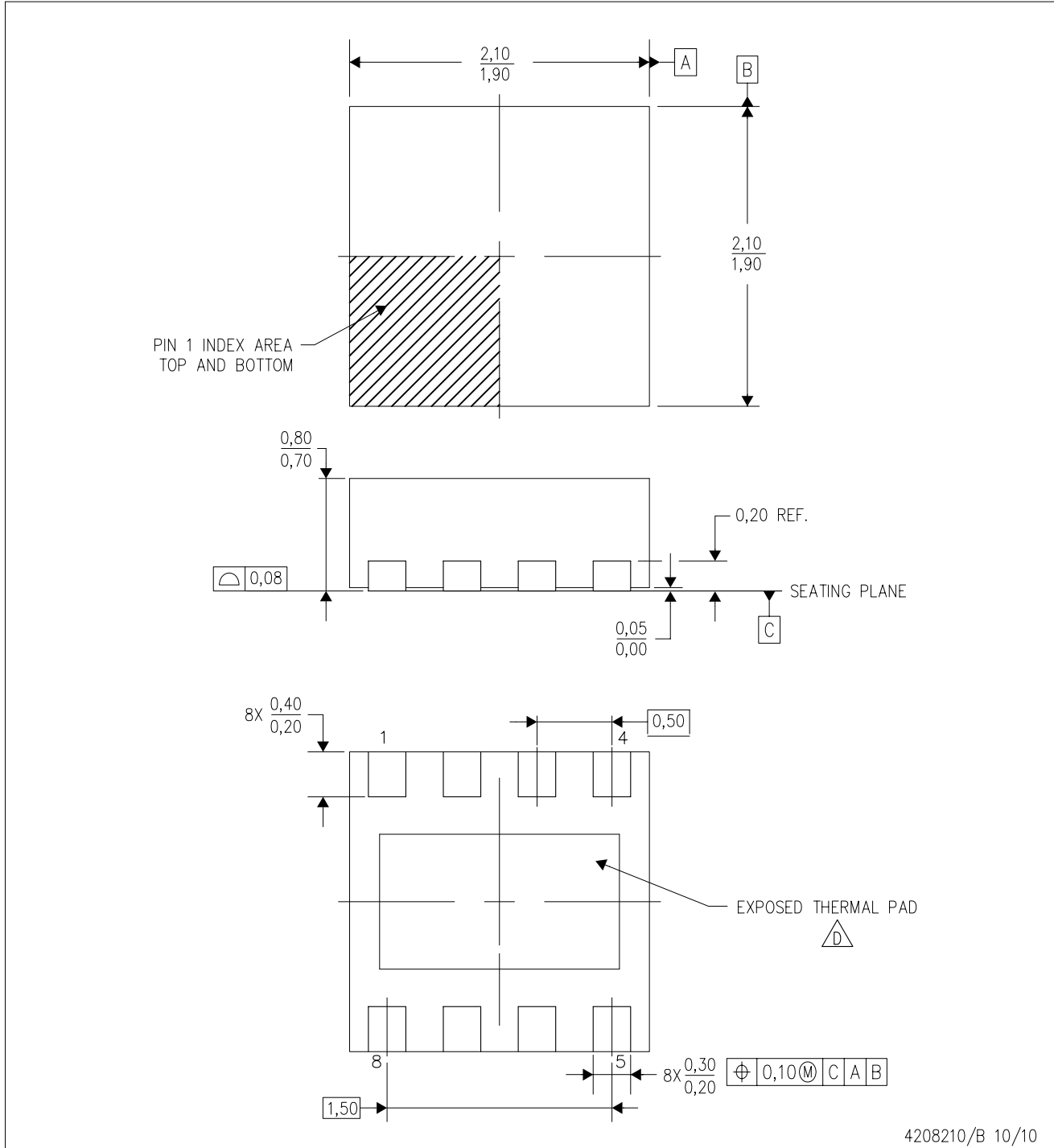
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DSG (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



4208210/B 10/10

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-Leads (QFN) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Falls within JEDEC MO-229.

## THERMAL PAD MECHANICAL DATA

DSG (S-PWSON-N8)

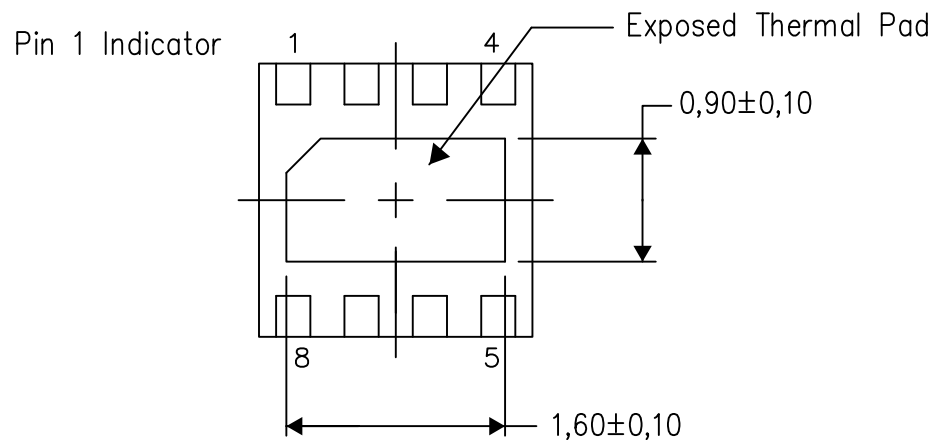
PLASTIC SMALL OUTLINE NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

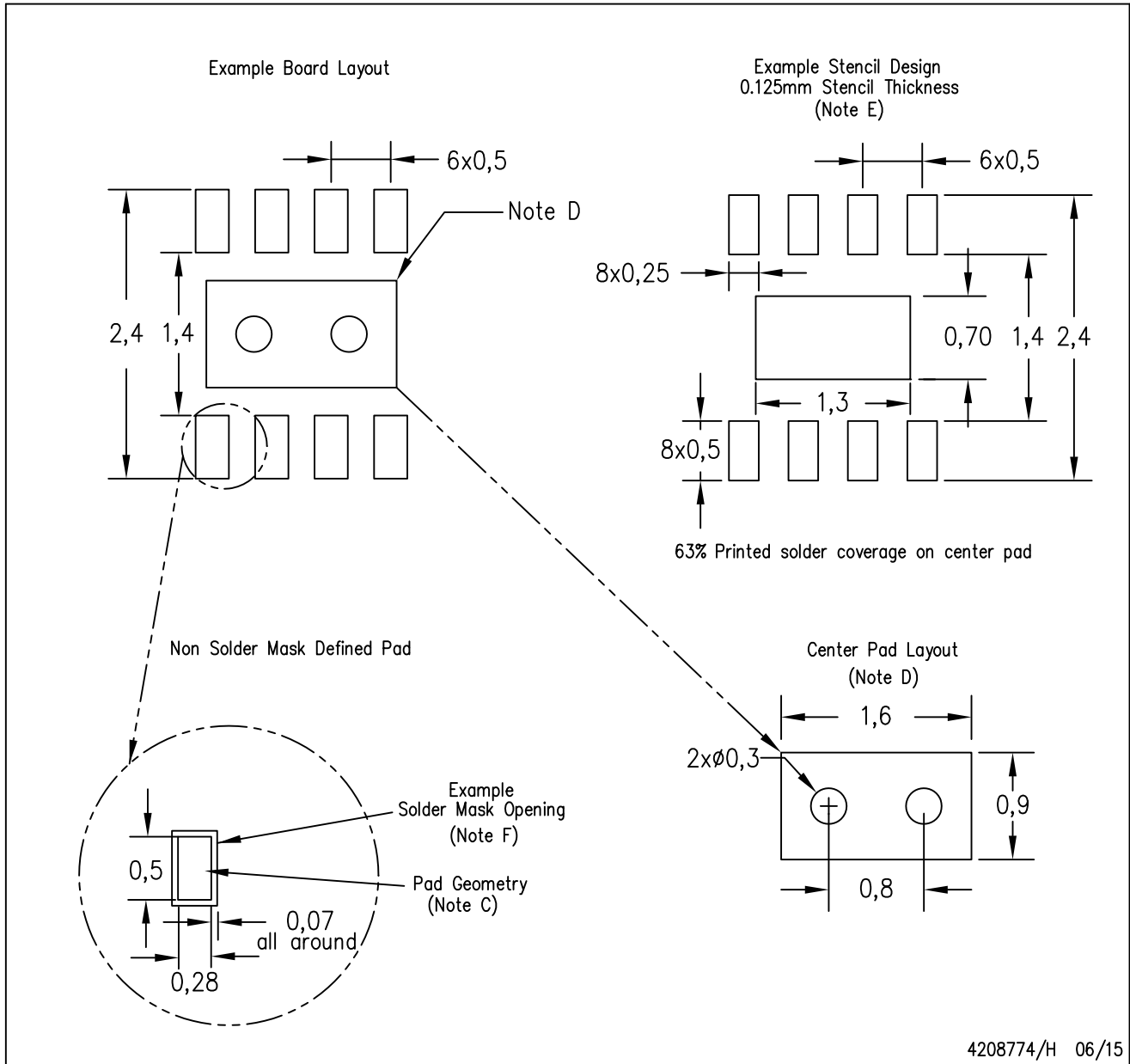


Bottom View

Exposed Thermal Pad Dimensions

4208347/1 06/15

NOTE: All linear dimensions are in millimeters



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for solder mask tolerances.

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