DATA SHEET

数据手册

GM8914

DC 平衡双向控制解串器

2016.9

成都振芯科技股份有限公司

DC 平衡双向控制解串器 GM8914

GM8914 **版本记录：2.0** **当前版本时间：2016 年 9 月**		
新旧版本改动比较：		
旧版 文档页数	**当前版本 文档页数**	**主题（和旧版本相比的主要变化）**
1	**1**	**数据率修改为 2.1Gbps**
7	**7**	**删除 12bit 模式,**

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DC 平衡双向控制解串器 GM8914

1 概述

GM8914 型 DC 平衡双向控制解串器，其主要功能是实现将 2.1Gbps 高速串行数据转换成 10 位并行控制信号，并同步输出一路时钟信号；同时低速通道将芯片控制信息调制到高速差分信号上传输给前级驱动器模块的功能。芯片内部集成终端电阻，可通过外部 I/0 或 I^2C 总线进行配置，支持 power down 模式。芯片 core 电源 V_{DDn} 为 1.8V，I/O 电源 V_{DDIO} 可支持 3.3V 和 1.8V 两种电压。

该芯片的主要应用领域是汽车 Advanced Driver Assistance Systems (ADAS)中 ECU(电子控制单元)视频处理器与防碰撞系统前端摄像机、后视镜摄像机和停车系统成像仪模块之间的无缝、独立双向、低时延通讯。

2 特征

a） 工作温度范围：-40℃～105℃；
b） 电源电压 V_{DDn}：1.8V；
c） 电源电压 V_{DDIO}：3.3V 或 1.8V；
d） 封装形式：QFN48；
e） 器件等级：工业级。

3 封装及引脚功能说明

本器件采用 48 引线的方形扁平无引脚封装（QFN48），引脚排序如下所示。

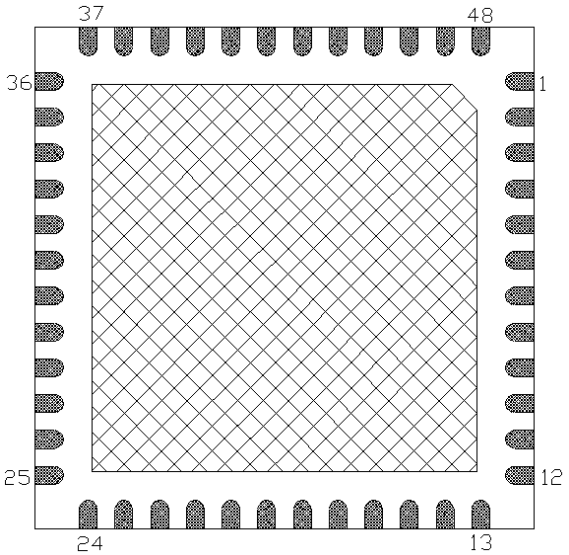


图 1 GM8914 引脚排布图

该芯片的各引脚功能描述见表 1：

表 1 芯片引脚功能说明

管脚名	序号	类型	描述
LVCMOS 并行接口			
ROUT[11:0]	11,12, 13,14, 15, 16,18, 19,21,22,23,24	0, LVCMOS	并行数据输出端
HSYNC	10	0, LVCMOS	Horizontal Sync 数据输出端

管脚名	序号	类型	描述
VSYNC	9	O, LVCMOS	Vertical Sync 数据输出端
RCLK	8	O, LVCMOS	Pixel Clock 数据输出端，时钟采样沿有 RFB 寄存器控制
LVCMOS 并行接口			
LOCK	32	O, LVCMOS	锁定状态输出端。LOCK = 1, PLL 锁定，输出有效数据；LOCK = 0, PLL 未锁定,输出并行数据状态受 OSS_SEL 控制。可作为测试点监测锁定状态，不用时请悬空。
PASS	42	O, LVCMOS	BIST 模式状态输出端，PASS = 1, 传输无误码；PASS = 0,传输至少有一个误码。可作为测试点监测连接状态，不用时请悬空。
通用双向接口			
GPIO[3:0]	25,26,27,28	I/O, LVCMOS	通用输入输出双向端口，可由寄存器配置成输入或输出端口。
双向控制总线 I^2C			
SCL	2	I/O，开漏输出	双向控制总线时钟端口，需要外接上拉电阻到 VDDIO。
SDA	1	I/O，开漏输出	双向控制总线数据端口，需要外接上拉电阻到 VDDIO。
MODE	37	I，LVCMOS	芯片模块控制端，通过电阻分压实现芯片模式控制。
IDX[0:1]	35,34	I，模拟输入	芯片地址指定端口。
控制端口			
PDB	30	I，LVCMOS	芯片关断模式控制端口，PDB = H, 芯片正常工作； PDB =L, 芯片进入 power down 模式。
LOCK	48	O，LVCMOS	锁定状态输出，LOCK = H, 芯片正常锁定； LOCK =L, 芯片失锁。
BISTEN	6	I，LVCMOS	BIST 测试模式控制输入。BISTEN = H,自测试模式； BISTEN =L, 正常传输模式。
PASS	47	O，LVCMOS	BIST 模式输出状态。PASS=H,BIST 模式无误码；PASS=L,BIST 模式至少存在一个误码。
OEN	5	I，LVCMOS	输出使能控制输入。
OSS_SEL	4	I，LVCMOS	输出休眠状态控制输入。
SEL	46	I，LVCMOS	差分输入通道选择,SEL=L,选择 RIN0±作为差分输入通道;SEL=H,选择 RIN1±作为差分输入通道。
FPD-LINK III 接口			
RIN0+	41	I/O，CML	差分输入正端，双向控制通道正端，该端必须采用 100nF 交流耦合电容设计。
RIN0-	42	I/O，CML	差分输入负端，双向控制通道负端，该端必须采用 100nF 交流耦合电容设计。
RIN1+	32	I/O，CML	差分输入正端，双向控制通道正端，该端必须采用 100nF 交流耦合电容设计。
RIN1-	33	I/O，CML	差分输入负端，双向控制通道负端，该端必须采用 100nF 交流耦合电容设计。
RES	43，44	/	保留管脚。
CMLOUTP/N	38,39	/	测试 pin。

管脚名	序号	类型	描述
电源和地 VDD (VDDn and VDDIO)电源上电时间必须要小于 1.5ms，如果慢于 1.5ms 就需要在 PDB 管脚增加到地的滤波电容，保证在电源上电完成后，再使能芯片。输入并行数据摆幅必须配合 VDDIO 电源进行同步设计，两者保持一致。			
VDDIO1/2/3	29,20,7	电源	LVCMOS I/O 电源，可接 1.8V±5%或 3.3V±10%。
VDDD	17	电源	数字电源，1.8V±5%
VDDSSCG	3	电源	SSCG 电源，1.8V±5%
VDDR	36	电源	RX 电源，1.8V±5%
VDDCML0/1	40，31	电源	CML 电源，1.8V±5%
VDDPLL	45	电源	PLL 电源，1.8V±5%
VSS	DAP	Ground	DAP 为芯片 GND 端，在芯片背面，PCB 设计上 DAP 连接至少需设计 16 个以上 GND 通孔，保证芯片有很好的地接触。

4 功能描述

功能框图按图 3 规定。器件主要实现将 2.1Gbps 高速串行数据转换成 10 位并行控制信号，并同步输出一路时钟信号；同时低速通道将芯片控制信息调制到高速差分信号上传输给前级驱动器模块的功能。并由接收器、驱动器、时钟与数据恢复、判决反馈均衡器、判决反馈均衡器数字算法控制、数字选择及状态控制、锁相环、数据解码和输出锁存模块组成。

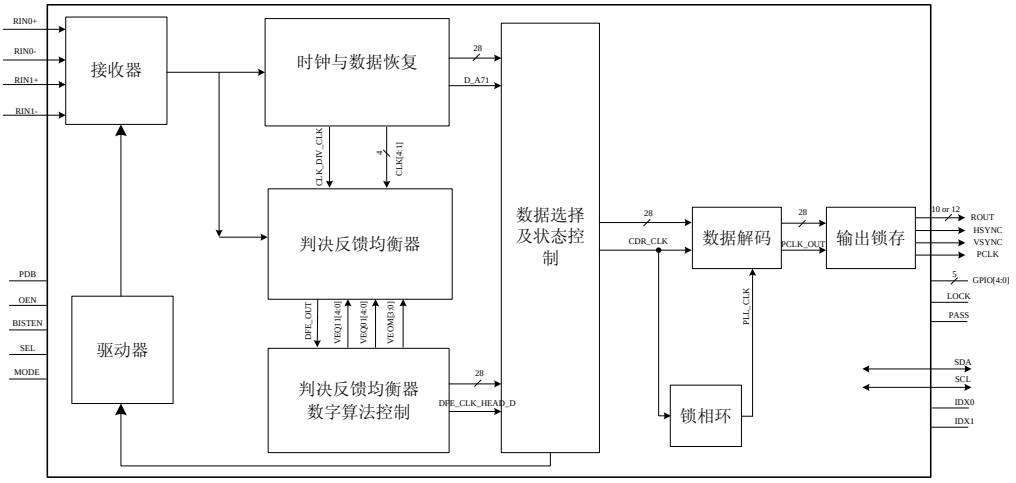


图 2 GM8914 功能框图

5 参数指标

5.1 极限工作条件

电源电压（V_{DDD}、V_{DDSSCG}、V_{DDR}、V_{DDPLL}、$V_{DDCML0/1}$）：-0.3V～2V

电源电压（$V_{DDIO1/2/3}$）：-0.3V～3.6V；

结温（T_j）：150℃；

引线耐焊接温度（T_h）（4s）：260℃；

功耗（P_D）：0.9W；

热阻（$R_{\theta Jc}$）：27℃/W；

贮存环境温度（T_{stg}）：-65℃～150℃；

静电放电敏感度（V_{ESD}）：2000V。

5.2 推荐工作条件

电源电压（V_{DDD}、V_{DDSSCG}、V_{DDR}、V_{DDPLL}、$V_{DDCML0/1}$）：1.8V±0.09V；

电源电压（$V_{DDIO1/2/3}$）：3.3V±0.3V、1.8V±0.09V；

输入时钟频率（f_{TCLK}）：25MHz~150MHz；

电源噪声电压（V_{noise}）：≤50mV；

工作温度（T_A）：-40℃～105℃。

5.3 静态参数

表 2 静态参数表

特 性	符号	条 件：除另有规定外，-40℃≤T_A≤105℃，$V_{DDIO1/2/3}$=3.3V，V_{DDD}=V_{DDSSCG}=V_{DDR}=V_{DDPLL}=$V_{DDCML0/1}$=1.8V	极限值 最小	极限值 最大	单位
TTL 输入高电平电压	V_{IH}	$V_{DDIO1/2/3}$=3.3V	2.0	—	V
		$V_{DDIO1/2/3}$=1.8V	1.17	—	V
TTL 输入低电平电压	V_{IL}	$V_{DDIO1/2/3}$=3.3V	-	0.8	V
		$V_{DDIO1/2/3}$=1.8V	—	0.63	V
TTL 输入电流	I_{IN}	$V_{DDIO1/2/3}$=3.6V，V_{IN}=0 或 $V_{DDIO1/2/3}$	—	±20	μA
TTL 输出高电平电压	V_{OH}	I_{OH}=-4mA，$V_{DDIO1/2/3}$=3.3V	2.4	—	V
		I_{OH}=-4mA，$V_{DDIO1/2/3}$=1.8V	1.35	—	V
TTL 输出低电平电压	V_{OL}	I_{OL}=4mA，$V_{DDIO1/2/3}$=3.3V	—	0.45	V
		I_{OL}=4mA，$V_{DDIO1/2/3}$=1.8V	—	0.40	V
TTL 输出关断电流	I_{OZ}	$V_{DDIO1/2/3}$=3.6V，V_{out}=0 或 $V_{DDIO1/2/3}$	—	±20	μA
TTL 输出短路电流大小	$\|I_{OS}\|$	$V_{DDIO1/2/3}$=3.6V，V_{out}=0 或 $V_{DDIO1/2/3}$	—	180	mA
差分终结电阻	R_T	—	80	120	Ω

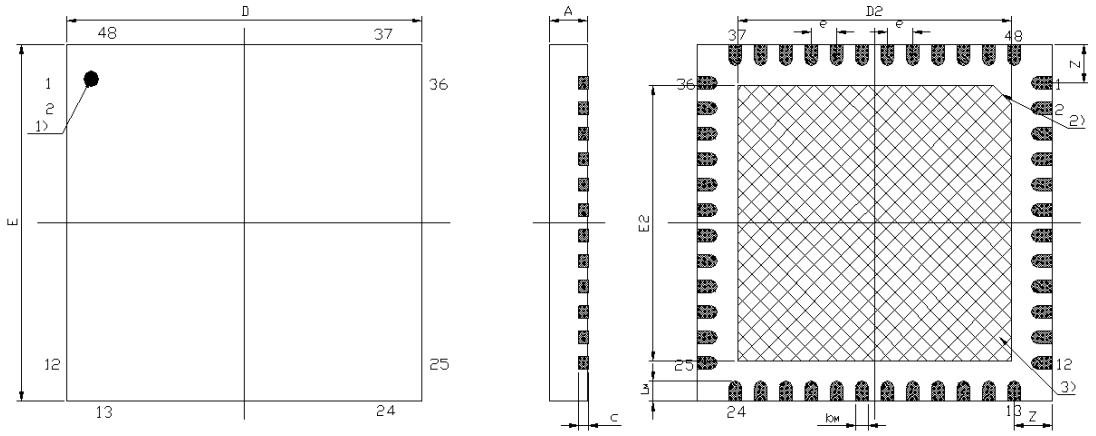
5.4 动态参数

表 3 动态参数表

特 性	符号	条 件：除另有规定外，-40℃≤T_A≤105℃，$V_{DDIO1/2/3}$=3.3V，V_{DDD}=V_{DDSSCG}=V_{DDR}=V_{DDPLL}=$V_{DDCML0/1}$=1.8V	极限值 最小	极限值 最大	单位
电源电流	I_{DD}	WORST CASE 数据输入	—	300	mA
最大串行数据率	S_D	f_{CLK}=150MHz（数据率为 2.1Gbps）	2.1	—	Gbps
TTL 输出数据上升时间	t_R		—	4	ns
TTL 输出数据下降时间	t_F		—	4	ns

6 机械尺寸

本器件采用 48 引线的方形扁平无引脚封装（QFN48）。外形尺寸按图 3 的规定。



注 1：顶视图 1 脚标示；

注 2：底视图 1 脚标示；

注 3：DAP 热沉地脚标示；

图 3 GM8914 尺寸图

具体的尺寸见下表：

表 4 外形尺寸参数 单位：mm

尺寸符号	数 值		
	最 小	公 称	最 大
A	0.70	—	0.80
b_M	0.18	—	0.30
L_M	0.35	—	0.45
c	0.18	—	0.23
e	—	0.50	—
D	—	—	7.10
E	—	—	7.10
Z	—	—	0.75
D_2	—	—	5.50
E_2	—	—	5.50

7 产品应用信息

7.1 典型应用图

GM8914 主要是跟 GM8913 配对应用于车载系统的主要应用于汽车 Advanced Driver Assistance Systems (ADAS)中 ECU(电子控制单元)视频处理器与防碰撞系统前端摄像机、后视镜摄像机和停车系统成像仪系统。

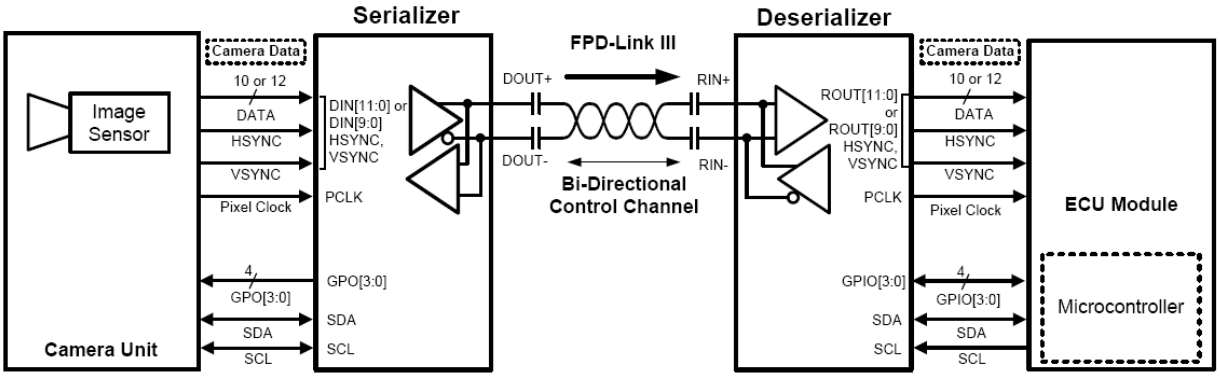


图 4 GM8914 应用图

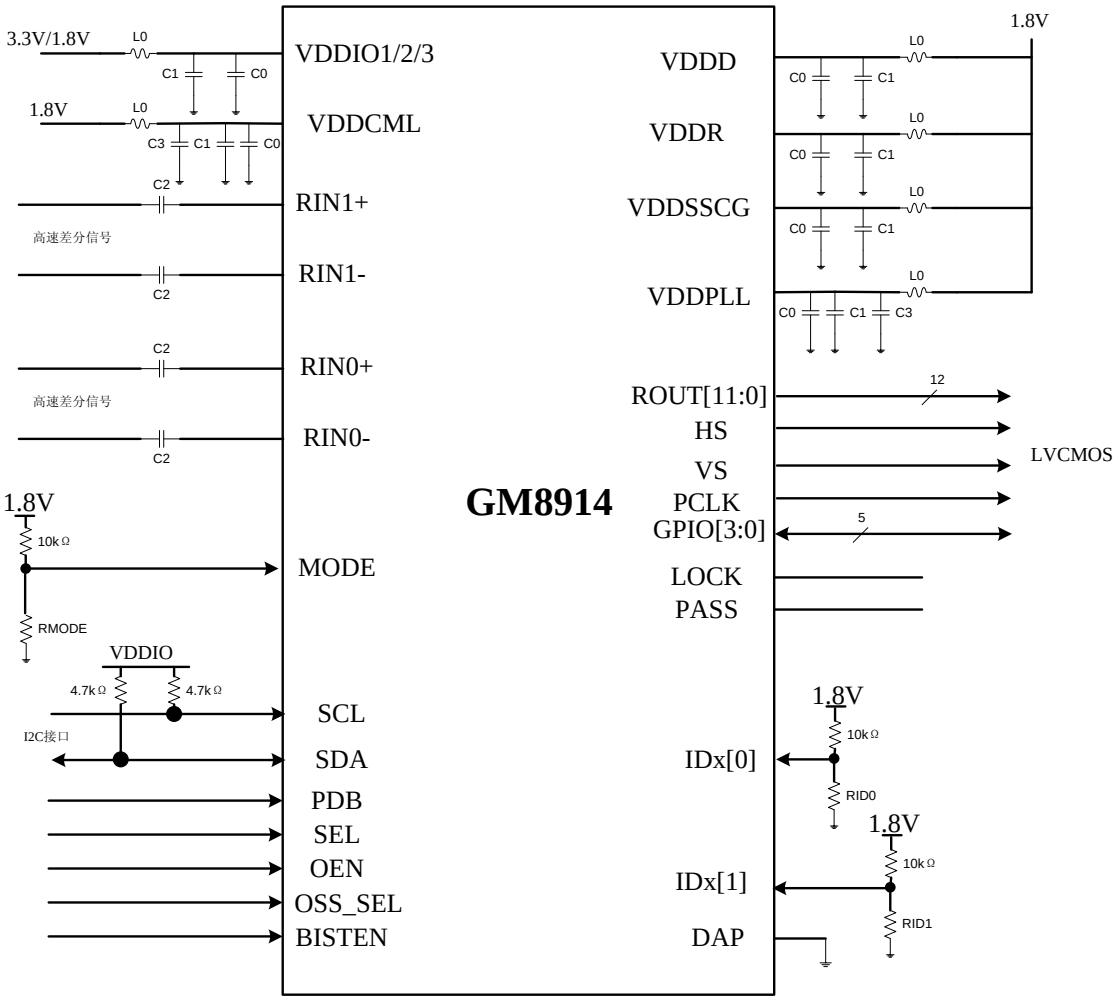


图 5 GM8914 推荐设计图

上图为 GM8906 典型应用中的连接图，其外围无源器件推荐值：电容 C0=0.1μF、C1=0.01μF、C2=0.1μF、C3=4.7μF；磁珠 L1=1KΩ /100MHz。IDX[1:0]和 RMODE 阻值配置详见配置表。

表 5 IDx[0]和 IDx[1]地址配置表

RID1(kΩ)误差 1%	RID0(kΩ) 误差 1%	地址(7'b)	地址(8'b)
0	0	0x60	0xC0
0	3	0x61	0xC2
0	11	0x62	0xC4
0	100	0x63	0xC6
3	0	0x64	0xC8
3	3	0x65	0xCA
3	11	0x66	0xCC
3	100	0x67	0xCE
11	0	0x68	0xD0
11	3	0x69	0xD2
11	11	0x6A	0xD4
11	100	0x6B	0xD6
100	0	0x6C	0xD8
100	3	0x6D	0xDA
100	11	0x6E	0xDC
100	100	0x6F	0xDE

表 6 RMODE 模式配置表

RMODE(Ω)误差 1%	MODE 模式
11K	10bit 模式，50MHz ~150MHz 像素时钟

表 7 输出状态控制表

输入				输出			
串行输入	PDB	OEN	OSS	LOCK	PASS	DATA，GPIO，I2S	CLK
X	L	X	X	Z	Z	Z	Z
X	H	L	L	L or H	L	L	L
X	H	L	H	L or H	Z	Z	Z
静态	H	H	L	L	L	L	L
静态	H	H	H	H	前一状态	L	L
动态	H	H	L	H	L	L	L
动态	H	H	H	H	有效输出	有效输出	有效输出

内部寄存器配置如下表所示。

表 8 寄存器配置

0x00	I2C Device ID	7:1	DEVICE ID	RW	0xC0'h (1100_000)	7-bit address of Deserializer; 0x60'h. (0110_000x'b) default
		0	Deserializer ID Select	RW		0: De-Serializer Device ID is set using address coming from CAD. 1: Register I2C Device ID overrides ID[x].
0x01	Reset	7:6	RSVD			Reserved.
		5	ANAPWDN	RW	0	This register can be set only through local I2C access. 1: Analog power-down : Powers Down the analog block in the Serializer. 0: No effect.
		4:2	RSVD			Reserved.
		1	Digital Reset 1	RW	0	Digital Reset Resets the entire digital block except registers. This bit is self-clearing. 1: Reset. 0: No effect.
		0	Digital Reset 0	RW	0	Digital Reset Resets the entire digital block including registers. This bit is self-clearing. 1: Reset. 0: No effect.
0x02	General Configuration 0	7	RSVD			Reserved.
		6	RSVD			Reserved.
		5	Auto-Clock	RW	0	1: Output PCLK or OSC clock when not LOCKED. 0: Only PCLK.
		4	RSVD	RW	0	Reserved.
		3:0	RSVD			Reserved.
0x03	General Configuration 1	7	RX Parity Checker Enable	RW	1	Forward Channel Parity Checker Enable. 1: Enable. 0: Disable.
		6	TX CRC Checker Enable	RW	1	Back Channel CRC Generator Enable. 1: Enable. 0: Disable.
		5	VDDIO Control	RW	1	Auto voltage control. 1: Enable (auto detect mode). 0: Disable.
		4	VDDIO Mode	RW	0	VDDIO voltage set. 1: 3.3V 0: 1.8V
		3	I2C Pass-Through	RW	1	II2C Pass-Through Mode. 1: Pass-Through Enabled. SER Alias 0x07 and Slave Alias 0x09-0x17. 0: Pass-Through Disabled.

		2	AUTO ACK	RW	0	Automatically Acknowledge I2C Remote Write When enabled, I2C writes to the Deserializer (or any remote I2C Slave, if I2C PASS ALL is enabled) are immediately acknowledged without waiting for the Deserializer to acknowledge the write. The accesses are then remapped to address specified in 0x06. This allows I2C bus without LOCK. 1: Enable. 0: Disable.
		1	Parity Error Reset	RW	0	Parity Error Reset, This bit is self-clearing. 1: Parity Error Reset. 0: No effect.
		0	RRFB	RW	1	Pixel Clock Edge Select. 1: Parallel Interface Data is strobed on the Rising Clock Edge. 0: Parallel Interface Data is strobed on the Falling Clock Edge.
0x04	EQ Feature Control	7:0	EQ level -when AEQ bypass is enabled EQ setting is provided by this register	RW	0x0F	Equalization gain. 0x0F = ~8.0 dB (minimum) 0x0F = ~11.0 dB 0x0F = ~12.5 dB 0x0F = ~14.0 dB 0x0F = ~16.0 dB (maximum)
0x05	**Reserved.**					
0x06	SER ID	7:1	Remote ID	RW	0x0C	Remote Serializer ID.
		0	Freeze Device ID	RW	0	Freeze Serializer Device ID Prevent auto-loading of the Serializer Device ID from the Forward Channel. The ID will be frozen at the value written.
0x07	SER Alias	7:1	Serializer Alias ID	RW	0x00	7-bit Remote Serializer Device Alias ID Configures the decoder for detecting transactions designated for an I2C Serializer device. The transaction will be remapped to the address specified in the SER ID register. A value of 0 in this field disables access to the remote I2C Serializer.
		0	RSVD			Reserved.
0x08	Slave ID[0]	7:1	Slave ID0	RW	0	7-bit Remote Slave Device ID 0 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID0, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RSVD			Reserved.

0x09	Slave ID[1]	7:1	Slave ID1	RW	0	7-bit Remote Slave Device ID 1 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID1, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RSVD			Reserved.
0x0A	Slave ID[2]	7:1	Slave ID2	RW	0x00	7-bit Remote Slave Device ID 2 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID2, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RSVD			Reserved.
0x0B	Slave ID[3]	7:1	Slave ID3	RW	0	7-bit Remote Slave Device ID 3 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID3, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RSVD			Reserved.
0x0C	Slave ID[4]	7:1	Slave ID4	RW	0	7-bit Remote Slave Device ID 4 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID4, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RSVD			Reserved.
0x0D	Slave ID[5]	7:1	Slave ID5	RW	0x00	7-bit Remote Slave Device ID 5 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID5 , the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RSVD			Reserved.

0x0E	Slave ID[6]	7:1	Slave ID6	RW	0	7-bit Remote Slave Device ID 6 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID6, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RSVD			Reserved.
0x0F	Slave ID[7]	7:1	Slave ID7	RW	0x00	7-bit Remote Slave Device ID 7 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID7, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RSVD			Reserved.
0x10	Slave Alias[0]	7:1	Slave Alias ID0	RW	0x00	7-bit Remote Slave Device Alias ID 0 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID0 register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RSVD			Reserved.
0x11	Slave Alias[1]	7:1	Slave Alias ID1	RW	0x00	7-bit Remote Slave Device Alias ID 1 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID1 register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RSVD			Reserved.
0x12	Slave Alias[2]	7:1	Slave Alias ID2	RW	0x00	7-bit Remote Slave Device Alias ID 2 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID2 register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RSVD			Reserved.

0x13	Slave Alias[3]	7:1	Slave Alias ID3	RW	0x00	7-bit Remote Slave Device Alias ID 3 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID3 register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RSVD			Reserved.
0x14	Slave Alias[4]	7:1	Slave Alias ID4	RW	0x00	7-bit Remote Slave Device Alias ID 4 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID4 register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RSVD			Reserved.
0x15	Slave Alias[5]	7:1	Slave Alias ID5	RW	0x00	7-bit Remote Slave Device Alias ID 5 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID5 register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RSVD			Reserved.
0x16	Slave Alias[6]	7:1	Slave Alias ID6	RW	0x00	7-bit Remote Slave Device Alias ID 6 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID6 register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RSVD			Reserved.
0x17	Slave Alias[7]	7:1	Slave Alias ID7	RW	0x00	7-bit Remote Slave Device Alias ID 7 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID7 register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RSVD			Reserved.

0x18	Parity Errors Threshold	7:0	Parity Error Threshold Byte 0	RW	0	Parity errors threshold on the Forward channel during normal information. This sets the maximum number of parity errors that can be counted using register 0x1A. Least significant Byte.
0x19	Parity Errors Threshold	7:0	Parity Error Threshold Byte 1	RW	0	Parity errors threshold on the Forward channel during normal operation. This sets the maximum number of parity errors that can be counted using register 0x1B. Most significant Byte.
0x1A	Parity Errors	7:0	Parity Error Byte 0	RW	0	Number of parity errors in the Forward channel during normal operation. Least significant Byte.
0x1B	Parity Errors	7:0	Parity Error Byte 1	RW	0	Number of parity errors in the Forward channel during normal operation. Most significant Byte.
0x1C	General Status	7:4	Rev-ID	R	0	Revision ID. 0x0000: Production
		3	RSVD			Reserved.
		2	Parity Error	R	0	Parity Error detected. 1: Parity Errors detected. 0: No Parity Errors.
		1	Signal Detect	R	0	1: Serial input detected. 0: Serial input not detected.
		0	Lock	R	0	De-Serializer CDR, PLL's clock to recovered clock frequency. 1: De-Serializer locked to recovered clock. 0: De-Serializer not locked.
0x1D	GPIO[1] and GPIO[0] Config	7	GPIO1 Output Value	RW	0	Local GPIO Output Value This value is the output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output.
		6	RSVD			Reserved.
		5	GPIO1 Direction	RW	1	Local GPIO Direction. 1: Input. 0: Output.
		4	GPIO1 Enable	RW	1	GPIO Function Enable. 1: Enable GPIO operation. 0: Enable normal operation.
		3	GPIO0 Output Value	RW	0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output.
		2	RSVD			Reserved.
		1	GPIO0 Direction	RW	1	Local GPIO Direction. 1: Input. 0: Output.
		0	GPIO0 Enable	RW	1	GPIO Function Enable. 1: Enable GPIO operation. 0: Enable normal operation.

7.2 应用说明

芯片应用中应注意以下几点：

a) 电源必须加滤波电容，推荐采用 0.1uF 和 0.01uF 的电容进行组合滤波，也可根据

实际情况考虑；

b) 信号的输入或输出端串联匹配电阻改善信号质量；
c) 应用过程中，芯片的电源电压、输入电压范围、测试温度以及测试条件等都需要严格遵守数据手册规定；
d) 用于测试和焊接的工作台面，测试仪器以及高低温箱等都必须具有防静电设施；
e) 测试和使用过程中，操作人员也必须带防静电腕带，在防静电台面上进行操作，禁止直接手持芯片；
f) 测试和使用过程中出现异常现象时，应该注意保护芯片。