

数据手册

GM8913

DC 平衡双向控制串行器

2016.9

成都振芯科技股份有限公司

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版本记录: 2.0		当前版本时间: 2016 年 9 月
新旧版本改动比较:		
旧版 文档页数	当前版本 文档页数	主题 (和旧版本相比的主要变化)
1	1	数据率修改为 2.1Gbps
8	8	删除 12bit 模式,

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DC 平衡双向控制串行器

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1 概述

GM8913 型 DC 平衡双向控制串行器，其主要功能是实现将 10 位并行控制信号和一路时钟信号串行为一路 2.1Gbps 高速串行数据；同时接收低速通道信号实现模式配对的功能。芯片内部集成终端电阻，可通过外部 I/O 或 I²C 总线进行配置，支持 power down 模式。芯片 core 电源 V_{DDn} 为 1.8V，I/O 电源 V_{DDIO} 可支持 3.3V 和 1.8V 两种电压。

该芯片的主要应用领域是汽车 Advanced Driver Assistance Systems (ADAS)中 ECU(电子控制单元)视频处理器与防碰撞系统前端摄像机、后视镜摄像机和停车系统成像仪模块之间的无缝、独立双向、低时延通讯。

2 特征

- a) 工作温度范围：-40℃~105℃；
- b) 电源电压 V_{DDn}：1.8V；
- c) 电源电压 V_{DDIO}：3.3V 或 1.8V；
- d) 封装形式：QFN32；
- e) 器件等级：工业级。

3 封装及引脚功能说明

本器件采用 32 引线的方形扁平无引脚封装（QFN32），引脚排序如下所示。

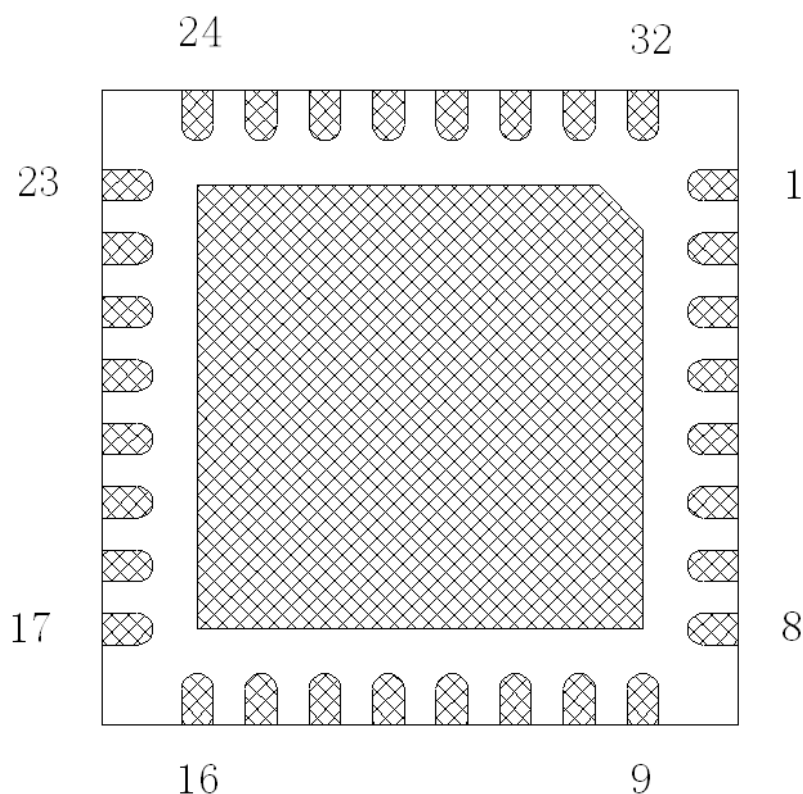


图 1 GM8913 引脚排布图

该芯片的各引脚功能描述见表 1:

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表 1 芯片引脚功能说明

管脚名	序号	类型	描述
LVCMOS 并行接口			
DIN[0:11]	19, 20, 21, 22, 23, 24, 26, 27, 29, 30, 31, 32	I, LVCMOS	并行数据输入端
HSYNC	1	I, LVCMOS	Horizontal Sync 数据输入端
VSYNC	2	I, LVCMOS	Vertical Sync 数据输入端
RCLK	3	I, LVCMOS	Pixel Clock 数据输入端, 时钟采样沿有 TRFB 寄存器控制
通用双向接口			
GPIO[1:0]	16, 15	0, LVCMOS	通用输入输出双向端口, 可由寄存器配置成输入或输出端口。
GPIO[2]/CLKOUT	17	0, LVCMOS	通用输入输出双向端口, 可由寄存器配置成输入或输出端口。在芯片配置成外部环振模式时, 该 pin 作为输出时钟 pin。
GPIO[3]/CLKIN	18	I/0, LVCMOS	通用输入输出双向端口, 可由寄存器配置成输入或输出端口。在芯片配置成外部环振模式时, 该 pin 作为输入时钟 pin。
双向控制总线 I ² C			
SCL	4	I/0, 开漏输出	双向控制总线时钟端口, 需要外接上拉电阻到 VDDIO。
SDA	5	I/0, 开漏输出	双向控制总线数据端口, 需要外接上拉电阻到 VDDIO。
MODE	8	I, LVCMOS	芯片模块控制端, 通过电阻分压实现芯片模式控制。
IDX	6	I, 模拟输入	芯片地址指定端口。
控制端口			
PDB	9	I, LVCMOS	芯片关断模式控制端口, PDB = H, 芯片正常工作; PDB = L, 芯片进入 power down 模式。
RES	7	I, LVCMOS	保留管脚。
FPD-LINK III 接口			
DOUT+	13	I/0, CML	差分输出正端, 双向控制通道正端, 该端必须采用 100nF 交流耦合电容设计。
DOUT-	12	I/0, CML	差分输出负端, 双向控制通道负端, 该端必须采用 100nF 交流耦合电容设计。
电源和地			
VDD (VDDn and VDDIO) 电源上电时间必须要小于 1.5ms, 如果慢于 1.5ms 就需要在 PDB 管脚增加到地的滤波电容, 保证在电源上电完成后, 再使能芯片。输入并行数据摆幅必须配合 VDDIO 电源进行同步设计, 两者保持一致。			
VDDPLL	10	电源	PLL 电源, 1.8V ± 5%
VDDT	11	电源	TX 电源, 1.8V ± 5%
VDDCML	14	电源	CML 电源, 1.8V ± 5%
VDDD	28	电源	数字电源, 1.8V ± 5%
VDDIO	25	电源	I/O 电源, 1.8V ± 5% 或 3.3V ± 10%。

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管脚名	序号	类型	描述
VSS	DAP	Ground	DAP 为芯片 GND 端，在芯片背面，PCB 设计上 DAP 连接至少需设计 9 个以上 GND 通孔，保证芯片有很好的地接触。

4 功能描述

功能框图按图 3 规定。器件主要实现将 10 位并行信号转换为 2.1Gbps 高速串行信号；同时低速通道接收器实现将串行控制信息解串译码的功能。并由接收器、驱动器、时钟与数据恢复、判决反馈均衡器、判决反馈均衡器数字算法控制、数字选择及状态控制、锁相环、数据解码和输出锁存模块组成。

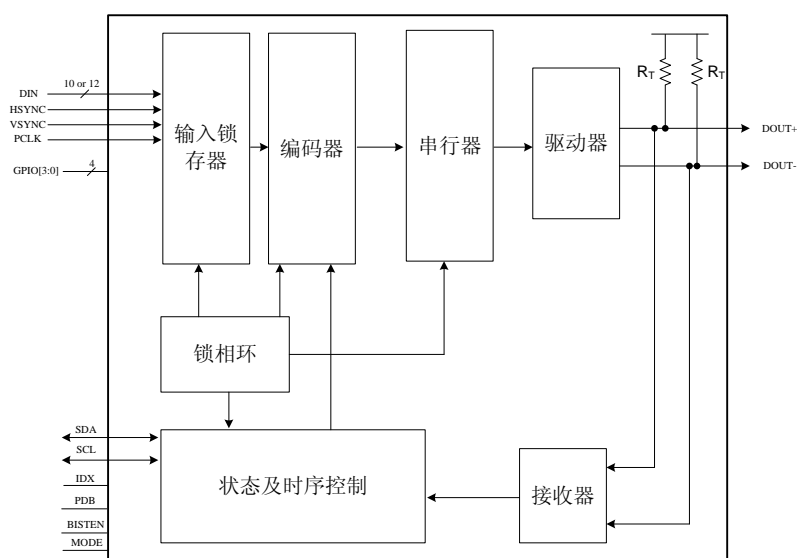


图 2 GM8913 功能框图

5 参数指标

5.1 极限工作条件

电源电压 (V_{DDPLL} , V_{DDT} , V_{DDCML} , V_{DDD}) : $-0.3V \sim 2V$

电源电压 (V_{DDIO}) : $-0.3V \sim 3.6V$;

结温 (T_j) : $150^{\circ}C$;

引线耐焊接温度 (T_h) (4s) : $260^{\circ}C$;

功耗 (P_D) : $0.9W$;

热阻 ($R_{\theta Jc}$) : $27^{\circ}C/W$;

贮存环境温度 (T_{stg}) : $-65^{\circ}C \sim 150^{\circ}C$;

静电放电敏感度 (V_{ESD}) : $2000V$ 。

5.2 推荐工作条件

电源电压 (V_{DDPLL} , V_{DDT} , V_{DDCML} , V_{DDD}) : $1.8V \pm 0.09V$;

电源电压 (V_{DDIO}) : $3.3V \pm 0.3V$ 、 $1.8V \pm 0.09V$;

输入时钟频率 (f_{CLK}) : $25MHz \sim 150MHz$;

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电源噪声电压 (V_{noise}) : $\leq 50\text{mV}$;工作温度 (T_A) : $-40^\circ\text{C} \sim 105^\circ\text{C}$ 。

5.3 静态参数

表 2 静态参数表

特性	符号	条件: 除另有规定外, $-40^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$, $V_{\text{DDIO}} = 3.3\text{V}$, $V_{\text{DDPLL}} = V_{\text{DDT}} = V_{\text{DDCML}} = V_{\text{DDD}} = 1.8\text{V}$	极限值		单位
			最小	最大	
发送器输出电压幅度	V_{OD}	$R_L = 100\Omega$	250	450	mV
TTL 输入高电平电压	V_{IH}	$V_{\text{DDIO}} = 3.3\text{V}$	2.0	—	V
		$V_{\text{DDIO}} = 1.8\text{V}$	1.17	—	V
TTL 输入低电平电压	V_{IL}	$V_{\text{DDIO}} = 3.3\text{V}$	—	0.8	V
		$V_{\text{DDIO}} = 1.8\text{V}$	—	0.63	V
TTL 输入电流	I_{IN}	$V_{\text{DDIO}} = 3.6\text{V}$, $V_{\text{IN}} = 0$ 或 V_{DDIO}	—	± 20	μA
TTL 输出高电平电压	V_{OH}	$I_{\text{OH}} = -4\text{mA}$, $V_{\text{DDIO}} = 3.3\text{V}$	2.4	—	V
		$I_{\text{OH}} = -4\text{mA}$, $V_{\text{DDIO}} = 1.8\text{V}$	1.35	—	V
TTL 输出低电平电压	V_{OL}	$I_{\text{OL}} = 4\text{mA}$, $V_{\text{DDIO}} = 3.3\text{V}$	—	0.45	V
		$I_{\text{OL}} = 4\text{mA}$, $V_{\text{DDIO}} = 1.8\text{V}$	—	0.40	V
TTL 输出短路电流	$ I_{\text{OS}} $	$V_{\text{DDIO}} = 3.6\text{V}$, $V_{\text{out}} = 0$ 或 V_{DDIO}	—	180	mA
TTL 输出关断电流	I_{OZ}	$V_{\text{DDIO}} = 3.6\text{V}$, $V_{\text{out}} = 0$ 或 V_{DDIO}	—	± 20	μA
差分终结电阻	R_T	—	80	120	Ω

5.4 动态参数

表 3 动态参数表

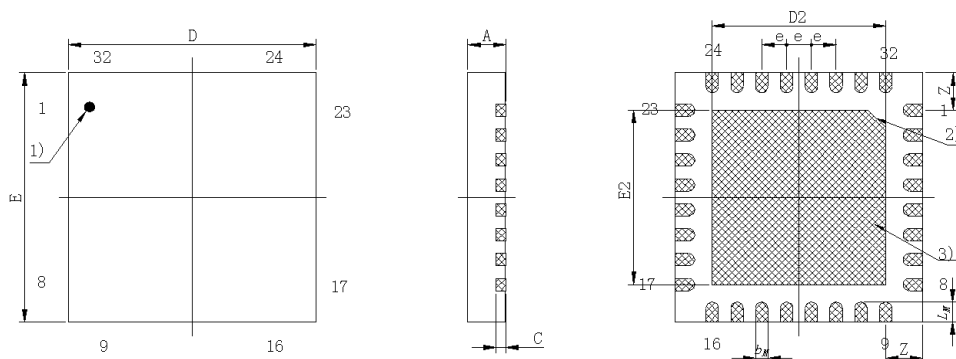
特性	符号	条件: 除另有规定外, $-40^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$, $V_{\text{DDIO}} = 3.3\text{V}$, $V_{\text{DDPLL}} = V_{\text{DDT}} = V_{\text{DDCML}} = V_{\text{DDD}} = 1.8\text{V}$	极限值		单位
			最小	最大	
输出差分信号总抖动	J_T	TTL 输入为全 0 数据	—	0.45	UI
电源电流	I_{DD}	WORST CASE 数据输入	—	200	mA
串行数据率	S_D	$f_{\text{CLK}} = 150\text{MHz}$ (数据率为 2.1Gbps)	—	2.1	Gbps
差分输出上升时间	t_R	f_{CLK} 输入时钟频率为 150MHz	—	0.33	ns
差分输出下降时间	t_F		—	0.33	ns

6 机械尺寸

本器件采用 32 引线的方形扁平无引脚封装 (QFN32)。外形尺寸按图 3 的规定。

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- 注 1: 顶视图 1 脚标示;
- 注 2: 底视图 1 脚标示;
- 注 3: DAP 热沉地脚标示;

图 3 GM8913 尺寸图

具体的尺寸见下表:

表 4 外形尺寸参数

单位: mm

尺寸符号	数 值		
	最 小	公 称	最 大
A	0.70	—	0.80
b_M	0.18	—	0.30
L_M	0.35	—	0.45
c	0.18	—	0.25
e	—	0.50	—
D	—	—	5.10
E	—	—	5.10
Z	—	—	0.85
D_2	—	—	3.60
E_2	—	—	3.60

7 产品应用信息

7.1 典型应用图

GM8913 主要是跟 GM8914 配对应用于车载系统的主要应用于汽车 Advanced Driver Assistance Systems (ADAS)中 ECU(电子控制单元)视频处理器与防碰撞系统前端摄像机、后视镜摄像机和停车系统成像仪系统。

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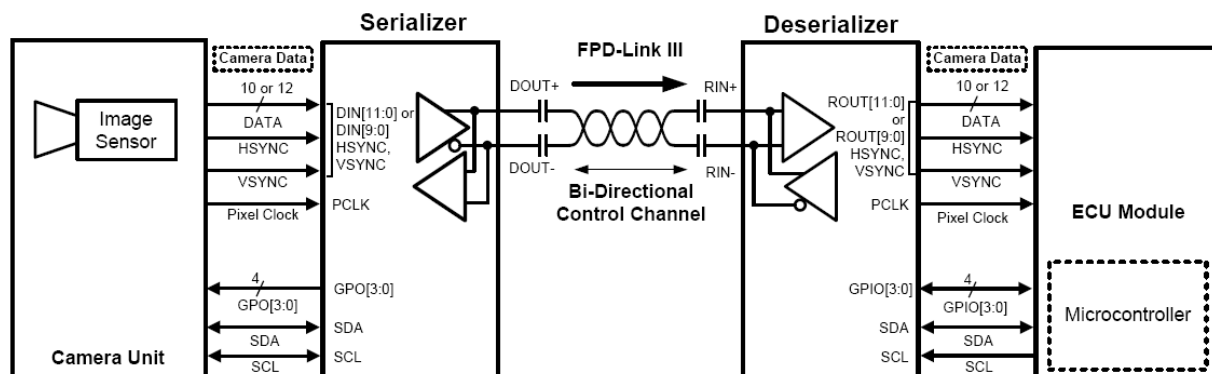


图 4 GM8913 应用图

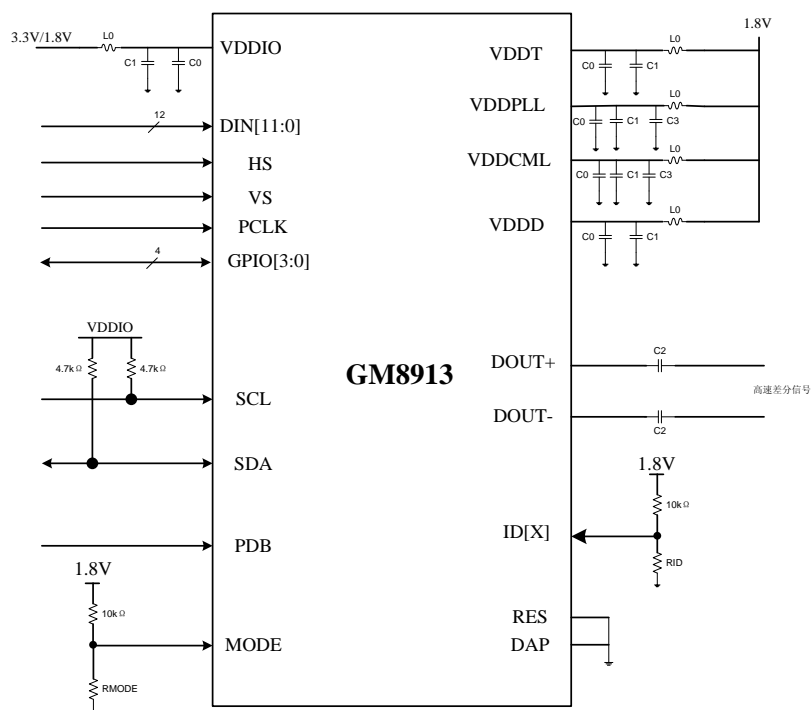


图 5 GM8913 推荐设计图

上图为 GM8906 典型应用中的连接图，其外围无源器件推荐值：电容 C0=0.1μF、C1=0.01μF、C2=0.1μF、C3=4.7μF；磁珠 L0=1KΩ/100MHz。IDX[1:0]和 RMODE 阻值配置详见配置表。

表 5 IDx 地址配置表

RID1(kΩ)误差 1%	地址(7'b)	地址(8'b)
0	0x58	0xB0
2	0x59	0xB2
4.7	0x5A	0xB4
8.2	0x5B	0xB6
14	0x5C	0xB8
100	0x5D	0xBA

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表 6 RMODE 模式配置表

RMODE(Ω)误差 1%	MODE 模式
100K	PCLK 采用前级像素时钟模式
4.7K	外接环振模式

内部寄存器配置如下表所示。

表 7 寄存器配置

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
0x00	I2C Device ID	7:1	DEVICE ID	RW	0xB0'h (1011_000)	7-bit address of Serializer; 0x58'h. (0101_100x'b) default.
		0	SER ID SEL			0: Device ID is from ID[x]. 1: Register I2C Device ID overrides ID[x].
0x01	Power and Reset	7	RSVD			Reserved.
		6	RDS	RW	0	Digital Output Drive Strength. 1: High Drive Strength. 0: Low Drive Strength.
		5	VDDIO Control	RW	1	Auto Voltage Control. 1: Enable. 0: Disable.
		4	VDDIO MODE	RW	1	VDDIO Voltage set. 1: VDDIO = 3.3V. 0: VDDIO = 1.8V.
		3	ANAPWDN	RW	0	This register can be set only through local I2C access. 1: Analog power-down. Powers Down the analog block in the Serializer. 0: No effect.
		2	RSVD	RW	0	Reserved.
		1	DIGITAL RESET1	RW	0	1: Resets the digital block except for register values. Does not affect device I2C Bus or Device ID. This bit is self-clearing. 0: Normal Operation.
		0	DIGITAL RESET0	RW	1	1: Digital Reset, resets the entire digital block including all register values. This bit is self-clearing. 0: Normal Operation.
0x02	Reserved.					
0x03	General Configuration	7	RX CRC Checker Enable	RW	1	Back-channel CRC Checker Enable. 1:Enable. 0: Disable.
		6	TX Parity Generator Enable	RW	1	Forward channel Parity Generator Enable. 1: Enable. 0: Disable.
		5	CRC Error Reset	RW	0	Clear CRC Error Counters. This bit is NOT self-clearing. 1: Clear Counters. 0: Normal Operation.

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		4	I2C Remote Write Auto Acknowledge	RW	0	Automatically Acknowledge I2C Remote Write. The mode works when the system is LOCKed. 1: Enable: When enabled, I2C writes to the Deserializer (or any remote I2C Slave, if I2C PASS ALL is enabled) are immediately acknowledged without waiting for the Deserializer to acknowledge the write. The accesses are then remapped to address specified in 0x06. 0: Disable.
		3	I2C Pass-Through All	RW	0	1: Enable Forward Control Channel pass-through of all I2C accesses to I2C IDs that do not match the Serializer I2C ID. The I2C accesses are then remapped to address specified in register 0x06. 0: Enable Forward Control Channel pass-through only of I2C accesses to I2C IDs matching either the remote Deserializer ID or the remote I2C IDs.
		2	I2C Pass-Through	RW	1	I2C Pass-Through Mode. 1: Pass-Through Enabled. DES Alias 0x07 and Slave Alias 0x09. 0: Pass-Through Disabled.
		1	OV_CLK2PLL	RW	0	1:Enabled : When enabled this register overrides the clock to PLL mode (External Oscillator mode or Direct PCLK mode) defined through MODE pin and allows selection through register 0x35 in the Serializer. 0: Disabled : When disabled, Clock to PLL mode (External Oscillator mode or Direct PCLK mode) is defined through MODE pin on the Serializer.
		0	TRFB	RW	1	Pixel Clock Edge Select. 1: Parallel Interface Data is strobed on the Rising Clock Edge. 0: Parallel Interface Data is strobed on the Falling Clock Edge.
0x04	Reserved.					
0x05	Mode Select	7	RSVD	RW	0	Reserved.
		6	RSVD	RW	0	Reserved.
		5	MODE_OVERRIDE	RW	0	Allows overriding mode select bits coming from back-channel. 1: Overrides MODE select bits. 0: Does not override MODE select bits.
		4	MODE_UP_TO_DATE	R	0	Indicates that the status of mode select from Deserializer is up to date.
		3	RSVD			Reserved.
		2	Pin_MODE_10-bit mode	R	0	1: 10-bit mode is selected. 0: 10-bit mode is not selected.
		1:0	RSVD			Reserved.

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0x06	DES ID	7:1	Deserializer Device ID	RW	0x00	7-bit Deserializer Device ID Configures the I2C Slave ID of the remote Deserializer. A value of 0 in this field disables I2C access to the remote Deserializer. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but should also assert the FREEZE DEVICE ID bit to prevent overwriting by the Bidirectional Control Channel.
		0	Freeze Device ID	RW	0	1: Prevents auto-loading of the Deserializer Device ID by the bidirectional control channel. The ID will be frozen at the value written. 0: Update.
0x07	DES Alias	7:1	Deserializer ALIAS ID	RW	0	7-bit Remote Deserializer Device Alias ID Configures the decoder for detecting transactions designated for an I2C Deserializer device. The transaction will be remapped to the address specified in the DES ID register. A value of 0 in this field disables access to the remote Deserializer.
		0	RSVD			Reserved.
0x08	SlaveID	7:1	SLAVE ID	RW	0x00	7-bit Remote Slave Device ID Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer and then to remote slave. A value of 0 in this field disables access to the remote I2C slave.
		0	RSVD			Reserved.
0x09	Slave Alias	7:1	SLAVE ALIAS ID	RW	0x00	7-bit Remote Slave Device Alias ID Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RSVD			Reserved.
0x0A	CRC Errors	7:0	CRC Error Byte 0	R	0	Number of back-channel CRC errors during normal operation. Least Significant byte.
0x0B	CRC Errors	7:0	CRC Error Byte 1	R	0	Number of back-channel CRC errors during normal operation. Most Significant byte.
0x0C	General Status	7:5	Rev-ID	R	0	Revision ID. 0x00: Production Revision ID.
		4	RX Lock Detect	R	0	1: RX LOCKED. 0: RX not LOCKED.

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		3	BIST CRC Error Status	R	0	1: CRC errors in BIST mode. 0: No CRC errors in BIST mode.
		2	PCLK Detect	R	0	1: Valid PCLK detected. 0: Valid PCLK not detected.
		1	DES Error	R	0	1: CRC error is detected during communication with Deserializer. This bit is cleared upon loss of link or assertion of CRC ERROR RESET in register 0x04. 0: No effect.
		0	LINK Detect	R	0	1: Cable link detected. 0: Cable link not detected. This includes any of the following faults: — Cable Open. — '+' and '-' shorted. — Short to GND. — Short to battery.
0x0D	GPO[0] and GPO[1] Configuration	7	GPO1 Output Value	RW	0	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled. The local GPIO direction is Output, and remote GPIO control is disabled.
		6	GPO1 Remote Enable	RW	1	Remote GPIO Control. 1: Enable GPIO control from remote Deserializer. The GPIO pin needs to be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Deserializer.
		5	GPO1 Direction	RW	0	1: Input. 0: Output.
		4	GPO0 Enable	RW	1	1: GPIO enable. 0: Tri-state.
		3	GPO0 Output Value	RW	0	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled. The local GPIO direction is Output, and remote GPIO control is disabled.
		2	GPO0 Remote Enable	RW	1	Remote GPIO Control. 1: Enable GPIO control from remote Deserializer. The GPIO pin needs to be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Deserializer.
		1	GPO0 Direction	RW	0	1: Input. 0: Output.
		0	GPO0 Enable	RW	1	1: GPIO enable. 0: Tri-state.
0x0E	GPO[2] and GPO[3] Configuration	7	GPO3 Output Value	RW	0	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled. The local GPIO direction is Output, and remote GPIO control is disabled.
		6	GPO3 Remote Enable	RW	0	Remote GPIO Control. 1: Enable GPIO control from remote Deserializer. The GPIO pin needs to be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Deserializer.
		5	GPO3 Direction	RW	1	1: Input. 0: Output.

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		4	GPO3 Enable	RW	1	1: GPIO enable. 0: Tri-state.
		3	GPO2 Output Value	RW	0	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled. The local GPIO direction is Output, and remote GPIO control is disabled.
		2	GPO2 Remote Enable	RW	1	Remote GPIO Control. 1: Enable GPIO control from remote Deserializer. The GPIO pin needs to be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Deserializer.
		1	GPO2 Direction	RW	0	1: Input. 0: Output.
		0	GPO2 Enable	RW	1	1: GPIO enable. 0: Tri-state.
0x0F	I2C Master Config	7:5	RSVD			Reserved.
		4:3	SDA Output Delay	RW	00	SDA Output Delay This field configures output delay on the SDA output. Setting this value will increase output delay in units of 50ns. Nominal output delay values for SCL to SDA are: 00: ~350ns 01: ~400ns 10: ~450ns 11: ~500ns
		2	Local Write Disable	RW	0	Disable Remote Writes to Local Registers Setting this bit to a 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Serializer registers from an I2C master attached to the Deserializer. Setting this bit does not affect remote access to I2C slaves at the Serializer.
		1	I2C Bus Timer Speed up	RW	0	Speed up I2C Bus Watchdog Timer. 1: Watchdog Timer expires after approximately 50 microseconds. 0: Watchdog Timer expires after approximately 1 second.
		0	I2C Bus Timer Disable	RW	0	1. Disable I2C Bus Watchdog Timer When the I2C Watchdog Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signaling occurs for approximately 1 second, the I2C bus will assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL. 0: No effect.
0x10	I2C Control	7	RSVD			Reserved.
		6:4	SDA Hold Time	RW	0x1	Internal SDA Hold Time. This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 50ns.
		3:0	I2C Filter Depth	RW	0x7	I2C Glitch Filter Depth This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will

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						be rejected. Units are 10ns.
0x11	SCL High Time	7:0	SCL High Time	RW	0x82	I2C Master SCL High Time This field configures the high pulse width of the SCL output when the Serializer is the Master on the local I2C bus. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum (4 μ s + 1 μ s of rise time for cases where rise time is very fast) SCL high time with the internal oscillator clock running at 26MHz rather than the nominal 20MHz.
0x12	SCL LOW Time	7:0	SCL Low Time	RW	0x82	I2C SCL Low Time This field configures the low pulse width of the SCL output when the Serializer is the Master on the local I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum (4.7 μ s + 0.3 μ s of fall time for cases where fall time is very fast) SCL low time with the internal oscillator clock running at 26MHz rather than the nominal 20MHz.
0x13	General Purpose Control	7:0	GPCR[7:0]	RW	0	1: High. 0: Low.
0x14	BIST Control	7:3	RSVD			Reserved.
		2:1	Clock Source	RW	0x0	Allows choosing different OSC clock frequencies for forward channel frame. OSC Clock Frequency in Functional Mode when OSC mode is selected or when the selected clock source is not present e.g. missing PCLK/ External Oscillator. See Table 5 for oscillator clock frequencies when PCLK/ External Clock is missing.
		0	RSVD			Reserved.
0x15–0x1D	Reserved.					
0x1E	BCC Watchdog Control	7:1	BCC Watchdog Timer	RW	0x7F	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2ms. This field should not be set to 0.
		0	BCC Watchdog Timer Disable	RW	0	Disable Bidirectional Control Channel Watchdog Timer. 1: Disables BCC Watchdog Timer operation. 0: Enables BCC Watchdog Timer operation.
0x1F–0x29	Reserved.					

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0x2A	CRC Errors	7:0	BIST Mode CRC Errors Count	R	0	Number of CRC Errors in the back channel when in BIST mode.
0x2B-0x34	Reserved.					
0x35	PLL Clock Overwrite	7:4	RSVD			Reserved.
		3	PIN_LOCK to External Oscillator	RW	0	Status of mode select pin. 1: Indicates External Oscillator mode is selected by mode-resistor. 0: External Oscillator mode is not selected by mode-resistor.
		2	RSVD		0	Reserved.
		1	LOCK to External Oscillator	RW	0	Affects only when 0x03[1]=1 (OV_CLK2PLL) and 0x35[0]=0. 1: Routes GPO3 directly to PLL. 0: Allows PLL to lock to PCLK.
		0	LOCK2OSC	RW	1	Affects only when 0x03[1]=1 (OV_CLK2PLL). 1: Allows internal OSC clock to feed into PLL. 0: Allows PLL to lock to either PCLK or external from GPO3.

7.2 应用说明

芯片应用中应注意以下几点：

- a) 电源必须加滤波电容，推荐采用 0.1uF 和 0.01uF 的电容进行组合滤波，也可根据实际情况考虑；
- b) 信号的输入或输出端串联匹配电阻改善信号质量；
- c) 应用过程中，芯片的电源电压、输入电压范围、测试温度以及测试条件等都需要严格遵守数据手册规定；
- d) 用于测试和焊接的工作台面，测试仪器以及高低温箱等都必须具有防静电设施；
- e) 测试和使用过程中，操作人员也必须带防静电腕带，在防静电台面上进行操作，禁止直接手持芯片；
- f) 测试和使用过程中出现异常现象时，应该注意保护芯片。