

PMV65XP

P-channel TrenchMOS™ extremely low level FET

Rev. 01 — 28 September 2004

Product data sheet

1. Product profile

1.1 General description

P-channel enhancement mode field effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Low threshold voltage
- Low on-state resistance.

1.3 Applications

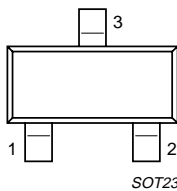
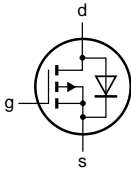
- Low power DC-to-DC converters
- Battery management
- Load switching
- Battery powered portable equipment.

1.4 Quick reference data

- $V_{DS} \leq -20$ V
- $I_D \leq -3.9$ A
- $R_{DSon} \leq 76$ m Ω
- $Q_{gd} = 0.65$ nC (typ).

2. Pinning information

Table 1: Discrete pinning

Pin	Description	Simplified outline	Symbol
1	gate (g)	 <p>SOT23</p>	 <p>003aaa671</p>
2	source (s)		
3	drain (d)		

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3. Ordering information

Table 2: Ordering information

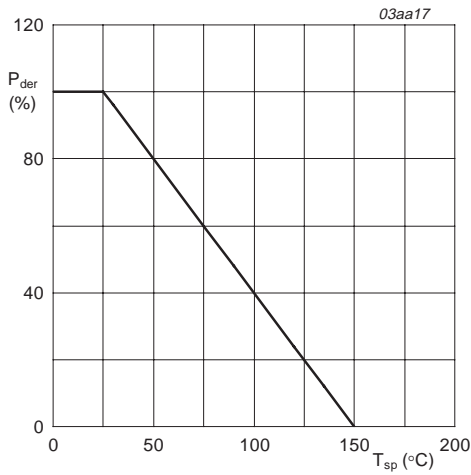
Type number	Package		Version
	Name	Description	
PMV65XP	SOT23	Plastic surface mounted package; 3 leads	SOT23

4. Limiting values

Table 3: Limiting values

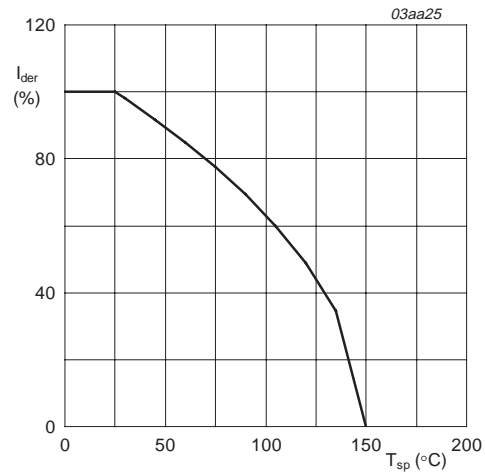
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-20	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	-20	V
V_{GS}	gate-source voltage (DC)		-	± 12	V
I_D	drain current (DC)	$T_{sp} = 25\text{ °C}$; $V_{GS} = -4.5\text{ V}$; Figure 2 and 3	-	-3.9	A
		$T_{sp} = 100\text{ °C}$; $V_{GS} = -4.5\text{ V}$; Figure 2	-	-2.5	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	-15.9	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; Figure 1	-	1.92	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{sp} = 25\text{ °C}$	-	-1.6	A
I_{SM}	peak source (diode forward) current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	-6.4	A



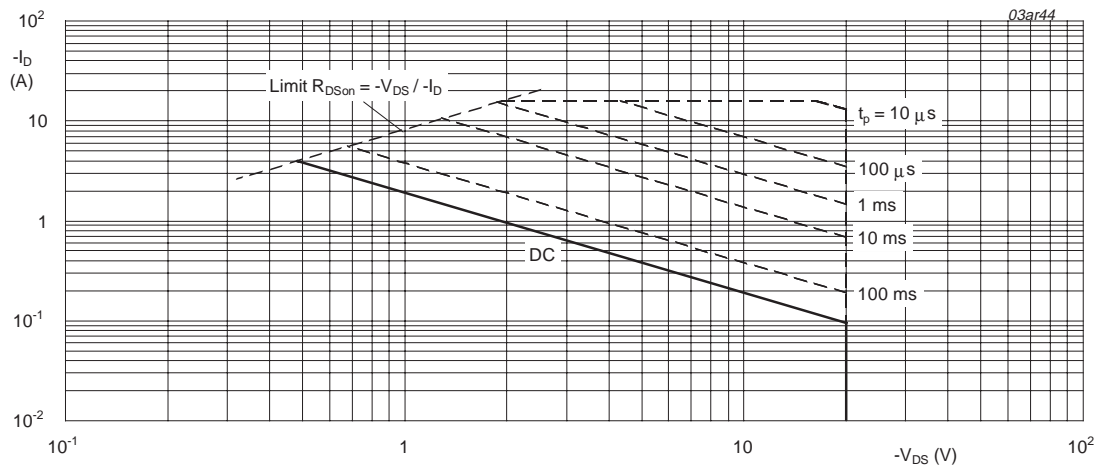
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



$T_{sp} = 25^{\circ}C$; I_{DM} is single pulse; $V_{GS} = -4.5 V$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Figure 4	-	-	65	K/W

5.1 Transient thermal impedance

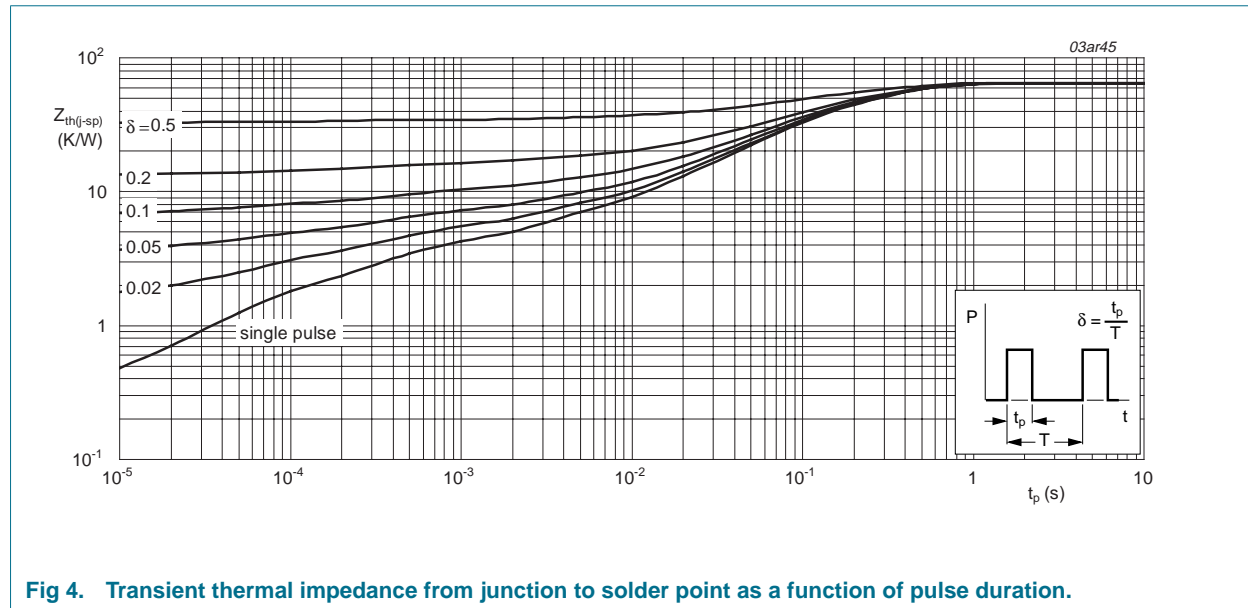
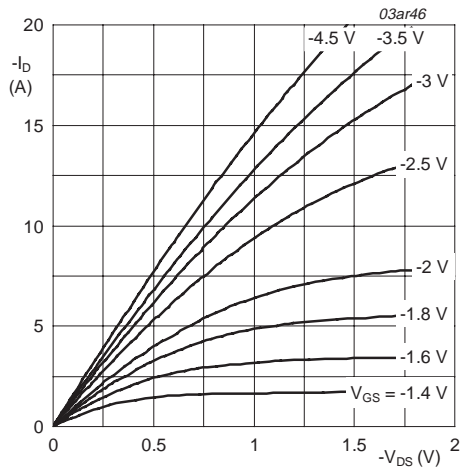


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.

6. Characteristics

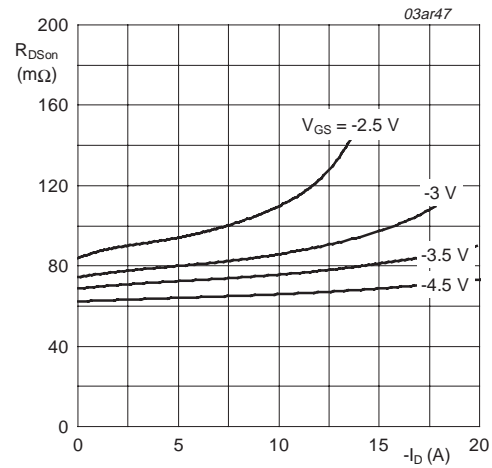
Table 5: Characteristics
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = -250 μA; V _{GS} = 0 V				
		T _j = 25 °C	-20	-	-	V
		T _j = -55 °C	-18	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = -1 mA; V _{DS} = V _{GS} ; Figure 9 and 10				
		T _j = 25 °C	-0.55	-0.75	-0.95	V
		T _j = 150 °C	-0.35	-	-	V
		T _j = -55 °C	-	-	-1.1	V
I _{DSS}	drain-source leakage current	V _{DS} = -20 V; V _{GS} = 0 V				
		T _j = 25 °C	-	-	-1	μA
		T _j = 150 °C	-	-	-100	μA
I _{GSS}	gate-source leakage current	V _{GS} = ±12 V; V _{DS} = 0 V	-	-10	-100	nA
R _{DS(on)}	drain-source on-state resistance	V _{GS} = -4.5 V; I _D = -2.8 A; Figure 6 and 8				
		T _j = 25 °C	-	65	76	mΩ
		T _j = 150 °C	-	104	122	mΩ
		V _{GS} = -2.5 V; I _D = -2.3 A; Figure 6 and 8	-	90	112	mΩ
Dynamic characteristics						
Q _{g(tot)}	total gate charge	I _D = -2.8 A; V _{DS} = -6 V; V _{GS} = -4.5 V; Figure 11	-	7.6	-	nC
Q _{gs}	gate-source charge		-	1.6	-	nC
Q _{gd}	gate-drain (Miller) charge		-	0.65	-	nC
V _{plat}	plateau voltage		-	-1.5	-	V
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = -20 V; f = 1 MHz; Figure 13	-	725	-	pF
C _{oss}	output capacitance		-	105	-	pF
C _{rss}	reverse transfer capacitance		-	80	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -6 V; R _L = 6 Ω;	-	7	-	ns
t _r	rise time	V _{GS} = -4.5 V; R _G = 6 Ω	-	21	-	ns
t _{d(off)}	turn-off delay time		-	68	-	ns
t _f	fall time		-	33	-	ns
Source-drain diode						
V _{SD}	source-drain (diode forward) voltage	I _S = -1.25 A; V _{GS} = 0 V; Figure 12	-	-0.77	-1.2	V



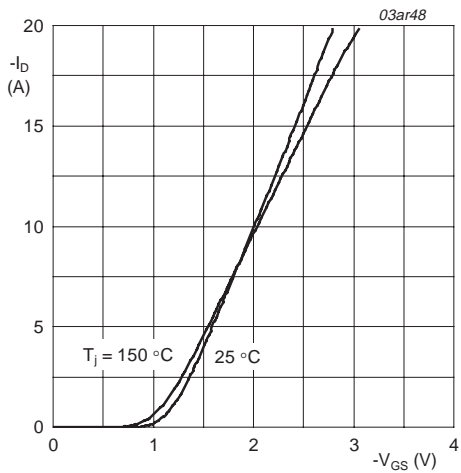
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



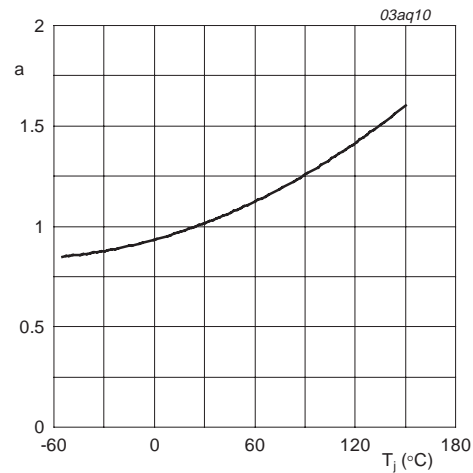
$T_j = 25\text{ }^\circ\text{C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values.



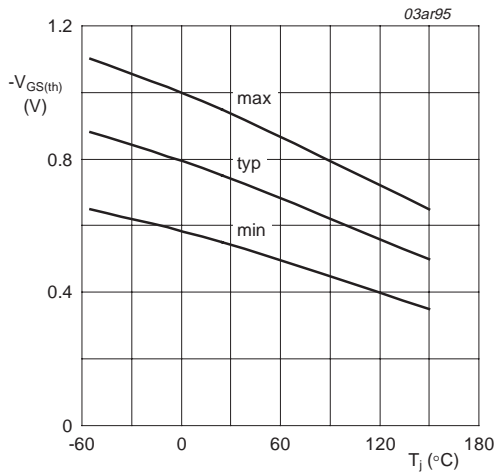
$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



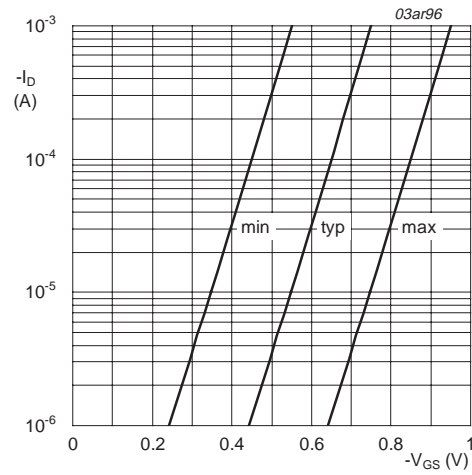
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



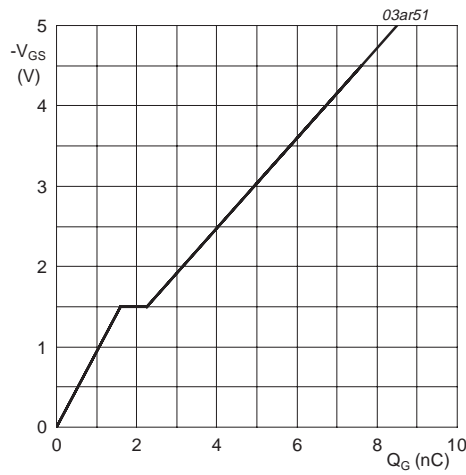
$I_D = -1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



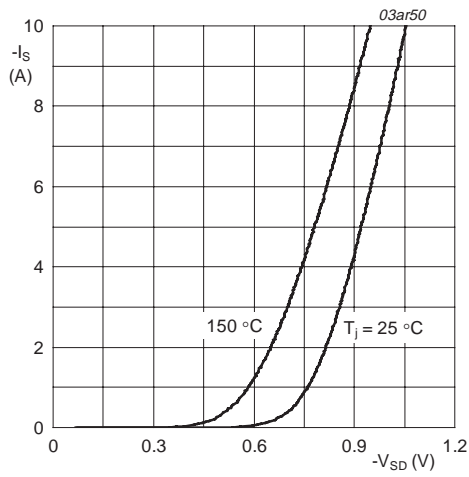
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = -5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



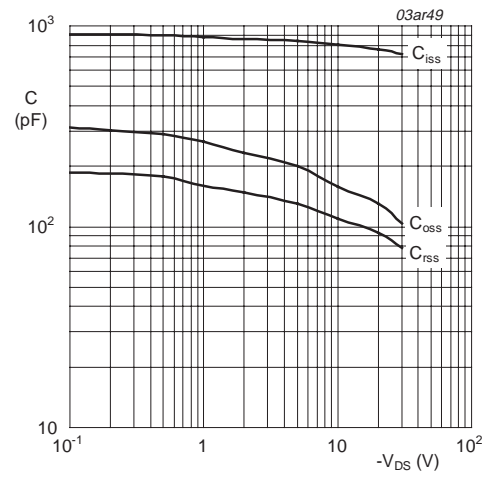
$I_D = -2.8 \text{ A}; V_{DS} = -6 \text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values.



$T_j = 25\text{ °C}$ and 150 °C ; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.

7. Package outline

Plastic surface mounted package; 3 leads

SOT23

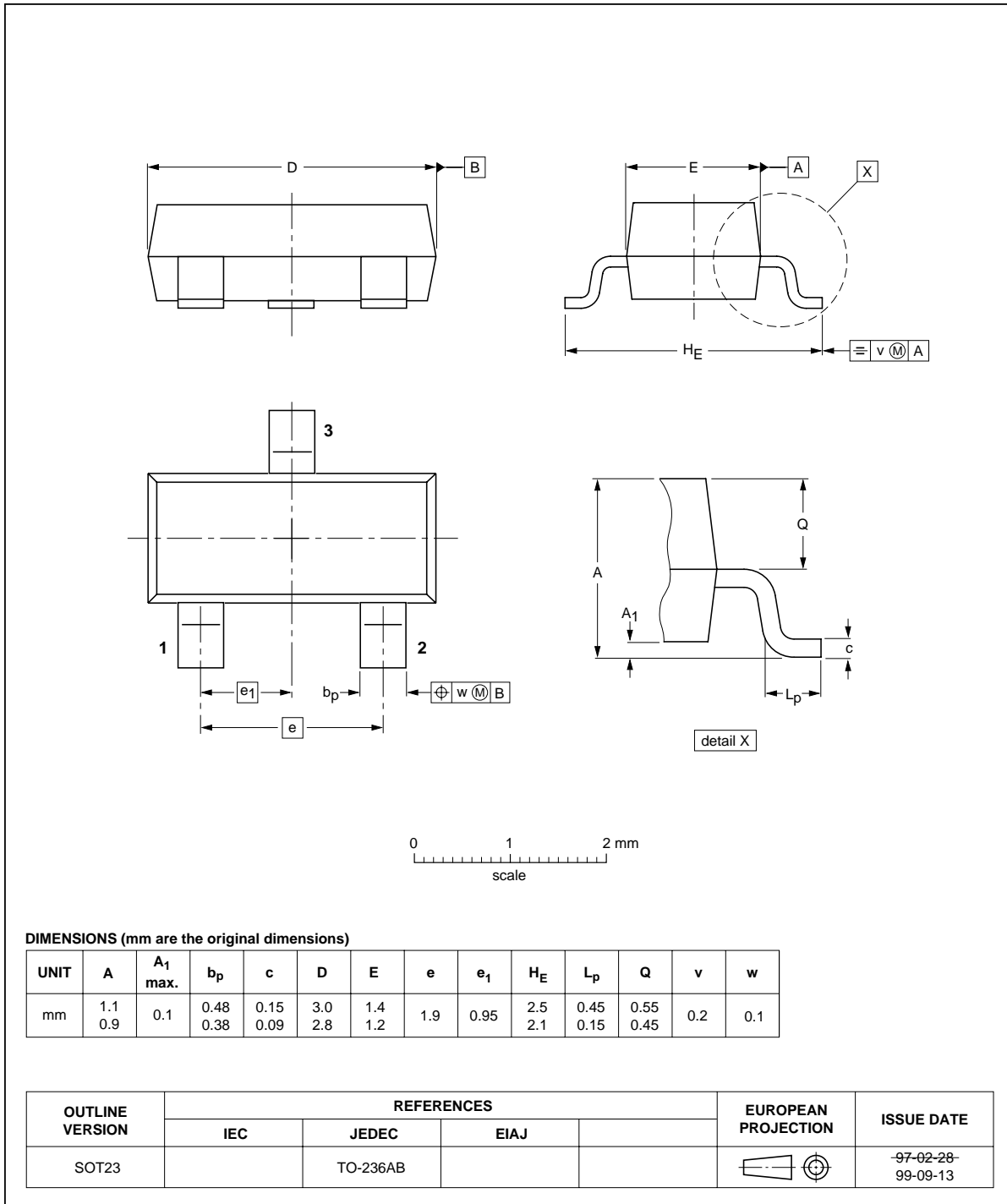


Fig 14. SOT23 package outline.



8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PMV65XP_1	20040928	Product data sheet	-	9397 750 13993	-

9. Data sheet status

Level	Data sheet status [1]	Product status [2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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