Features

- Precision supply-voltage monitor
  - 4.63V (PT7M7xxxL)
  - 4.38V (PT7M7xxxM)
  - 3.08V (PT7M7xxxT)
  - 2.93V (PT7M7xxxS)
  - 2.63V (PT7M7xxxR)
  - 2.32V (PT7M7xxxZ)
  - 2.20V (PT7M7xxxY)
  - 4.00V (PT7M7xxxJ)
- 200ms reset pulse width
- Debounced CMOS-compatible manual-reset input (7811, 7812, 7823, 7825, 7342-7344)
- Reset Output Signal for Watchdog and Power Abnormal, Manual Reset
- Reset Push-Pull output (PT7M7809,7811,7823, 7824,7825,7342,7345)
- Reset Open-Drain output (PT7M7803/7343)
- Voltage monitor for power-fail or low battery warning
- Guaranteed $\overline{\text{RESET}}$/RESET valid at V_{CC} = 1.0V

Discription

The PT7M7xxx family microprocessor (µP) supervisory circuits are targeted to improve reliability and accuracy of power-supply circuitry in µP systems. These devices reduce the complexity and number of components required to monitor power-supply and battery functions.

The main functions are:
1. Asserting reset output during power-up, power-down and brownout conditions for µP system;
2. Detecting power failure or low-battery conditions with a 1.25V threshold detector;
3. Watchdog functions;
4. Manual reset.

Applications

- Power-supply circuitry in µP systems

Ordering Information

No.	Part No	Package	No.	Part No	Package
1	PT7M7803XT	SOT23-3	12	PT7M7345XTA	SOT23-6
2	PT7M7809XT		13	PT7M7811XTB	SOT143
3	PT7M7810XT		14	PT7M7812XTB	
4	PT7M7811XTA	SOT23-5	15	PT7M7803XDE	Die Form
5	PT7M7812XTA		16	PT7M7809XDE	
6	PT7M7823XTA		17	PT7M7810XDE	
7	PT7M7824XTA		18	PT7M7811XDE	
8	PT7M7825XTA		19	PT7M7812XDE	
9	PT7M7342XTA	SOT23-6	20	PT7M7823XDE	
10	PT7M7343XTA		21	PT7M7824XDE	
11	PT7M7344XTA		22	PT7M7825XDE	

Note: lead free package is available by adding E at the end of each part no. For example: PT7M7803XTE for SOT23-3 lead free package.

Suffix: X -- Monitored Voltage

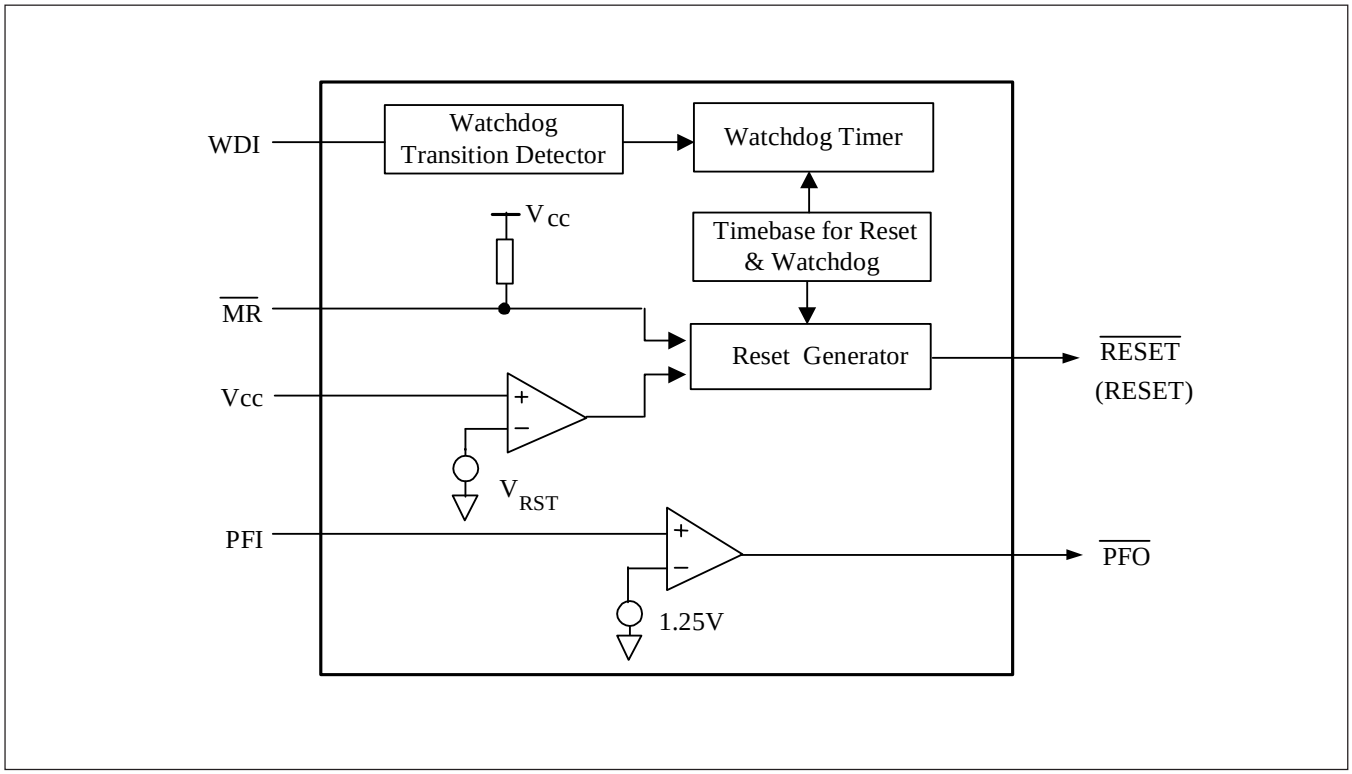
Suffix X	L	M	T	S	R	Z	Y	J
Reset Threshold(V)	4.36	4.38	3.08	2.93	2.63	2.32	2.20	4.00

Function Comparison

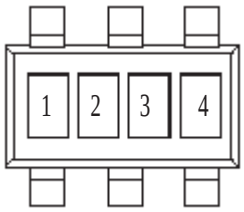
No.	Part No.	$\overline{\text{RESET}}$ output		RESET output (push-pull)	Manual Reset Input	Power Fail Detector (1.25V)	Watchdog Input
		Push-Pull	Open-Drain				
1	PT7M7803XT	-	√	-	-	-	-
2	PT7M7809XT	√	-	-	-	-	-
3	PT7M7810XT	-	-	√	-	-	-
4	PT7M7811XTA	√	-	-	√	-	-
5	PT7M7812XTA	-	-	√	√	-	-
6	PT7M7823XTA	√	-	-	√	-	√
7	PT7M7824XTA	√	-	√	-	-	√
8	PT7M7825XTA	√	-	√	√	-	-
9	PT7M7342XTA	√	-	-	√	√	-
10	PT7M7343XTA	-	√	-	√	√	-
11	PT7M7344XTA	-	-	√	√	√	-
12	PT7M7345XTA	√	-	√	-	√	-
13	PT7M7811XTB	√	-	-	√	-	-
14	PT7M7811XTB	-	-	√	√	-	-
15	PT7M7803XDE	-	√	-	-	-	-
16	PT7M7809XDE	√	-	-	-	-	-
17	PT7M7810XDE	-	-	√	-	-	-
18	PT7M7811XDE	√	-	-	√	-	-
19	PT7M7812XDE	-	-	√	√	-	-
20	PT7M7823XDE	√	-	-	√	-	√
21	PT7M7824XDE	√	-	√	-	-	√
22	PT7M7825XDE	√	-	√	√	-	-

Block Diagram

Block Diagram



Marking Information



Code	Description
1 2	Part Number
3	Year
4	Work Week

Part Number Code

Code 1 2	Part No.	Code 1 2	Part No.	Code 1 2	Part No.
AA	PT7M7809L	BC	PT7M7803L	CE	PT7M7342L
AB	PT7M7809M	BD	PT7M7803M	CF	PT7M7342M
AC	PT7M7809T	BE	PT7M7803T	CG	PT7M7342T
AD	PT7M7809S	BF	PT7M7803S	CH	PT7M7342S
AE	PT7M7809R	BG	PT7M7803R	CI	PT7M7342R
AF	PT7M7809Z	BH	PT7M7803Z	CJ	PT7M7342Z
AG	PT7M7809Y	BI	PT7M7803Y	CK	PT7M7342Y
sd	PT7M7809J	jm	PT7M7803J	sk	PT7M7342J
AH	PT7M7810L	BJ	PT7M7823L	CL	PT7M7343L
AI	PT7M7810M	BK	PT7M7823M	CM	PT7M7343M
AJ	PT7M7810T	BL	PT7M7823T	CN	PT7M7343T
AK	PT7M7810S	BM	PT7M7823S	CO	PT7M7343S
AL	PT7M7810R	BN	PT7M7823R	CP	PT7M7343R
AM	PT7M7810Z	BO	PT7M7823Z	CQ	PT7M7343Z
AN	PT7M7810Y	BP	PT7M7823Y	CR	PT7M7343Y
se	PT7M7810J	sh	PT7M7823J	sl	PT7M7343J
AO	PT7M7811L	BQ	PT7M7824L	CS	PT7M7344L
AP	PT7M7811M	BR	PT7M7824M	CT	PT7M7344M
AQ	PT7M7811T	BS	PT7M7824T	CU	PT7M7344T
AR	PT7M7811S	BT	PT7M7824S	CV	PT7M7344S
AS	PT7M7811R	BU	PT7M7824R	CW	PT7M7344R
AT	PT7M7811Z	BV	PT7M7824Z	CX	PT7M7344Z
AU	PT7M7811Y	BW	PT7M7824Y	CY	PT7M7344Y
sf	PT7M7811J	si	PT7M7824J	sm	PT7M7344J
AV	PT7M7812L	BX	PT7M7825L	CZ	PT7M7345L
AW	PT7M7812M	BY	PT7M7825M	DA	PT7M7345M
AX	PT7M7812T	BZ	PT7M7825T	DB	PT7M7345T
AY	PT7M7812S	CA	PT7M7825S	DC	PT7M7345S
AZ	PT7M7812R	CB	PT7M7825R	DD	PT7M7345R
BA	PT7M7812Z	CC	PT7M7825Z	DE	PT7M7345Z
BB	PT7M7812Y	CD	PT7M7825Y	DF	PT7M7345Y
sg	PT7M7812J	sj	PT7M7825J	sn	PT7M7345J

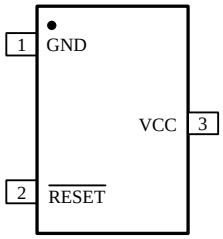
Note: lead free package is available by adding line above the first code. For example: Part Number code of PT7M7809LE is $\overline{\text{A}}$A.

Pin Information

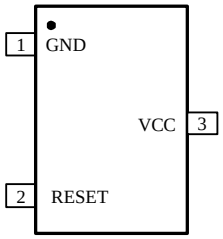
Pin Configuration

SOT23-3

PT7M7803
PT7M7809

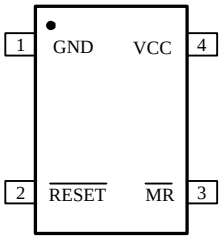


PT7M7810

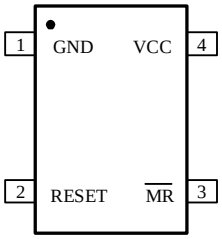


SOT143

PT7M7811

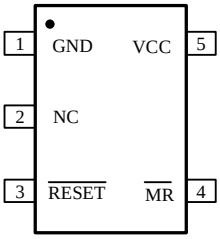


PT7M7812

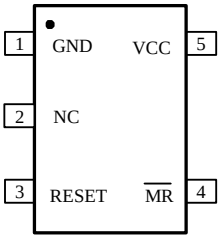


SOT23-5

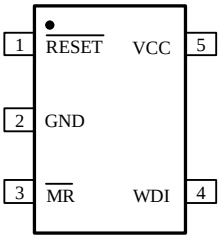
PT7M7811



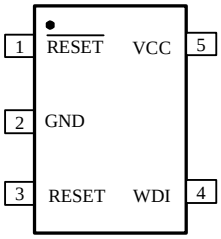
PT7M7812



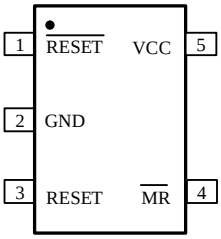
PT7M7823



PT7M7824

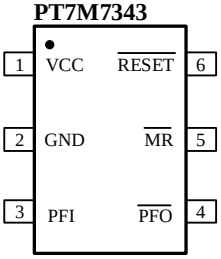


PT7M7825

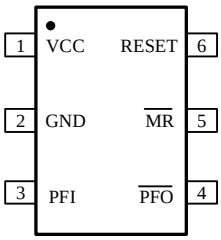


SOT23-6

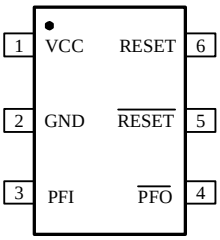
PT7M7342
PT7M7343



PT7M7344



PT7M7345

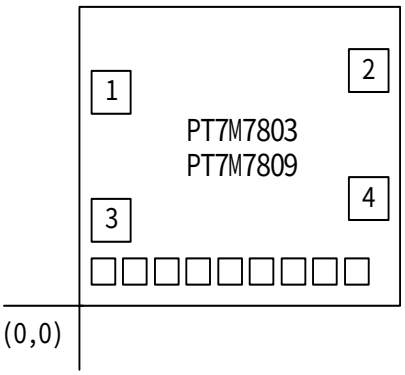


Pin Description

Pin Name	Type	Description
$\overline{MR}$	I	**Manual-Reset: (CMOS).** Active low. Pull low to force a reset. Reset remains asserted for the duration of the Reset Timeout Period after $\overline{MR}$ transitions from low to high. Leave unconnected or connected to VCC if not used.
Vcc	Power	**Power Supply:** Reset is asserted when V_{CC} drops below the Reset Threshold Voltage (V_{RST}). Reset remains asserted until V_{CC} rises above V_{RST} and keep asserted for the duration of the Reset Timeout Period (t_{RS}) once V_{CC} rises above V_{RST}.
GND	Ground	**Ground Reference** for all signals
PFI	I	**Power-Fail Voltage Monitor Input.** When PFI <V_{PFT} , $\overline{PFO}$ goes low. Connect PFI to GND or Vcc when not used.
$\overline{PFO}$	O	**Power-Fail Output:** it gets low and sinks current when PFI is less than 1.25V; otherwise $\overline{PFO}$ stays high.
WDI	I	**Watchdog Input (CMOS).** If WDI remains high or low for the duration of the watchdog timeout period (t_{WD}), the internal watchdog timer trigger a reset output. Floating WDI or connecting WDI to a high-impedance three-state buffer disables the watchdog feature. The internal watchdog timer clears whenever reset is asserted or WDI occurs a rising or falling edge.
$\overline{RESET}$	O	**Active-Low Reset Output (Push-Pull or Open-Drain).** It goes low when Vcc is below the reset threshold. It remains low for about 200ms after one of the following occurs: Vcc rises above the reset threshold (V_{RST}), the watchdog triggers a reset, or $\overline{MR}$ goes from low to high.
RESET	O	**The inverse of $\overline{RESET}$**, active high. Whenever $\overline{RESET}$ is high, RESET is low.
NC	-	**No connection**

Pad Identification

PT7M7803, PT7M7809

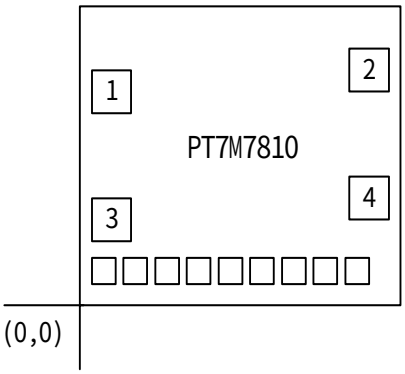


No.	Symbol	Location (X,Y)
1	GND	(97.40, 414.60)
2	$\overline{\text{RESET}}$	(557.40, 450.90)
3	Vcc	(95.30, 210.30)
4	NC	(557.40, 210.30)

Note:

1)Wafer Size: 6 inch
2)Wafer Thickness: 675um
3)Chip Size: 770um*780um (include scribe line width 100um*100um)
4)PAD Location: Refer above diagram and table. PAD size75um*75um
5)PAD discription refer to Pin discription

PT7M7810

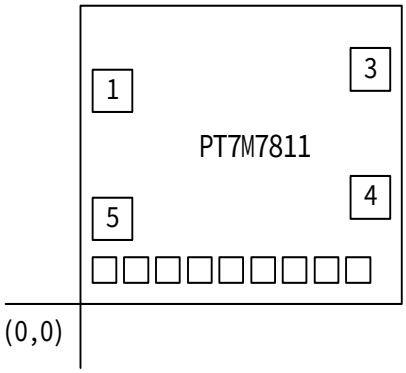


No.	Symbol	Location (X,Y)
1	GND	(97.40, 414.60)
2	RESET	(557.40, 450.90)
3	Vcc	(95.30, 210.30)
4	NC	(557.40, 210.30)

Note:

1)Wafer Size: 6 inch
2)Wafer Thickness: 675um
3)Chip Size: 770um*780um (include scribe line width 100um*100um)
4)PAD Location: Refer above diagram and table. PAD size75um*75um
5)PAD discription refer to Pin discription

PT7M7811

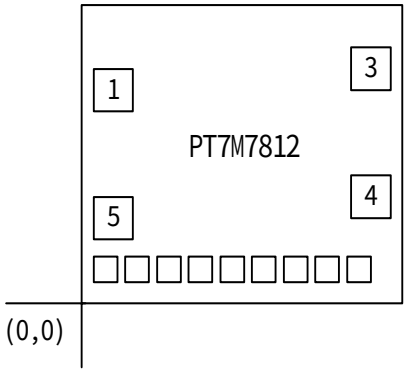


No.	Symbol	Location (X,Y)
1	GND	(97.40, 414.60)
3	$\overline{\text{RESET}}$	(557.40, 450.90)
4	$\overline{\text{MR}}$	(95.30, 210.30)
5	Vcc	(557.40, 210.30)

Note:

1)Wafer Size: 6 inch
2)Wafer Thickness: 675um
3)Chip Size: 770um*780um (include scribe line width 100um*100um)
4)PAD Location: Refer above diagram and table. PAD size75um*75um
5)PAD discription refer to Pin discription

PT7M7812

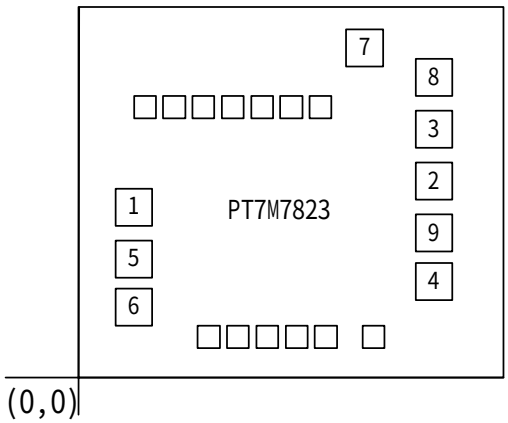


No.	Symbol	Location (X,Y)
1	GND	(97.40, 414.60)
3	RESET	(557.40, 450.90)
4	$\overline{\text{MR}}$	(95.30, 210.30)
5	Vcc	(557.40, 210.30)

Note:

1)Wafer Size: 6 inch
2)Wafer Thickness: 675um
3)Chip Size: 770um*780um (include scribe line width 100um*100um)
4)PAD Location: Refer above diagram and table. PAD size75um*75um
5)PAD discription refer to Pin discription

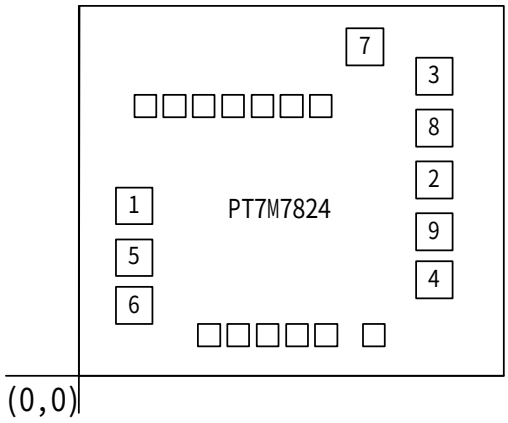
PT7M7823



No.	Symbol	Location (X,Y)
1	$\overline{\text{RESET}}$	(151.05, 326.25)
2	GND	(815.60, 381.55)
3	$\overline{\text{MR}}$	(815.60, 579.75)
4	WDI	(815.60, 183.35)
5	Vcc	(151.05, 227.05)
6	NC	(151.05, 128.05)
7	NC	(626.80, 622.00)
8	NC	(815.60, 579.75)
9	NC	(815.60, 282.55)

Note:
1)Wafer Size: 6 inch
2)Wafer Thickness: 675um
3)Chip Size: 1060um*810um (include scribe line width 100um*100um)
4)PAD Location: Refer above diagram and table.PAD Size75um*75um
5)PAD discription refer to Pin discription

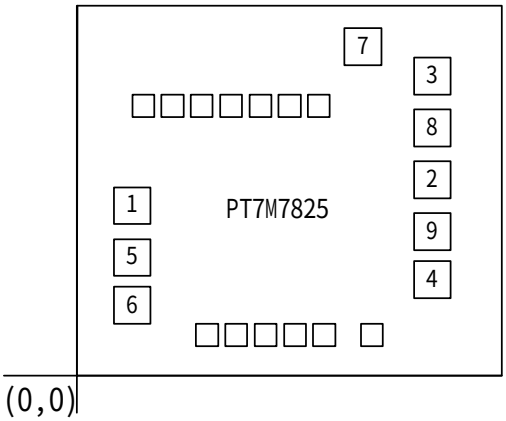
PT7M7824



No.	Symbol	Location (X,Y)
1	$\overline{\text{RESET}}$	(151.05, 326.25)
2	GND	(815.60, 381.55)
3	RESET	(815.60, 579.75)
4	WDI	(815.60, 183.35)
5	Vcc	(151.05, 227.05)
6	NC	(151.05, 128.05)
7	NC	(626.80, 622.00)
8	NC	(815.60, 579.75)
9	NC	(815.60, 282.55)

Note:
1)Wafer Size: 6 inch
2)Wafer Thickness: 675um
3)Chip Size: 1060um*810um (include scribe line width 100um*100um)
4)PAD Location: Refer above diagram and table.PAD Size75um*75um
5)PAD discription refer to Pin discription

PT7M7825



No.	Symbol	Location (X,Y)
1	$\overline{\text{RESET}}$	(151.05, 326.25)
2	GND	(815.60, 381.55)
3	$\overline{\text{RESET}}$	(815.60, 579.75)
4	MR	(815.60, 183.35)
5	Vcc	(151.05, 227.05)
6	NC	(151.05, 128.05)
7	NC	(626.80, 622.00)
8	NC	(815.60, 579.75)
9	NC	(815.60, 282.55)

Note:
1)Wafer Size: 6 inch
2)Wafer Thickness: 675um
3)Chip Size: 1060um*810um (include scribe line width 100um*100um)
4)PAD Location: Refer above diagram and table.PAD Size75um*75um
5)PAD discription refer to Pin discription

Functional Description

Reset Output

A microprocessor (µP) reset input starts the µP in a known state. Whenever the µP is in an unknown state, it should be held in reset. The supervisory circuits assert reset during power-up and prevent code execution errors during power-down or brownout conditions.

On power-up, once Vcc reaches about 1.0V, $\overline{\text{RESET}}$ is a guaranteed logic low of 0.4V or less. As Vcc rises, $\overline{\text{RESET}}$ stays low. When Vcc rises above the reset threshold, an internal timer releases $\overline{\text{RESET}}$ after about 200ms. $\overline{\text{RESET}}$ pulses low whenever Vcc drops below the reset threshold, i.e. brownout condition. If brownout occurs in the middle of a previously initiated reset pulse, the pulse continues for at least another 200ms. On power-down, once Vcc falls below the reset threshold, $\overline{\text{RESET}}$ stays low and is guaranteed to be 0.4V or less until Vcc drops below 1.0V. Watchdog Timing Diagram shows the timing relationship.

The active-high RESET output is simply the inverse of the $\overline{\text{RESET}}$ output, and is guaranteed to be valid with Vcc down to 1.0V.

Watchdog Timer

The PT7M7**xxx** watchdog circuit monitors the µP activity. If the µP does not toggle the watch-dog input (WDI) within 1.6s, reset asserts. As long as reset is asserted or the WDI input is toggled, the watchdog timer will stay clear and will not count. As soon as reset is released, the timer will start counting. WDI input pulses as short as 50ns can be detected.
Disable the watchdog function by leaving WDI unconnected or by three-stating driver connected to WDI.

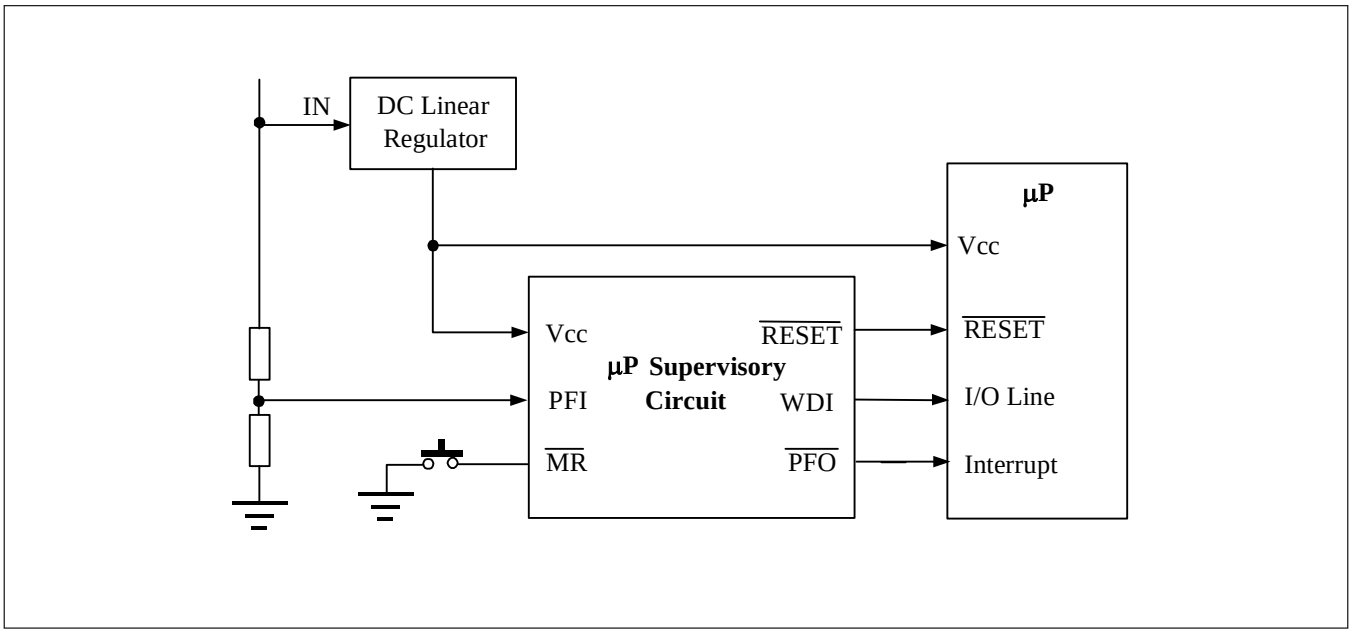
Manual Reset

The manual-reset input ($\overline{\text{MR}}$) allows reset to be triggered by a push button switch. $\overline{\text{MR}}$ has an internal pullup resistor, so it can be left open when not used.

Power-Fail Comparator

The power-fail comparator can be used for various purposes because its output and noninverting input are not internally connected. The inverting input is internally connected to a 1.25V reference.

Typical Application Circuit



Detailed Specifications

Absolute Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Ambient Temperature with Power Applied ..... -40°C to +85°C
Supply Voltage to Ground Potential (Vcc to GND) ..... -0.3V to +7.0V
DC Input Voltage (All inputs except Vcc and GND) ..... -0.3V to V_{CC}+0.3V
DC Output Current (All outputs) 20mA
Power Dissipation 320mW
(Depend on package)

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Condition

DC Electrical Characteristics

Sym	Description	Test Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage for 7xxxL/M/J		4.5	5.0	5.5	V
	Supply Voltage for 7xxxT/S		3.0	3.3	5.5	V
	Supply Voltage for 7xxxR/Z/Y		2.7	3.0	5.5	V
V_{IH}	Input High Voltage		$0.7V_{CC}$			V
V_{IL}	Input Low Voltage				$0.3V_{CC}$	V
T_A	Operating Temperature		-40		85	°C

DC Electrical Characteristics

(Vcc=V_{RN}+5% to 5.5V, T_A= -40~85°C, unless otherwise noted)

Symbol	Description	Test Conditions		Min	Typ	Max	Unit
V_{CC}	Operating Voltage Range	-		1	-	5.5	V
I_{CC}	Supply Current	Vcc = 5V, No load	7803/09/10/11/12	-	6	18	µA
			7823/24/25, 73xx	-	13	36	
V_{IH}	Input High Voltage	Pin: $\overline{MR}$, WDI		0.7×Vcc	-	-	V
V_{IL}	Input Low Voltage	Pin: $\overline{MR}$, WDI		-	-	0.3×Vcc	V
V_{RST}	Reset Threshold Voltage(Note1)	T_A= 25°C	PT7M7xxx(except 7809R/M)	V_{RN}-1.5%	V_{RN}	V_{RN}+1.5%	V
			PT7M7809R	V_{RN}-1.0%	V_{RN}	V_{RN}+1.0%	
			PT7M7809M	4.273	4.330	4.386	
		TA= -40~85°C	PT7M7xxxL	4.514	4.63	4.746	
			PT7M7xxxM(except 7809M)	4.271	4.380	4.490	
			PT7M7809M	4.221	4.330	4.438	
			PT7M7xxxT	3.003	3.08	3.157	
			PT7M7xxxJ	3.890	4.00	4.10	
			PT7M7xxxS	2.857	2.93	3.003	
			PT7M7xxxR	2.564	2.63	2.696	
			PT7M7xxxZ	2.262	2.32	2.378	
			PT7M7xxxY	2.145	2.20	2.255	
V_{RTH}	Reset Threshold Hysteresis(Note 1)	Vcc varies between V_{RN}±5%	PT7M7823/24/25L/M/T/S	-	12	-	mV
			PT7M7823/24/25R	-	4	-	
			Others	-	50	-	
V_{OH}	Output High Voltage(Except PT7M7823/24/25)	Vcc ≥ 4.5V Isource=800µA		Vcc-1.5	-	-	V
		Vcc ≥ 2.7V Isource=500µA		0.8×Vcc	-	-	
		Vcc ≥ 1.8V Isource=150µA		0.8×Vcc	-	-	
		Vcc ≥ 1.0V Isource=4µA		0.8×Vcc	-	-	
	Output High Voltage(PT7M7823/24/25)	PT7M7823/24/25L/M, Vcc = V_{RST} Max, I_{SOURCE}=120uA		Vcc-1.5	-	-	
		PT7M7823/24/25T/S/R, Vcc=V_{RST} Max, I_{SOURCE}=30uA		0.8×Vcc	-	-	
V_{OL}	Output Low Voltage	Vcc ≥ 4.5V Isink=3.2mA		-	-	0.4	V
		Vcc ≥ 2.7V Isink=1.2mA		-	-	0.3	
		Vcc ≥ 1.0V Isink=100µA		-	-	0.3	
I_{LKG}	Open-Drain Output Leakage Current	V_{CC} > V_{TH}(MAX) for PT7M7803 and PT7M7343		-	-	1	µA
V_{PFT}	PFI Input Threshold	V_{PFI} varies from 1.5V and 1.0V		1.2	1.25	1.3	V
I_{PFI}	PFI Input Leakage Current	-		-	-	±25	nA
I_{WDI}	Average WDI Input Current (Note 2)	WDI connected to V_{CC}: 5.5V		-	120	160	µA
		WDI connected to GND		-20	-15	-	
I_{source}	$\overline{RESET}$ Output Short-Circuit Current (only for PT7M7823/24/25)	PT7M7823/24/25L/M, $\overline{RESET}$=0V, Vcc=5.5V		-	-	800	µA
		PT7M7823/24/25T/S/R, $\overline{RESET}$=0V, Vcc=3.6V		-	-	400	
r	MR pull-up resistor (internal)	PT7M7811/7812		10	20	30	kΩ
		PT7M7823/7824/7825		35	52	75	
		PT7M7342/7343/7344		60	-	-	

* Valid for both $\overline{RESET}$ and RESET. V_{RST} is voltage threshols when V_{CC} falls from high to low. V_{RN} is nominal reset threshold voltage.

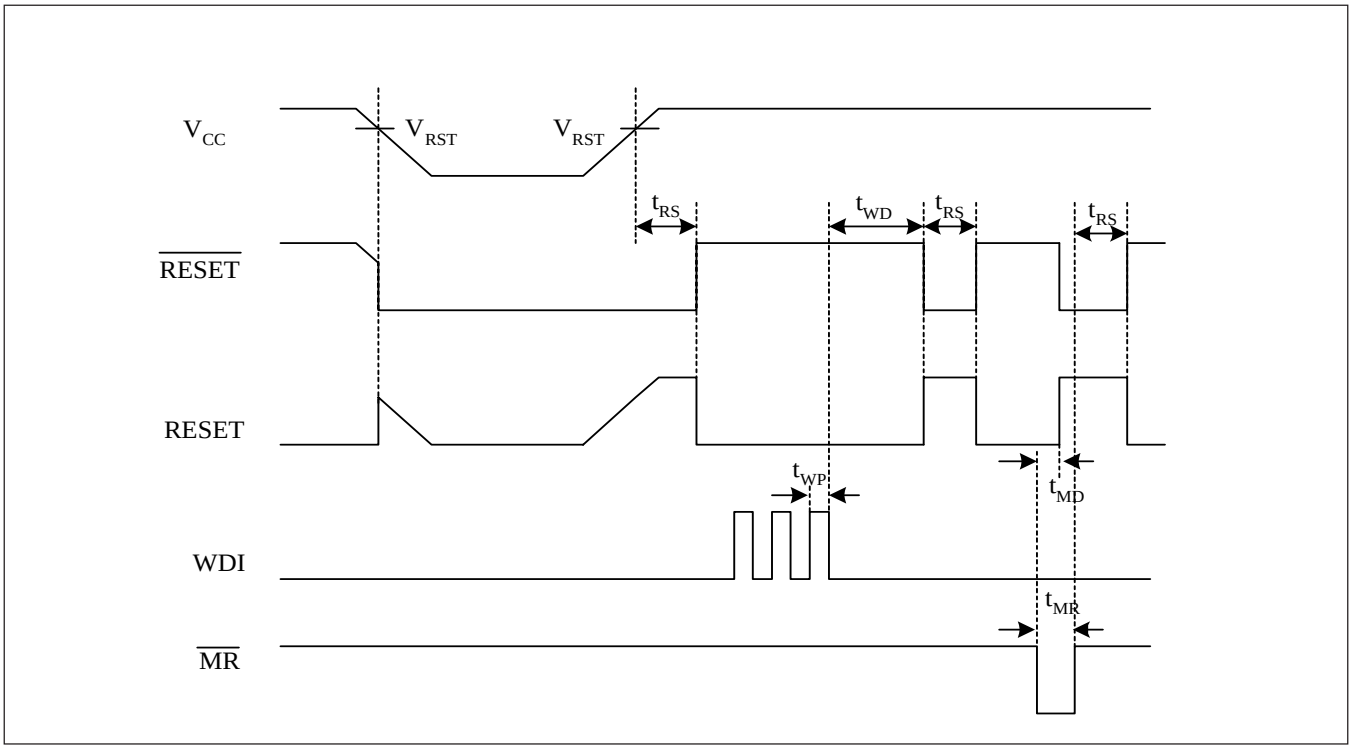
** WDI is internally serviced within the watchdog period if WDI is left unconnected.

AC Electrical Characteristics

AC Electrical Characteristics

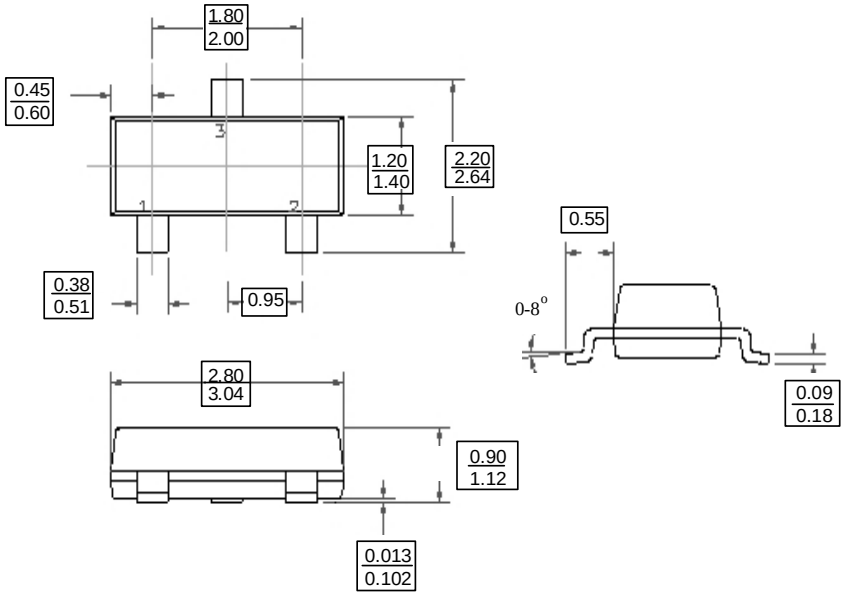
Sym	Description	Test Conditions	Min	Typ	Max	Units
t_{RS}	Reset Pulse Width	$\overline{MR}$ from low to High, T_A=25C	140	200	400	ms
t_{WD}	Watchdog Timeout Period	WDI and $\overline{MR}$ tied to V_{CC}, $V_{CC} > V_{RN} + 5\%$ T_A=25C	0.9	1.6	2.25	s
t_{MR}	$\overline{MR}$ Pulse Width		1			µs
t	$\overline{MR}$ to RESET Delay	V = 5.0V			250	ns
t_{WP}	WDI Pulse Width		50			ns

Watchdog Timing Diagram



Mechanical Information

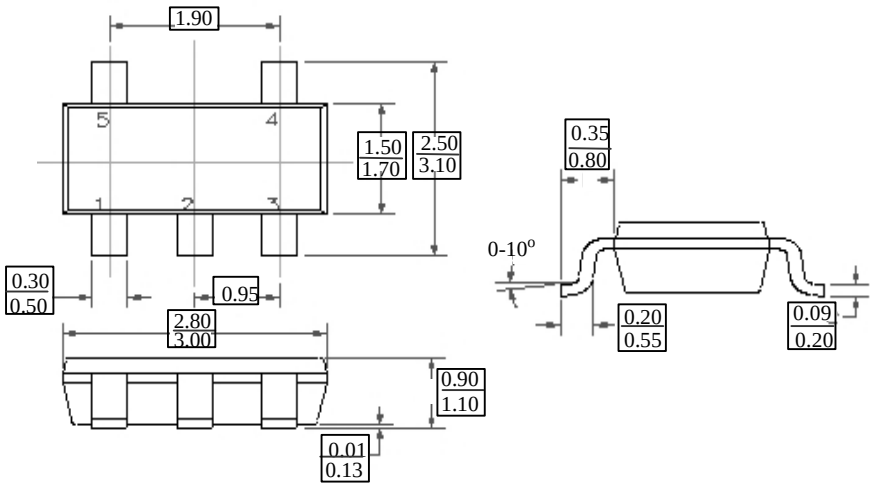
SOT23-3



X.XX / X.XX DENOTES DIMENSIONS IN MILLIMETERS

Note:
1) Controlling dimensions in millimeters.
2) Ref: JEDEC TO-236AB

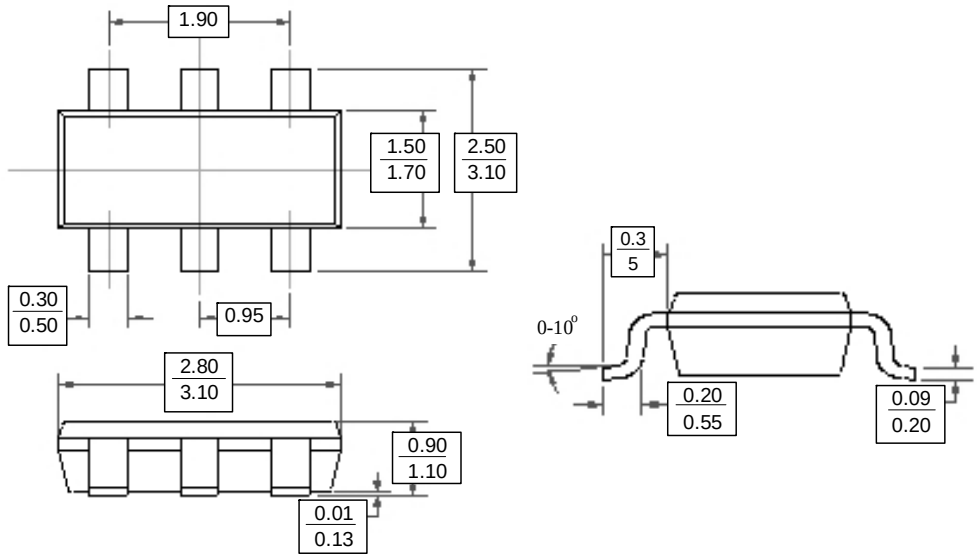
SOT23-5



X.XX / X.XX DENOTES DIMENSIONS IN MILLIMETERS

Note:
1) Controlling dimensions in millimeters.
2) Ref: JEDEC MO-178AA

SOT23-6

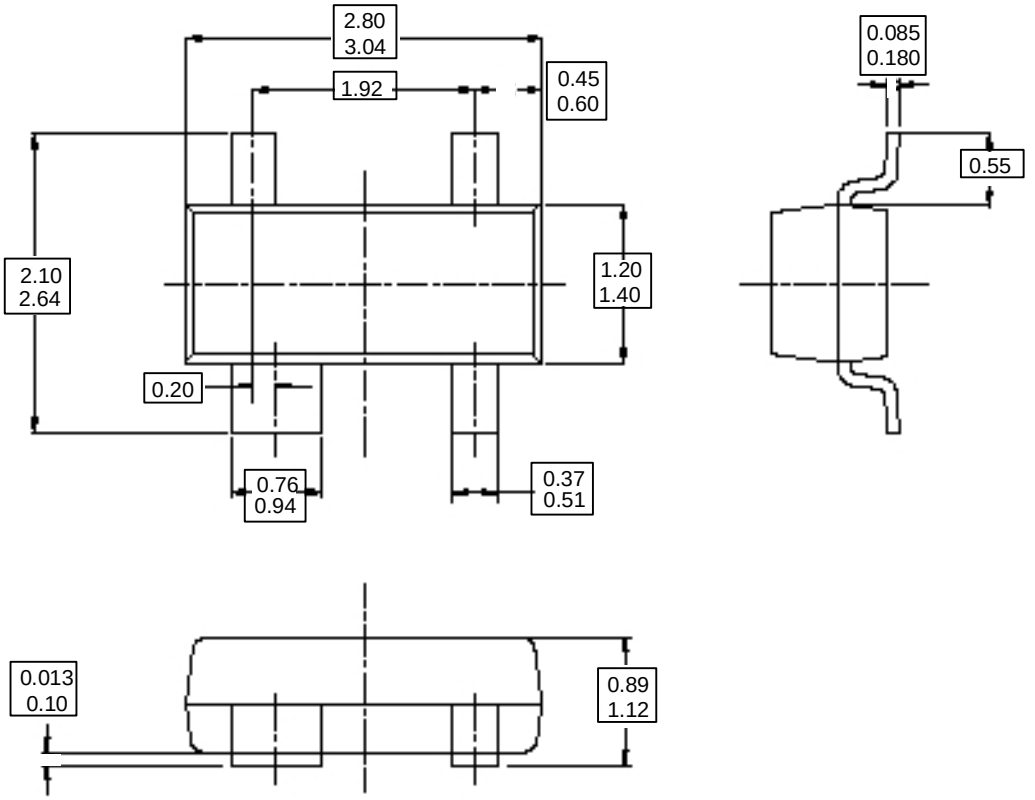


X.XX / X.XX — DENOTES DIMENSIONS IN MILLIMETERS

Note:

1) Controlling dimensions in millimeters.
2) Ref: JEDEC MO-178AB

SOT143



X.XX
X.XX

DENOTES DIMENSIONS
IN MILLIMETERS

Note:

1) Controlling dimensions in millimeters.
2) Dimensions are inclusive of plating.

Notes

Pericom Technology Inc.

Email: support@pti.com.cn Web-Site: www.pti.com.cn, www.pti-ic.com

China: No. 20 Building, 3/F, 481 Guiping Road, Shanghai, 200233, China
Tel: (86)-21-6485 0576 Fax: (86)-21-6485 2181

Asia Pacific: Unit 1517, 15/F, Chevalier Commercial Centre, 8 Wang Hoi Rd, Kowloon Bay, Hongkong
Tel: (852)-2243 3660 Fax: (852)- 2243 3667

U.S.A.: 3545 North First Street, San Jose, California 95134, USA
Tel: (1)-408-435 0800 Fax: (1)-408-435 1100