TQP3M9007

¼W High Linearity LNA Gain Block

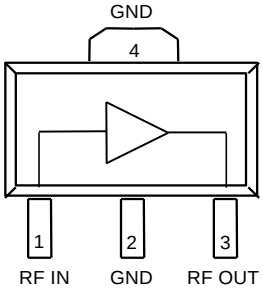
Product Description

The TQP3M9007 is a high linearity low noise gain block amplifier in a low-cost surface-mount package. At 1.9 GHz, the amplifier typically provides 13 dB gain, +41 dBm OIP3, and 1.3 dB Noise Figure while drawing 125 mA current. The device is housed in a lead free / green / RoHS-compliant industry-standard SOT-89 package.

The TQP3M9007 has the benefit of having high linearity while also providing very low noise across a broad range of frequencies. This allows the device to be used in both receive and transmit chains for high performance systems. The amplifier is internally matched using a high performance E-pHEMT process and only requires an external RF choke and blocking/bypass capacitors for operation from a single +5 V supply. The internal active bias circuit also enables stable operation over bias and temperature variations.

The TQP3M9007 covers the 0.1 – 4 GHz frequency band and is targeted for wireless infrastructure or other applications requiring high linearity and/or low noise figure.

Functional Block Diagram



SOT-89 Package

Product Features

- 100 – 4000 MHz
- 13 dB Gain at 1.9 GHz
- 1.3 dB Noise Figure at 1.9 GHz
- +41 dBm Output IP3
- +23.6 dBm P1dB
- 50 Ω Cascadable Gain Block
- Unconditionally Stable
- High Input Power Capability
- +5 V Single Supply, 125 mA Current
- SOT-89 Package

Applications

- Repeaters
- Mobile Infrastructure
- LTE / WCDMA / CDMA / EDGE
- General Purpose Wireless

Ordering Information

Part No.	Description
TQP3M9007	1000 pieces on a 7” reel (standard)
TQP3M9007-PCB	0.5 – 4 GHz Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−55 to +150°C
RF Input Power, CW, 50 Ω, T=25 °C	+20 dBm
Device Voltage (V_{DD})	+7 V

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (V_{DD})	+3.0	+5.0	+5.25	V
T_{CASE}	−40		+105	°C
Tj for >10^6 hours MTTF			+190	°C

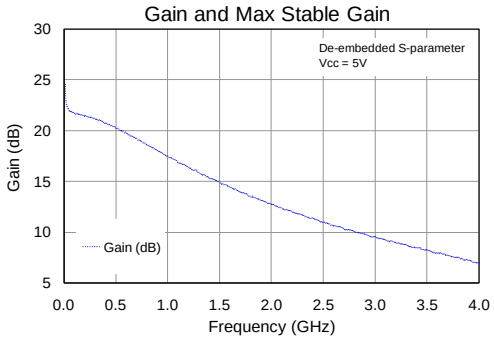
Electrical specifications are measured under bias, signal and temperature conditions as specified. Specifications are not guaranteed over all recommended operating conditions.

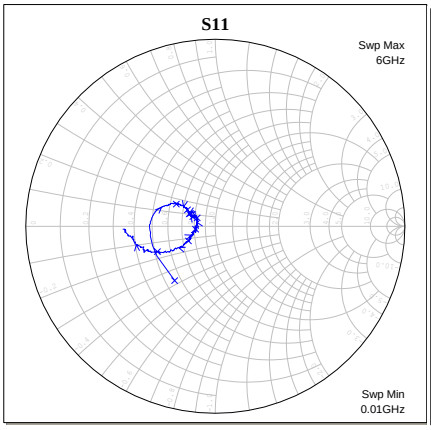
Electrical Specifications

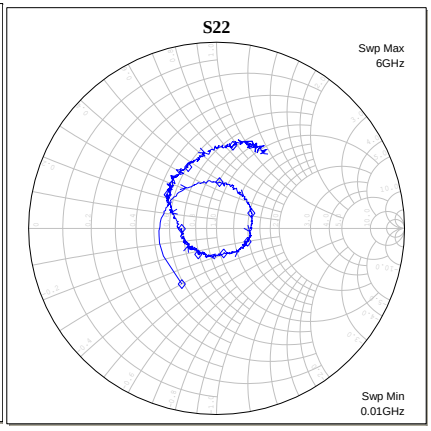
Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		100		4000	MHz
Test Frequency			1900		MHz
Gain		11.5	13	14.5	dB
Input Return Loss			18		dB
Output Return Loss			13		dB
Output P1dB			+23.6		dBm
Output IP3	See Note 1.	+37	+41		dBm
Noise Figure			1.3		dB
Current, I_{DD}			125	150	mA
Thermal Resistance, θ_{jc}	Junction to case		52		°C / W

Notes:
1. Test conditions unless otherwise noted: V_{DD}=+5 V, Temp=+25 °C, 50 Ω system
2. OIP3 is measured with two tones at an output power of 4 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule. 2:1 rule gives relative value with respect to fundamental tone.

Device Characterization Data





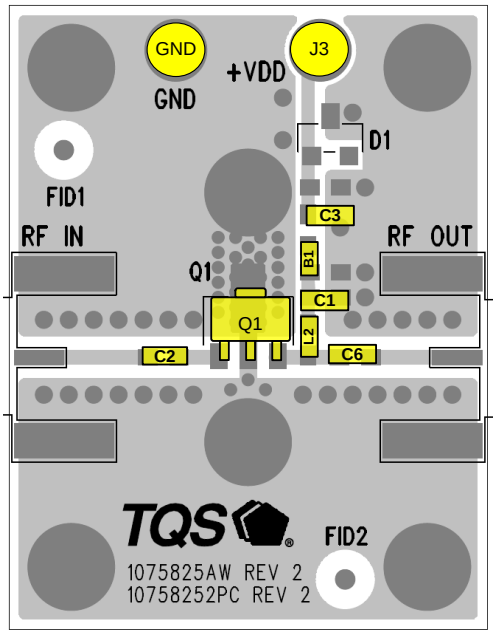


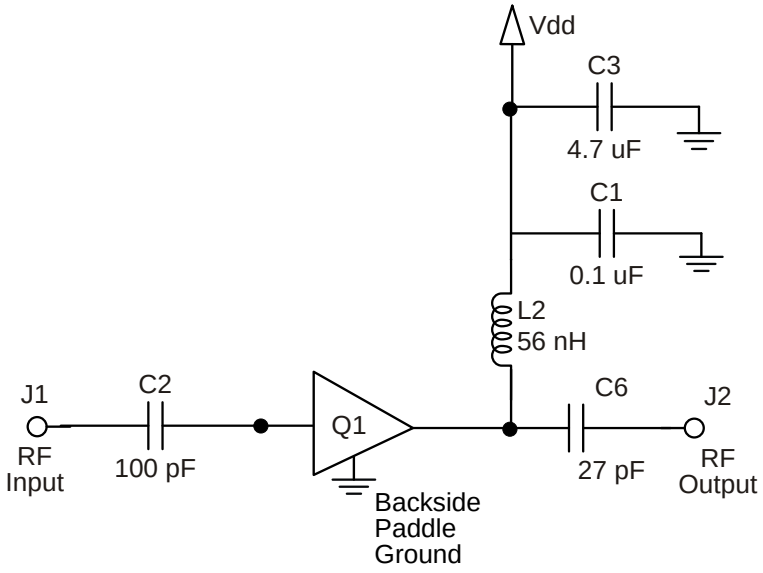
S-Parameters

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	−9.21	−171.69	21.92	165.87	−28.66	7.52	−10.26	−177.68
100	−9.18	178.66	21.72	164.31	−28.54	8.08	−10.62	166.81
200	−9.58	168.58	21.39	154.89	−28.25	11.48	−10.93	145.14
400	−11.09	155.91	20.71	134.86	−27.05	16.59	−11.61	112.74
800	−13.55	148.37	18.58	99.19	−24.58	17.74	−12.39	63.78
1000	−14.69	147.37	17.47	84.06	−23.58	14.87	−13.43	40.99
1200	−15.31	148.14	16.33	70.48	−22.59	12.31	−13.72	23.70
1500	−16.32	152.38	14.85	52.18	−21.45	6.08	−14.84	−3.77
1900	−16.36	155.45	13.11	30.26	−19.96	−2.85	−15.21	−32.08
2000	−16.44	154.43	12.73	25.52	−19.77	−5.72	−15.43	−42.20
2200	−16.55	154.33	11.98	15.20	−19.13	−12.30	−16.18	−54.41
2500	−16.78	153.75	10.97	0.51	−18.24	−20.16	−16.76	−84.02
2600	−16.83	154.69	10.59	−4.70	−18.14	−23.60	−16.24	−91.43
3000	−17.62	157.51	9.53	−24.26	−17.17	−36.43	−16.21	−128.42
3500	−18.79	154.34	8.24	−48.07	−16.19	−53.90	−14.74	−165.72
4000	−20.11	176.37	7.01	−72.56	−15.53	−72.99	−11.54	154.74

Notes:
1. Test Conditions: V_{DD}=+5 V, I_{DD}=125 mA, T=+25 °C, 50 ohm system, calibrated to device leads

Application Circuit Configuration





Notes:
1. See PC Board Layout, under Application Information section, for more information.
2. Components shown on the silkscreen but not on the schematic are not used.
3. B1 (0 Ω jumper) may be replaced with copper trace in the target application layout.
4. All components are of 0603 size unless stated on the schematic.
5. C6 and L2 value are critical for linearity performance.

Bill of Material – TQP3M9007-PCB

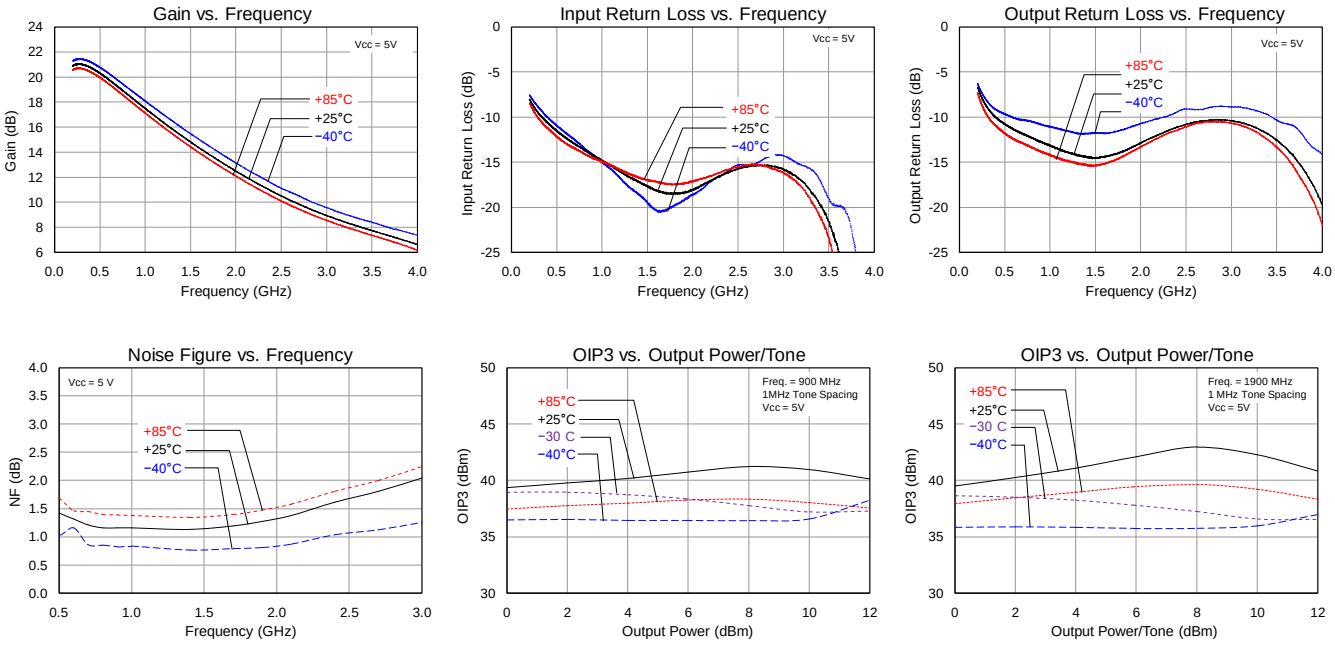
Reference Designation	Value	Description	Manufacturer	Part Number
Q1		High Linearity LNA Gain Block	Qorvo	TQP3M9007
C2	100 pF	Cap, Chip, 0603, +50V, NPO, 5%	various	
C6	27 pF	Cap, Chip, 0603, +50V, NPO, 5%	various	
C1	0.1 µF	Cap, Chip, 0603, +16V, X7R, 10%	various	
L2	56 nH	Ind, Chip, 0603, 5%	various	
C3	4.7 µF	Cap, Chip, 0603, +6.3V, X5R, 20%	various	
B1	0 Ω	Res, Chip, 0603, 1/16W, 5%	various	

Typical Performance – TQP3M9007-PCB

Parameter	Typical Value					Units
Frequency	500	900	1900	2100	2600	MHz
Gain	20	18	13	12	10	dB
Input Return Loss	11.5	14	18	17.5	15.5	dB
Output Return Loss	10.5	13	13	12	10.5	dB
Output P1dB	+22.9	+23.3	+23.5	+23.8	+24.0	dBm
OIP3 (2)	+39.3	+40.2	+41.1	+42.2	+42.2	dBm
Noise figure (3)	1.4	1.2	1.3	1.4	1.8	dB

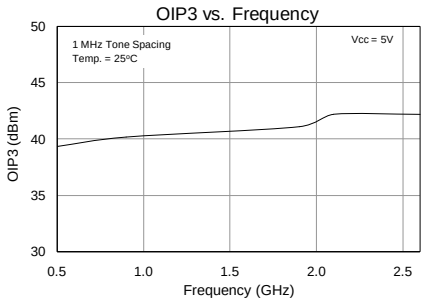
Notes:
1. Test conditions unless otherwise noted: V_{DD}=+5 V, I_{DD}=125mA, Temp=+25°C, 50 Ω system.
2. OIP3 measured with two tones at an output power of +4 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule.
3. Noise figure data shown in the table above is measured on evaluation board and corrected for the board loss of about 0.13 dB at 1.9 GHz.

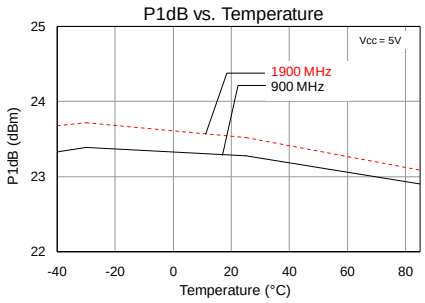
Performance Plots – TQP3M9007-PCB

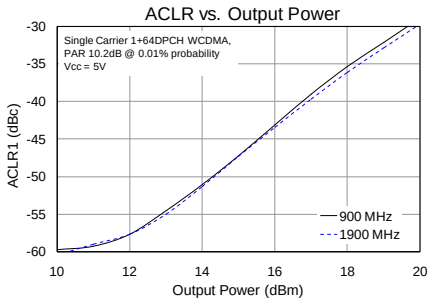


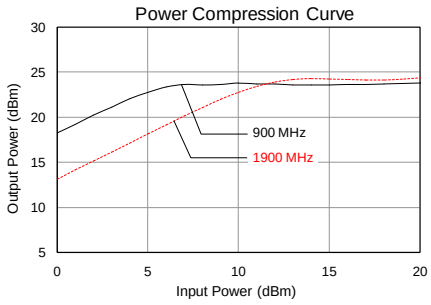
Notes:
1. Performance plots data is measured using TQP3M9007-PCB. Noise figure plot has been corrected for evaluation board loss of 0.13 dB at 1.9 GHz.
2. Test conditions unless otherwise noted: V_{DD}=+5 V, I_{DD}=125 mA, Temp=+25°C, 50 Ω system.

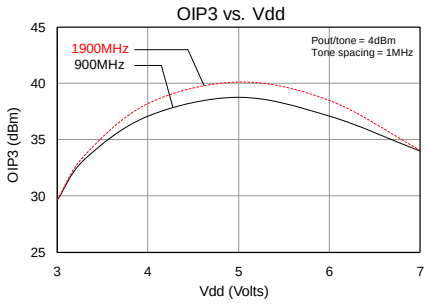
Performance Plots – TQP3M9007-PCB

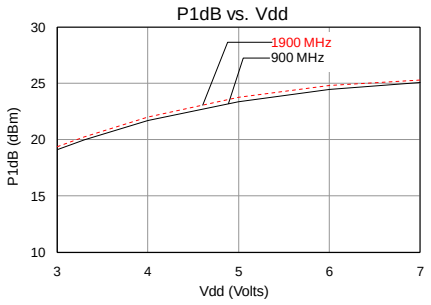


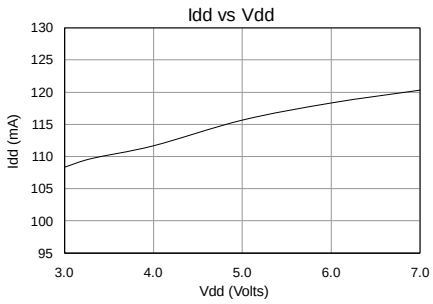






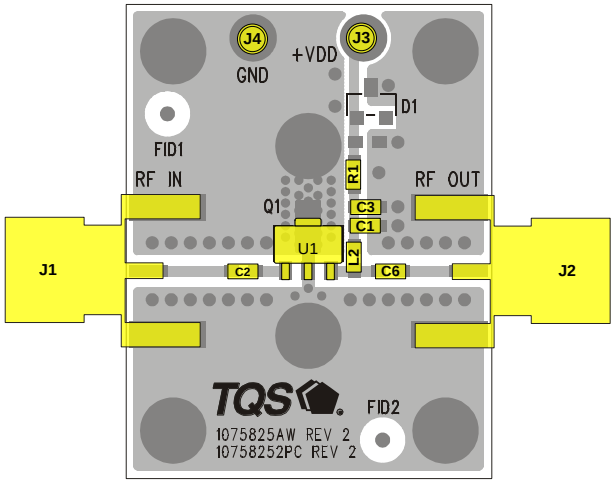


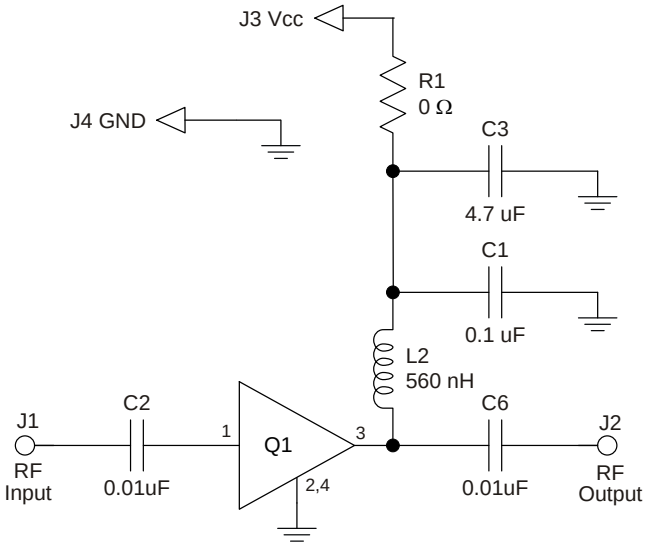




Notes:
1. Performance plots data is measured using TQP3M9007-PCB. Noise figure plot has been corrected for evaluation board loss of 0.13 dB at 1.9 GHz.
2. Test conditions unless otherwise noted: V_{DD}=+5 V, I_{DD}=125 mA, Temp=+25°C, 50 Ω system.

Application Circuit Configuration – 30 to 500 MHz





Notes:
1. See PC Board Layout, under Application Information section, for more information.
2. Components shown on the silkscreen but not on the schematic are not used.
3. The recommended component values are dependent on the frequency of operation.

Bill of Material − TQP3M9007 – 30 to 500 MHz

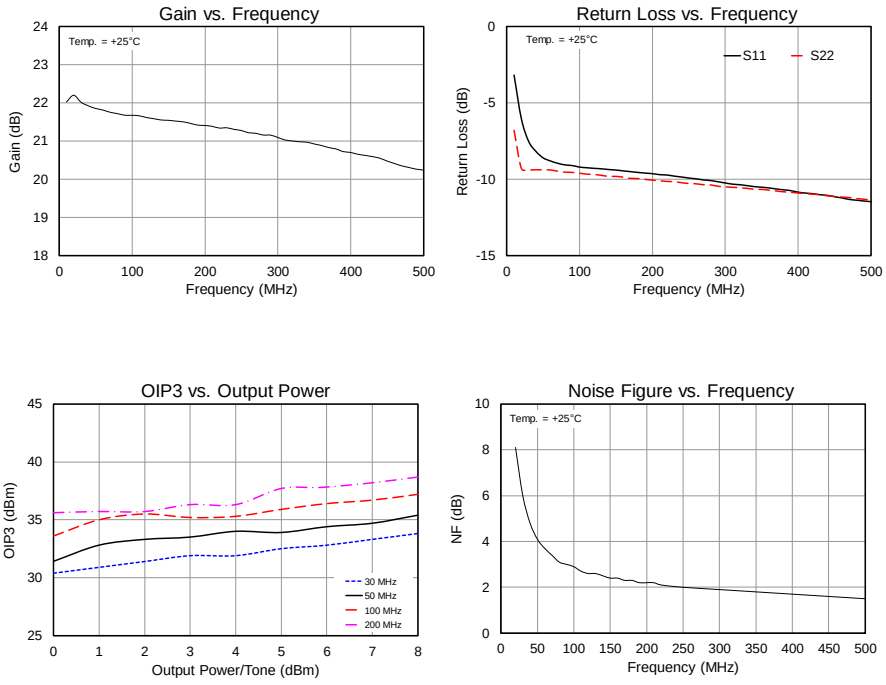
Reference Designation	Value	Description	Manufacturer	Part Number
Q1		High Linearity LNA Gain Block	Qorvo	TQP3M9007
C2, C6	0.01 uF	Cap, Chip, 0603, +50V, X7R, 5%	various	
C1	0.1 µF	Cap, Chip, 0603, +16V, X7R, 10%	various	
L2	560 nH	Ind, Chip, 0603, 5%	various	
C3	4.7 µF	Cap, Chip, 0603, +6.3V, X5R, 20%	various	
R1	0 Ω	Res, Chip, 0603, 1/16W, 5%	various	

Typical Performance − TQP3M9007 – 30 to 500 MHz

Parameter	Typical Value			Units
Frequency	30	100	200	MHz
Gain	22	21.7	21.4	dB
Input Return Loss	7.5	9.2	9.6	dB
Output Return Loss	9.4	9.6	10.1	dB
Output P1dB	+23.2	+23.3	+23.4	dBm
OIP3 (2)	+31.9	+35.3	+36.3	dBm
Noise figure	6.0	4.1	2.2	dB

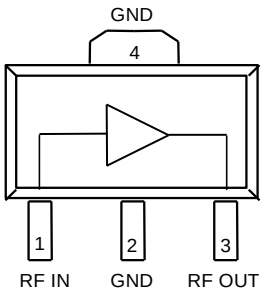
Notes:
1. Test conditions unless otherwise noted: V_{DD}=+5 V, I_{DD}=125 mA, Temp=+25°C, 50 Ω system.
2. OIP3 measured with two tones at an output power of +4 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule.

Performance Plots − TQP3M9007 – 30 to 500 MHz



Notes:
1. Test conditions unless otherwise noted: V_{DD}=+5 V, I_{DD}=125 mA, Temp=+25°C, 50 Ω system.

Pin Configuration and Description



Pin No.	Label	Description
1	RF Input	Input, matched to 50 ohms. External DC Block is required.
3	V_{dd} / RFout	Output, matched to 50 ohms, External DC Block is required and supply voltage.
2, 4	GND Paddle	Backside Paddle. Multiple vias should be employed to minimize inductance and thermal resistance; see page 7 for mounting configuration.

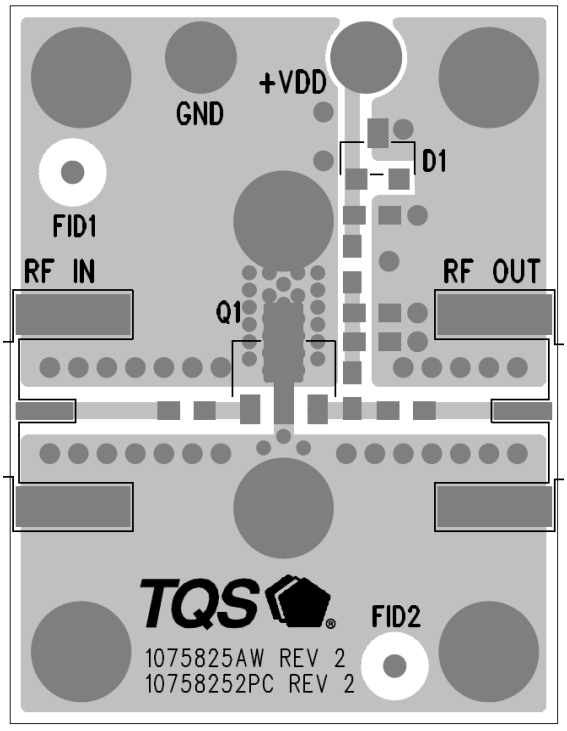
Applications Information

PCB Board Layout

Top RF layer is .014" NELCO N4000-13, ϵ_r = 3.9, 4 total layers (0.062" thick) for mechanical rigidity. Metal layers are 1-oz copper. 50 ohm Microstrip line details: width = .029", spacing = .035"

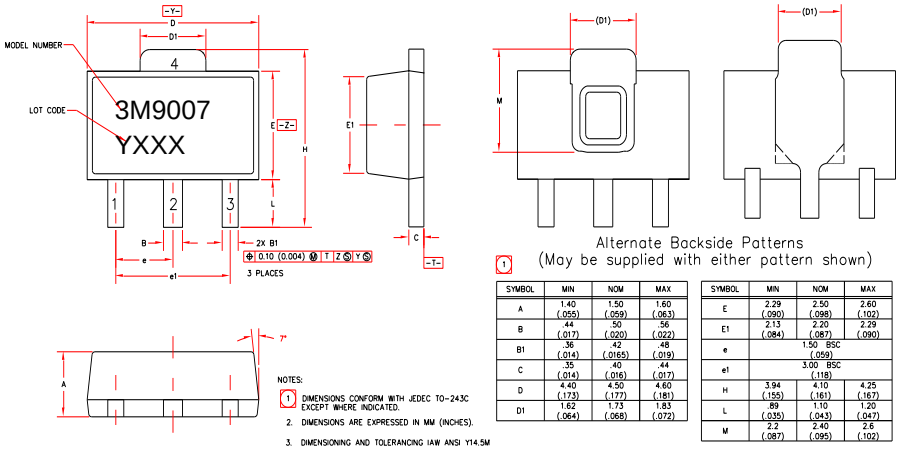
The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

For further technical information, Refer to www.tiquint.com



Package Marking and Dimensions

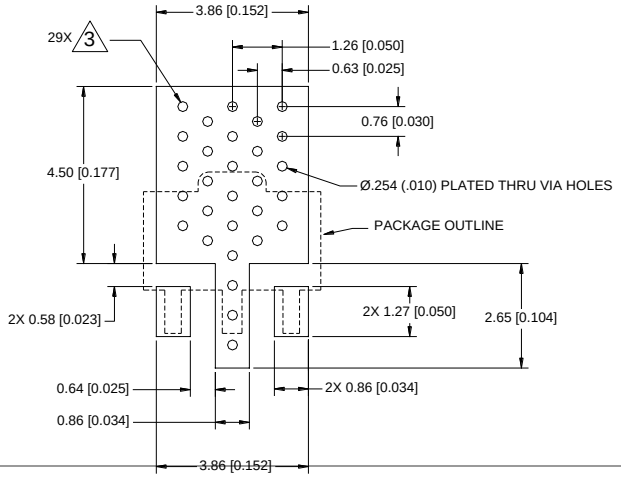
Part number: 3M9007
Assembly code: ‘Y’ is last digit of part manufacture year. ‘XXX’ is lot code.



SYMBOL	MIN	NOM	MAX
A	1.40 (.055)	1.50 (.059)	1.60 (.063)
B	.44 (.017)	.50 (.020)	.56 (.022)
B1	.36 (.014)	.42 (.0165)	.48 (.019)
C	.35 (.014)	.40 (.016)	.44 (.017)
D	4.40 (.173)	4.50 (.177)	4.60 (.181)
D1	1.62 (.064)	1.73 (.068)	1.83 (.072)

SYMBOL	MIN	NOM	MAX
E	2.29 (.090)	2.50 (.098)	2.60 (.102)
E1	2.13 (.084)	2.20 (.087)	2.29 (.090)
e		1.50 BSC (.059)	
e1		3.00 BSC (.118)	
H	3.94 (.155)	4.10 (.161)	4.25 (.167)
L	.89 (.035)	1.10 (.043)	1.20 (.047)
M	2.2 (.087)	2.40 (.095)	2.6 (.102)

PCB Mounting Pattern



Notes:

1. All dimensions are in millimeters[inches]. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25mm (0.10”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1A	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (HBM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: NiPdAu

RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment). This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free
- Qrovo Green

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com
Tel: 1-844-890-8163
Email: customer.support@qorvo.com

For technical questions and application information:

Email: sjcapplications.engineering@qorvo.com

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