10A EcoSpeed® Integrated FET Regulator with Programmable LDO

Features

- Power System
  - Input voltage — 3V to 28V
  - Bias voltage — 3V to 5.5V LDO or external
  - Up to 96% peak efficiency
  - Integrated bootstrap switch
  - Programmable LDO output — 200mA
  - Reference tolerance — 1% T_J= -40 to +125 °C
  - Programmable soft start time
- Logic Input/Output Control
  - Independent EN controls for LDO and switcher
  - Programmable V_{IN} UVLO threshold
  - Power good output
  - Selectable PSAVE or FCM mode
- Protection
  - Over-voltage and under-voltage
  - TC compensated $R_{DS(ON)}$ sensed current limit
  - Thermal Shutdown
- Output Capacitor Types
  - High ESR — SP, POSCAP, OSCON
  - Ceramic capacitors
- Package
  - Lead-free package — 5x5mm, 32-Pin MLPQ
  - RoHS/WEEE compliant and Halogen free

Applications

- Networking and telecommunication equipment
- Printers, DSL, and STB applications
- Embedded systems and power supply modules
- Point of load power supplies

Description

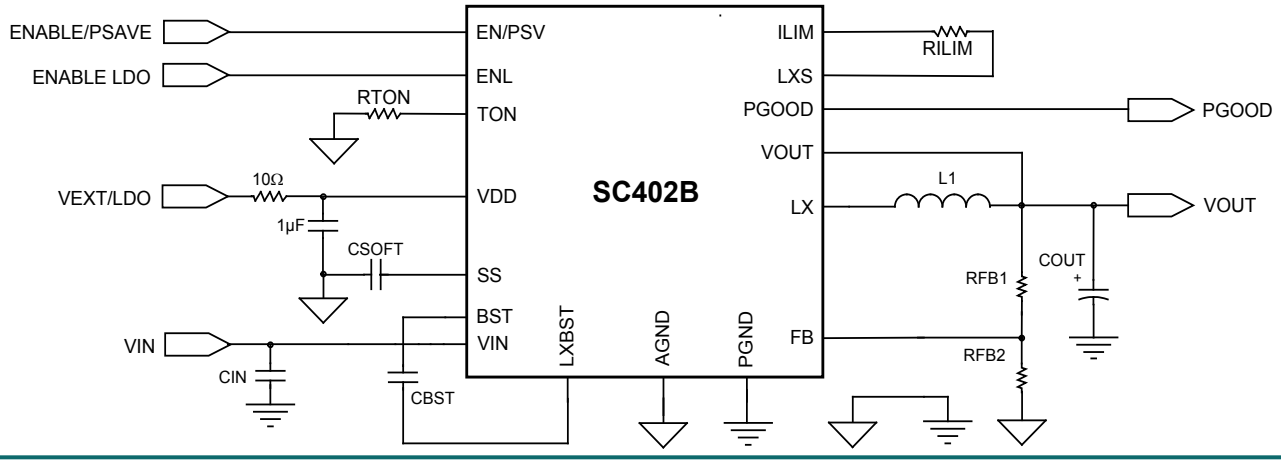
The SC402B is a stand-alone synchronous EcoSpeed® buck power supply which incorporates Semtech's advanced patented adaptive on-time control architecture. This provides excellent light-load efficiency and fast transient response. It features integrated power MOSFETs, a bootstrap switch, and a programmable LDO in a 5x5mm package. The device is highly efficient and uses minimal PCB area. The SC402B has the same package and pin configuration as the entire SC40x series for compatibility.

The SC402B supports using standard capacitor types such as electrolytic or specialty polymer, in addition to ceramic, at switching frequencies up to 1MHz. The programmable frequency, synchronous operation, and selectable power-save provide high efficiency operation over a wide load range.

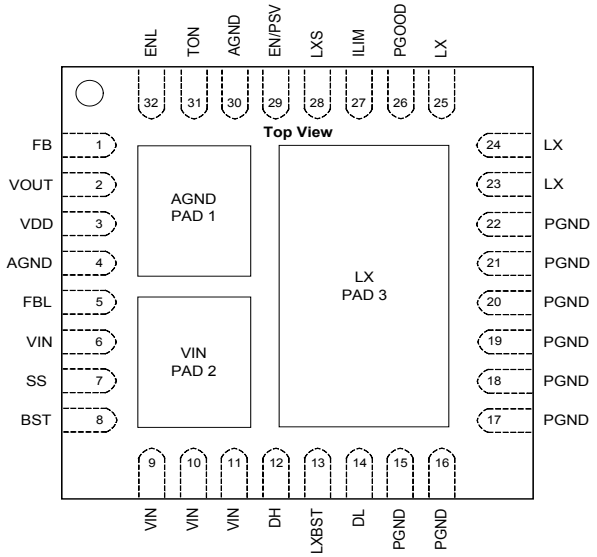
Additional features include a programmable soft-start, programmable cycle-by-cycle over-current limit protection, under-voltage and over-voltage protection, soft shutdown, and selectable power-save operation. The device also provides separate enable inputs for the PWM controller and LDO as well as a power good output for the PWM controller.

The wide input and programmable frequency make the device extremely flexible and easy to use in a broad range of applications.

Typical Application Circuit



Pin Configuration



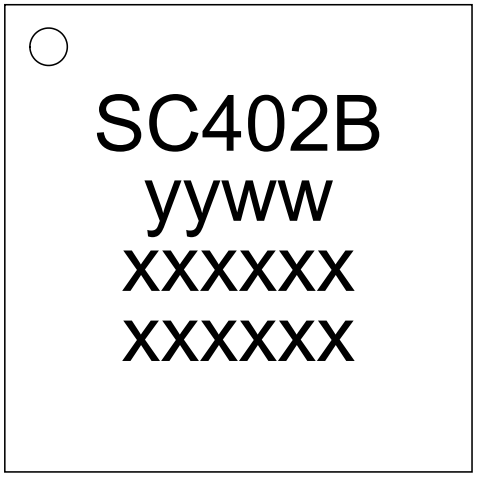
SC402B
MLPQ-32; 5x5, 32 LEAD

Ordering Information

Device	Package
SC402BMLTRT[1][2]	MLPQ-32 5X5
SC402BEVB	Evaluation Board

Notes:
1) Available in tape and reel only. A reel contains 3000 devices.
2) Lead-free, Halogen free, and RoHS/WEEE compliant

Marking Information



yyww = Date Code
xxxxxx = Semtech Lot Number
xxxxxx = Semtech Lot Number

Absolute Maximum Ratings

LX to PGND (V) ..... -0.3 to +30
LX to PGND (V) (transient — 100ns max.) ..... -2 to +30
VIN to PGND (V) ..... -0.3 to +30
VIN to VDD (V) ..... -0.4
EN/PSV, PGOOD, ILIM, to GND (V) ..... -0.3to+(VDD+0.3)
SS, VOUT, FB, FBL, to GND (V) ..... -0.3to+(VDD+0.3)
VDD to PGND (V) ..... -0.3 to +6
TON to PGND (V) ..... -0.3 to +(VDD - 1.5)
ENL (V) ..... -0.3 to V_{IN}
DH, BST to LX (V) ..... -0.3 to +6.0
DH, BST to PGND (V) ..... -0.3 to +35
DL to PGND (V) ..... -0.3 to +6.0
AGND to PGND (V) ..... -0.3 to +0.3
ESD Protection Level[1] (kV) 2

Recommended Operating Conditions

Input Voltage (V) ..... 3.0 to 28
VDD to PGND (V) ..... 3.0 to 5.5
VOUT to PGND (V) ..... 0.6 to 5.5

Thermal Information

Storage Temperature (°C) ..... -60 to +150
Maximum Junction Temperature (°C) 150
Operating Junction Temperature (°C) ..... -40 to +125
Thermal resistance, junction to ambient [2] (°C/W)
High-side MOSFET 25
Low-side MOSFET 20
PWM controller and LDO thermal resistance 50
Peak IR Reflow Temperature (°C) 260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114.
(2) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless specified: V_{IN} =12V, T_A = +25°C for Typ, -40 to +85 °C for Min and Max, T_J < 125°C, VDD = +5V, Typical Application Circuit

Parameter	Conditions	Min	Typ	Max	Units
Input Supplies					
Input Supply Voltage	$V_{IN} \geq$ VDD	3		28	V
VDD Voltage		3		5.5	V
VIN UVLO Threshold[1]	Sensed at ENL pin, rising edge	2.40	2.60	2.95	V
	Sensed at ENL pin, falling edge	2.23	2.40	2.57	
VIN UVLO Hysteresis	EN/PSV = High		0.25		V
VDD UVLO Threshold	Measured at VDD pin, rising edge	2.5		3.0	V
	Measured at VDD pin, falling edge	2.4		2.9	
VDD UVLO Hysteresis			0.2		V
VIN Supply Current	ENL , EN/PSV = 0V, V_{IN} = 28V		10	20	µA
	Standby mode; ENL=VDD, EN/PSV = 0V		130		

Electrical Characteristics (continued)

Parameter	Conditions	Min	Typ	Max	Units
Input Supplies (continued)					
VDD Supply Current	ENL , EN/PSV = 0V, no external 5V VDD		3	7	µA
	ENL , EN/PSV = 0V, external 5V VDD supply		190	300	
	EN/PSV = VDD (PSAVE), No load, VFB > 600mV		0.7		mA
	VDD = 5V, f_{SW} = 250kHz, EN/PSV = floating , no load(2)		8		
	VDD = 3V, f_{SW} = 250kHz, EN/PSV = floating , no load(2)		5		
FB On-Time Threshold	Static V_{IN} and load, T_J = 0 to +125 °C	0.595	0.6	0.605	V
	Static V_{IN} and load, T_J = 40 to +125 °C	0.594	0.6	0.606	V
Frequency Range	Continuous mode operation (FCM)			1000	kHz
Bootstrap Switch Resistance			10		Ω
Timing					
On-Time	Continuous mode operation, V_{IN} = 12V, V_{OUT} = 5V, f_{SW}= 300kHz, R_{TON} = 133kΩ	999	1110	1220	ns
Minimum On-Time (2)			80		ns
Minimum Off-Time (2)	VDD = 5V		250		ns
	VDD = 3V		370		
Soft-Start					
Soft-Start Current			3.0		µA
Soft-Start Voltage(2)	When V_{OUT} reaches regulation		1.5		V
Analog Inputs/Outputs					
VOUT Input Resistance			500		kΩ
Current Sense					
Zero-Crossing Detector Threshold	LX - PGND	-3	0	+3	mV
Power Good					
Power Good Threshold	Upper limit, V_{FB} > internal 600mV reference		+20		%
	Lower limit, V_{FB} < internal 600mV reference		-10		%
Start-Up Delay Time (between PWM enable and PGOOD high)	VDD = 5V, C_{SS} = 10nF		12		ms
	VDD = 3V, C_{SS} = 10nF		7		

Electrical Characteristics (continued)

Parameter	Conditions	Min	Typ	Max	Units
Power Good (continued)					
Power Good start-up Delay Threshold on SS pin	SS voltage when PGOOD goes high		64		%VDD
Fault (noise immunity) Delay Time[2]			5		µs
Leakage				1	µA
Power Good On-Resistance			10		Ω
Fault Protection					
Valley Current Limit [3]	VDD = 5V, R_{ILIM} = 6810, T_J = 0 to +125 °C	8.5	10	11.5	A
	VDD = 3V, R_{ILIM} = 6810		9		
I_{LIM} Source Current			10		µA
I_{LIM} Comparator Offset	With respect to AGND	-10	0	+10	mV
Output Under-Voltage Fault	V_{FB} with respect to internal 600mV reference, 8 consecutive clocks		-25		%
Smart Power-save Protection Threshold [2]	V_{FB} with respect to internal 600mV reference		+10		%
Over-Voltage Protection Threshold	V_{FB} with respect to internal 600mV reference		+20		%
Over-Voltage Fault Delay[2]			5		µs
Over-Temperature Shutdown[2]	10°C hysteresis		150		°C
Logic Inputs/Outputs					
Logic Input High Voltage	ENL	1.0			V
Logic Input Low Voltage	ENL			0.4	V
EN/PSV Input for PSAVE Operation [2]	VDD = 5V	2.2		5	V
EN/PSV Input for Forced Continuous Operation [2]		1		2	V
EN/PSV Input for Disabling Switcher		0		0.4	V
EN/PSV Input Bias Current	EN/PSV= VDD or AGND	-10		+10	µA
ENL Input Bias Current	ENL = V_{IN} = 28V		10	18	µA
FBL, FB Input Bias Current	FBL, FB = VDD or AGND	-1		+1	µA

Electrical Characteristics (continued)

Parameter	Conditions	Min	Typ	Max	Units
Linear Regulator (LDO)					
FBL Accuracy	VLDO load = 5mA	0.728	0.75	0.773	V
LDO Current Limit	Short-circuit protection, V_{IN} = 12V, V_{DD} < 0.75V		65		mA
	Start-up and foldback, V_{IN} = 12V, 0.75 < V_{DD} < 90% of final V_{DD} value		115		
	Operating current limit, V_{IN} = 12V, V_{DD} > 90% of final V_{DD} value	135	200		
VLDO to VOUT Switch-over Threshold (4)		-130		+130	mV
VLDO to VOUT Non-switch-over Threshold (4)		-500		+500	mV
VLDO to VOUT Switch-over Resistance	V_{OUT} = +5V		2		Ω
LDO Drop Out Voltage (5)	From V_{IN} to V_{DD}, V_{DD} = +5V, I_{VLDO} = 100mA		1.2		V

Notes:

(1) V_{IN} UVLO is programmable using a resistor divider from VIN to ENL to AGND. The ENL voltage is compared to an internal reference.

(2) Typical value measured on standard evaluation board.

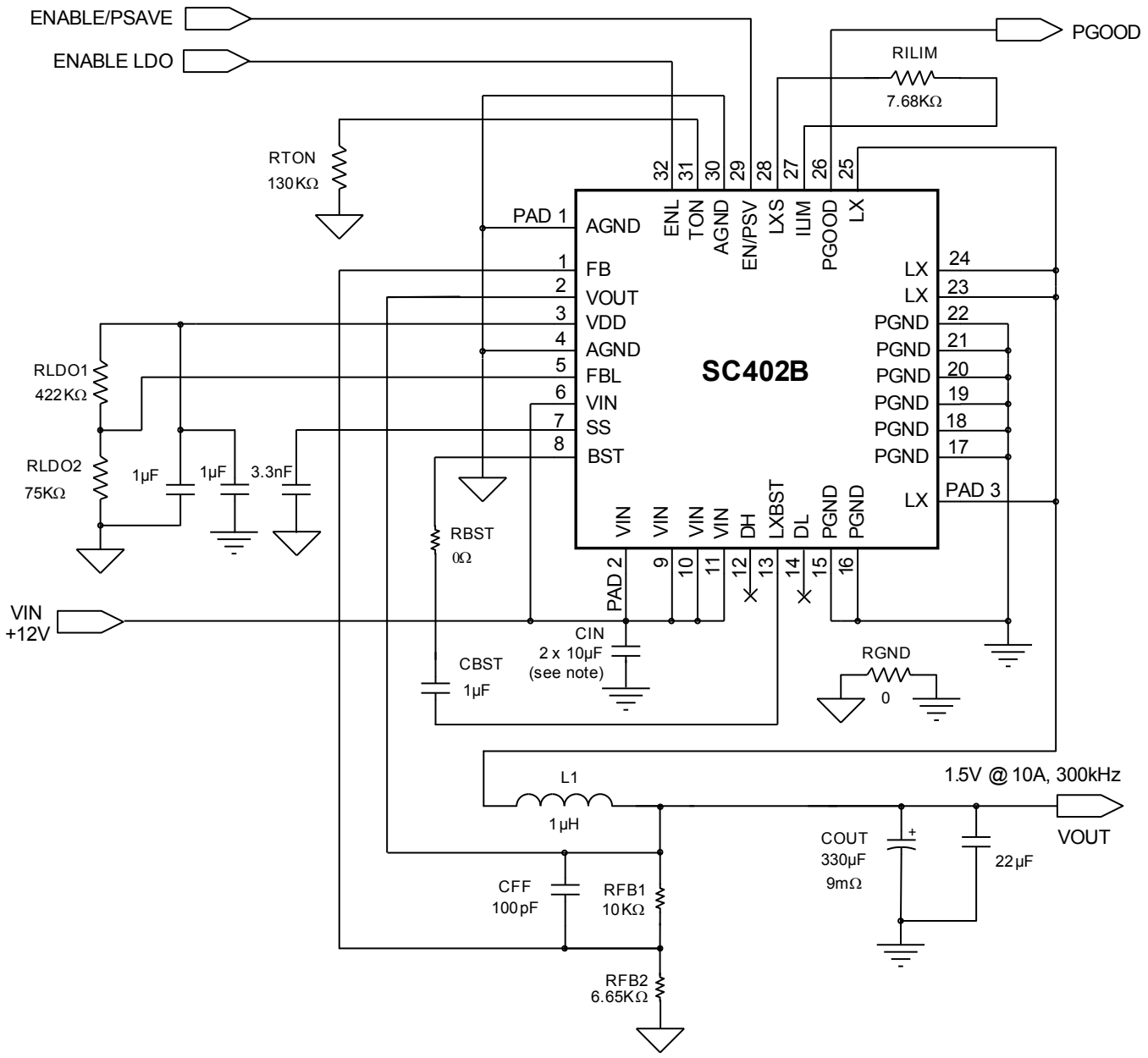
(3) SC402B has first order temperature compensation for over current. Results vary based upon the PCB thermal layout.

(4) The switch-over threshold is the maximum voltage differential between the VDD and VOUT pins which ensures that VLDO will internally switch-over to VOUT. The non-switch-over threshold is the minimum voltage differential between the VLDO and VOUT pins which ensures that VLDO will not switch-over to VOUT.

(5) The LDO drop out voltage is the voltage at which the LDO output drops 2% below the nominal regulation point.

Detailed Application Circuit — 1

Internal LDO Used as Bias



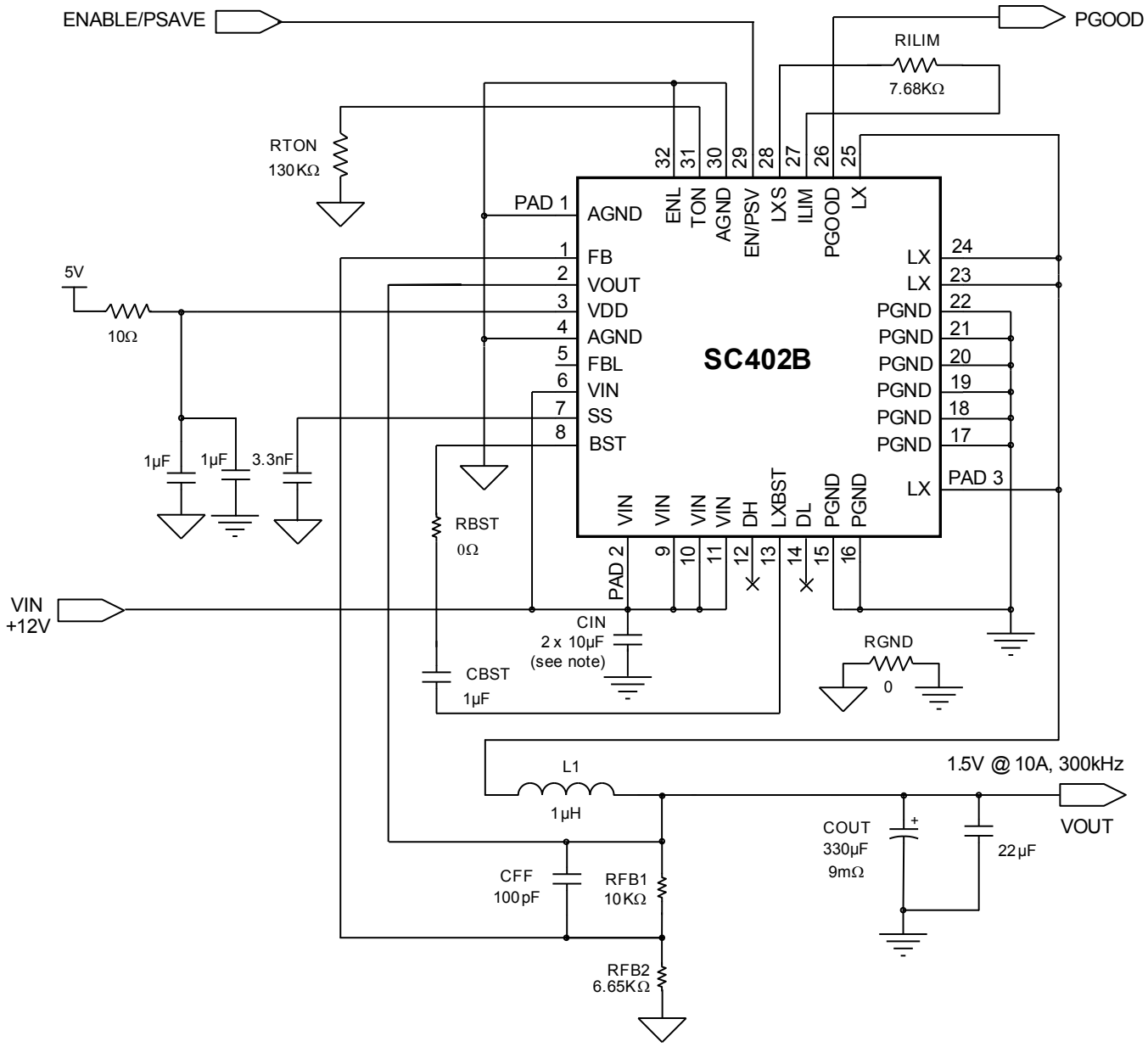
Key Components

Component	Value	Manufacturer	Part Number	Web
CIN (see note)	2 x 10µF/25V	Murata	GRM32DR71E106KA12L	www.murata.com
COUT	330µF/9mΩ	Panasonic	EEF-SX0E331ER	www.panasonic.com
L1	1.0µH/3mΩ	Cyntec	PIMB104T-1R0MS	www.cyntec.com

NOTE: The quantity of 10µF input capacitors required varies with the application requirements.

Detailed Application Circuit — 2

External 3.3V - 5V Used as Bias



Key Components

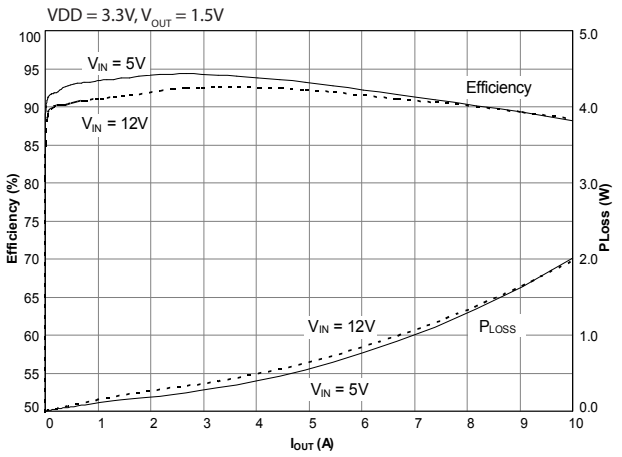
Component	Value	Manufacturer	Part Number	Web
CIN (see note)	2 x 10µF/25V	Murata	GRM32DR71E106KA12L	www.murata.com
COUT	330µF/9mΩ	Panasonic	EEF-SX0E331ER	www.panasonic.com
L1	1.0µH/3mΩ	Cyntec	PIMB104T-1R0MS	www.cyntec.com

NOTE: The quantity of 10µF input capacitors required varies with the application requirements.

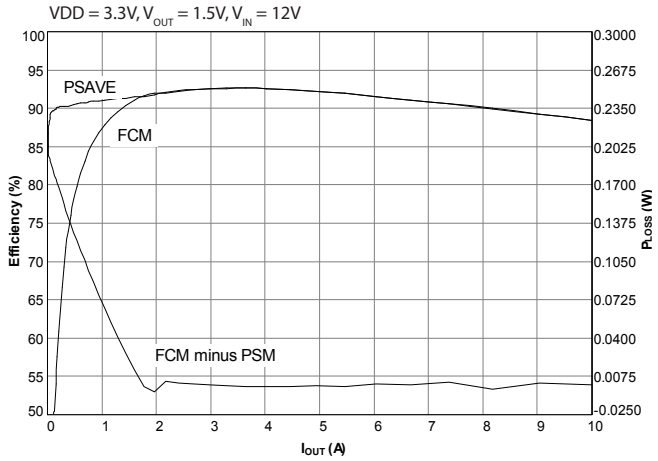
Typical Characteristics

Characteristics in this section are based on using the Typical Application Circuit on page 8.

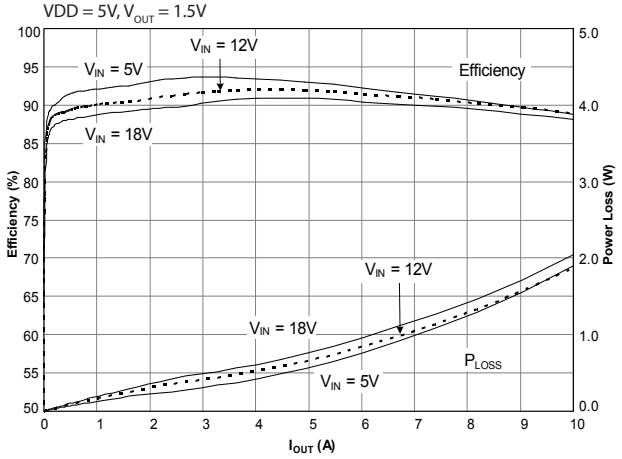
Efficiency/Power Loss vs. Load — PSAVE Mode



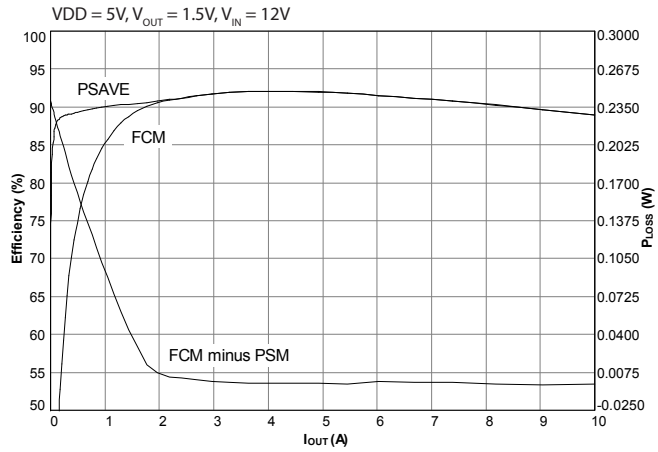
Efficiency/Power Loss — PSAVE vs. FCM



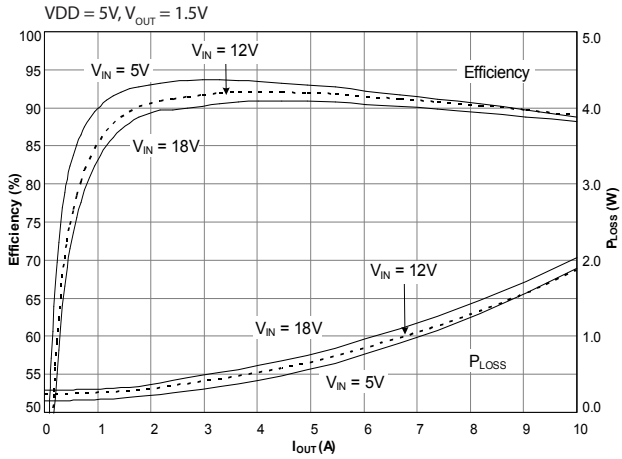
Efficiency/Power Loss vs. Load — PSAVE Mode



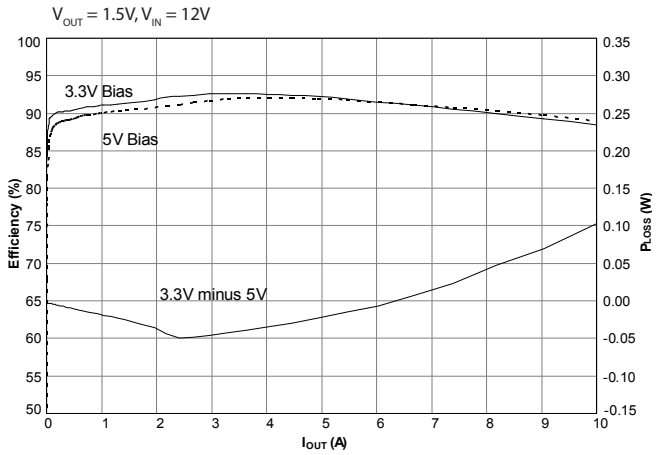
Efficiency/Power Loss — PSAVE vs. FCM



Efficiency/Power Loss vs. Load — FCM



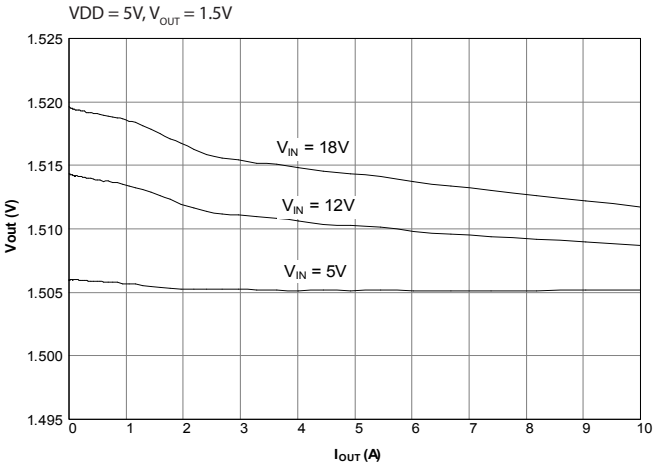
Efficiency/Power Loss — PSAVE



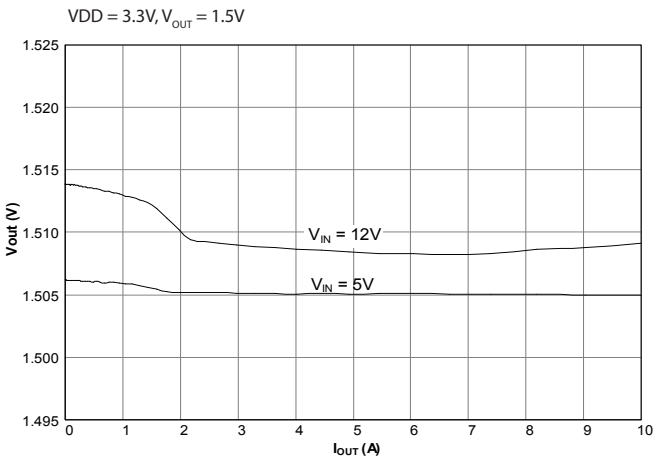
Typical Characteristics (continued)

Characteristics in this section are based on using the Typical Application Circuit on page 8.

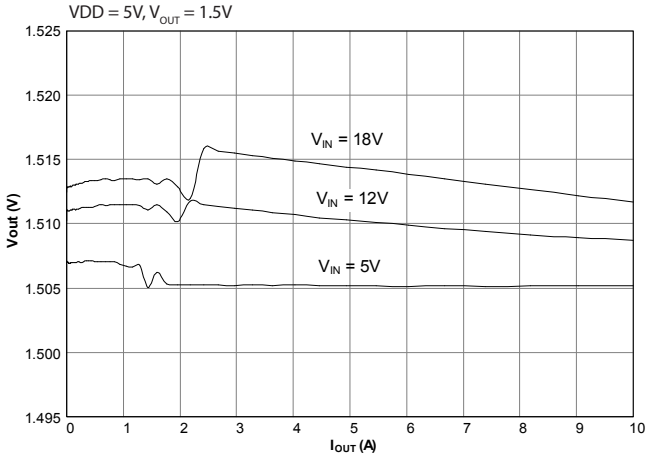
Load Regulation — FCM



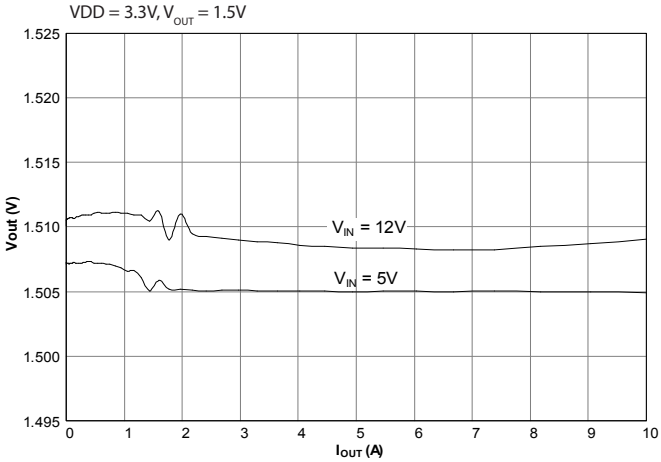
Load Regulation — FCM



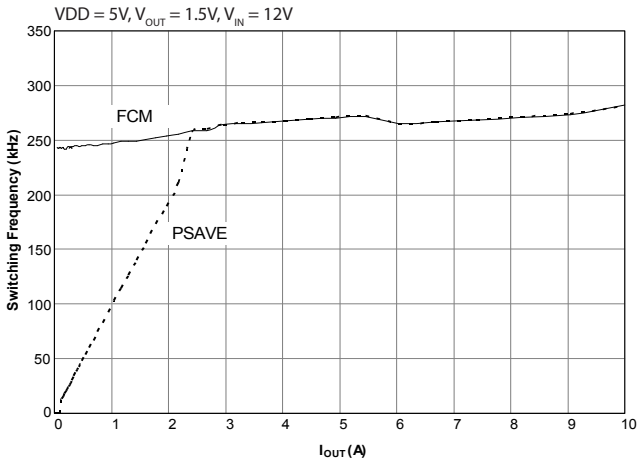
Load Regulation — PSAVE Mode



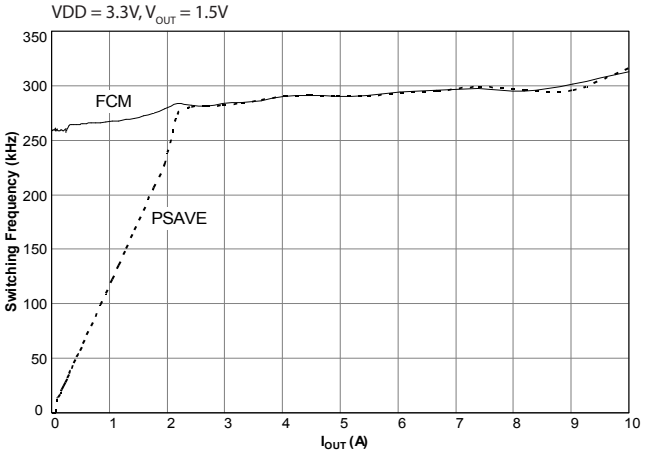
Load Regulation — PSAVE



Switching Frequency — PSAVE Mode vs. FCM



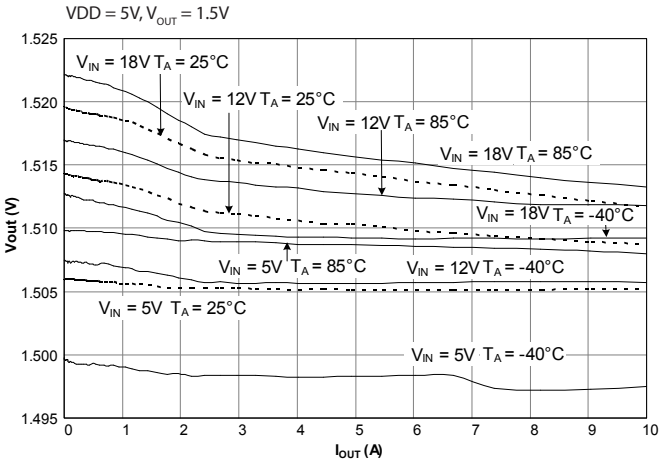
Switching Frequency — PSAVE Mode vs. FCM



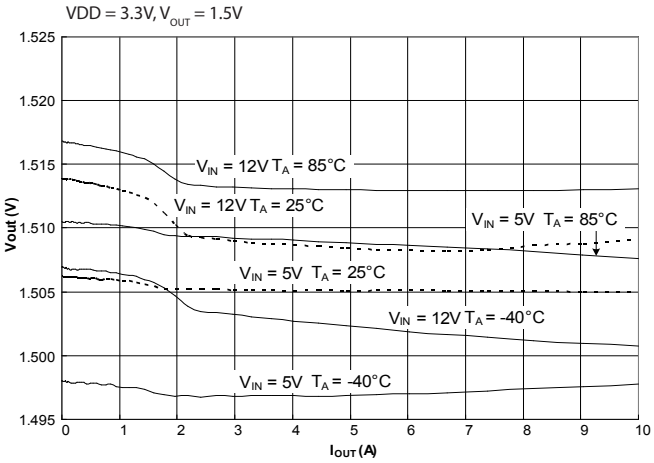
Typical Characteristics (continued)

Characteristics in this section are based on using the Typical Application Circuit on page 8.

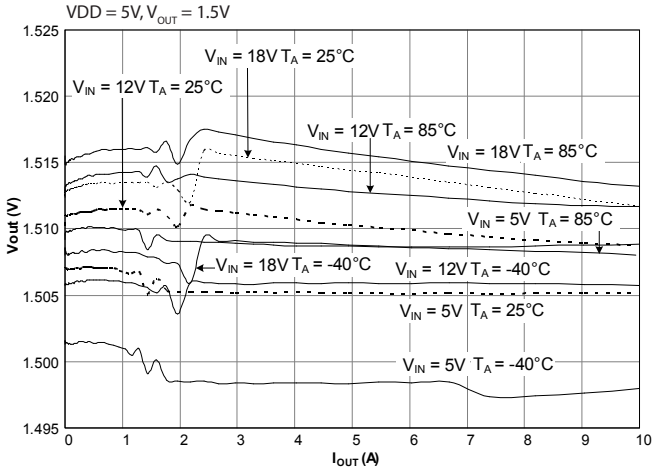
Load Regulation vs. Temperature — FCM



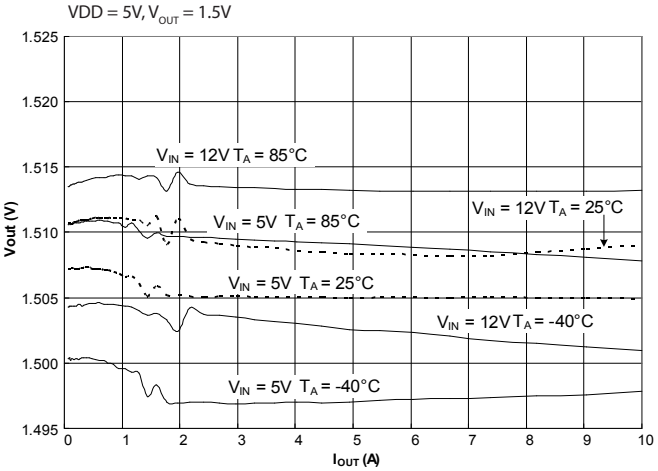
Load Regulation vs. Temperature — FCM



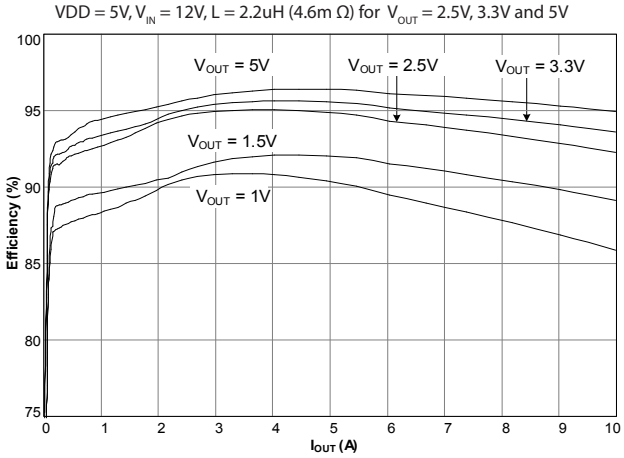
Load Regulation vs. Temperature — PSAVE



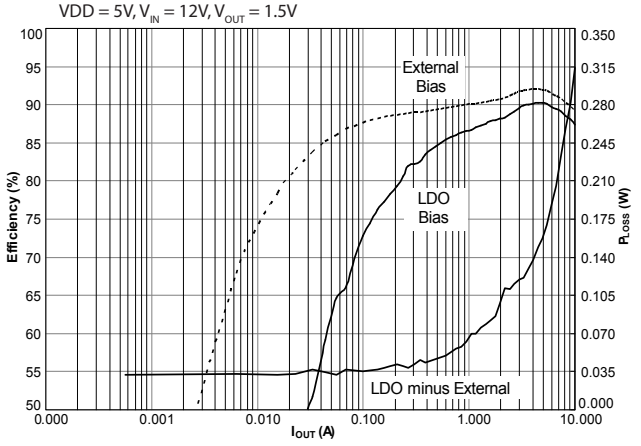
Load Regulation vs. Temperature — PSAVE



Efficiency Variation with V_{OUT} — PSAVE



Efficiency/Power Loss vs. Load — PSAVE Mode

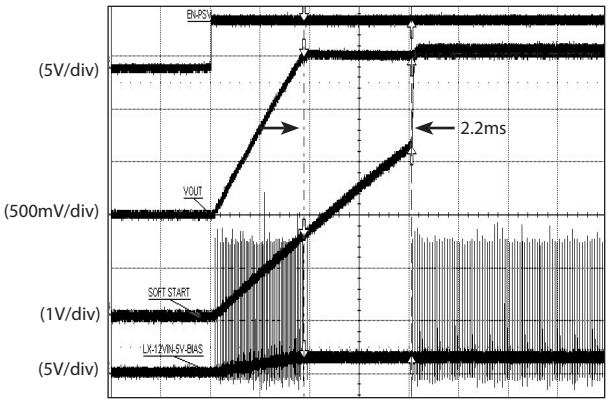


Typical Characteristics (continued)

Characteristics in this section are based on using the Typical Application Circuit on page 8.

Start-up — EN/PSV

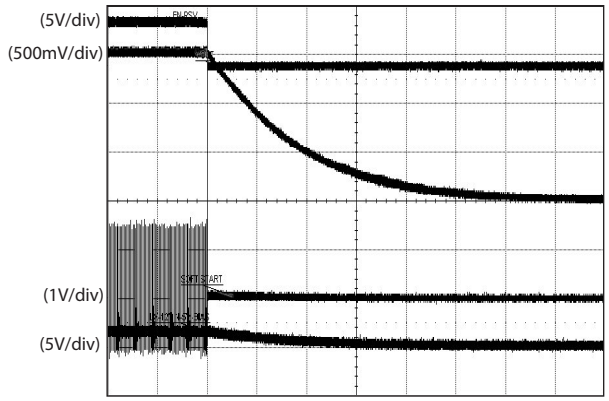
VDD = 5V, V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 0A



Time (1ms/div)

Shutdown — EN/PSV

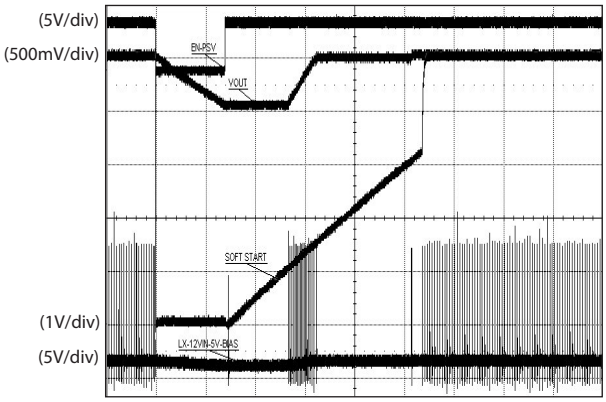
VDD = 5V, V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 0A



Time (2ms/div)

Start-up (Pre-Bias) — EN/PSV

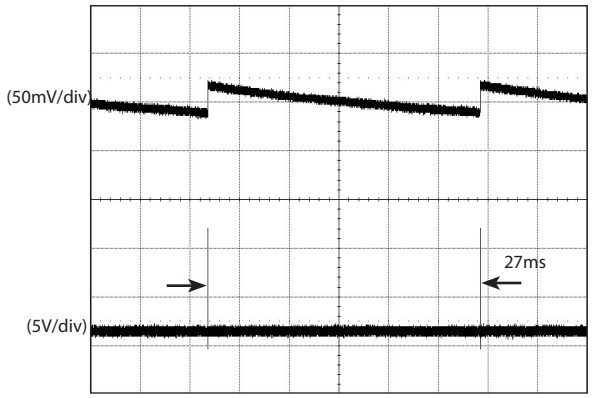
VDD = 5V, V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 0A



Time (2 ms/div)

Power Save Mode

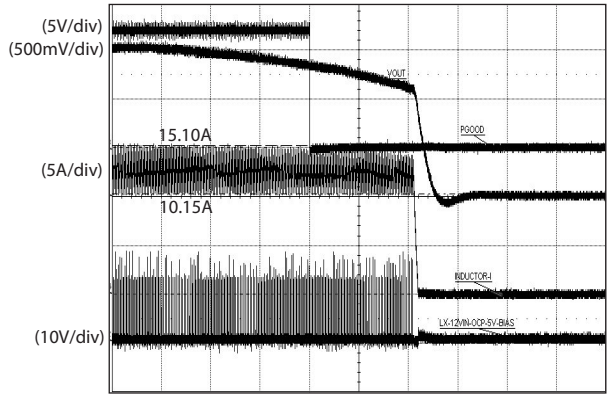
VDD = 5V, V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 0A



Time (5ms/div)

Over Current Protection — Under-Voltage Protection

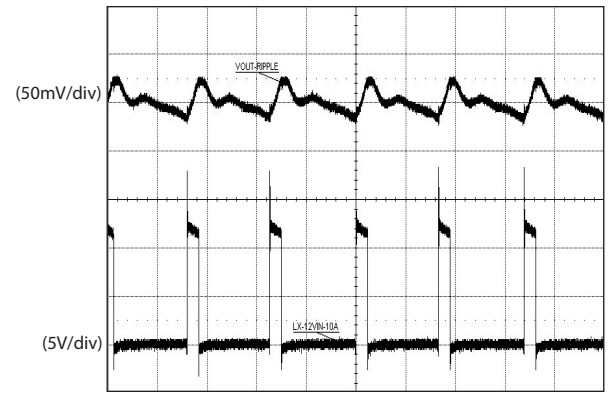
V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = OC regulated at 10.15A



Time (100µs/div)

Forced Continuous Mode

VDD = 5V, V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 10A



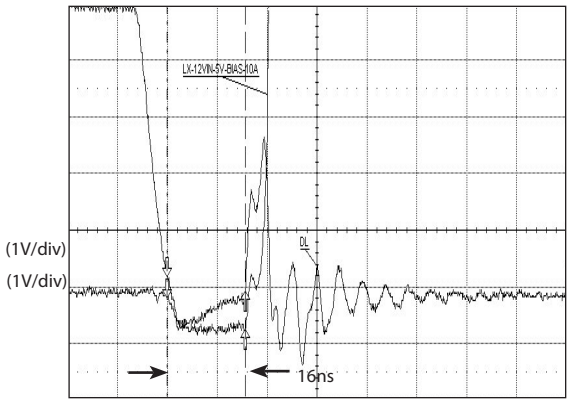
Time (2µs/div)

Typical Characteristics (continued)

Characteristics in this section are based on using the Typical Application Circuit on page 8.

Rising Edge Dead-time — LX

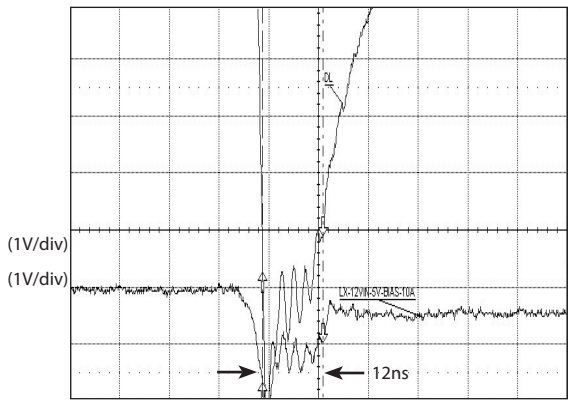
VDD = 5V, V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 10A



Time (10ns/div)

Falling Edge Dead-time — LX

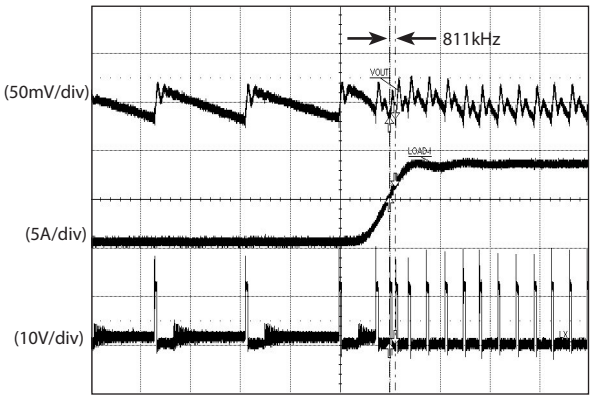
VDD = 5V, V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 10A



Time (10ns/div)

Transient Response — PSAVE Load Rising

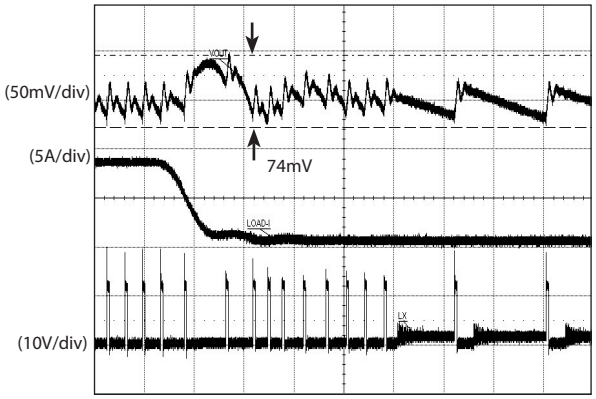
VDD = 5V, V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 0.5A to 8.5A, di/dt = 1A/µs



Time (10µs/div)

Transient Response — PSAVE Load Falling

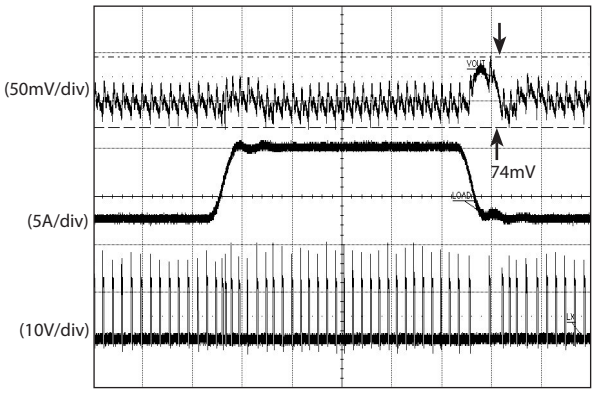
VDD = 5V, V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 8.5A to 0.5A, di/dt = 1A/µs



Time (10µs/div)

Transient Response — FCM

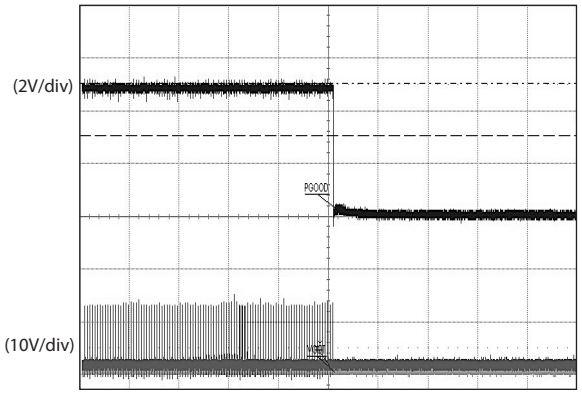
VDD = 5V, V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 2.5A to 10A, di/dt = 1A/µs



Time (20µs/div)

Over Temperature Shutdown — 159°C

V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 0A, LDO mode

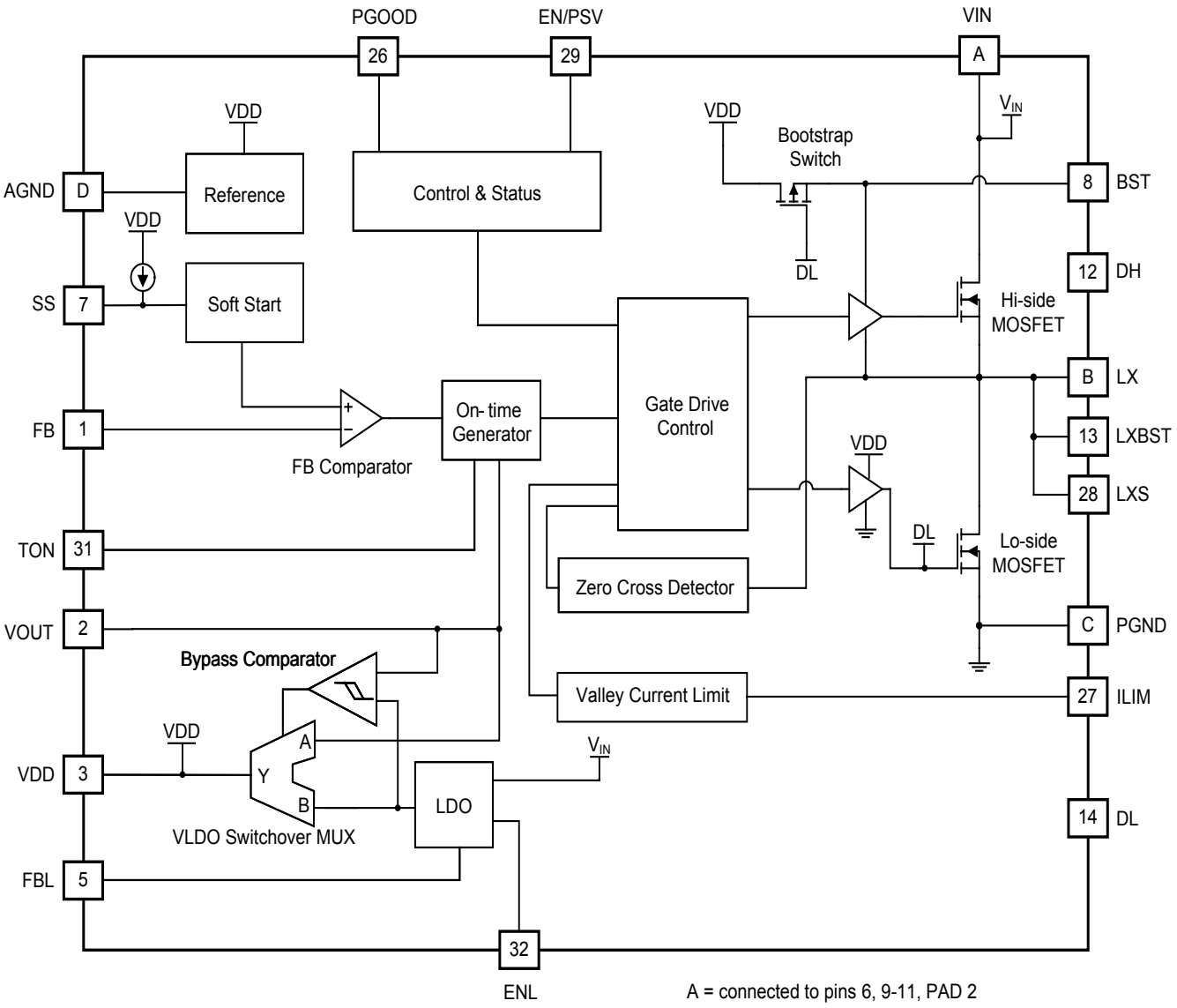


Time (500µs/div)

Pin Descriptions

Pin #	Pin Name	Pin Function
1	FB	Feedback input for switching regulator used to program the output voltage — connect to an external resistor divider from VOUT to AGND.
2	VOUT	Switcher output voltage sense pin — also the input to the internal switch-over between VOUT and VLDO. The voltage at this pin must be less than or equal to the voltage at the VDD pin.
3	VDD	Bias supply for the IC — when using the internal LDO as a bias power supply, VDD is the LDO output. When using an external power supply as the bias for the IC, the LDO output should be disabled.
4, 30, PAD 1	AGND	Analog ground
5	FBL	Feedback input for the internal LDO — used to program the LDO output. Connect to an external resistor divider from VDD to AGND.
6, 9-11, PAD 2	VIN	Input supply voltage
7	SS	The soft start ramp will be programmed by an internal current source charging a capacitor on this pin.
8	BST	Bootstrap pin — connect a capacitor of at least 100nF from BST to LX to develop the floating supply for the high-side gate drive.
12	DH	High-side gate drive
13	LXBST	LX Boost — connect to the BST capacitor.
23-25, PAD 3	LX	Switching (phase) node
14	DL	Low-side gate drive
15-22	PGND	Power ground
26	PGOOD	Open-drain power good indicator — high impedance indicates power is good. An external pull-up resistor is required.
27	ILIM	Current limit sense pin — used to program the current limit by connecting a resistor from ILIM to LXS.
28	LXS	LX sense — connects to R_{ILIM}
29	EN/PSV	Enable/power save input for the switching regulator — connect to AGND to disable the switching regulator, connect to VDD to operate with power save mode and float to operate in forced continuous mode.
31	TON	On-time programming input — set the on-time by connecting through a resistor to AGND
32	ENL	Enable input for the LDO — connect ENL to AGND to disable the LDO. Drive with logic signal for logic control, or program the VIN UVLO with a resistor divider between VIN, ENL, and AGND.

Block Diagram



A = connected to pins 6, 9-11, PAD 2
B = connected to pins 23-25, PAD 3
C = connected to pins 15-22
D = connect to pins 4, 30, PAD 1

Applications Information

Synchronous Buck Converter

The SC402B is a step down synchronous DC-DC buck converter with integrated power MOSFETs and a 200mA capable programmable LDO. The device is capable of 10A operation at very high efficiency. A space saving 5x5 (mm) 32-pin package is used. The programmable operating frequency of up to 1MHz enables optimizing the configuration for PCB area and efficiency.

The buck controller uses a pseudo-fixed frequency adaptive on-time control. This control method allows fast transient response which permits the use of smaller output capacitors.

In addition to the following information, the user can click on the applicable link to go to the SC402B online C-SIM design and simulation tool, which will lead the user through the design process.

Input Voltage Requirements

The SC402B requires two input supplies for normal operation: V_{IN} and VDD. V_{IN} operates over a wide range from 3V to 28V. VDD requires a 3V to 5.5V supply input that can be an external source or the internal LDO configured to supply 3V to 5.5V from V_{IN}.

Power Up Sequence

When the SC402B uses an external power source at the VDD pin, the switching regulator initiates the start up when V_{IN}, VDD and EN/PSV are above their respective thresholds. When EN/PSV is at a logic high, VDD needs to be applied after V_{IN} rises. It is also recommended to use a10Ω resistor between an external power source and the VDD pin. To start up by using the EN/PSV pin when both VDD and V_{IN} are above their respective thresholds, apply EN/PSV to enable the start-up process. For SC402B in self-biased mode, refer to the LDO section for a full description.

Shutdown

The SC402B can be shutdown by pulling either VDD or EN/PSV below its threshold. When using an external power source, it is recommended that the VDD voltage ramps down before the V_{IN} voltage. When VDD is active and EN/PSV at low logic, the output voltage discharges into the VOUT pin through an internal FET.

Psuedo-fixed Frequency Adaptive On-time Control

The PWM control method used by the SC402B is pseudo-fixed frequency, adaptive on-time, as shown in Figure 1. The ripple voltage generated at the output capacitor ESR is used as a PWM ramp signal. This ripple is used to trigger the on-time of the controller.

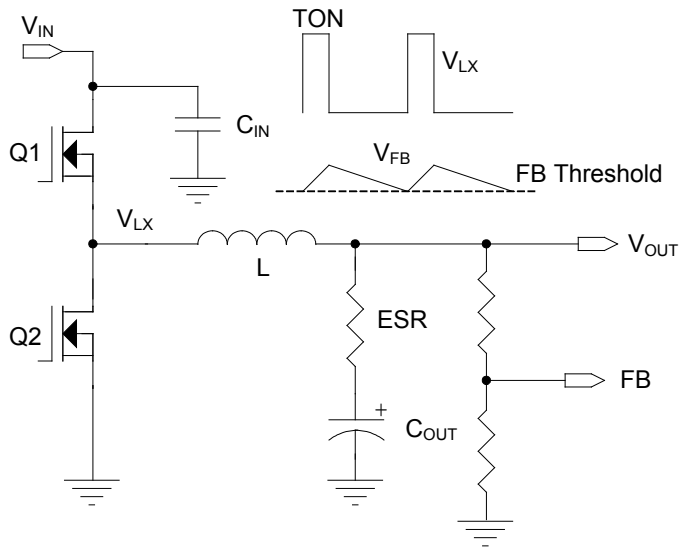


Figure 1 — PWM Control Method, V_{OUT} Ripple

The adaptive on-time is determined by an internal one-shot timer. When the one-shot is triggered by the output ripple, the device sends a single on-time pulse to the high-side MOSFET. The pulse period is determined by V_{OUT} and V_{IN}; the period is proportional to output voltage and inversely proportional to input voltage. With this adaptive on-time arrangement, the device automatically anticipates the on-time needed to regulate V_{OUT} for the present V_{IN} condition and at the selected frequency.

The advantages of adaptive on-time control are:

- Predictable operating frequency compared to other variable frequency methods
- Reduced component count by eliminating the error amplifier and compensation components
- Reduced component count by removing the need to sense and control inductor current
- Fast transient response — the response time is controlled by a fast comparator instead of a typically slow error amplifier.
- Reduced output capacitance due to fast transient response

Applications Information (continued)

One-Shot Timer and Operating Frequency

The one-shot timer operates as shown in Figure 2. The FB Comparator output goes high when V_{FB} is less than the internal 600mV reference. This feeds into the gate drive and turns on the high-side MOSFET, and also starts the one-shot timer. The one-shot timer uses an internal comparator and a capacitor. One comparator input is connected to V_{OUT}, the other input is connected to the capacitor. When the on-time begins, the internal capacitor charges from zero volts through a current which is proportional to V_{IN}. When the capacitor voltage reaches V_{OUT}, the on-time is completed and the high-side MOSFET turns off.

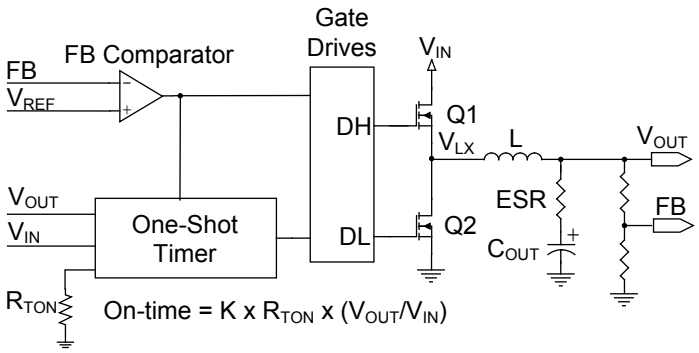


Figure 2 — On-Time Generation

This method automatically produces an on-time that is proportional to V_{OUT} and inversely proportional to V_{IN}. Under steady-state conditions, the switching frequency can be determined from the on-time by the following equation.

$$f_{SW} = \frac{V_{OUT}}{T_{ON} \times V_{IN}}$$

The SC402B uses an external resistor to set the on-time which indirectly sets the frequency. The on-time can be programmed to provide an operating frequency up to 1MHz using a resistor between the TON pin and ground. The resistor value is selected by the following equation.

$$R_{TON} = \frac{k}{25pF \times f_{SW}}$$

The constant, k, equals 1 when VDD is greater than 3.6V. If VDD is less than 3.6V and V_{IN} is greater than (VDD -1.75) x 10, k is shown by the following equation.

$$k = \frac{(VDD - 1.75) \times 10}{V_{IN}}$$

The maximum R_{TON} value allowed is shown by the following equation.

$$R_{TON\_MAX} = \frac{V_{IN\_MIN}}{15\mu A}$$

V_{OUT} Voltage Selection

The switcher output voltage is regulated by comparing V_{OUT} as seen through a resistor divider at the FB pin to the internal 600mV reference voltage, see Figure 3.

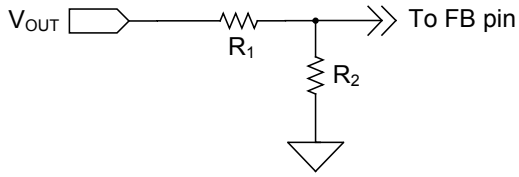


Figure 3 — Output Voltage Selection

Note that this control method regulates the valley of the output ripple voltage, not the DC value. The DC output voltage V_{OUT} is offset by the output ripple according to the following equation.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_1}{R_2}\right) + \left(\frac{V_{RIPPLE}}{2}\right)$$

When a large capacitor is placed in parallel with R_1 (C_{TOP}) V_{OUT} is shown by the following equation.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_1}{R_2}\right) + \left(\frac{V_{RIPPLE}}{2}\right) \times \sqrt{\frac{1 + (R_1 \omega C_{TOP})^2}{1 + \left(\frac{R_2 \times R_1}{R_2 + R_1} \omega C_{TOP}\right)^2}}$$

Enable and Power-save Inputs

The EN/PSV input is used to enable or disable the switching regulator. When EN/PSV is low (grounded), the switching regulator is off and in its lowest power state. When off, the output of the switching regulator soft-discharges the output into a 15Ω internal resistor via the VOUT pin. When EN/PSV is allowed to float, the pin voltage will float to 33% of the voltage at VDD. The switching regulator turns on with power-save disabled and all switching is in forced continuous mode.

When EN/PSV is high (above 44% of the voltage at VDD), the switching regulator turns on with power save enabled.

Applications Information (continued)

The SC402B PSAVE operation reduces the switching frequency according to the load for increased efficiency at light load conditions.

Forced Continuous Mode Operation

The SC402B operates the switcher in FCM (Forced Continuous Mode) by floating the EN/PSV pin (see Figure 4). In this mode one of the power MOSFETs is always on, with no intentional dead time other than to avoid cross-conduction. This feature results in uniform frequency across the full load range with the trade-off being poor efficiency at light loads due to the high-frequency switching of the MOSFETs. DH is gate signal to drive upper MOSFET. DL is lower gate signal to drive lower MOSFET.

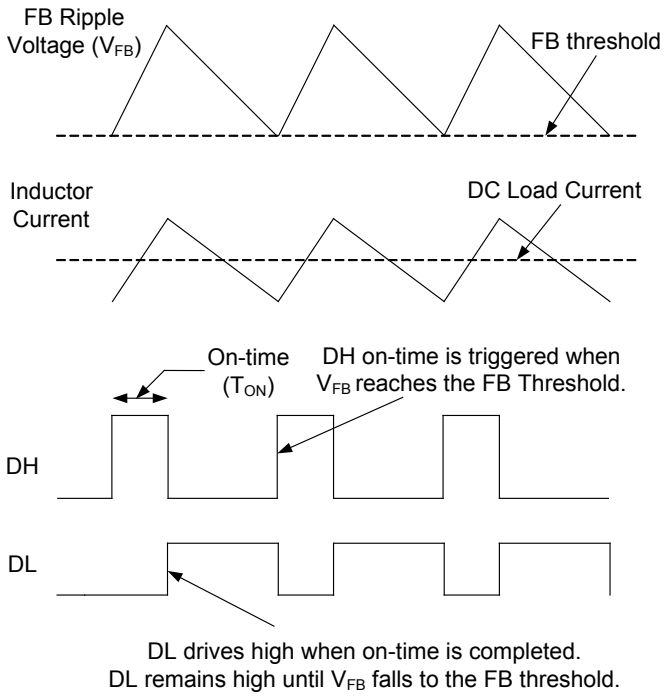


Figure 4 — Forced Continuous Mode Operation

Power-save Operation

The SC402B provides power-save operation at light loads with no minimum operating frequency. With power-save enabled, the internal zero crossing comparator monitors the inductor current via the voltage across the low-side MOSFET during the off-time. If the inductor current falls to zero for 8 consecutive switching cycles, the controller enters power-save operation. It will turn off the low-side MOSFET on each subsequent cycle provided that the current crosses zero. At this time both MOSFETs remain off until V_{FB} drops to the 600mV threshold. Because the MOSFETs are off, the load is supplied by the output capacitor.

If the inductor current does not reach zero on any switching cycle, the controller immediately exits power-save and returns to forced continuous mode.

Figure 5 shows power-save operation at light loads.

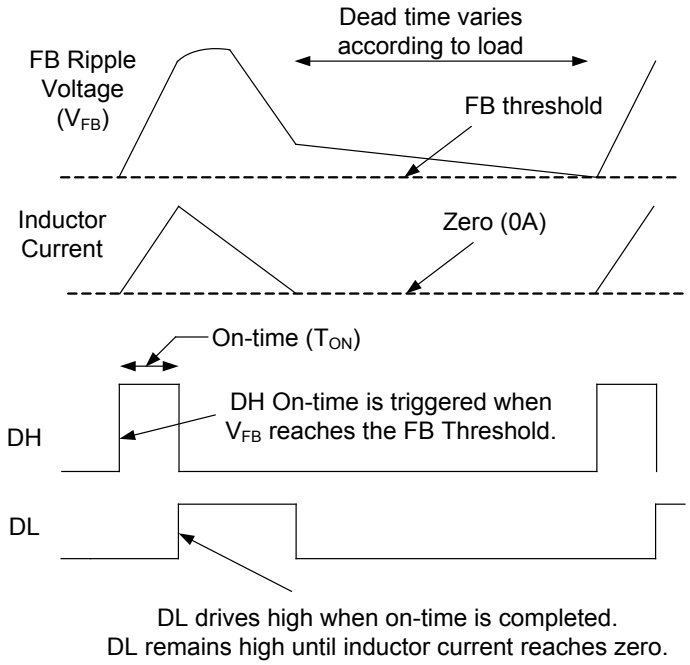


Figure 5 — Power-save Operation

Smart Power-save Protection

Active loads may leak current from a higher voltage into the switcher output. Under light load conditions with power-save enabled, this can force V_{OUT} to slowly rise and reach the over-voltage threshold, resulting in a hard shutdown. Smart power save prevents this condition. When the FB voltage exceeds 10% above nominal, the device immediately disables power save, and DL drives high to turn on the low-side MOSFET. This draws current from V_{OUT} through the inductor and causes V_{OUT} to fall. When V_{FB} drops back to the 600mV trip point, a normal T_{ON} switching cycle begins. This method prevents a hard OVP shutdown and also cycles energy from V_{OUT} back to V_{IN}. It also minimizes operating power by avoiding forced conduc-

Applications Information (continued)

tion mode operation. Figure 6 shows typical waveforms for the Smart Power Save feature.

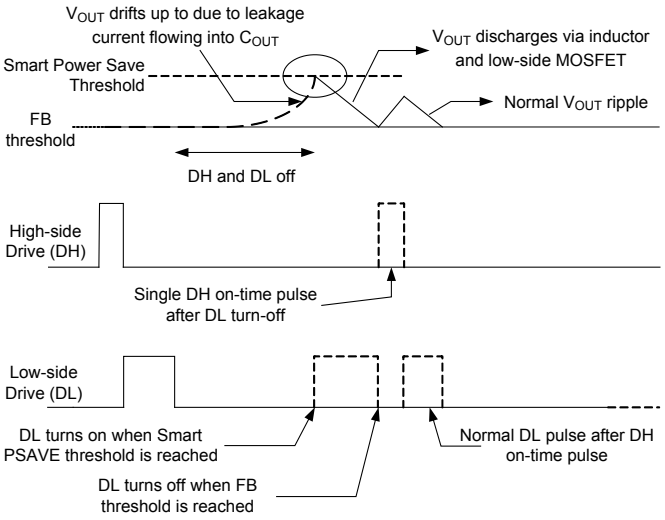


Figure 6 — Smart Power Save

SmartDrive™

For each DH pulse the DH driver initially turns on the high-side MOSFET at a lower speed, allowing a softer, smooth turn-off of the low-side diode. Once the diode is off and the LX voltage has risen 0.5V above PGND, the SmartDrive circuit automatically drives the high-side MOSFET on at a rapid rate. This technique reduces switching losses while maintaining high efficiency and also avoids the need for snubbers for the power MOSFETs.

Current Limit Protection

The device features programmable current limiting, which is accomplished by using the RDS_{ON} of the lower MOSFET for current sensing. The current limit is set by R_{ILIM} resistor. The R_{ILIM} resistor connects from the ILIM pin to the LXS pin which is also the drain of the low-side MOSFET. When the low-side MOSFET is on, an internal ~10µA current flows from the ILIM pin and through the R_{ILIM} resistor, creating a voltage drop across the resistor. While the low-side MOSFET is on, the inductor current flows through it and creates a voltage across the RDS_{ON}. The voltage across the MOSFET is negative with respect to ground. If this MOSFET voltage drop exceeds the voltage across R_{ILIM}, the voltage at the ILIM pin will be negative and current limit will activate. The current limit then keeps the low-side MOSFET on and will not allow another high-side on-time, until the current in the low-side MOSFET reduces enough to bring the ILIM voltage back up to zero. This method regulates the inductor valley current at the level shown by ILIM in Figure 7.

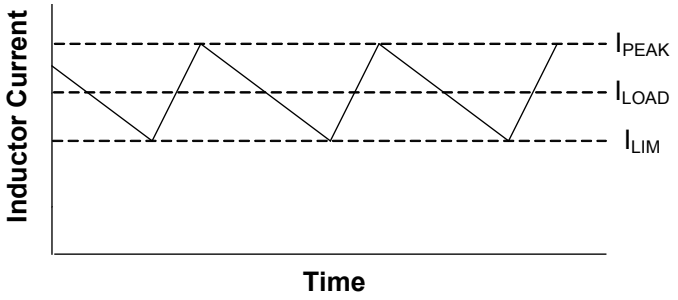


Figure 7 — Valley Current Limit

Setting the valley current limit to 10A results in a peak inductor current of 10A plus peak ripple current. In this situation, the average (load) current through the inductor is 10A plus one-half the peak-to-peak ripple current.

The internal 10µA current source is temperature compensated at 4100ppm in order to provide tracking with the RDS_{ON}.

The R_{ILIM} value is calculated by the following equation.

$$R_{ILIM} = 670 \times I_{LIM} \times [0.0647 \times (5V - VDD) + 1]$$

When selecting a value for R_{ILIM} be sure not to exceed the absolute maximum voltage value for the ILIM pin. Note that because the low-side MOSFET with low RDS_{ON} is used for current sensing, the PCB layout, solder connections, and PCB connection to the LX node must be done carefully to obtain good results. R_{ILIM} should be connected directly to LXS (pin 28).

Soft-Start of PWM Regulator

SC402B has a programmable soft-start time that is controlled by an external capacitor at the SS pin. After the controller meets both UVLO and EN/PSV thresholds, the controller has an internal current source of 3µA flowing

Applications Information (continued)

through the SS pin to charge the capacitor. During the start up process (Figure 8), 50% of the voltage at the SS pin is used as the reference for the FB comparator. The PWM comparator issues an on-time pulse when the voltage at the FB pin is less than 40% of the SS pin. As a result, the output voltage follows the SS voltage. The output voltage reaches and maintains regulation when the soft start voltage is $\geq$ 1.5V. The time between the first LX pulse and V_{OUT} reaching regulation is the soft-start time (t_{SS}). The calculation for the soft-start time is shown by the following equation.

$$t_{SS} = C_{SS} \times \frac{1.5V}{3\mu A}$$

The voltage at the SS pin continues to ramp up and eventually equals 64% of V_{DD}. After the soft start completes, the FB pin voltage is compared to an internal reference of 0.6V. The delay time between the V_{OUT} regulation point and PGOOD going high is shown by the following equation.

$$t_{PGOOD\text{-}DELAY} = \frac{C_{SS} \times (0.64 \times V_{DD} - 1.5V)}{3\mu A}$$

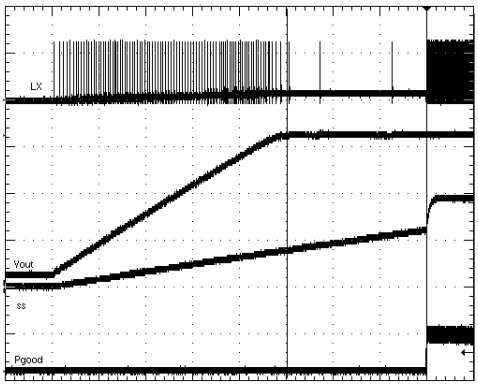


Figure 8 — Soft-start Timing Diagram

Pre-Bias Startup

The SC402B can start up normally even when there is an existing output voltage present. The soft start time is still the same as normal start up (when the output voltage starts from zero). The output voltage starts to ramp up when 40% of the voltage at SS pin meets the existing FB voltage level. Pre-bias startup is achieved by turning off the lower gate when the inductor current falls below zero. This method prevents the output voltage from discharging.

Power Good Output

The PGOOD (power good) output is an open-drain output which requires a pull-up resistor. When the voltage at the FB pin is 10% below the nominal voltage, PGOOD is pulled low. It is held low until the output voltage returns above -8% of nominal.

PGOOD will transition low if the V_{FB} pin exceeds +20% of nominal, which is also the over-voltage shutdown threshold. PGOOD also pulls low if the EN/PSV pin is low when VDD is present.

Output Over-Voltage Protection

Over-voltage protection becomes active as soon as the device is enabled. The threshold is set at 600mV + 20% (720mV). When V_{FB} exceeds the OVP threshold, DL latches high and the low-side MOSFET is turned on. DL remains high and the controller remains off, until the EN/PSV input is toggled or VDD is cycled. There is a 5µs delay built into the OVP detector to prevent false transitions. PGOOD is also low after an OVP event.

Output Under-Voltage Protection

When V_{FB} falls 25% below its nominal voltage (falls to 450mV) for eight consecutive clock cycles, the switcher is shut off and the DH and DL drives are pulled low to tri-state the MOSFETs. The controller stays off until EN/PSV is toggled or VDD is cycled.

VDD UVLO, and POR

UVLO (Under-Voltage Lock-Out) circuitry inhibits switching and tri-states the DH/DL drivers until VDD rises above 3.0V. An internal POR (Power-On Reset) occurs when VDD exceeds 3.0V, which resets the fault latch and a soft-start counter cycle begins which prepares for soft-start. The SC402B then begins a soft-start cycle. The PWM will shut off if VDD falls below 2.4V.

Applications Information (continued)

LDO Regulator

SC402B has an option to bias the switcher by using an internal LDO from V_{IN}. The LDO output is connected to VDD internally. The output of the LDO is programmable by using external resistors from the VDD pin to AGND (see Figure 9). The feedback pin (FBL) for the LDO is regulated to 750mV.

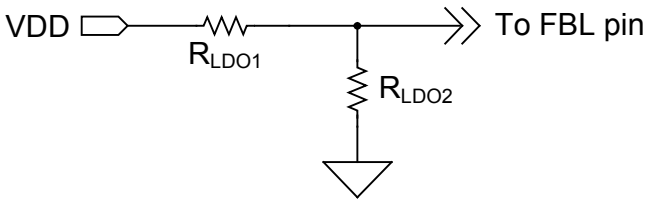


Figure 9 — LDO Output Voltage Selection

The LDO output voltage is set by the following equation.

$$VLDO = 750mV \times \left(1 + \frac{R_{LDO1}}{R_{LDO2}}\right)$$

A minimum capacitance of 1µF referenced to AGND is normally required at the output of the LDO for stability.

Note that if the LDO voltage is set lower than 4.5V, the minimum output capacitance for the LDO is 10uF.

LDO ENL Functions

The ENL input is used to enable/disable the internal LDO. When ENL is a logic low, the LDO is off. When ENL is above the V_{IN} UVLO threshold, the LDO is enabled and the switcher is also enabled if the EN/PSV and VDD are above their threshold. The table below summarizes the function of ENL and EN/PSV pins.

EN/PSV	ENL	LDO	Switcher
Disabled	Low, < 0.4V	OFF	OFF
Enabled	Low, < 0.4V	OFF	ON
Disabled	1.0V < High < 2.6V	ON	OFF
Enabled	1.0V < High < 2.6V	ON	OFF
Disabled	High, > 2.6V	ON	OFF
Enabled	High, > 2.6V	ON	ON

The ENL pin also acts as the switcher under-voltage lockout for the V_{IN} supply. When SC402B is self-biased from the LDO and runs from the V_{IN} power source only, the V_{IN} UVLO feature can be used to prevent false UV faults for the PWM output by programming with a resistor divider at the VIN, ENL and AGND pins. When SC402B has an external bias voltage at VDD and the ENL pin is used to program the V_{IN} UVLO feature, the voltage at FBL needs to be higher than 750mV to force the LDO off.

Timing is important when driving ENL with logic and not implementing V_{IN} UVLO. The ENL pin must transition from high to low within 2 switching cycles to avoid the PWM output turning off. If ENL goes below the VIN UVLO threshold and stays above 1V, then the switcher will turn off but the LDO will remain on.

LDO Start-up

Before start-up, the LDO checks the status of the following signals to ensure proper operation can be maintained.

1. ENL pin
2. V_{IN} input voltage

When the ENL pin is high and V_{IN} is above the UVLO point, the LDO will begin start-up. During the initial phase, when the V_{DD} voltage (which is the LDO output voltage) is less than 0.75V, the LDO initiates a current-limited start-up (typically 65mA) to charge the output capacitors while protecting from a short circuit event. When V_{DD} is greater than 0.75V but still less than 90% of its final value (as sensed at the FBL pin), the LDO current limit is increased to ~115mA. When V_{DD} has reached 90% of the final value (as sensed at the FBL pin), the LDO current limit is increased to ~200mA and the LDO output is quickly driven to the nominal value by the internal LDO regulator. It is recommended that during LDO start-up to hold the PWM switching off until the LDO has reached 90% of the final value. This prevents overloading the current-limited LDO output during the LDO start-up.

Applications Information (continued)

Due to the initial current limitations on the LDO during power up (Figure 10), any external load attached to the VDD pin must be limited to less than the start up current before the LDO has reached 90% of its final regulation value.

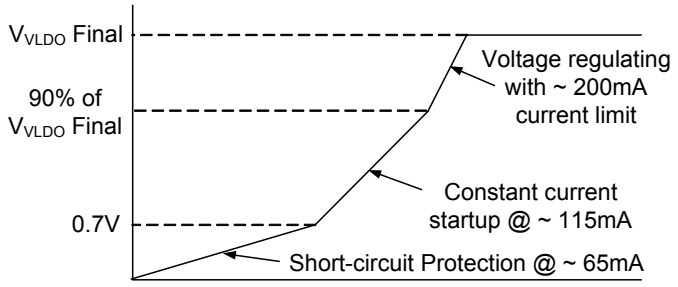


Figure 10 — LDO Start-Up

LDO Switch-Over Operation

The SC402B includes a switch-over function for the LDO. The switch-over function is designed to increase efficiency by using the more efficient DC-DC converter to power the LDO output, avoiding the less efficient LDO regulator when possible. The switch-over function connects the VDD pin directly to the VOUT pin using an internal switch. When the switch-over is complete the LDO is turned off, which results in a power savings and maximizes efficiency. If the LDO output is used to bias the SC402B, then after switch-over the device is self-powered from the switching regulator with the LDO turned off.

The switch-over starts 32 switching cycles after PGOOD output goes high. The voltages at the VDD and VOUT pins are then compared; if the two voltages are within ±300mV of each other, the VDD pin connects to the VOUT pin using an internal switch, and the LDO is turned off. To avoid unwanted switch-over, the minimum difference between the voltages for VOUT and VDD should be ±500mV.

It is not recommended to use the switch-over feature for an output voltage less than VDD UVLO threshold since the SC402B is not operational below that threshold.

Switch-over MOSFET Parasitic Diodes

The switch-over MOSFET contains parasitic diodes that are inherent to its construction, as shown in Figure 11. If the voltage at the VOUT pin is higher than VDD, then the respective diode will turn on and the current will flow through this diode. This has the potential of damaging the device. Therefore, V_{OUT} must be less than VDD to prevent damaging the device.

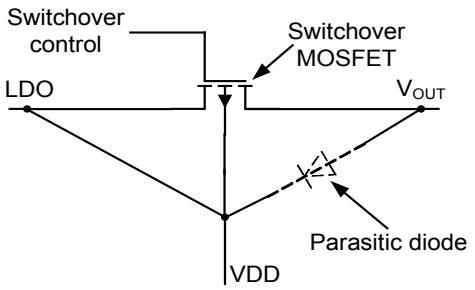


Figure 11— Switch-over MOSFET Parasitic Diodes

Design Procedure

When designing a switch mode supply the input voltage range, load current, switching frequency, and inductor ripple current must be specified.

The maximum input voltage (V_{INMAX}) is the highest specified input voltage. The minimum input voltage (V_{INMIN}) is determined by the lowest input voltage after evaluating the voltage drops due to connectors, fuses, switches, and PCB traces.

The following parameters define the design.

- Nominal output voltage (V_{OUT})
- Static or DC output tolerance
- Transient response
- Maximum load current (I_{OUT})

Applications Information (continued)

There are two values of load current to evaluate — continuous load current and peak load current. Continuous load current relates to thermal stresses which drive the selection of the inductor and input capacitors. Peak load current determines instantaneous component stresses and filtering requirements such as inductor saturation, output capacitors, and design of the current limit circuit.

The following values are used in this design.

- V_{IN} = 12V ± 10%
- V_{OUT} = 1.5V ± 4%
- f_{SW} = 300kHz
- Load = 10A maximum

Frequency Selection

Selection of the switching frequency requires making a trade-off between the size and cost of the external filter components (inductor and output capacitor) and the power conversion efficiency.

The desired switching frequency is 300kHz which results from using components selected for optimum size and cost.

A resistor (R_{TON}) is used to program the on-time (indirectly setting the frequency) using the following equation.

$$R_{TON} = \frac{k}{25pF \times f_{SW}}$$

To select R_{TON}, use the maximum value for V_{IN}, and for T_{ON} use the value associated with maximum V_{IN}.

$$T_{ON} = \frac{V_{OUT}}{V_{INMAX} \times f_{SW}}$$

T_{ON} = 379 ns at 13.2V_{IN}, 1.5V_{OUT}, 300kHz

Substituting for R_{TON} results in the following solution.

R_{TON} = 133.3kΩ, use R_{TON} = 130kΩ

Inductor Selection

In order to determine the inductance, the ripple current must first be defined. Low inductor values result in smaller size but create higher ripple current which can reduce efficiency. Higher inductor values will reduce the ripple current/voltage and for a given DC resistance are more efficient. However, larger inductance translates directly into larger packages and higher cost. Cost, size, output ripple, and efficiency are all used in the selection process.

The ripple current will also set the boundary for PSAVE operation. The switching will typically enter PSAVE mode when the load current decreases to 1/2 of the ripple current. For example, if ripple current is 4A then PSAVE operation will typically start for loads less than 2A. If ripple current is set at 40% of maximum load current, then PSAVE will start for loads less than 20% of maximum current.

The inductor value is typically selected to provide a ripple current that is between 25% to 50% of the maximum load current. This provides an optimal trade-off between cost, efficiency, and transient performance.

During the on-time, voltage across the inductor is (V_{IN} - V_{OUT}). The equation for determining inductance is shown next.

$$L = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{I_{RIPPLE}}$$

Example

In this example, the inductor ripple current is set equal to 45% of the maximum load current. Therefore ripple current will be 45% x 10A or 4.5A. To find the minimum inductance needed, use the V_{IN} and T_{ON} values that correspond to V_{INMAX}.

$$L = \frac{(13.2 - 1.5) \times 379ns}{4.5A} = 0.99\mu H$$

A slightly larger value of 1µH is selected. This will decrease the maximum I_{RIPPLE} to 4.43A.

Note that the inductor must be rated for the maximum DC load current plus 1/2 of the ripple current.

Applications Information (continued)

The ripple current under minimum V_{IN} conditions is also checked using the following equations.

$$T_{ON\_VINMIN} = \frac{25pF \times R_{TON} \times V_{OUT}}{V_{INMIN}} = 451ns$$

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{L}$$

$$I_{RIPPLE\_VINMIN} = \frac{(10.8 - 1.5) \times 451ns}{1\mu H} = 4.19A$$

Capacitor Selection

The output capacitors are chosen based upon required ESR and capacitance. The maximum ESR requirement is controlled by the output ripple requirement and the DC tolerance. The output voltage has a DC value that is equal to the valley of the output ripple plus 1/2 of the peak-to-peak ripple. A change in the output ripple voltage will lead to a change in DC voltage at the output.

The design goal for output voltage ripple is 3% of 1.5V or 45mV. The maximum ESR value allowed is shown by the following equations.

$$ESR_{MAX} = \frac{V_{RIPPLE}}{I_{RIPPLEMAX}} = \frac{45mV}{4.43A}$$

$$ESR_{MAX} = 10.2\ m\Omega$$

The output capacitance is usually chosen to meet transient requirements. A worst-case load release, from maximum load to no load at the exact moment when inductor current is at the peak, determines the required capacitance. If the load release is instantaneous (load changes from maximum to zero in < 1µs), the output capacitor must absorb all the inductor's stored energy. This will cause a peak voltage on the capacitor according to the following equation.

$$COUT_{MIN} = \frac{L\left(I_{OUT} + \frac{1}{2} \times I_{RIPPLEMAX}\right)^2}{(V_{PEAK})^2 - (V_{OUT})^2}$$

Assuming a peak voltage V_{PEAK} of 1.65V (150mV rise upon load release), and a 10A load release, the required capacitance is shown by the next equation.

$$COUT_{MIN} = \frac{1\mu H\left(10 + \frac{1}{2} \times 4.43\right)^2}{(1.65)^2 - (1.5)^2}$$

$$COUT_{MIN} = 316\mu F$$

During the load release time, the voltage cross the inductor is approximately $-V_{OUT}$. This causes a down-slope or falling di/dt in the inductor. If the load di/dt is not much faster than the di/dt of the inductor, then the inductor current will tend to track the falling load current. This will reduce the excess inductive energy that must be absorbed by the output capacitor, therefore a smaller capacitance can be used.

The following can be used to calculate the needed capacitance for a given dI_{LOAD}/dt.

Peak inductor current is shown by the next equation.

$$I_{LPK} = I_{MAX} + 1/2 \times I_{RIPPLEMAX}$$

$$I_{LPK} = 10 + 1/2 \times 4.43 = 12.215A$$

$$\text{Rate of change of Load Current} = \frac{dI_{LOAD}}{dt}$$

I_{MAX} = maximum load release = 10A

$$C_{OUT} = I_{LPK} \times \frac{L \times \frac{I_{LPK}}{V_{OUT}} - \frac{I_{MAX}}{dI_{LOAD}} \times dt}{2(V_{PK} - V_{OUT})}$$

Example

$$\frac{dI_{LOAD}}{dt} = \frac{2.5A}{1\mu s}$$

This would cause the output current to move from 10A to 0A in 4µs, giving the minimum output capacitance requirement shown in the following equation.

$$C_{OUT} = 12.215 \times \frac{1\mu H \times \frac{12.215}{1.5} - \frac{10}{2.5} \times 1\mu s}{2(1.65 - 1.5)}$$

$$C_{OUT} = 169\ \mu F$$

Applications Information (continued)

Note that C_{OUT} is much smaller in this example, 169µF compared to 316µF based on a worst-case load release. To meet the two design criteria of minimum 316µF and maximum 10.2mΩ ESR, select one capacitor of 330µF and 9mΩ ESR.

It is recommended that an additional small capacitor be placed in parallel with C_{OUT} in order to filter high frequency switching noise.

Stability Considerations

Unstable operation is possible with adaptive on-time controllers, and usually takes the form of double-pulsing or ESR loop instability.

Double-pulsing occurs due to switching noise seen at the FB input or because the FB ripple voltage is too low. This causes the FB comparator to trigger prematurely after the 250ns minimum off-time has expired. In extreme cases the noise can cause three or more successive on-times. Double-pulsing will result in higher ripple voltage at the output, but in most applications it will not affect operation. This form of instability can usually be avoided by providing the FB pin with a smooth, clean ripple signal that is at least 10mVp-p, which may dictate the need to increase the ESR of the output capacitors. It is also imperative to provide a proper PCB layout as discussed in the Layout Guidelines section.

Another way to eliminate doubling-pulsing is to add a small (~ 10pF) capacitor across the upper feedback resistor, as shown in Figure 12. This capacitor should be left unpopulated until it can be confirmed that double-pulsing exists. Adding the C_{TOP} capacitor will couple more ripple into FB to help eliminate the problem. An optional connection on the PCB should be available for this capacitor.

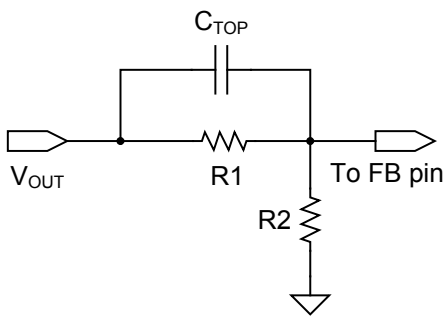


Figure 12 — Capacitor Coupling to FB Pin

ESR loop instability is caused by insufficient ESR. The details of this stability issue are discussed in the ESR Requirements section. The best method for checking stability is to apply a zero-to-full load transient and observe the output voltage ripple envelope for overshoot and ringing. Ringing for more than one cycle after the initial step is an indication that the ESR should be increased.

ESR Requirements

A minimum ESR is required for two reasons. One reason is to generate enough output ripple voltage to provide 10mVp-p at the FB pin (after the resistor divider) to avoid double-pulsing.

The second reason is to prevent instability due to insufficient ESR. The on-time control regulates the valley of the output ripple voltage. This ripple voltage is the sum of the two voltages. One is the ripple generated by the ESR, the other is the ripple due to capacitive charging and discharging during the switching cycle. For most applications the minimum ESR ripple voltage is dominated by the output capacitors, typically SP or POSCAP devices. For stability the ESR zero of the output capacitor should be lower than approximately one-third the switching frequency. The formula for minimum ESR is shown by the following equation.

$$ESR_{MIN} = \frac{3}{2 \times \pi \times C_{OUT} \times f_{sw}}$$

Using Ceramic Output Capacitors

When the system is using high ESR value capacitors, the feedback voltage ripple lags the phase node voltage by 90 degrees. Therefore, the converter is easily stabilized. When the system is using ceramic output capacitors, the ESR value is normally too small to meet the above ESR criteria. As a result, the feedback voltage ripple is 180 degrees from the phase node and behaves in an unstable manner. In this application it is necessary to add a small

Applications Information (continued)

virtual ESR network that is composed of two capacitors and one resistor, as shown in Figure 13.

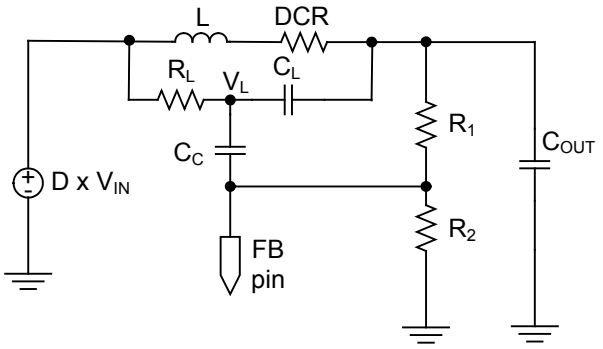


Figure 13 — Virtual ESR Ramp Circuit

The ripple voltage at FB is a superposition of two voltage sources: the voltage across C_L and output ripple voltage. They are defined in the following equations.

$$Vc_L = \frac{I_L \times DCR(s \times L/DCR + 1)}{S \times R_L C_L + 1}$$

$$\Delta V_{OUT} = \frac{\Delta I_L}{8C \times f_{SW}}$$

Figure 14 shows the magnitude of the ripple contribution due to C_L at the FB pin.

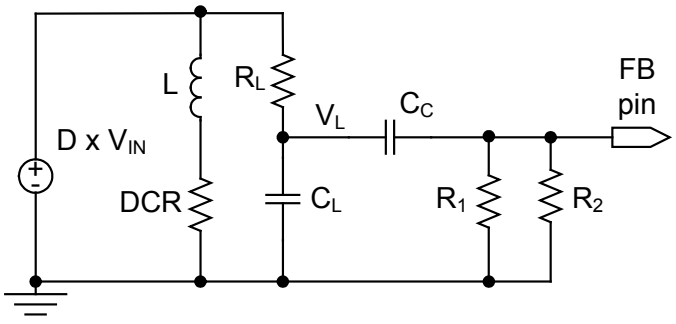


Figure 14 — FB Voltage by CL Voltage

It is shown by the following equation.

$$VFBc_L = Vc_L \times \frac{(R_1 // R_2) \times S \times C_C}{(R_1 // R_2) \times S \times C_C + 1}$$

Figure 15 shows the magnitude of the ripple contribution due to the output voltage ripple at the FB pin.

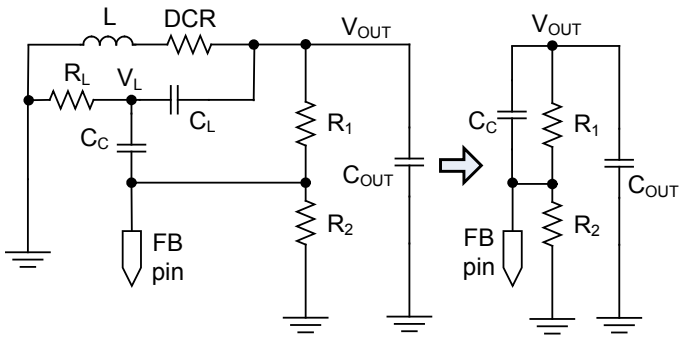


Figure 15 — FB Voltage by Output Voltage

It is shown by the following equation.

$$VFB\Delta V_{OUT} = \Delta V_{OUT} \times \frac{R_2}{R_1 // \frac{1}{S \times C_C} + R_2}$$

The purpose of this network is to couple the inductor current ripple information into the feedback voltage such that the feedback voltage has 90 degrees phase lag to the switching node similar to the case of using standard high ESR capacitors. This is illustrated in Figure 16.

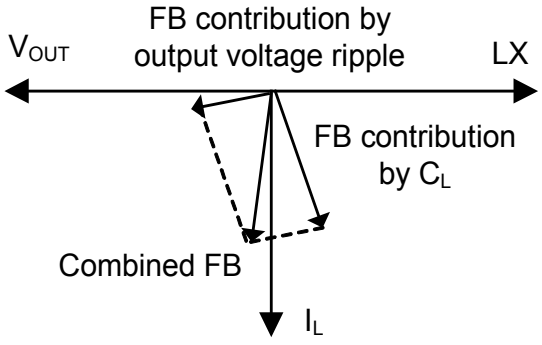


Figure 16 — FB voltage in Phasor Diagram

The magnitude of the feedback ripple voltage, which is dominated by the contribution from C_L, is controlled by the value of R_1, R_2 and C_C. If the corner frequency of (R_1// R_2) x C_C is too high, the ripple magnitude at the FB pin will be smaller, which can lead to double-pulsing. Conversely, if the corner frequency of (R_1// R_2) x C_C is too low, the ripple magnitude at FB pin will be higher. Since the

Applications Information (continued)

SC402B regulates to the valley of the ripple voltage at the FB pin, a high ripple magnitude is undesirable as it significantly impacts the output voltage regulation. As a result, it is desirable to select a corner frequency for (R_1// R_2) x C_C to achieve enough, but not excessive, ripple magnitude and phase margin. The component values for R_1, R_2, and C_C should be calculated using the following procedure.

Select C_L (typical 10nF) and R_L to match with L and DCR time constant using the following equation.

$$R_L = \frac{L}{DCR \times C_L}$$

Select C_C by using the following equation.

$$C_C \approx \frac{1}{R_1 // R_2} \times \frac{3}{2 \times \pi \times f_{sw}}$$

The resistor values (R_1 and R_2) in the voltage divider circuit set the V_{OUT} for the switcher. The typical value for C_C is from 10pF to 1nF.

Dropout Performance

The output voltage adjustment range for continuous conduction operation is limited by the fixed 250ns (typical) minimum off-time of the one-shot. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on and off times.

The duty-factor limitation is shown by the next equation.

$$DUTY = \frac{T_{ON(MIN)}}{T_{ON(MIN)} + T_{OFF(MAX)}}$$

The inductor resistance and MOSFET on-state voltage drops must be included when performing worst-case dropout duty-factor calculations.

System DC Accuracy (V_{OUT} Controller)

Three factors affect V_{OUT} accuracy: the trip point of the FB error comparator, the ripple voltage variation with line and load, and the external resistor tolerance. The error comparator offset is trimmed so that under static conditions it trips when the feedback pin is 750mV, 1%.

The on-time pulse from the SC402B in the design example is calculated to give a pseudo-fixed frequency of 300kHz. Some frequency variation with line and load is expected. This variation changes the output ripple voltage. Because adaptive on-time converters regulate to the valley of the output ripple, ½ of the output ripple appears as a DC regulation error. For example, if the output ripple is 50mV with V_{IN} = 6 volts, then the measured DC output will be 25mV above the comparator trip point. If the ripple increases to 80mV with V_{IN} = 25V, then the measured DC output will be 40mV above the comparator trip. The best way to minimize this effect is to minimize the output ripple.

The use of 1% feedback resistors may result in up to 1% error. If tighter DC accuracy is required, 0.1% resistors should be used.

The output inductor value may change with current. This will change the output ripple and therefore will have a minor effect on the DC output voltage. The output ESR also affects the output ripple and thus has a minor effect on the DC output voltage.

Switching Frequency Variation

The switching frequency varies with load current as a result of the power losses in the MOSFETs and DCR of the inductor. For a conventional PWM constant-frequency converter, as load increases the duty cycle also increases slightly to compensate for IR and switching losses in the MOSFETs and inductor. An adaptive on-time converter must also compensate for the same losses by increasing the effective duty cycle (more time is spent drawing energy from V_{IN} as losses increase). The on-time is essentially constant for a given V_{OUT}/V_{IN} combination, to offset the losses the off-time will tend to reduce slightly as load increases. The net effect is that switching frequency increases slightly with increasing load.

Applications Information (continued)

PCB Layout Guidelines

The optimum layout for the SC402B is shown in Figure 17. This layout shows an integrated FET buck regulator with a maximum current of 10A. The total PCB area is approximately 25 x 29 mm with single side components.

Critical Layout Guidelines

The following critical layout guidelines must be followed to ensure proper performance of the device.

- IC Decoupling capacitors
- PGND plane
- AGND island
- FB, VOUT, and other analog control signals
- C_{SS}
- BST, ILIM, and LX
- C_{IN} and C_{OUT} placement and Current Loops

IC Decoupling Capacitors

- A 1 µF capacitor must be located as close as possible to the IC and directly connected to pins 3 (VDD) and 4 (AGND).
- Another 1 µF capacitor must be located as close as possible to the IC and directly connected to pins 3 (VDD) and PGND plane.

PGND Plane

- PGND requires its own copper plane with no other signal traces routed on it.
- Copper planes, multiple vias and wide traces are needed to connect PGND to input capacitors, output capacitors, and the PGND pins on the IC.
- The PGND copper area between the input capacitors, output capacitors and PGND pins must be as tight and compact as possible to reduce the area of the PCB that is exposed to noise due to current flow on this node.

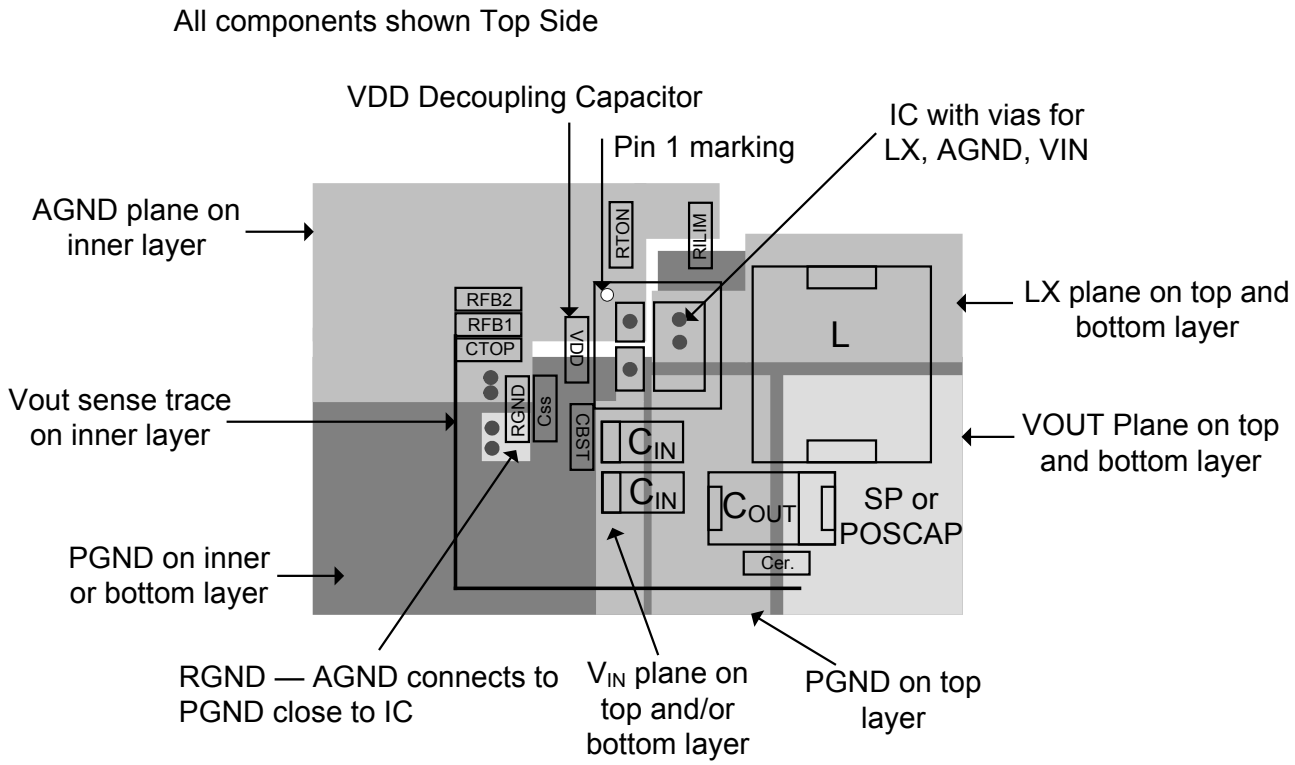


Figure 17 — PCB Layout

Applications Information (continued)

AGND Island

- AGND should have its own island of copper with no other signal traces routed on this layer that connects the AGND pins and pad of the IC to the analog control components.
- All of the components for the analog control circuitry should be located so that the connections to AGND are done by wide copper traces or vias down to AGND.
- Connect PGND to AGND with a short trace or 0Ω resistor. This connection should be as close to the IC as possible.

FB, VOUT, and Other Analog Control Signals

- The connection from the V_{OUT} power to the analog control circuitry must be routed from the output capacitors and located on a quiet layer.
- The traces between Vout and the analog control circuitry (VOUT, and FB pins) must be wide, short and routed away from noise sources, such as BST, LX, VIN, and PGND between the input capacitors, output capacitors, and the IC.
- The feedback components for the switcher and the LDO need to be as close to the FB and FBL pins of the IC as possible to reduce the possibility of noise corrupting these analog signals.

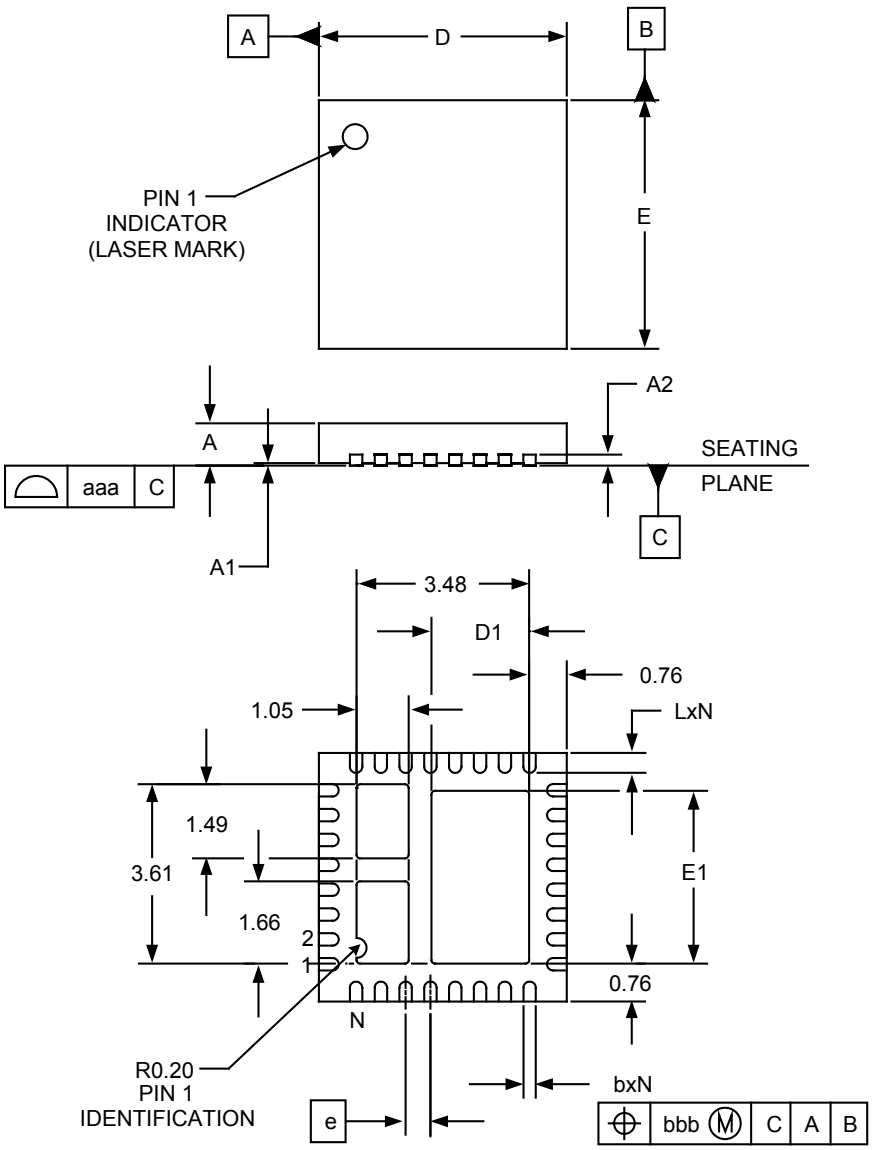
BST, ILIM,TON,SS and LX

- The connections for the boost capacitor between the BST and LXBST must be short, wide and directly connected.
- ILIM and TON nodes must be as short as possible to ensure the best accuracy in current limit and on time.
- R_{ILIM} should be close to the IC and connected between LXS (pin 28) and ILIM (pin 27) only.
- R_{TON} should be close to the IC and connected between TON (pin 31) and AGND (pin 30).
- C_{SOFT} should be close to the IC and kept away from the boost capacitor. Connect the AGND end of C_{SOFT} to the AGND plane at pin 4.
- The LX node between the IC and the inductor should be wide enough to handle the inductor current and short enough to eliminate the possibility of LX noise corrupting other signals.
- Multiple vias should be used on the LX PAD to provide good thermals and connection to an internal or bottom layer LX plane.

Capacitors and Current Loops

- Figure 17 shows the placement of input/output capacitors and inductor. This placement shows the smallest current loops between the input/output capacitors, the SC402B and the inductor to reduce the IR drop across the copper.

Outline Drawing — MLPQ-5x5-32

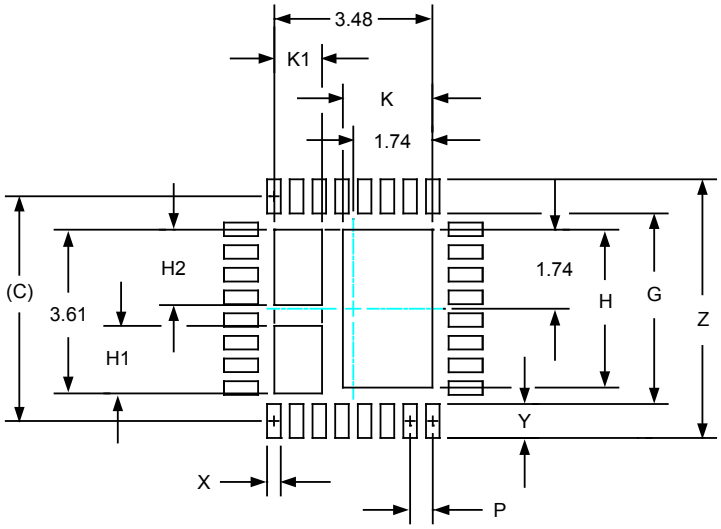


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.039	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.193	.197	.201	4.90	5.00	5.10
D1	.076	.078	.080	1.92	1.97	2.02
E	.193	.197	.201	4.90	5.00	5.10
E1	.135	.137	.139	3.43	3.48	3.53
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	32			32		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern — MLPQ-5x5-32



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.195)	(4.95)
G	.165	4.20
H	.137	3.48
H1	.059	1.49
H2	.065	1.66
K	.078	1.97
K1	.041	1.05
P	.020	0.50
X	.012	0.30
Y	.030	0.75
Z	.224	5.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
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   COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD
   SHALL BE CONNECTED TO A SYSTEM GROUND PLANE.
   FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR
   FUNCTIONAL PERFORMANCE OF THE DEVICE.
4. SQUARE PACKAGE-DIMENSIONS APPLY IN BOTH X AND Y DIRECTIONS.

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