

Applications

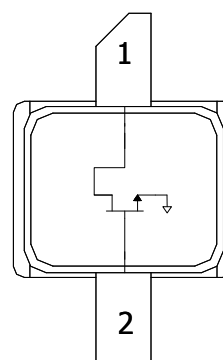
- Military radar
- Civilian radar
- Professional and military radio communications
- Test instrumentation
- Wideband or narrowband amplifiers
- Jammers



Product Features

- Frequency: DC to 6 GHz
- Output Power (P_{3dB}): 42.7 W at 3 GHz
- Linear Gain: >14 dB at 3 GHz
- Operating Voltage: 28 V
- Low thermal resistance package

Functional Block Diagram



General Description

The Qorvo T2G6003028-FS is a 30W (P_{3dB}) discrete GaN on SiC HEMT which operates from DC to 6 GHz. The device is constructed with Qorvo's proven QGaN25 process, which features advanced field plate techniques to optimize power and efficiency at high drain bias operating conditions. This optimization can potentially lower system costs in terms of fewer amplifier line-ups and lower thermal management costs.

Lead-free and ROHS compliant

Evaluation boards are available upon request.

Pin Configuration

Pin No.	Label
1	V_D / RF OUT
2	V_G / RF IN
Flange	Source

Ordering Information

Part	ECCN	Description
T2G6003028-FS	EAR99	Packaged part Flangeless
T2G6003028-FS-EVB1	EAR99	5.4 – 5.9 GHz Evaluation Board
T2G6003028-FS-EVB2	EAR99	1.3 – 1.9 GHz Evaluation Board

Absolute Maximum Ratings

Parameter	Value
Breakdown Voltage (V_{D0})	100 V
Gate Voltage Range (V_G)	-7 to 0 V
Drain Current (I_D)	5.5 A
Gate Current (I_G)	-10 to 28 mA
Power Dissipation (P_D)	47.5 W
RF Input Power, CW, $T = 25^\circ\text{C}$ (P_{IN})	40 dBm
Channel Temperature (T_{CH})	275 $^\circ\text{C}$
Mounting Temperature (30 Seconds)	320 $^\circ\text{C}$
Storage Temperature	-40 to 150 $^\circ\text{C}$

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions⁽¹⁾

Parameter	Value
Drain Voltage Range (V_D)	12 - 40 V
Drain Quiescent Current (I_{DQ})	200 mA (Typ.)
Peak Drain Current (I_D)	1.7 A (Typ.)
Gate Voltage (V_G)	-3.3 V (Typ.)
Channel Temperature (T_{CH})	225 $^\circ\text{C}$ (Max)
Power Dissipation, CW (P_D)	35 W (Max)
Power Dissipation, Pulse (P_D) ⁽²⁾	40 W (Max)

- Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.
- Pulse Width = 380 μs , Duty Cycle = 50%

RF Characterization – Optimum Power Tuned Load Pull Performance

Test conditions unless otherwise noted: $T = 25^\circ\text{C}$.

Parameter	Typical Value						Units
	1	2	3	4	5	6	
Frequency (F)	1	2	3	4	5	6	GHz
Drain Voltage (V_D)	28	28	28	28	28	28	V
Bias Current (I_{DQ})	200	200	200	200	200	200	mA
Output P3dB (P_{3dB})	45.7	46	46.3	46.5	46.8	46.2	dBm
PAE @ P3dB (PAE_{3dB})	64.9	64.2	68.1	54.6	55.9	54.7	%
Gain @ P3dB (G_{3dB})	19.9	15.7	11.3	10.1	10.7	12.1	dB

Notes:

- $V_d = 28\text{ V}$, $I_{dq} = 200\text{ mA}$, Pulse Width = 100 μs , Duty Cycle = 20%
- Characteristic Impedance (Z_0) = 10 Ω . See pg. 18 for Load Pull Reference Planes.

RF Characterization – Optimum Efficiency Tune Load Pull Performance

Test conditions unless otherwise noted: $T = 25^\circ\text{C}$.

Parameter	Typical Value						Units
	1	2	3	4	5	6	
Frequency (F)	1	2	3	4	5	6	GHz
Drain Voltage (V_D)	28	28	28	28	28	28	V
Bias Current (I_{DQ})	200	200	200	200	200	200	mA
Output P3dB (P_{3dB})	43.1	43.1	44.6	44.1	44.9	45.7	dBm
PAE @ P3dB (PAE_{3dB})	73	76	46.1	65.1	69.5	60	%
Gain @ P3dB (G_{3dB})	19.7	16.2	11.7	10.8	12.4	12.9	dB

Notes:

- $V_d = 28\text{ V}$, $I_{dq} = 200\text{ mA}$, Pulse Width = 100 μs , Duty Cycle = 20%
- Characteristic Impedance (Z_0) = 10 Ω . See pg. 18 for Load Pull Reference Planes.

RF Characterization – Performance at 5.6 GHz ^(1, 2)

Symbol	Parameter	Min	Typical	Max	Units
G _{LIN}	Linear Gain	12.0	14.0	17.0	dB
P _{3dB}	Output Power at 3 dB Gain Compression	43.0	44.6	46.0	dBm
DE _{3dB}	Drain Efficiency at 3 dB Gain Compression	45.0	54.0	70.0	%
G _{3dB}	Gain at 3 dB Compression	9.0	11.0	14.0	dB

Notes:

1. Performance at 5.6 GHz in the 5.4 to 5.9 GHz Evaluation Board
2. V_{DS} = 28 V, I_{DQ} = 200 mA; Pulse: 100μs, 20%

RF Characterization – Mismatch Ruggedness at 5.6 GHz ⁽¹⁾

Test conditions unless otherwise noted: T_A = 25 °C, V_D = 28 V, I_{DQ} = 200 mA

Symbol	Parameter	Typical
VSWR	Impedance Mismatch Ruggedness	10:1

Notes:

1. P_{1dB} CW Input Power under matched condition.

Thermal and Reliability - CW ⁽¹⁾

Parameter	Test Conditions	Value	Units
Thermal Resistance, θ_{JC}	$P_D = 30\text{ W}$, $T_{base} = 85^\circ\text{C}$	3.82	$^\circ\text{C/W}$
Maximum Channel Temperature, T_{CH}		200	$^\circ\text{C}$
Median Lifetime, T_M		1.54E7	Hrs
Thermal Resistance, θ_{JC}	$P_D = 35\text{ W}$, $T_{base} = 85^\circ\text{C}$	4.01	$^\circ\text{C/W}$
Maximum Channel Temperature, T_{CH}		225	$^\circ\text{C}$
Median Lifetime, T_M		1.80E6	Hrs
Thermal Resistance, θ_{JC}	$P_D = 40\text{ W}$, $T_{base} = 85^\circ\text{C}$	4.22	$^\circ\text{C/W}$
Maximum Channel Temperature, T_{CH}		254	$^\circ\text{C}$
Median Lifetime, T_M		1.93E5	Hrs
Thermal Resistance, θ_{JC}	$P_D = 45\text{ W}$, $T_{base} = 85^\circ\text{C}$	4.43	$^\circ\text{C/W}$
Maximum Channel Temperature, T_{CH}		284	$^\circ\text{C}$
Median Lifetime, T_M		2.41E4	Hrs

Notes:

1. Thermal resistance calculated to bottom of package.

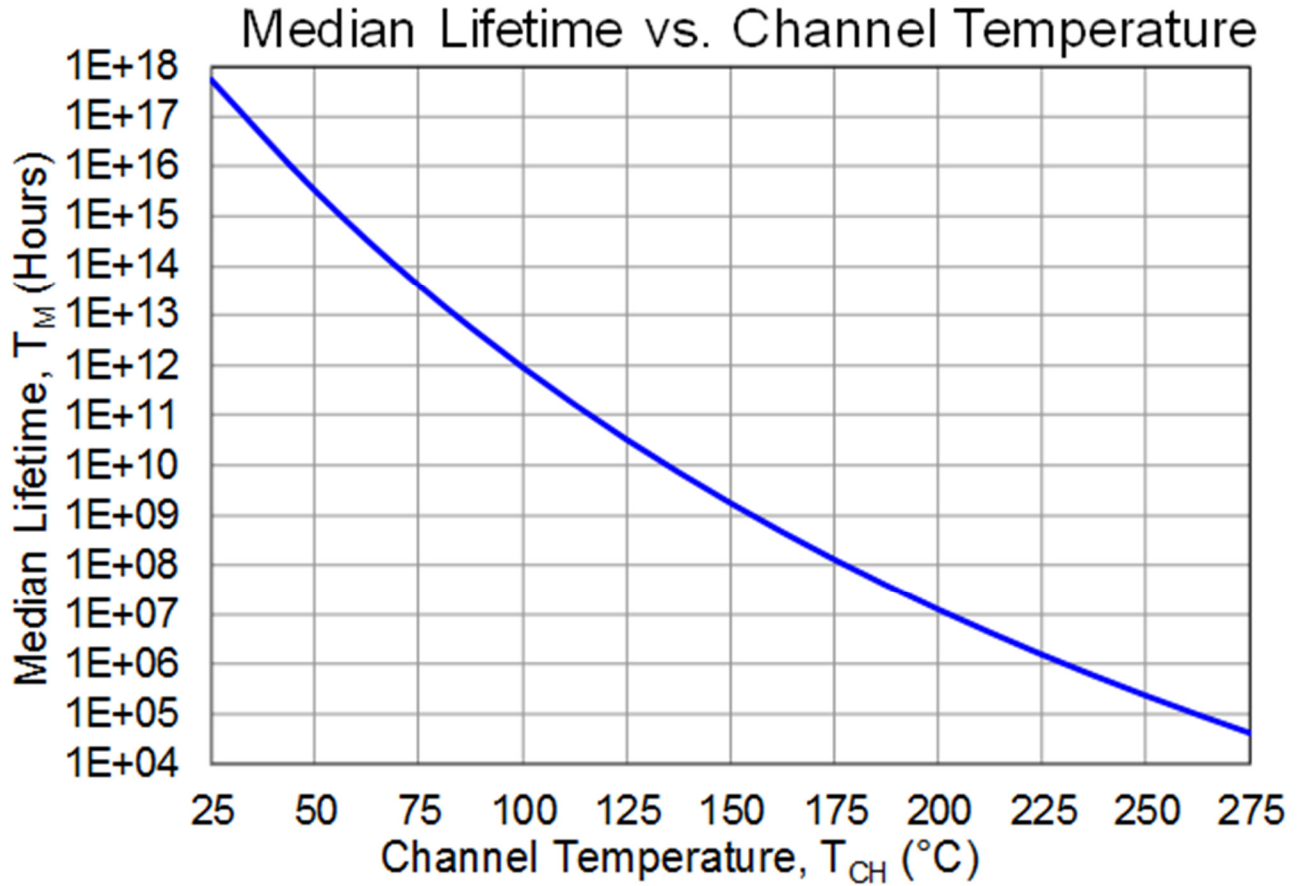
Thermal and Reliability - Pulsed ⁽¹⁾

Parameter	Test Conditions	Value	Units
Thermal Resistance, θ_{JC}	$P_D = 40\text{ W}$, $T_{base} = 85^\circ\text{C}$ Pulse Width = 100 μS Duty Cycle = 5%	2.33	$^\circ\text{C/W}$
Peak Channel Temperature, T_{CH}		178	$^\circ\text{C}$
Median Lifetime, T_M		2.52E9	Hrs
Thermal Resistance, θ_{JC}	$P_D = 40\text{ W}$, $T_{base} = 85^\circ\text{C}$ Pulse Width = 100 μS Duty Cycle = 10%	2.43	$^\circ\text{C/W}$
Peak Channel Temperature, T_{CH}		182	$^\circ\text{C}$
Median Lifetime, T_M		8.60E8	Hrs
Thermal Resistance, θ_{JC}	$P_D = 40\text{ W}$, $T_{base} = 85^\circ\text{C}$ Pulse Width = 100 μS Duty Cycle = 20%	2.68	$^\circ\text{C/W}$
Peak Channel Temperature, T_{CH}		192	$^\circ\text{C}$
Median Lifetime, T_M		1.65E8	Hrs
Thermal Resistance, θ_{JC}	$P_D = 40\text{ W}$, $T_{base} = 85^\circ\text{C}$ Pulse Width = 100 μS Duty Cycle = 50%	3.18	$^\circ\text{C/W}$
Peak Channel Temperature, T_{CH}		212	$^\circ\text{C}$
Median Lifetime, T_M		1.10E7	Hrs

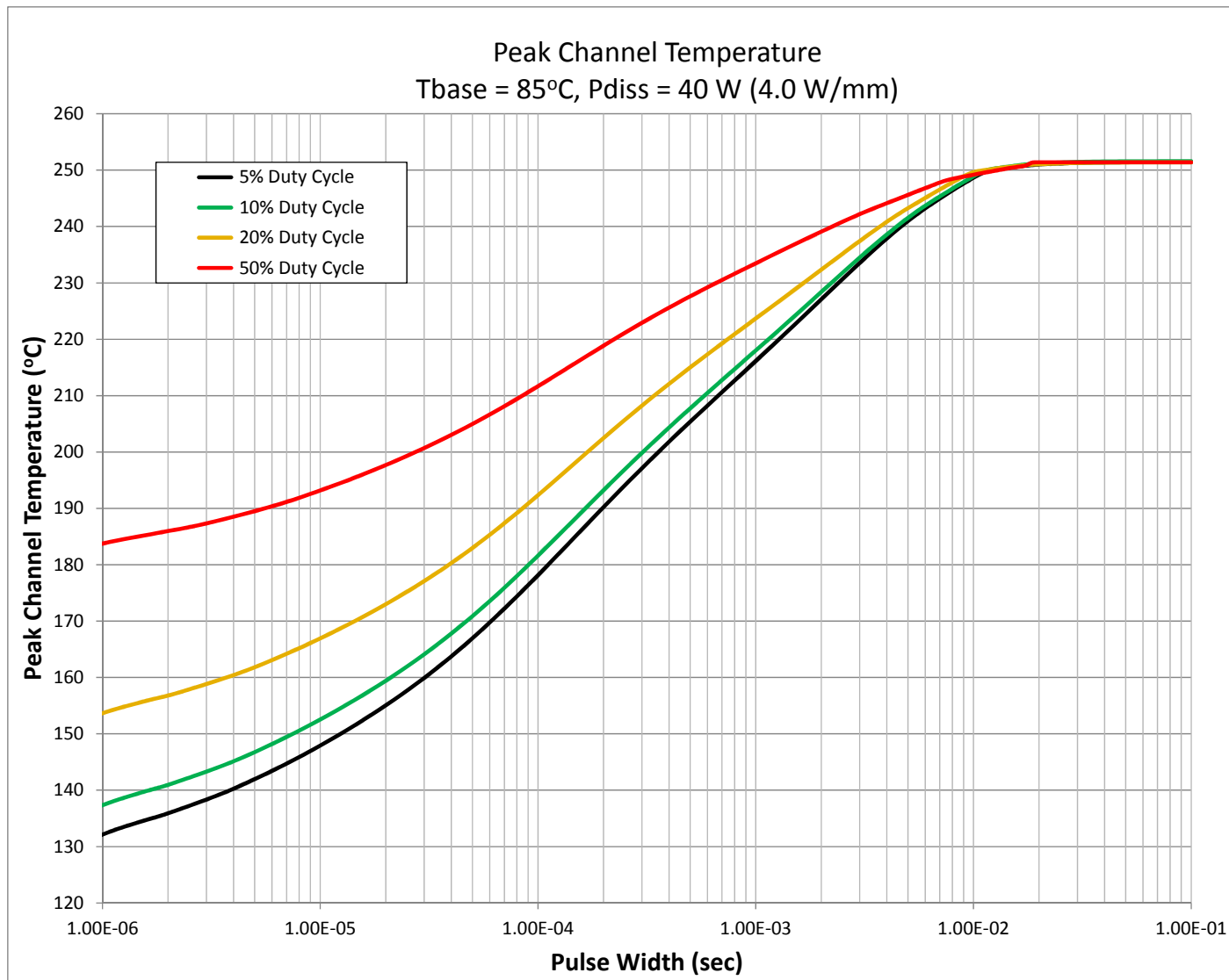
Notes:

2. Thermal resistance calculated to bottom of package.

Median Lifetime



Maximum Channel Temperature

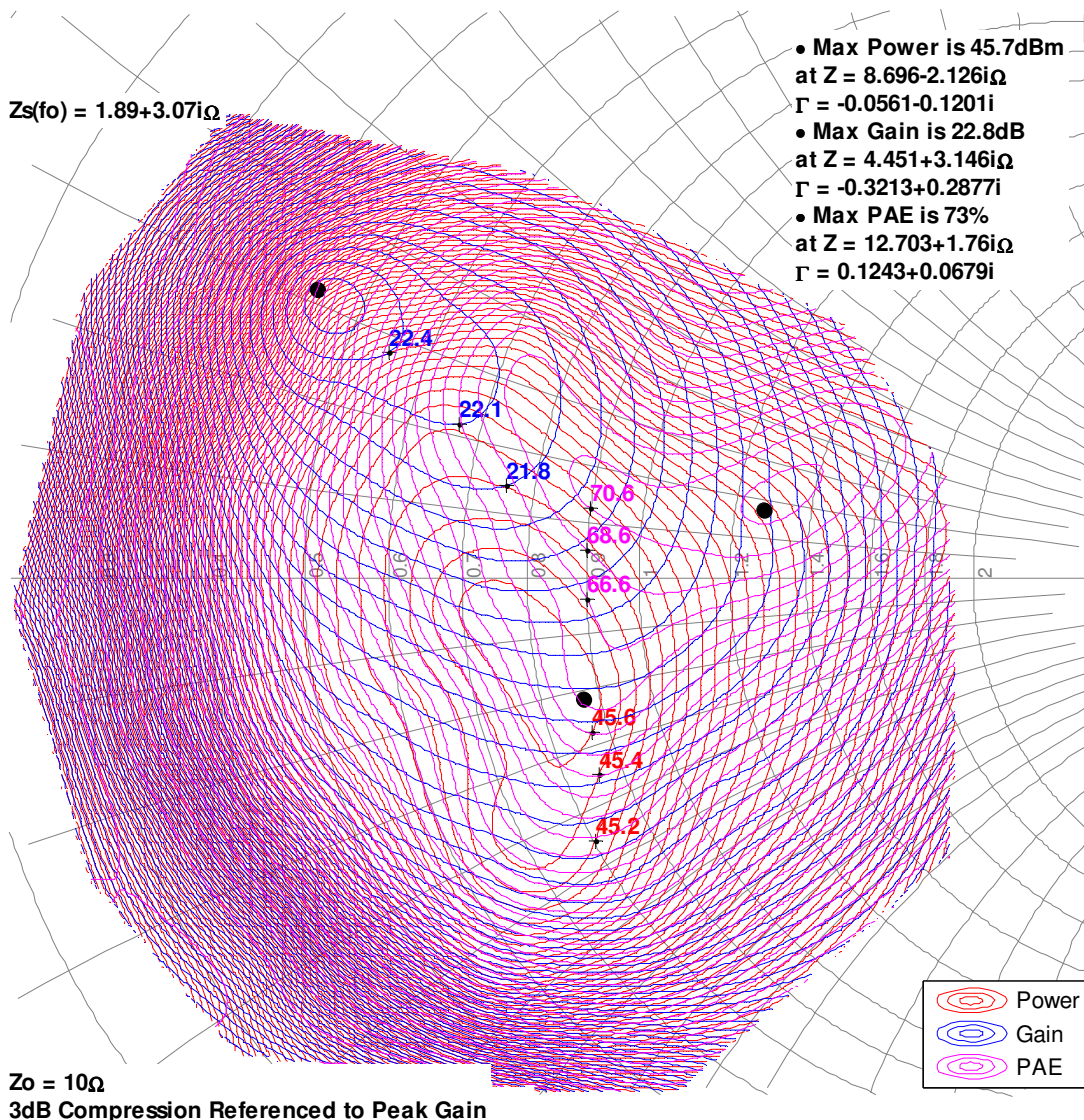


Load Pull Smith Charts (1, 2, 3)

Notes:

1. Test Conditions: $V_{DS} = 28\text{ V}$, $I_{DQ} = 200\text{ mA}$
2. Test Signal: Pulse Width = 100 μsec , Duty Cycle = 20%
3. See pg. 18 for load pull reference planes.

1GHz, Load-pull

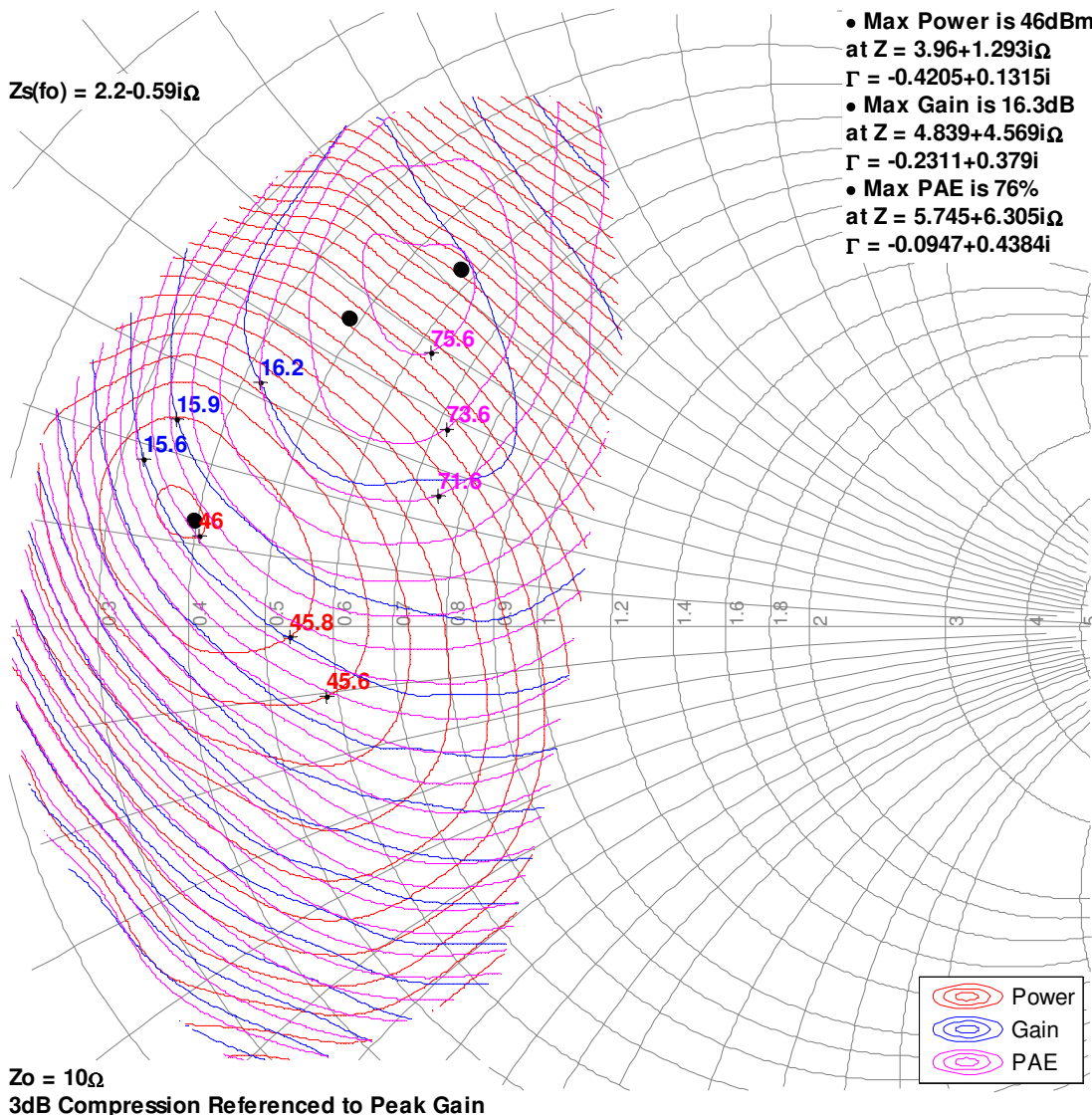


Load Pull Smith Charts (1, 2, 3)

Notes:

1. Test Conditions: $V_{DS} = 28\text{ V}$, $I_{DQ} = 200\text{ mA}$
2. Test Signal: Pulse Width = 100 μsec , Duty Cycle = 20%
3. See pg. 18 for load pull reference planes.

2GHz, Load-pull

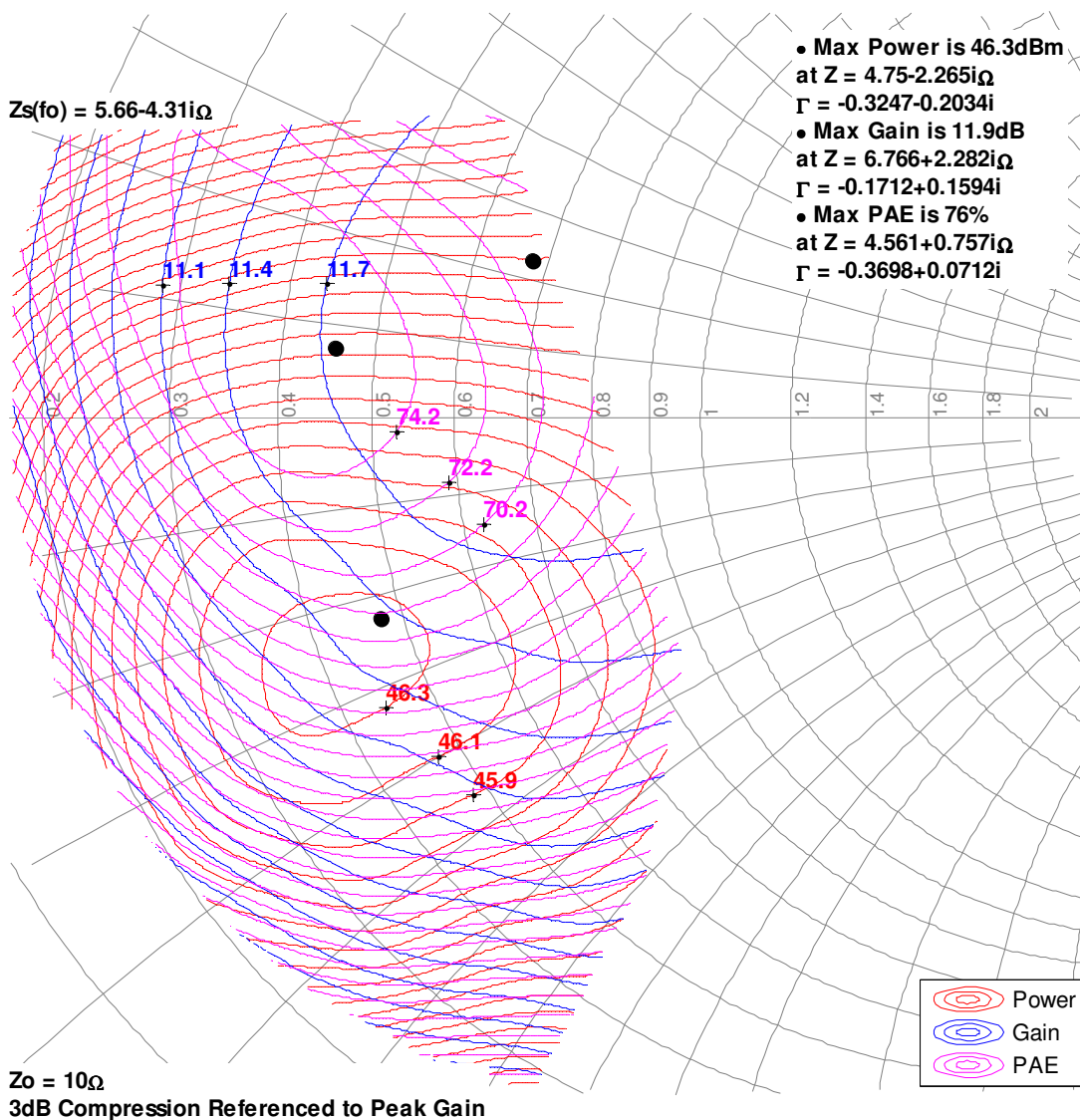


Load Pull Smith Charts (1, 2, 3)

Notes:

1. Test Conditions: $V_{DS} = 28\text{ V}$, $I_{DQ} = 200\text{ mA}$
2. Test Signal: Pulse Width = 100 μsec , Duty Cycle = 20%
3. See pg. 18 for load pull reference planes.

3GHz, Load-pull

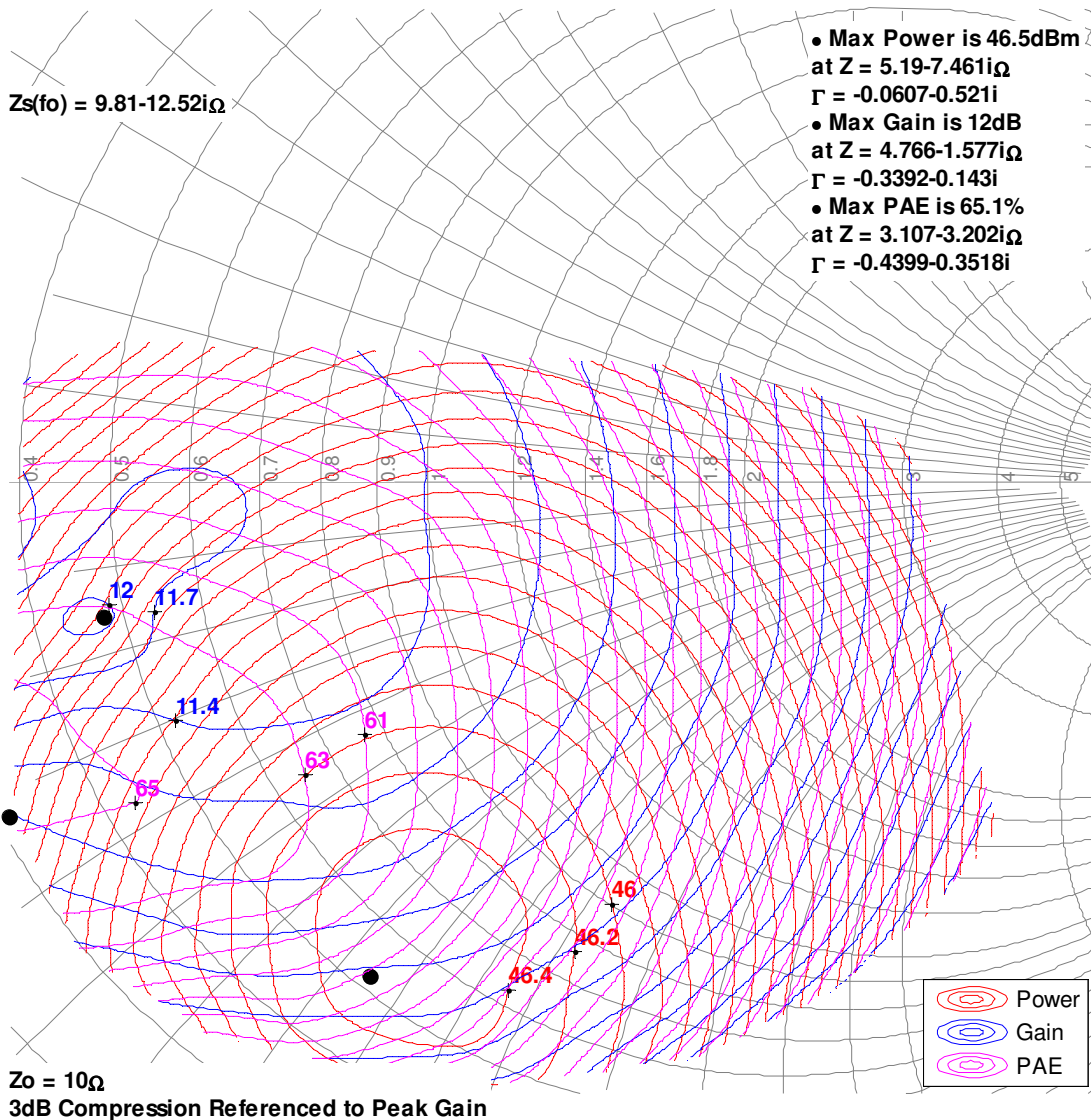


Load Pull Smith Charts (1, 2, 3)

Notes:

1. Test Conditions: $V_{DS} = 28\text{ V}$, $I_{DQ} = 200\text{ mA}$
2. Test Signal: Pulse Width = 100 μsec , Duty Cycle = 20%
3. See pg. 18 for load pull reference planes.

4GHz, Load-pull

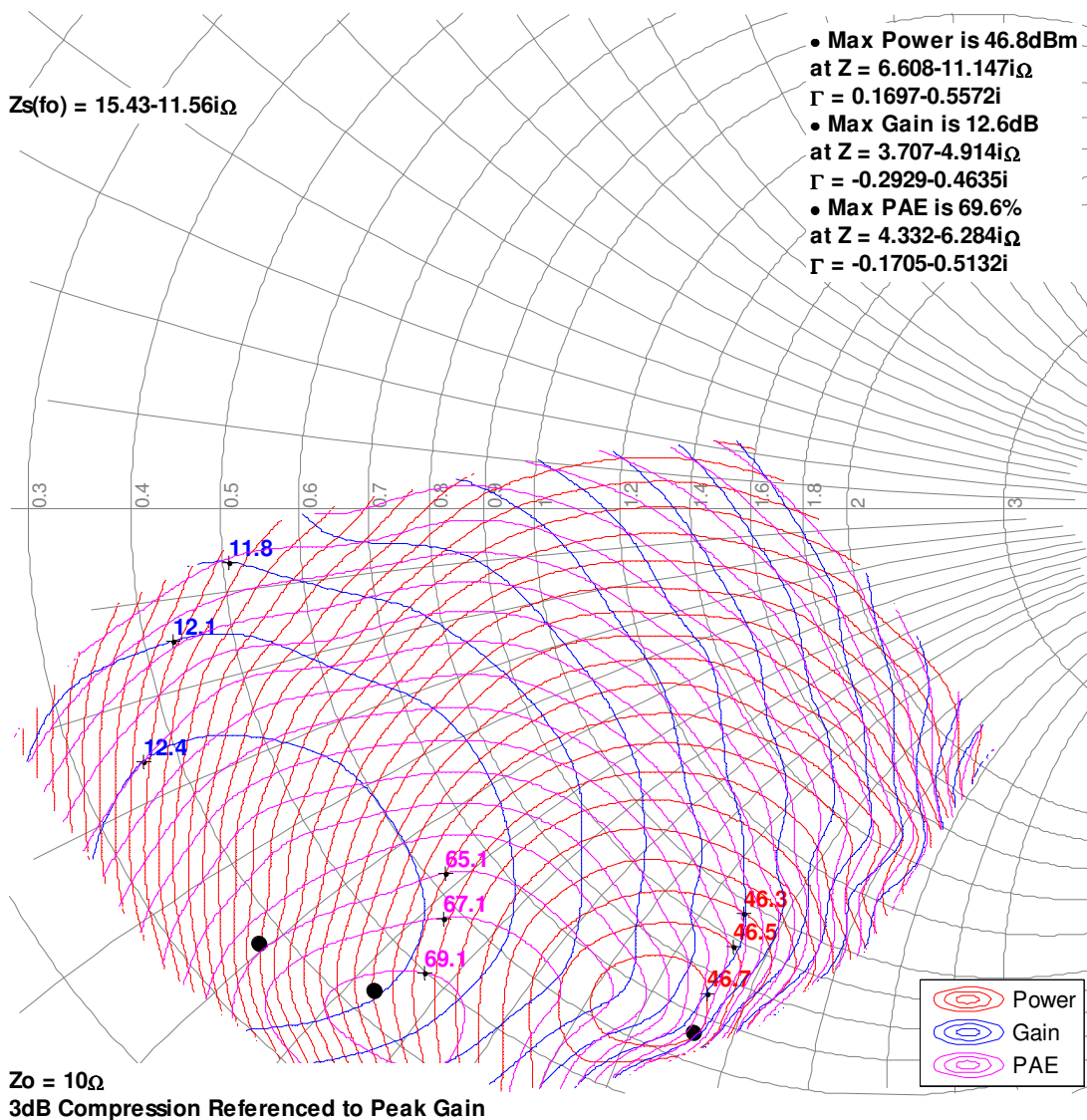


Load Pull Smith Charts (1, 2, 3)

Notes:

1. Test Conditions: $V_{DS} = 28\text{ V}$, $I_{DQ} = 200\text{ mA}$
2. Test Signal: Pulse Width = 100 μsec , Duty Cycle = 20%
3. See pg. 18 for load pull reference planes.

5GHz, Load-pull

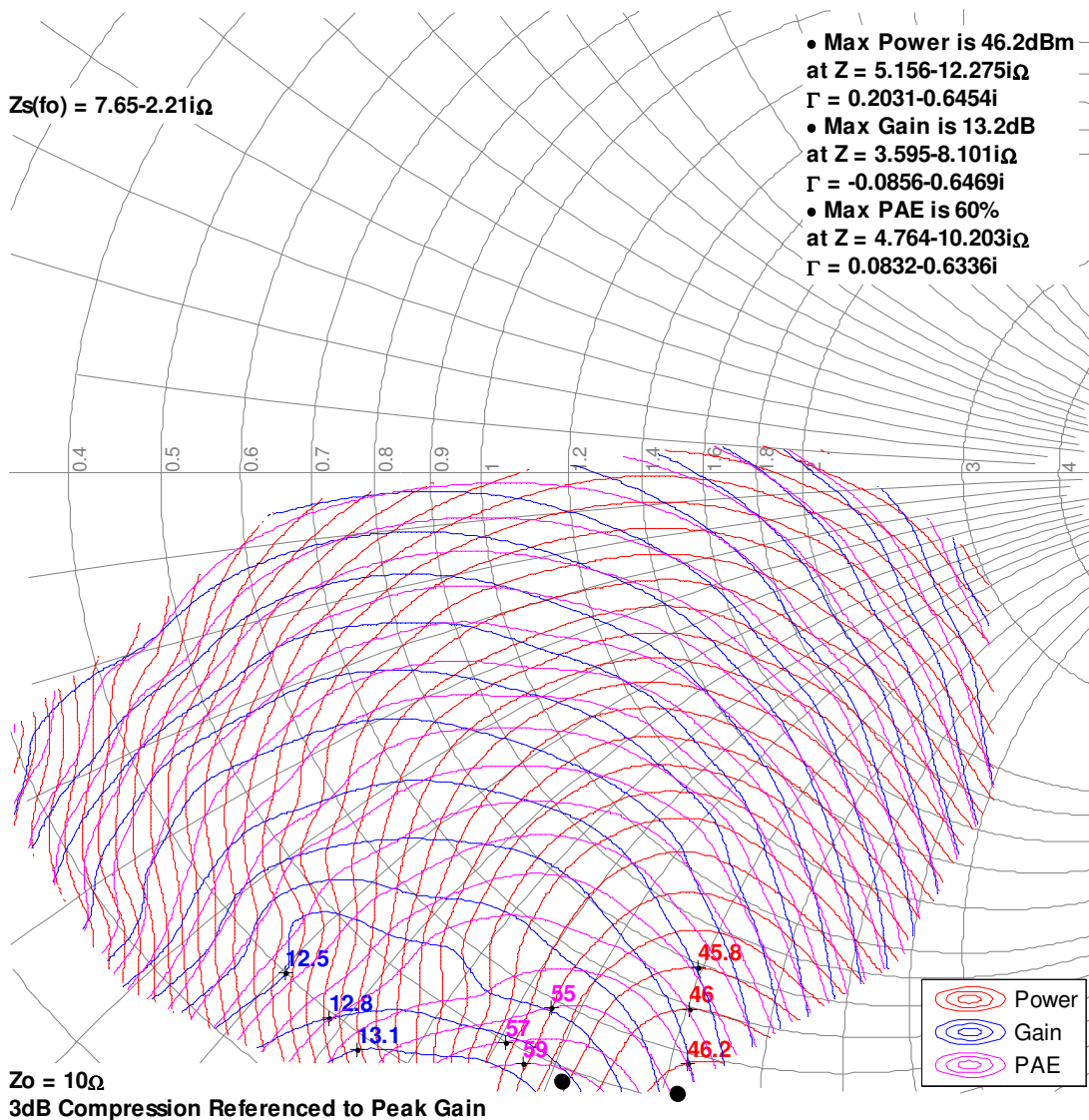


Load Pull Smith Charts (1, 2, 3)

Notes:

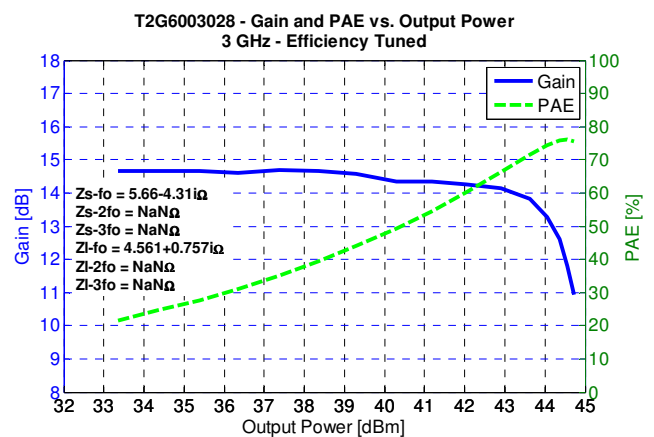
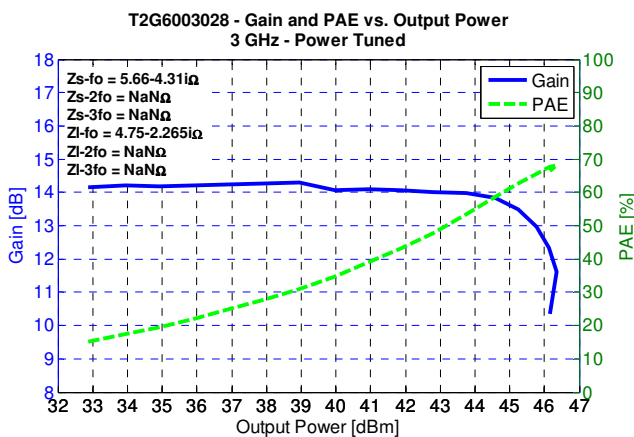
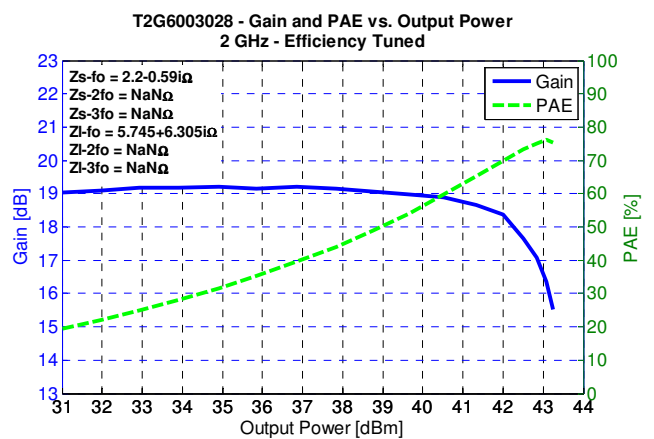
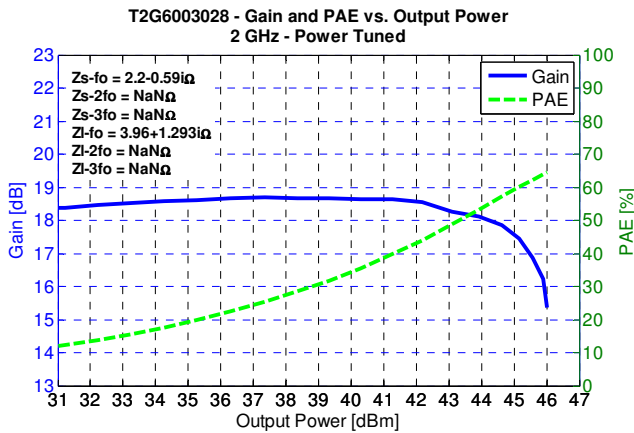
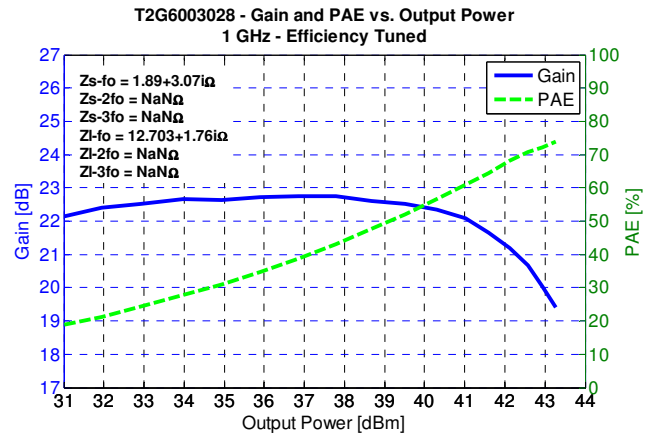
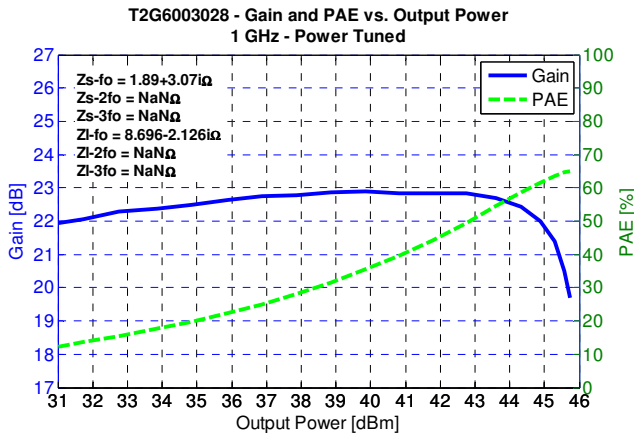
1. Test Conditions: $V_{DS} = 28\text{ V}$, $I_{DQ} = 200\text{ mA}$
2. Test Signal: Pulse Width = 100 μsec , Duty Cycle = 20%
3. See pg. 18 for load pull reference planes.

6GHz, Load-pull



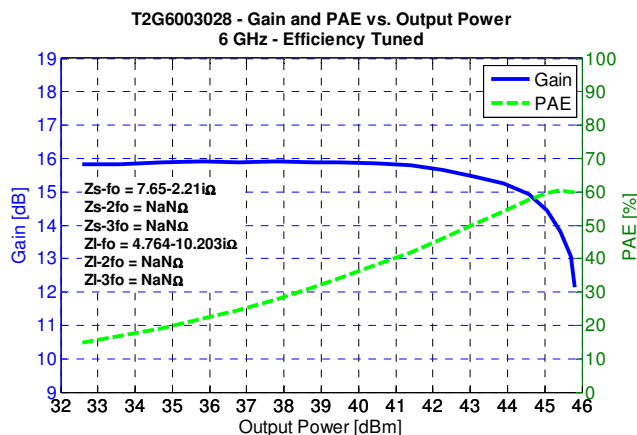
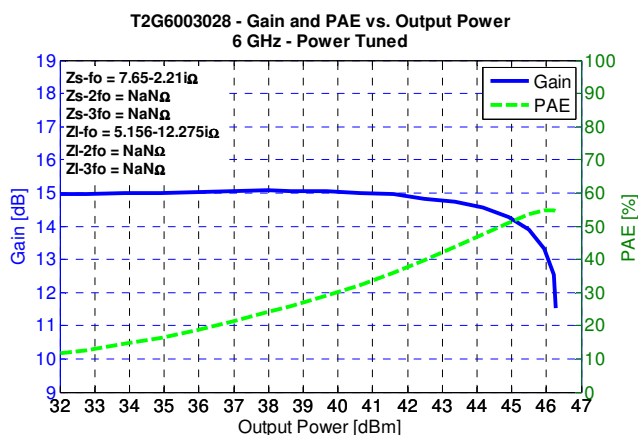
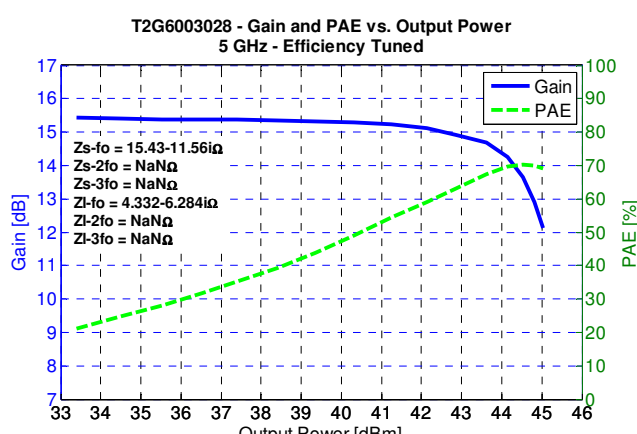
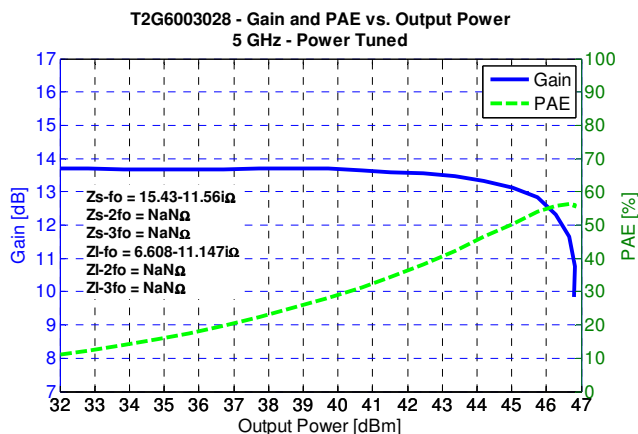
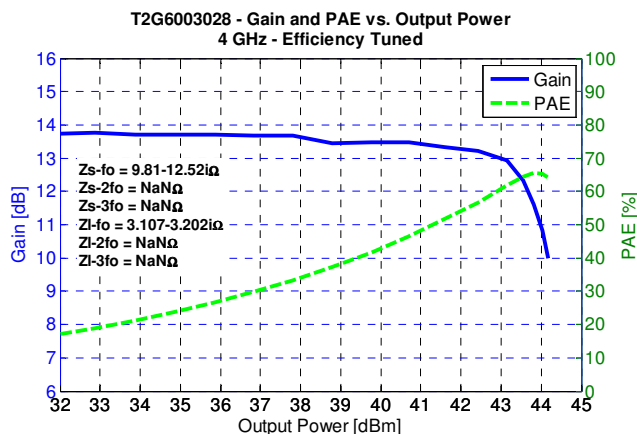
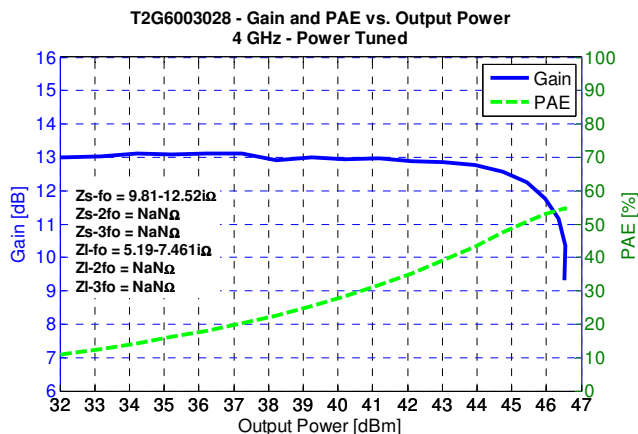
Characterization Drive-up ^(1, 2)

- V_d = 28 V, I_{dq} = 200 mA, Pulse Width = 100 uS, Duty Cycle = 20%
- NaN means the parameter is either unavailable or undefined.



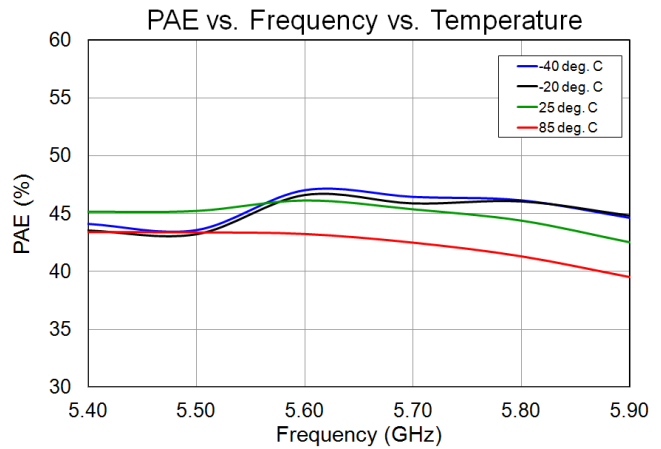
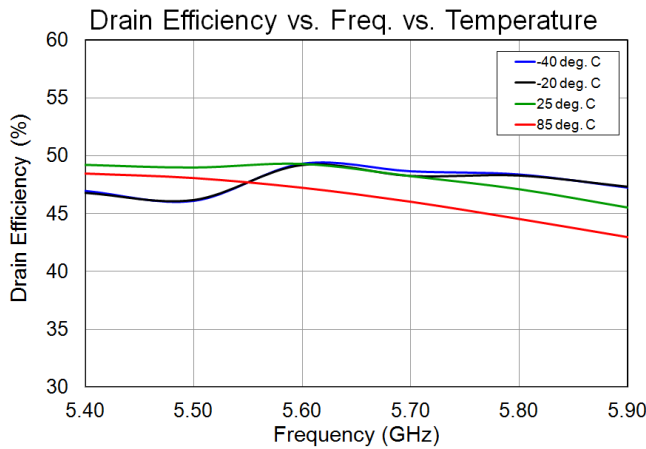
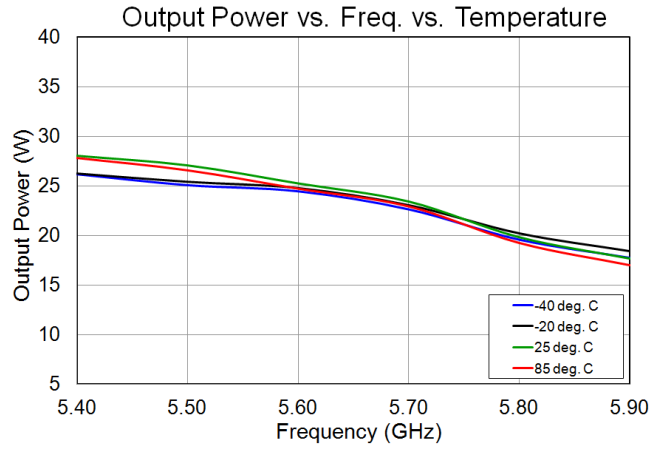
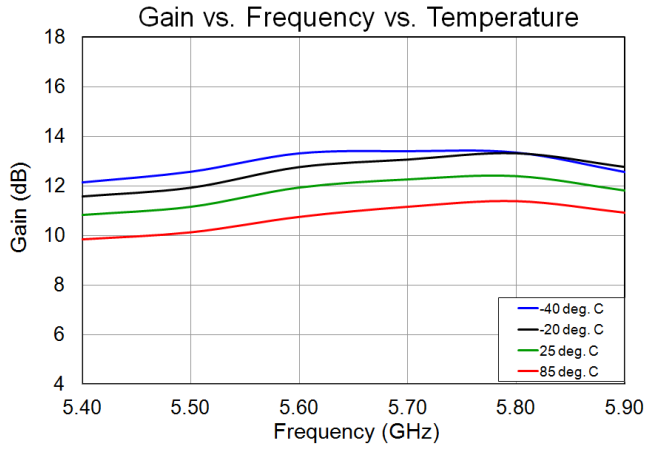
Characterization Drive-up ^(1, 2)

- V_d = 28 V, I_{dq} = 200 mA, Pulse Width = 100 uS, Duty Cycle = 20%
- NaN means the parameter is either unavailable or undefined.



Performance Over Temperature (1, 2)

Performance measured in Qorvo's 5.4 GHz to 5.9 GHz Evaluation Board at 3 dB compression.

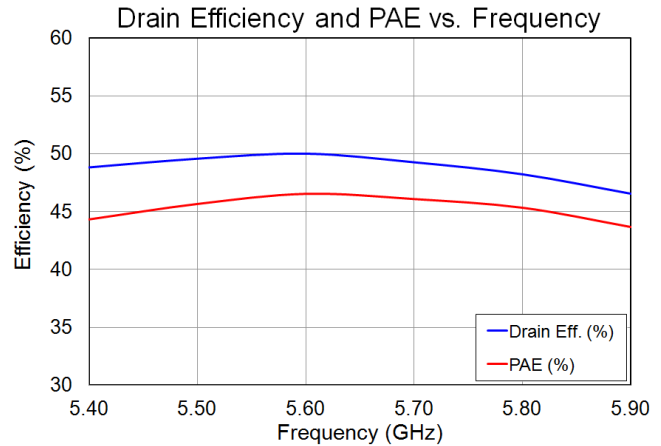
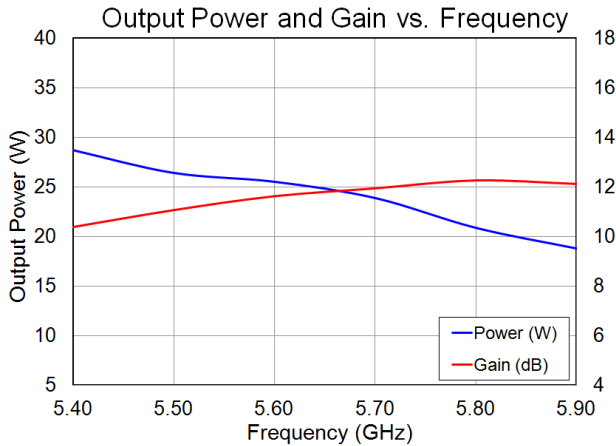


Notes:

1. Test Conditions: $V_{DS} = 28\text{ V}$, $I_{DQ} = 200\text{ mA}$
2. Test Signal: Pulse Width = 100 μs , Duty Cycle = 20%

Evaluation Board Performance (1, 2)

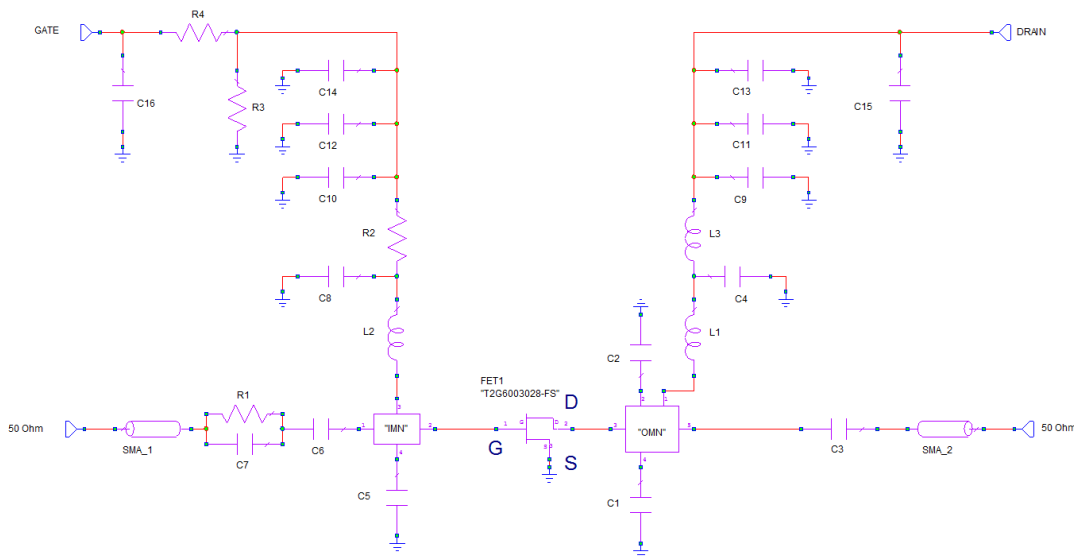
Performance at 3 dB Compression



Notes:

1. Test Conditions: $V_{DS} = 28\text{ V}$, $I_{DQ} = 200\text{ mA}$
2. Test Signal: Pulse Width = $100\text{ }\mu\text{s}$, Duty Cycle = 20 %

Application Circuit



Bias-up Procedure

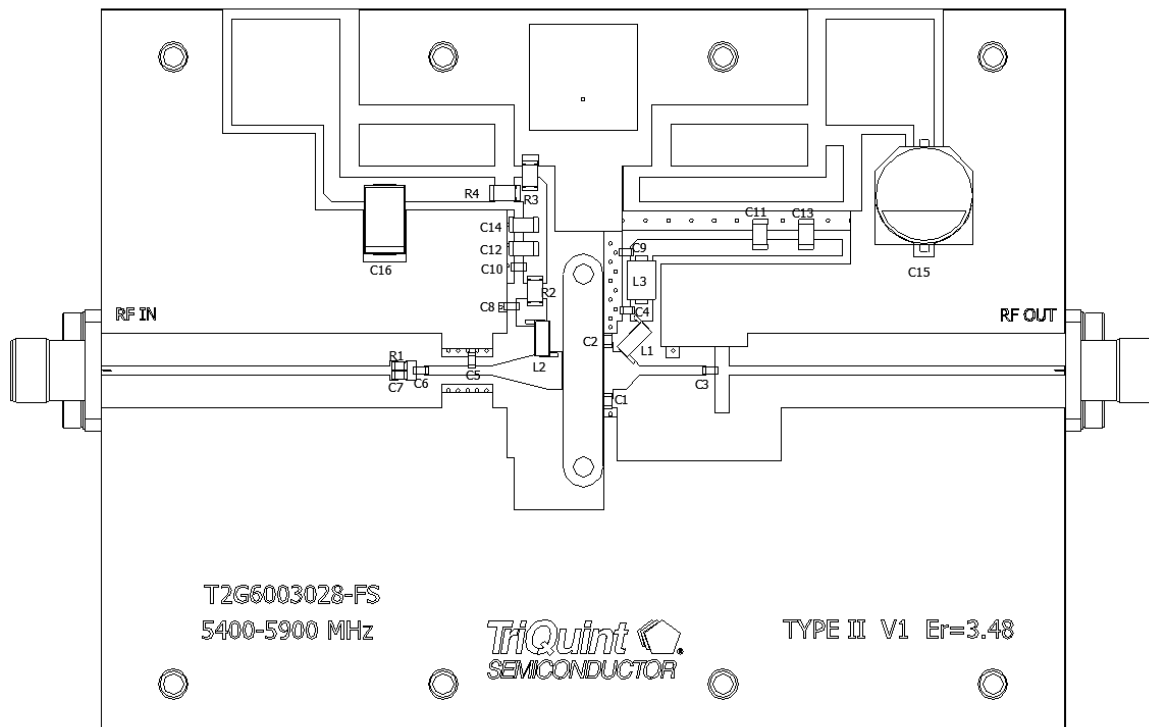
- Set gate voltage (V_G) to -5.0 V .
- Set drain current (I_D) limit to 220 mA .
- Set drain voltage (V_D) to 28 V .
- Slowly increase V_G until quiescent I_D is 200 mA .
- Set drain current (I_D) to 2.8 A .
- Apply RF signal.

Bias-down Procedure

- Turn off RF signal.
- Turn off V_D and wait 1 second to allow drain capacitor discharge.
- Turn off V_G .

Evaluation Board Layout

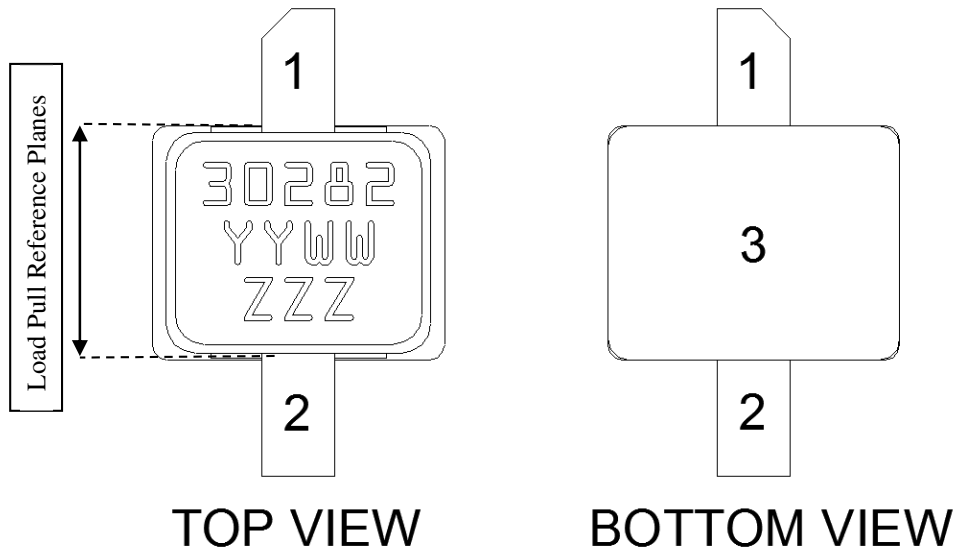
Top RF layer is 0.020" thick Rogers RO4350B, $\epsilon_r = 3.48$. The pad pattern shown has been developed and tested for optimized assembly at Qorvo Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances.



Bill of Materials

Reference Design	Value	Qty	Manufacturer	Part Number
C1	0.3 pF	1	ATC	ATC600S0R3
C2	0.2 pF	1	ATC	ATC600S0R2
L1, L2	8.8 NH	2	COILCRAFT	1606-8
C3, C4, C6, C7, C8	3 pF	5	ATC	ATC600S3R0
C5	0.4 pF	1	ATC	ATC600S0R5
R1	97.6 Ohms	1	Venkel	CR0604-16w-97R6FT
R2	4.7 Ohms	1	Newark	37C0064
R3	330 Ohms	1	Newark	TNPW1206330RBT9ET1-E3
R4	50 Ohms	1	ATC	CRCW120651R0FKEA
C9, C10	220 pF	2	AVX	AVX06035C22KAT2A
C11, C12	2200 pF	2	Vitramon	VJ1206Y222KXA
C13, C14	22000 pF	2	Vitramon	VJ1206Y223KXA
C15	220 uF	1	United Chemi-Con	EMVY500ADA221MJA0G
C16	1.0 uF	1	Allied	541-1231
L3	48 Ohm	1	Ferrite, Laird Tech.	28F0121-0SR-10

Pin Layout



Note:

The T2G6003028-FS will be marked with the “30282” designator and a lot code marked below the part designator. The “YY” represents the last two digits of the calendar year the part was manufactured, the “WW” is the work week of the assembly lot start, and the “ZZZ” is an auto-generated number.

Pin Description

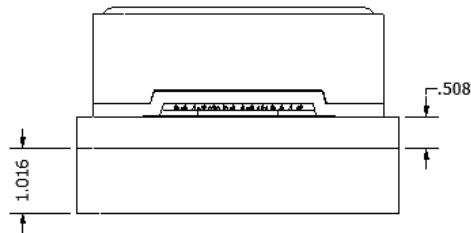
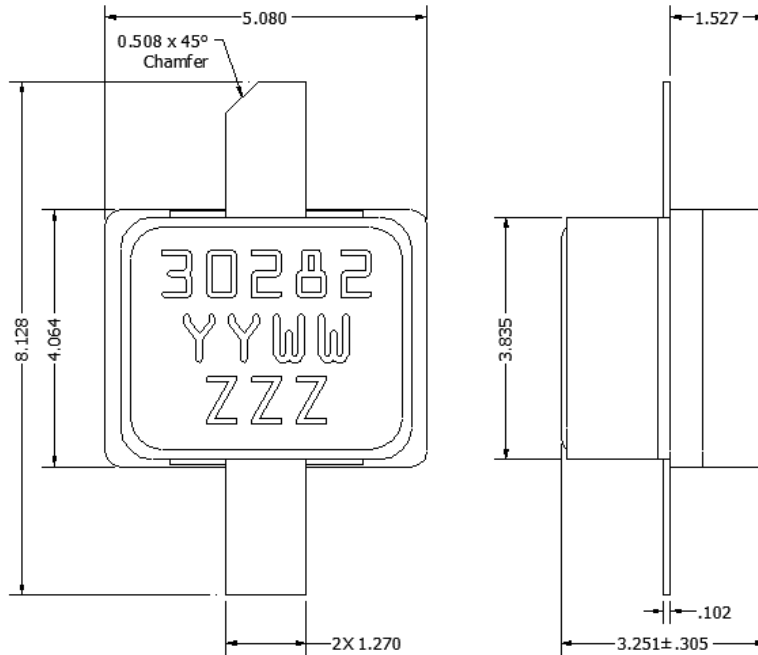
Pin	Symbol	Description
1	V_D / RF OUT	Drain voltage / RF Output matched to 50 ohms; see EVB Layout on page 17 as an example.
2	V_G / RF IN	Gate voltage / RF Input matched to 50 ohms; see EVB Layout on page 17 as an example.
3	Flange	Source connected to ground; see EVB Layout on page 17 as an example.

Notes:

Thermal resistance measured to bottom of package

Mechanical Information

All dimensions are in millimeters.



TOLERANCES
 X.XX = ± .25
 X.XXX = ± .127
 X.XXXX = ± .0254
 ANGLES = 0.5°

Note:

This package is lead-free/RoHS-compliant. The plating material on the leads is NiAu. It is compatible with both lead-free (maximum 260 °C reflow temperature) and tin-lead (maximum 245°C reflow temperature) soldering processes.

Product Compliance Information

ESD Sensitivity Ratings



Caution! ESD-Sensitive Device

ESD Rating: Class 1A
 Value: Passes ≥ 250 V to < 500 V max.
 Test: Human Body Model (HBM)
 Standard: JEDEC Standard JESD22-A114

MSL Rating

Level 3 at $+260$ °C convection reflow
 The part is rated Moisture Sensitivity Level 3 at 260 °C per JEDEC standard IPC/JEDEC J-STD-020.

ECCN

US Department of Commerce EAR99

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260 °C

RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Recommended Soldering Temperature Profile

