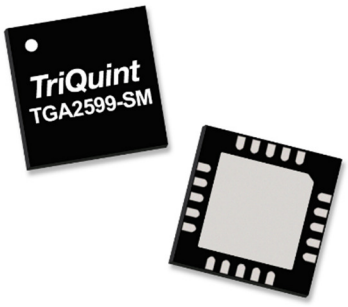
TGA2599-SM

5.0-8.0 GHz GaN Driver Amplifier

Applications

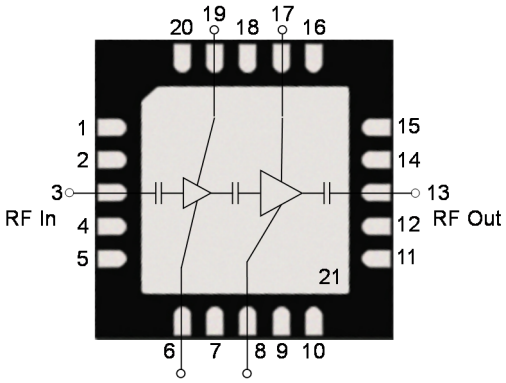
- C-Band Radar
- Communications



Product Features

- Frequency Range: 5.0-8.0 GHz
- Small Signal Gain: > 23 dB
- Power: > 33 dBm
- PAE: > 34%
- IM3: -25 dBc
- Bias: V_D = 25 V, I_{DQ} = 50 mA
- Package Dimensions: 4.0 x 4.0 x 0.85 mm

Functional Block Diagram



General Description

TriQuint's TGA2599-SM is a packaged driver amplifier fabricated on TriQuint's TQGaN25 0.25um GaN on SiC production process. The TGA2599-SM operates from 5.0 to 8.0GHz and provides 33 dBm of output power with 15 dB of large signal gain and 34 % power-added efficiency.

Using GaN MMIC technology and plastic packaging, the TGA2599-SM provides a low cost driver solution that provides the added benefit of operating on the same voltage rail as the corresponding GaN HPA. It can also serve as the primary amplifier on lower power architectures.

The TGA2599 is offered in a small 4 x 4 mm plastic overmold QFN, fully matched to 50 ohms and includes integrated DC blocking caps on both RF ports allowing for simple system integration.

Lead-Free & RoHS compliant.

Evaluation Boards are available on request.

Pad Configuration

Pad Number	Symbol
3	RF Input
6	V_{G1}
8	V_{G2}
13	RF Output
17	V_{D2}
19	V_{D1}
1-2,4-5,7,9-12,14-16,18, 20, 21	GND

Ordering Information

Part	ECCN	Description
TGA2599-SM	EAR99	5.0-8.0 GHz GaN Driver Amplifier

Absolute Maximum Ratings

Parameter	Value
Drain Voltage (V_D)	40 V
Gate Voltage Limits (V_G)	-8 V, 0 V
Drain Current (I_{D1}, I_{D2})	128, 260 mA
Gate Current (I_{G1}, I_{G2} @T_{CH}=200 ℃)	1.4, 2.8 mA
Power Dissipation, 85 ℃ (Pdiss)	5.5 W
Input Power, CW, 50 Ω [1]	30 dBm
Input Power, CW, VSWR 10:1 [1]	25 dBm
Channel Temperature (T_{CH})	200 ℃

Notes:

1. V_D = 25V, I_{DQ} = 50mA, T_B = 85 ℃

Recommended Operating Conditions

Parameter	Value
Drain Voltage (V_D)	25 V
Gate Voltage (V_G)	-2.75 V
Quiescent Drain Current (I_{DQ})	50 mA
Operating Drain Current (I_{D_DRIVE})	250 mA

Electrical Specifications

Test conditions, unless otherwise noted: T = 25 ℃, CW input power, part mounted to EVB (page 11)

Parameter	Min	Typical	Max	Units
Operating Frequency Range	5.0		8.0	GHz
Output Power (@ Pin = 18 dBm)		> 33		dBm
Power Added Efficiency (@ Pin = 18 dBm)		> 34		%
Small Signal Gain		> 23		dB
Input Return Loss		> 17		dB
Output Return Loss		> 4		dB

Specifications

Thermal and Reliability Information

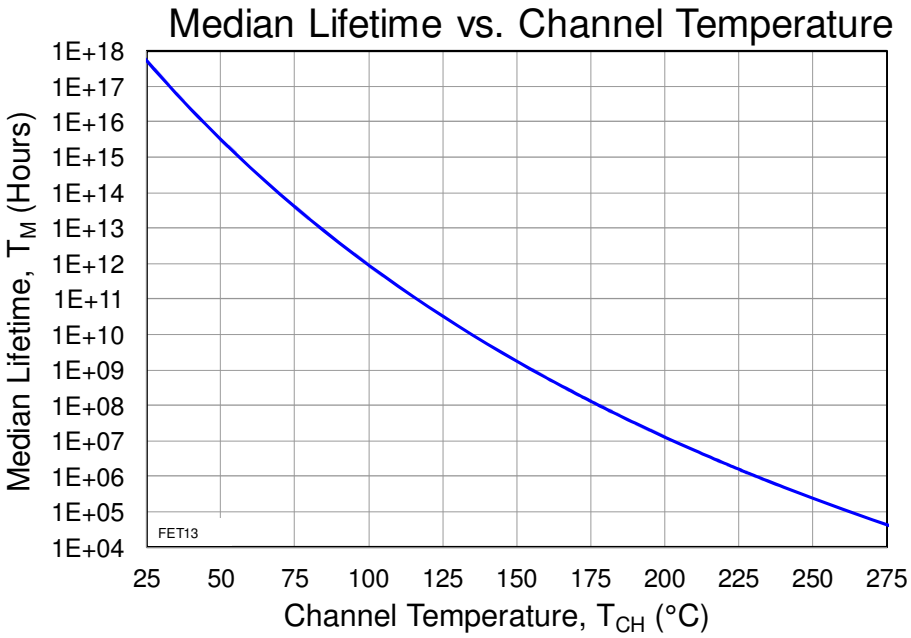
Parameter	Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{PKG} = 85°C, V_D = 25 V, I_{D_DRIVE} = 250 mA, Freq. = 8.0 GHz, P_{IN} = 18 dBm, P_{OUT} = 33 dBm, P_{DISS} = 4.2 W	24.5	ºC/W
Channel Temperature (T_{CH}) (1)		188	°C
Median Lifetime (T_M)		3.45E07	Hrs

Note:

1. Die mounted to 8 mil CDA194 frame base using 2815A epoxy, package backside temperature fixed at 85 °C.

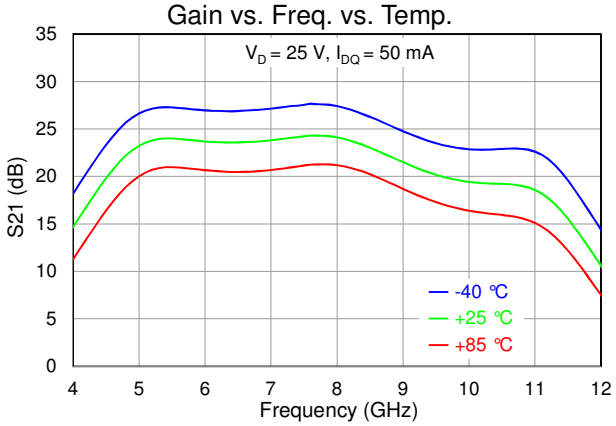
Median Lifetime

Test Conditions: 40 V; Failure Criterion = 10% reduction in $I_{D\ MAX}$

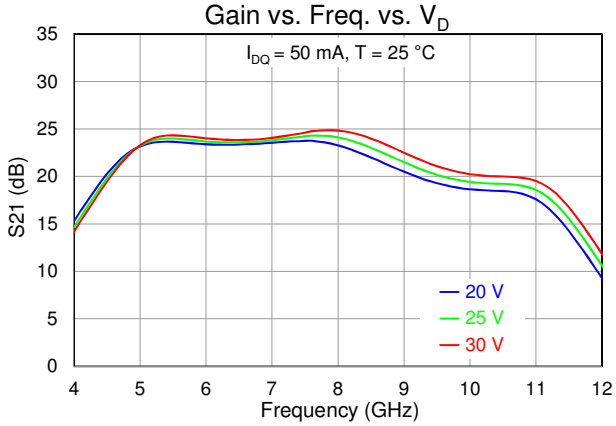


Typical Performance

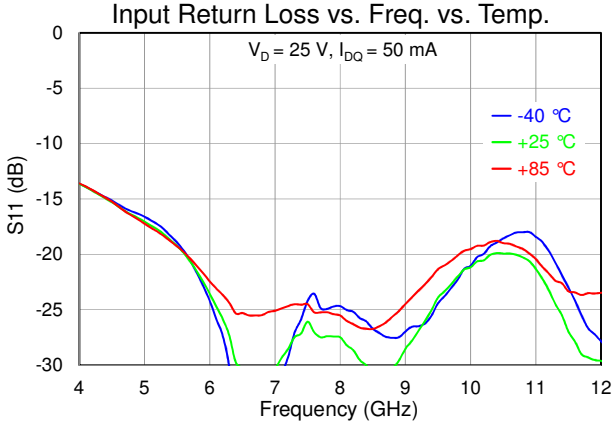
Gain vs. Freq. vs. Temp.



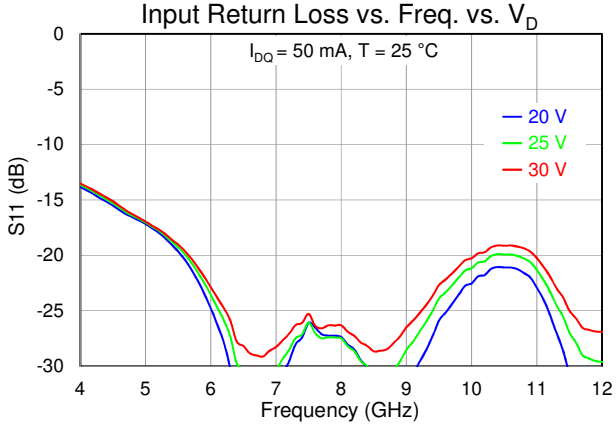
Gain vs. Freq. vs. V_D



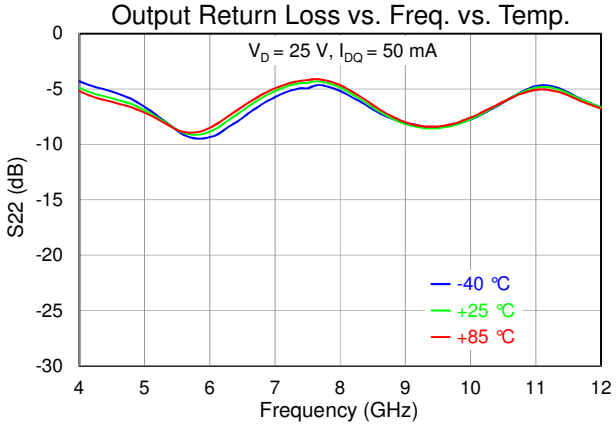
Input Return Loss vs. Freq. vs. Temp.



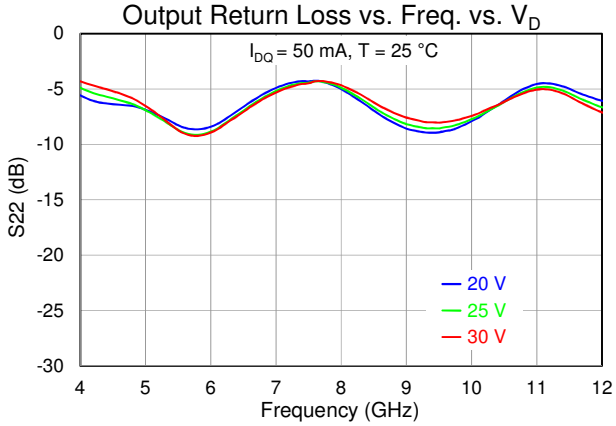
Input Return Loss vs. Freq. vs. V_D



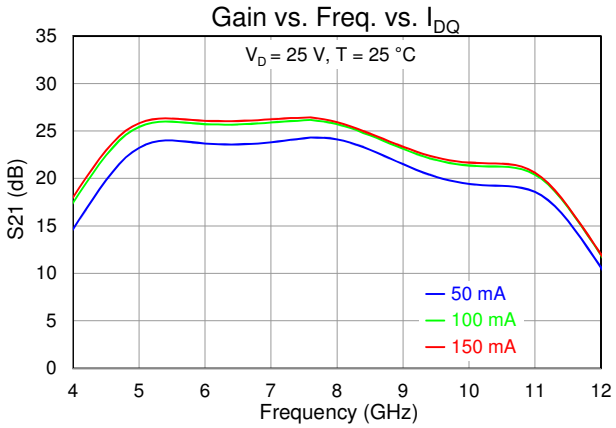
Output Return Loss vs. Freq. vs. Temp.

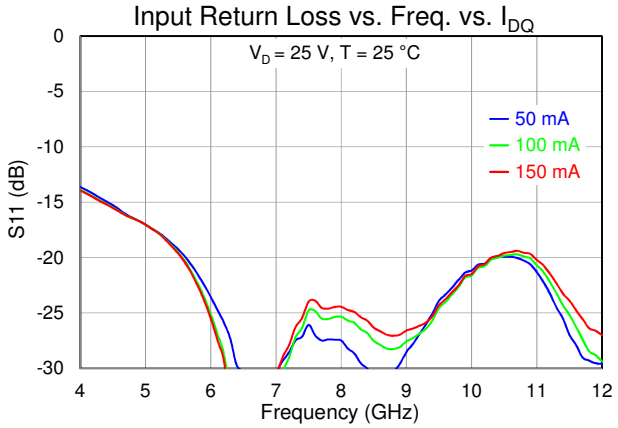


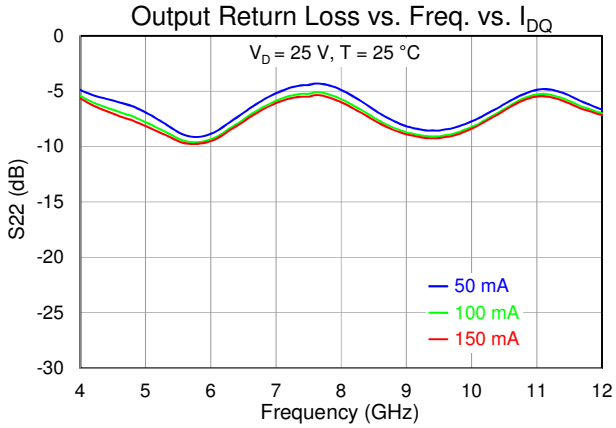
Output Return Loss vs. Freq. vs. V_D



Typical Performance

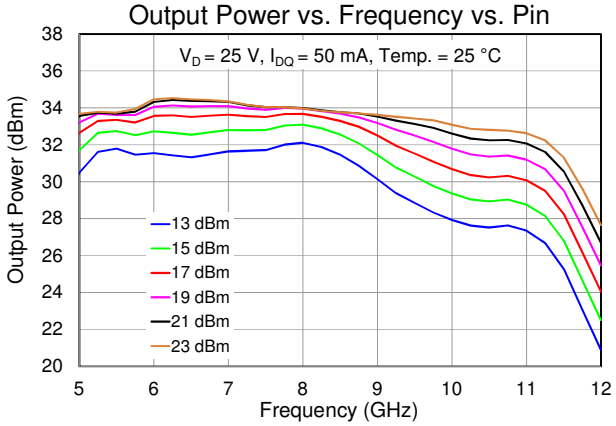




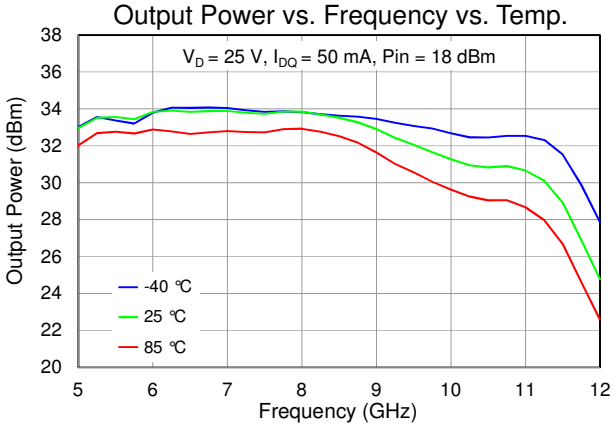


Typical Performance

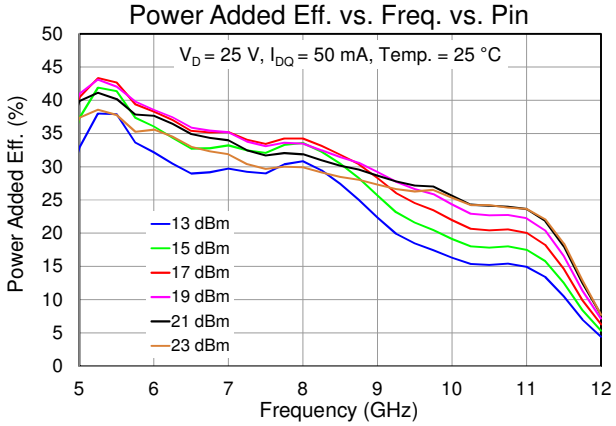
Output Power vs. Frequency vs. Pin



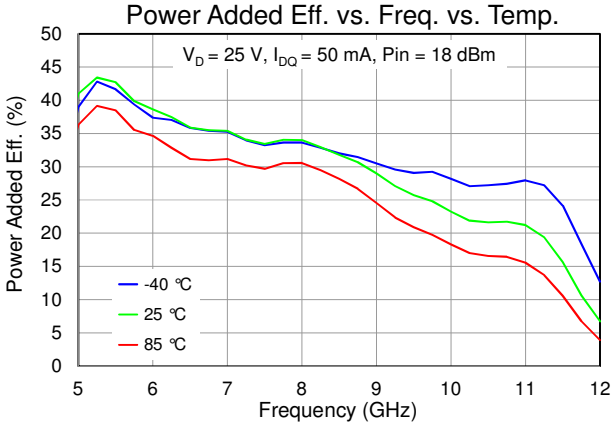
Output Power vs. Frequency vs. Temp.



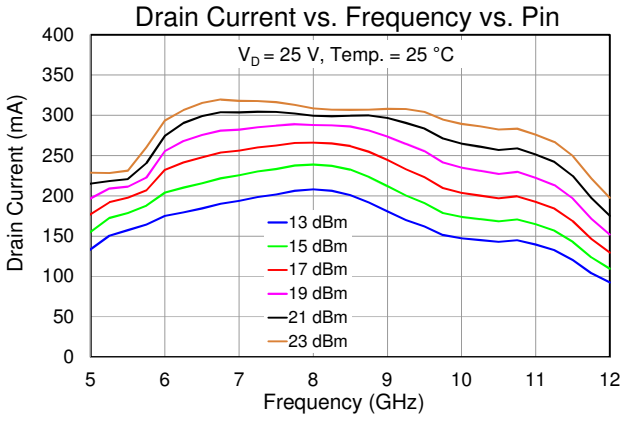
Power Added Eff. vs. Freq. vs. Pin



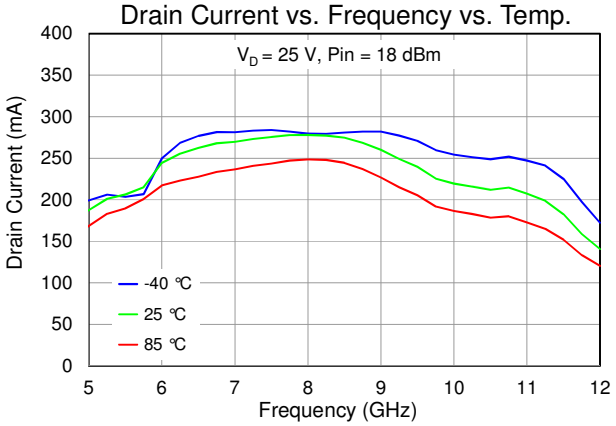
Power Added Eff. vs. Freq. vs. Temp.



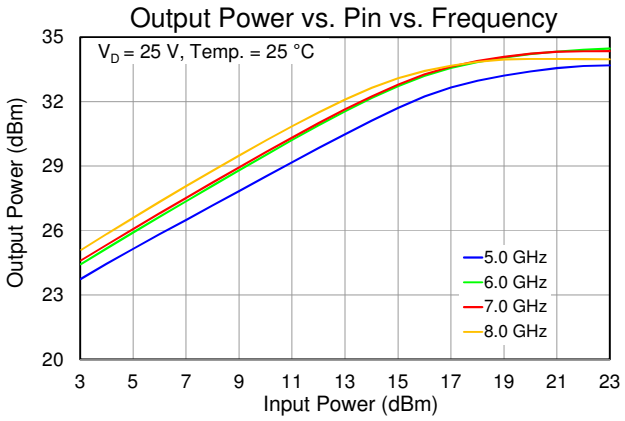
Drain Current vs. Frequency vs. Pin

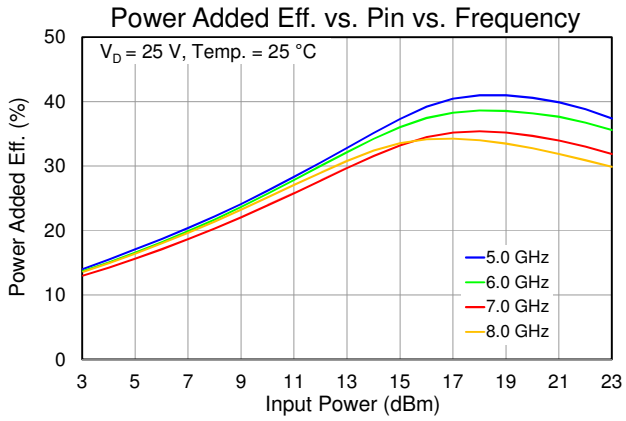


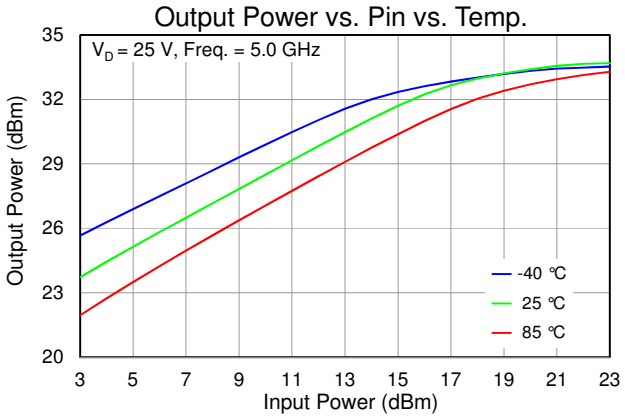
Drain Current vs. Frequency vs. Temp.

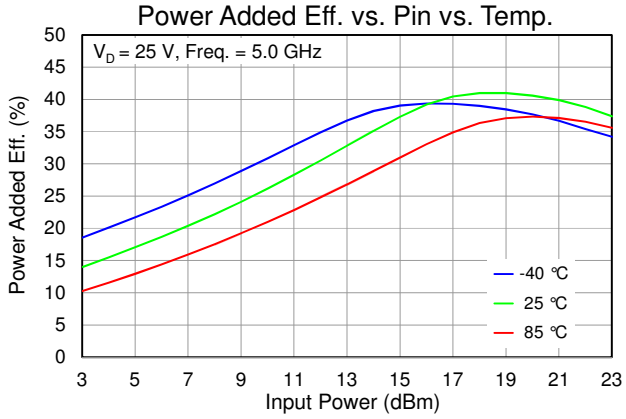


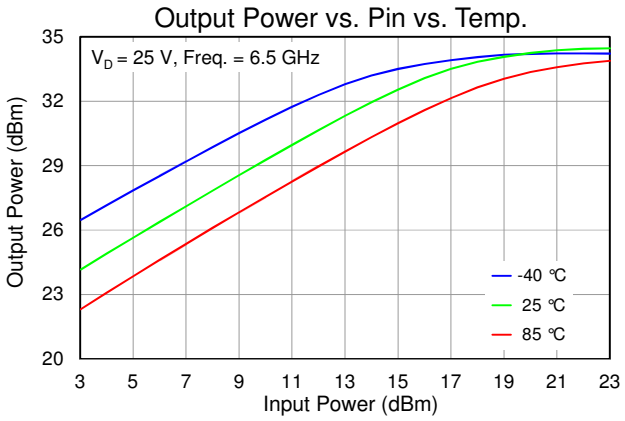
Typical Performance

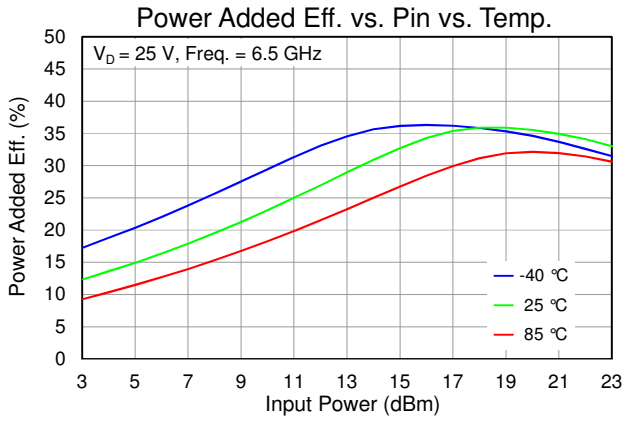






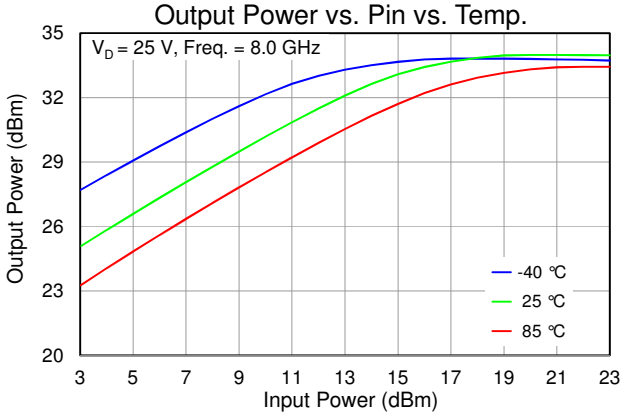




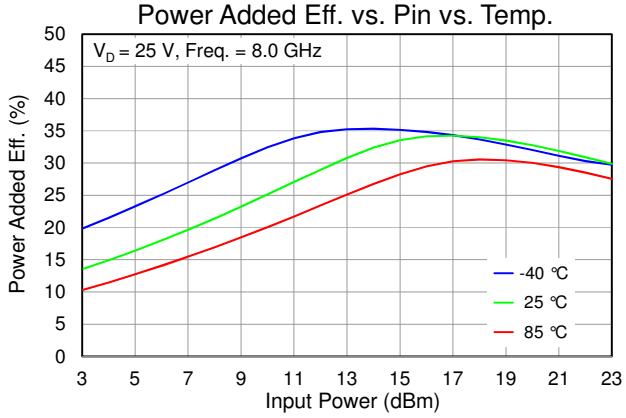


Typical Performance

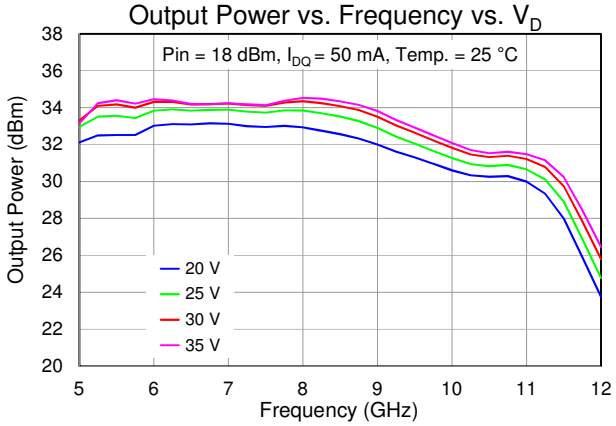
Output Power vs. Pin vs. Temp.



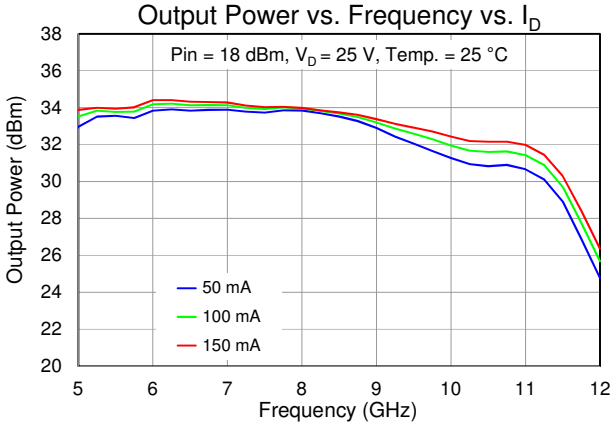
Power Added Eff. vs. Pin vs. Temp.



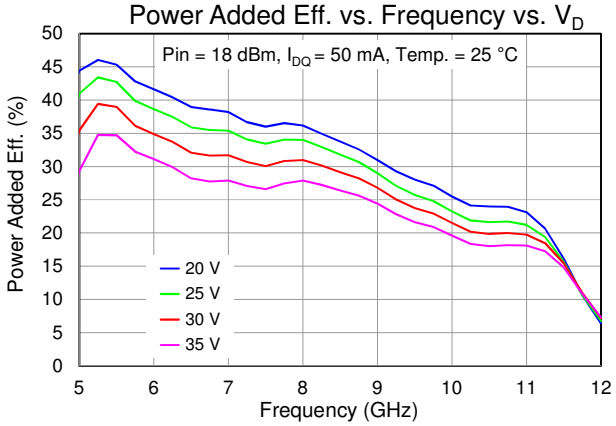
Output Power vs. Frequency vs. V_D



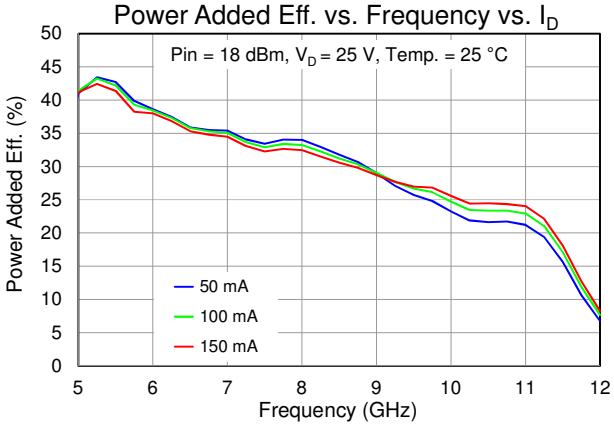
Output Power vs. Frequency vs. I_D



Power Added Eff. vs. Frequency vs. V_D



Power Added Eff. vs. Frequency vs. I_D



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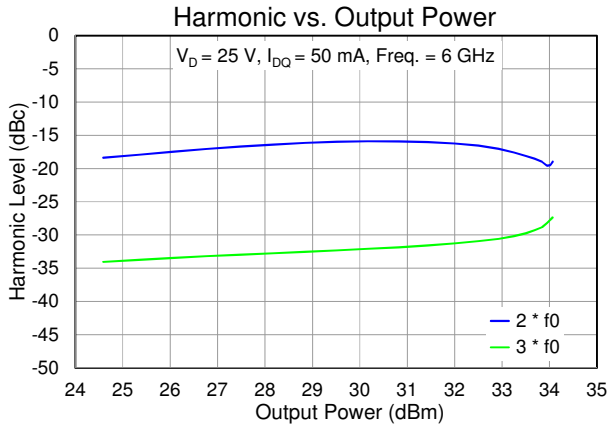
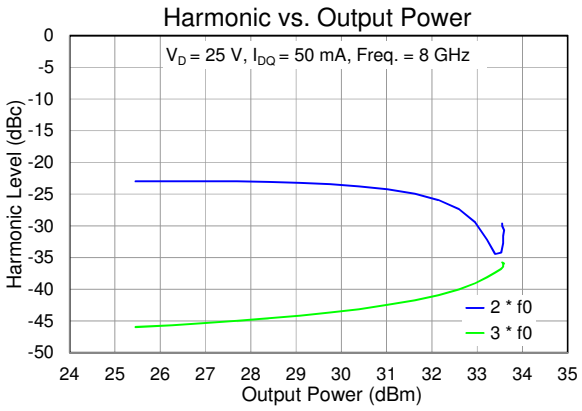
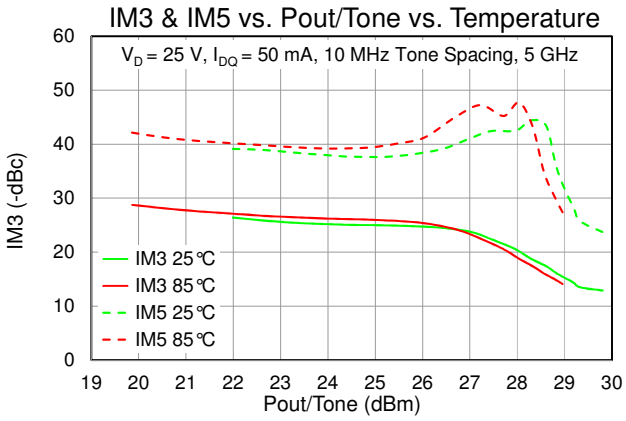
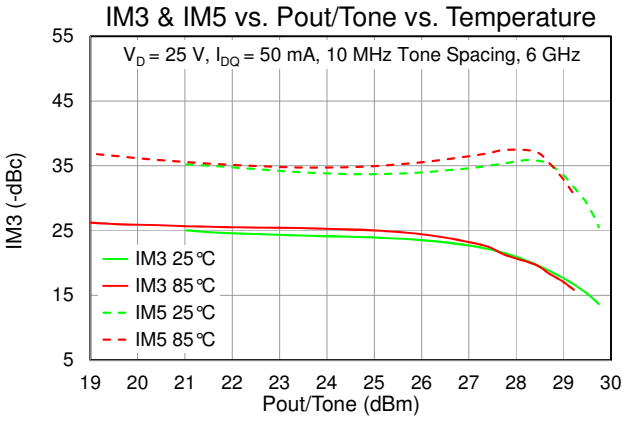
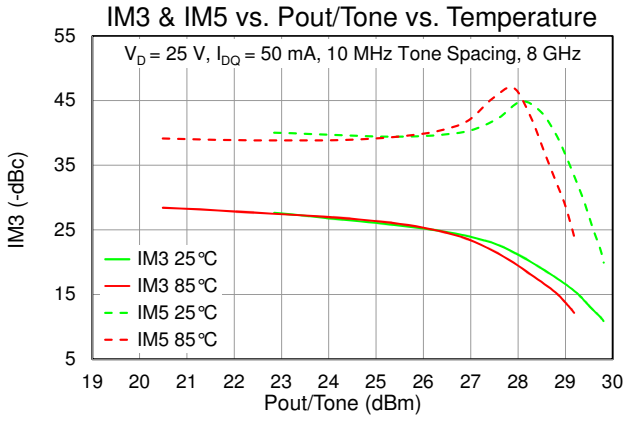


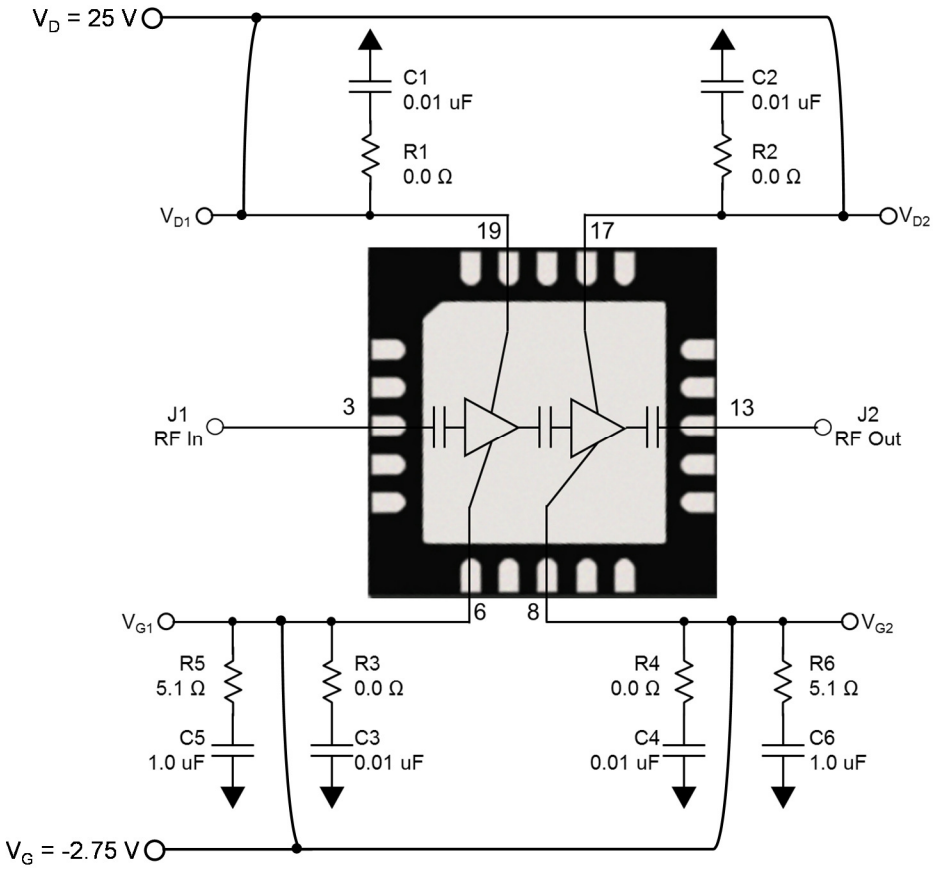








Application Circuit



Note: V_{D1}/V_{D2} and V_{G1}/V_{G2} can be tied together in application

Bias-up Procedure
1. Set I_D limit to 400 mA, I_G limit to 4.5 mA
2. Set V_{G1}/V_{G2} to -5.0V
3. Set V_{D1}/V_{D2} +25V
4. Adjust V_{G1}/V_{G2} more positive until I_{DQ} = 50 mA
5. Apply RF signal

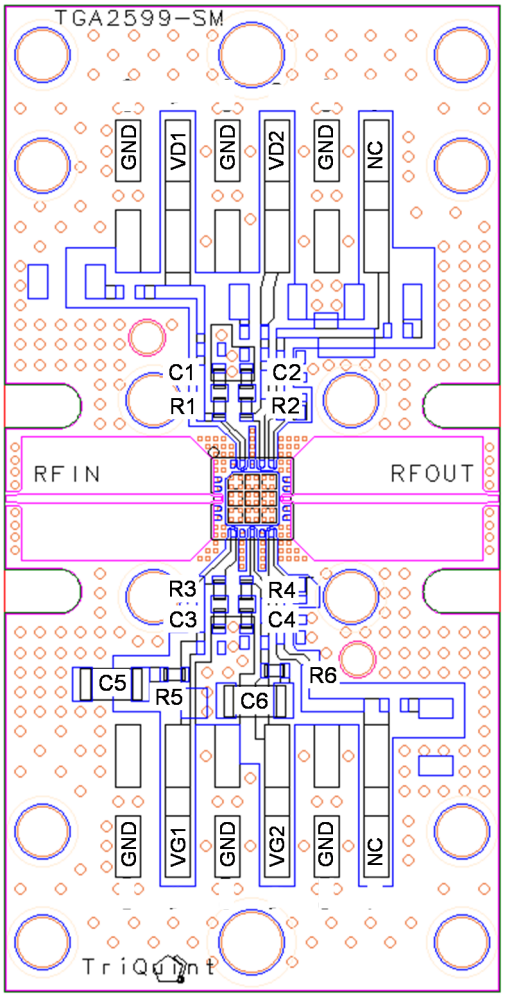
Bias-down Procedure
1. Turn off RF signal
2. Set V_{G1}/V_{G2} to -5.0V. Ensure I_{DQ} ~ 0mA
3. Set V_{D1}/V_{D2} to 0V
4. Turn off V_{D1}/V_{D2} supply
5. Turn off V_{G1}/V_{G2} supply

Applications Information

Evaluation Board Layout

RF Layer is 0.008" thick Rogers Corp. RO4003C, εr = 3.38. Metal layers are 0.5 oz. copper. The microstrip line at the connector interface is optimized for the Southwest Microwave end launch connector 1092-02A-5.

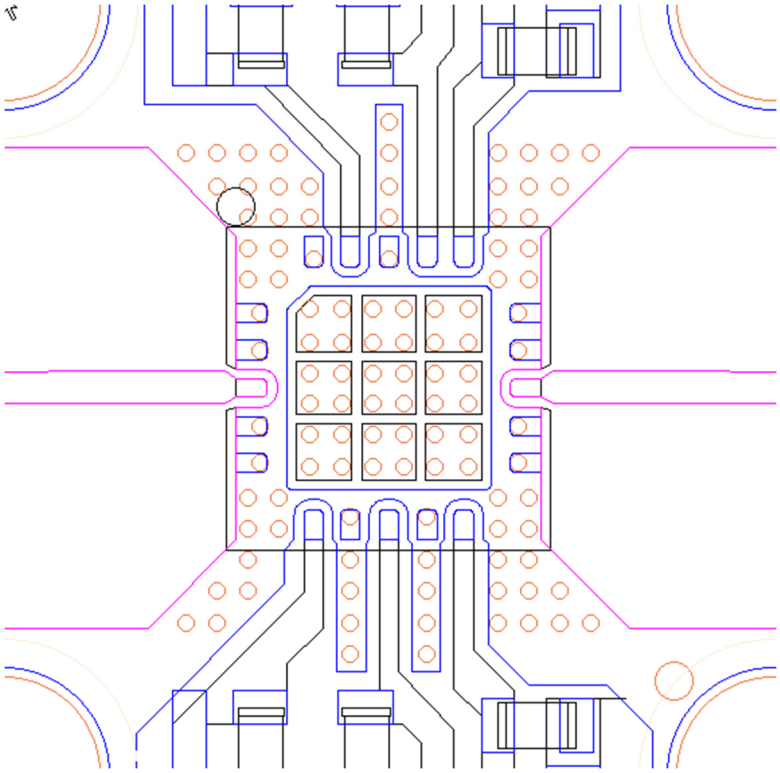
The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.



Bill of Materials

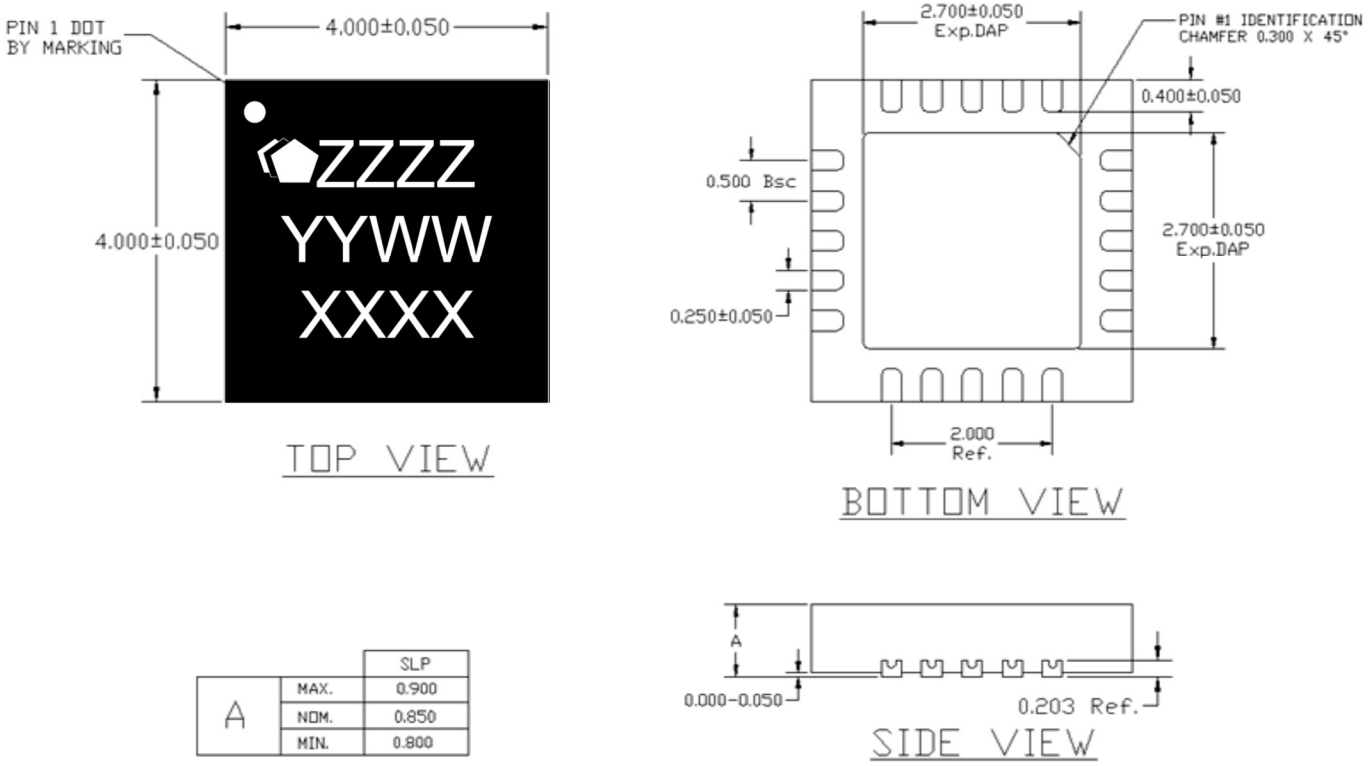
Ref. Designation	Value	Description	Manufacturer	Part Number
C1 – C4	0.01 uF	Cap., 50V, 10% X7R, 0402 case	Various	
C5 – C6	1.0 uF	Cap., 50V, 10% X5R, 1206 case	Various	
R1 – R4	0.0 Ohms	Resistor, 0402 case	Various	
R5 – R6	5.1 Ohms	Resistor, 0402 case	Various	

Mounting Detail



Note:
Multiple vias should be employed under package center paddle to minimize inductance and thermal resistance.

Mechanical Information

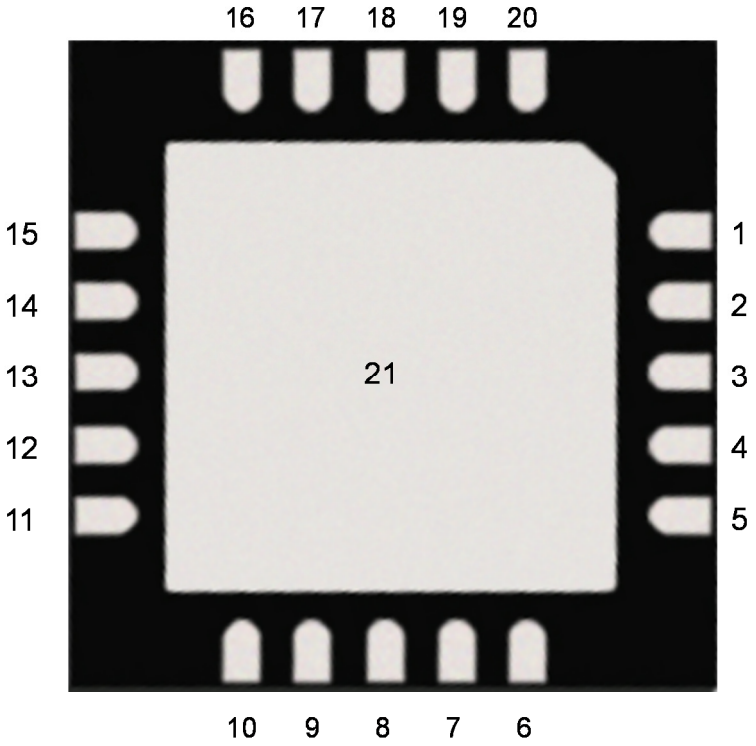


The TGA2599-SM will be marked with the "ZZZZ" and "YYWW" designators and a lot code marked below the part designator. Here, the "ZZZZ" will be "2599". The "YY" represents the last two digits of the year the part was manufactured, the "WW" is the work week, and the "XXXX" is an auto-generated number.

This package is lead-free/RoHS-compliant. This package is compatible with both lead free and tin-lead soldering processes.

Dimensions are in millimeters.

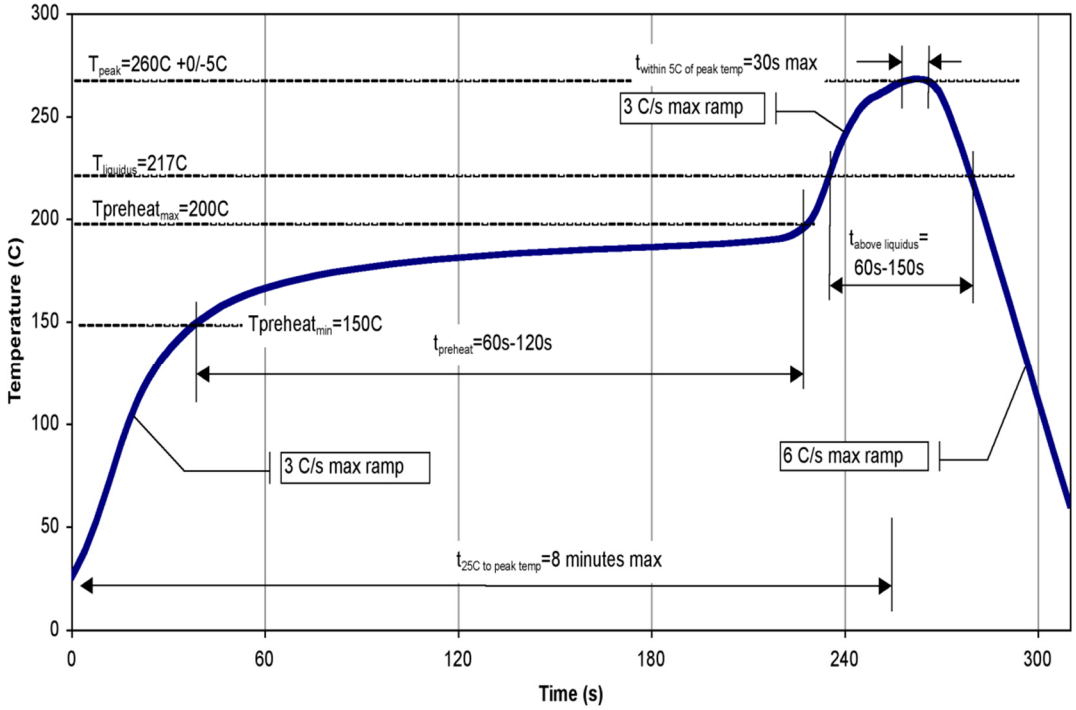
Pad Description



Bottom view of package base

Pin Number	Label	Description
3	RF Input	RF input, matched to 50 Ω, DC blocked
6	V_{G1}	First stage gate voltage. Bias network required. V_{G1} and V_{G2} can be tied together in application.
8	V_{G2}	Second stage gate voltage. Bias network required. V_{G1} and V_{G2} can be tied together in application.
13	RF Output	RF output, matched to 50 Ω, DC blocked
17	V_{D2}	Second stage drain voltage. Bias network required. V_{D1} and V_{D2} can be tied together in application.
19	V_{D1}	First stage drain voltage. Bias network required. V_{D1} and V_{D2} can be tied together in application.
1-2,4-5,7,9-12,14-16,18, 20	GND	Connected to ground paddle (21); must be grounded to PCB to improve isolation.
21	GND	Backside paddle. Multiple vias should be employed to minimize inductance and thermal resistance.

Recommended Soldering Temperature Profile



Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating:	TBD
Value:	TBD
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

ECCN

US Department of Commerce: EAR99

Solderability

Compatible with the latest version of J-STD-020 Lead free solder, 260 °C.

MSL Rating

TBD at 260 °C convection reflow
The part is rated Moisture Sensitivity Level TBD
JEDEC standard IPC/JEDEC J-STD-020.

RoHS-Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free