TGA2752-SM

7.1 – 8.5 GHz Power Amplifier

Product Overview

The Qorvo TGA2752-SM is a C-Band Power Amplifier with integrated power detector. The TGA2752-SM operates from 7.1 – 8.5 GHz and is designed using Qorvo's power GaAs pHEMT and GaN HEMT production processes.

The TGA2752-SM typically provides 40 dBm of saturated output power with small signal gain of 28 dB. Third Order Intercept is 48 dBm at 30 dBm SCL.

The TG2752-SM is available in a low-cost, surface mount 42 lead 7x9 QFN package and is ideally suited for Point-to-Point Radio.

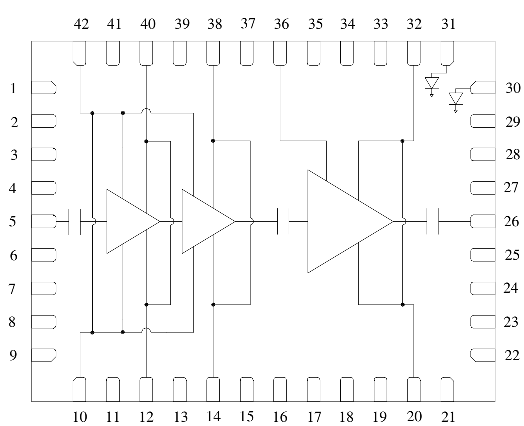
Lead-free and RoHS compliant

42-Lead 7.0 x 9.0 x 0.9 mm Package

Key Features

- Frequency Range: 7.1 – 8.5 GHz
- Power: +40 dBm Psat
- Gain: 28 dB
- TOI: 48 dBm at 30 dBm/tone
- Integrated Power Detector
- Bias: V_{D1} = V_{D2} = +6 V, I_{D1} + I_{D2} = 1000 mA, V_{D3} = +28V, I_{D3} = 190mA
- Package Dimensions: 7.0 x 9.0 x 0.9 mm

Functional Block Diagram



Top View

Applications

- Point-to-Point Radio
- Linear C-band Sat-Com

Ordering Information

Part No.	ECCN	Description
TGA2752-SM T/R	3A001.b.2.b.2	500 pieces on a 7" reel (standard)
TGA2752-SM Eval Board	EAR99	Evaluation Board
TGA2752-SM, Sample	3A001.b.2.b.2	Waffle Tray with 4 pcs

Absolute Maximum Ratings

Parameter	Rating
Drain Voltage, V_{D1}, V_{D2}	+9 V
Drain Voltage, V_{D3}	+32 V
Drain Current, I_{D1} + I_{D2}	2443 mA
Drain Current, I_{D3}	825 mA
Gate Voltage, V_{G12}	–1.2V / +0.5V
Gate Voltage, V_{G3}	–8V / 0V
Power Dissipation, Driver Stages, P_{DISS}	7.2 W
Power Dissipation, Final Stage, P_{DISS}	17 W
RF Input Power, CW, 50 Ω, T = 25 °C	+29 dBm
GaAs Channel Temperature, T_{CH}	200 °C
GaN Channel Temperature, T_{CH}	275 °C
Mounting Temperature (30 Seconds)	260 °C
Storage Temperature	–40 to 150 °C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Operating Temp. Range	–40	+25	+85	°C
V_{D1}, V_{D2}		+6		V
V_{D3}		+28		V
I_{D1} + I_{D2}		1000		mA
I_{D3}		190		mA
V_{G12}		–0.65		V
V_{G3}		–2.6		V
I_{D1} + I_{D2} drive (at +34 dBm Pout)		1050		mA
I_{D3} drive (at +34 dBm Pout)		400		mA

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions (1)	Min	Typ	Max	Units
RF Frequency Range		7.1		8.5	GHz
Small Signal Gain		24	28		dB
Input Return Loss, IRL			12		dB
Output Return Loss, ORL			15		dB
Output Power at Saturation, Psat		+38	+40		dBm
Output Power at 1dB Gain Compression, P1dB			+30		dBm
Output Third Order Intercept, TOI @ 30 dBm/Tone			+48		dBm
Gain Temperature Coefficient			–0.035		dB / °C
Power Temperature Coefficient			–0.012		dBm / °C

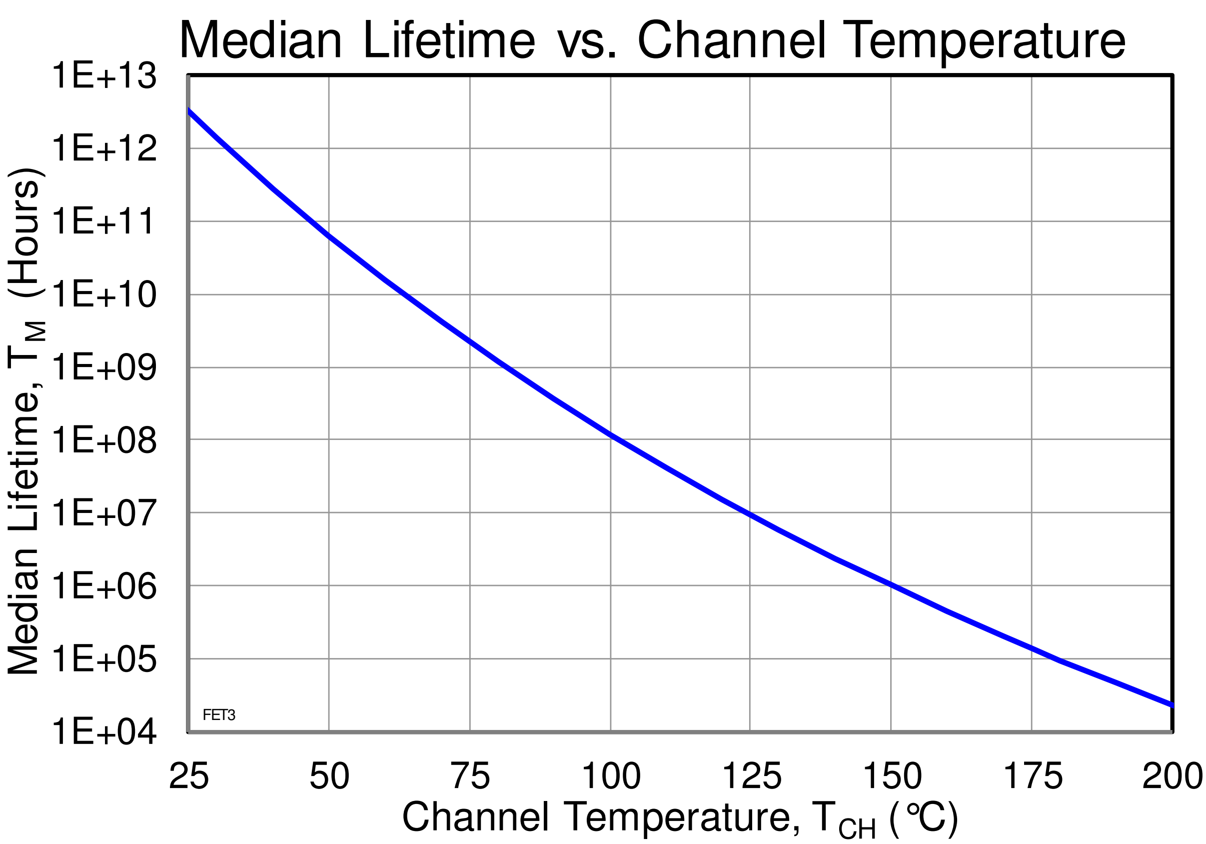
Notes:
1. Test conditions unless otherwise noted: V_{D1} = V_{D2} = +6 V, I_{D1} + I_{D2} = 1000 mA, V_{G1} = V_{G2} = −0.7 V, V_{D3} = +28 V, I_{D3} = 190 mA, V_{G3} = −2.6 V, Temp = +25 °C, Z_0 = 50 Ω

Thermal and Reliability Information (Driver Stages)

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	CW $T_{baseplate}$ = +85 °C, $V_{D\ Driver}$ = +6 V, I_{DQ} = 1000 mA, P_{DISS} = 6.0 W	9	ºC/W
Channel Temperature, T_{CH}		139	°C
Median Lifetime (T_M)		2.6 x 10^6	Hrs
Thermal Resistance (θ_{JC}) (1)	CW $T_{baseplate}$ = +85 °C, $V_{D\ Driver}$ = +6 V, $I_{D\ Driver}$ = 1050 mA, P_{OUT} = +34 dBm, P_{DISS} = 6.3 W	9.05	ºC/W
Channel Temperature, T_{CH} (Under RF)		142	°C
Median Lifetime (T_M)		2.0 x 10^6	Hrs

Notes:
1. Thermal resistance measured at back of package.

Median Lifetime

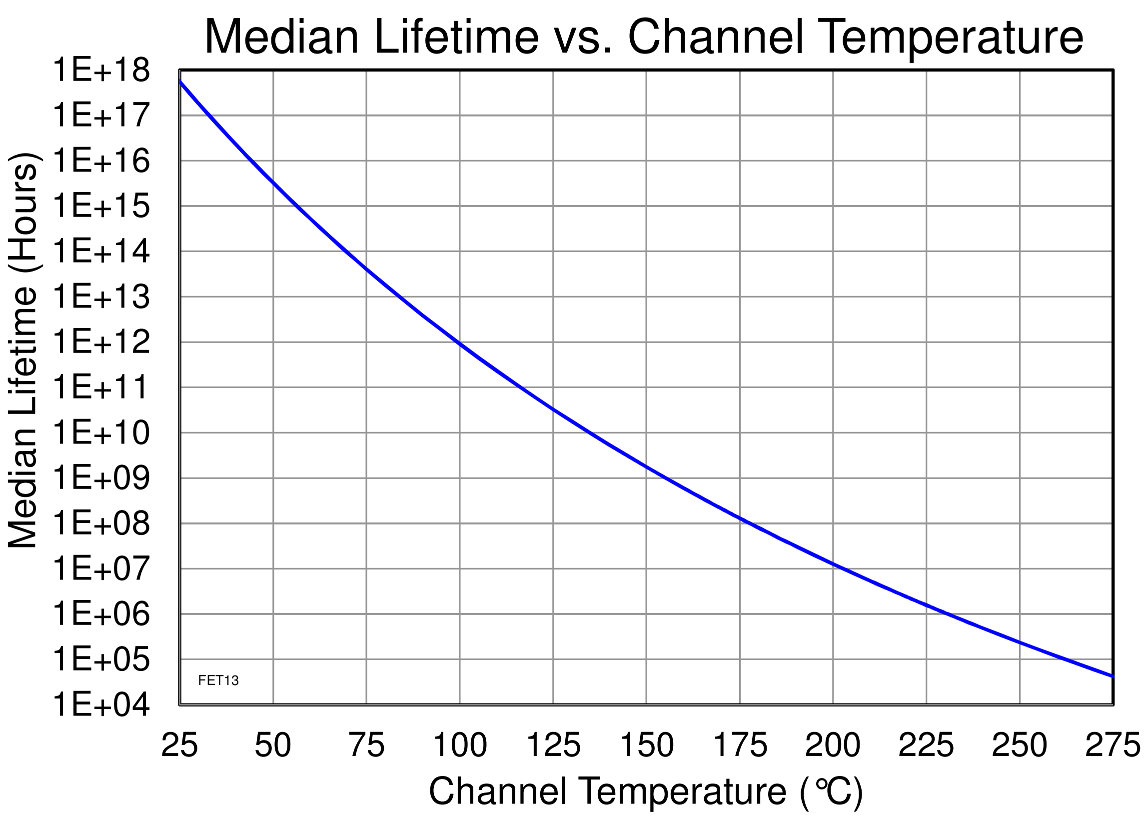


Thermal and Reliability Information (Final Stage)

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	CW $T_{baseplate}$ = +85 °C, $V_{D\ Driver}$ = +28 V, I_{DQ} = 190 mA, P_{DISS} = 5.3 W	8.3	ºC/W
Channel Temperature, T_{CH}		129	°C
Median Lifetime (T_M)		2.01 x 10^{10}	Hrs
Thermal Resistance (θ_{JC}) (1)	CW $T_{baseplate}$ = +85 °C, $V_{D\ Driver}$ = +28 V, $I_{D\ Final}$ = 400 mA, P_{OUT} = +34 dBm, P_{DISS} = 8.7 W	8.16	ºC/W
Channel Temperature, T_{CH} (Under RF)		156	°C
Median Lifetime (T_M)		9.14 x 10^8	Hrs

Notes:
1. Thermal resistance measured at back of package.

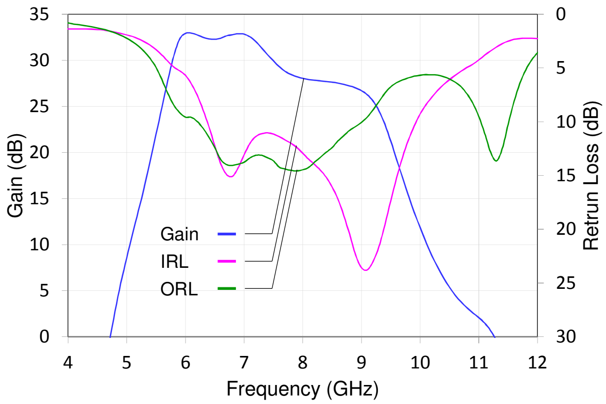
Median Lifetime



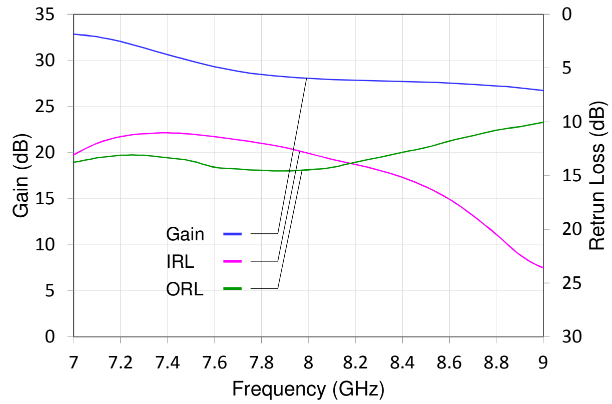
Performance Plots

Test conditions unless otherwise noted: $V_{D1} = V_{D2} = +6$ V, $I_{D1} + I_{D2} = 1000$ mA, $V_{G1} = V_{G2} = -0.65$ V, $V_{D3-} = +28$ V, $I_{D3} = 190$ mA, $V_{G3} = -2.6$ V, Temp = +25 °C, $Z_0 = 50\ \Omega$

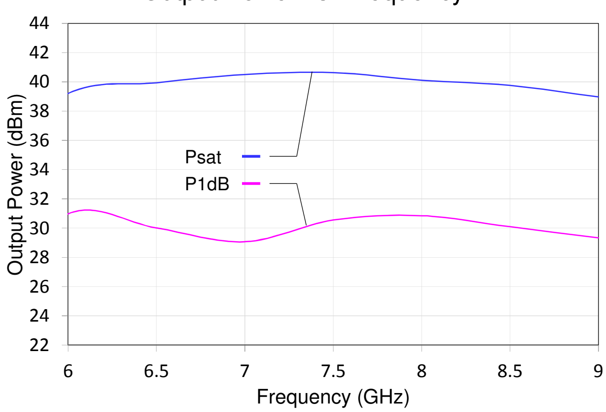
S-Parameters vs. Frequency



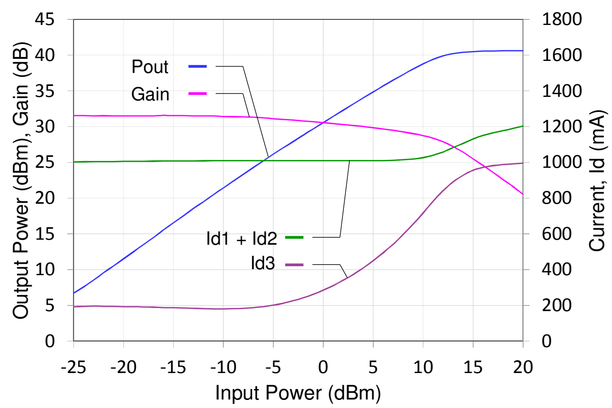
S-Parameters vs. Frequency



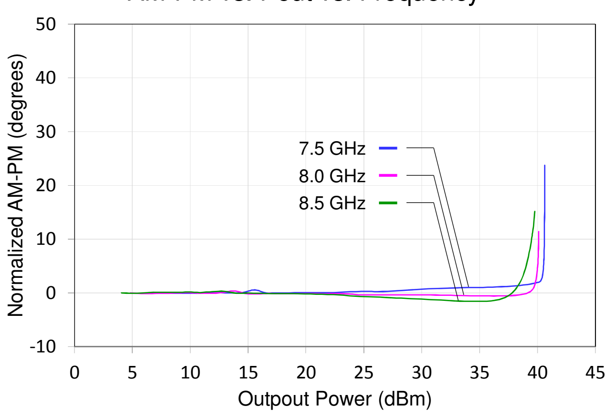
Output Power vs. Frequency



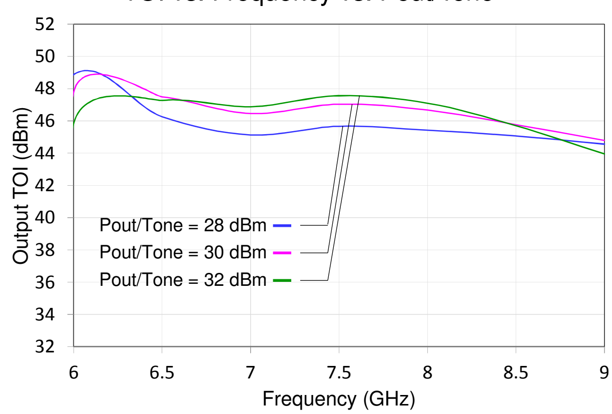
Pout, Gain, Id vs. Pin @ 7.5 GHz



AM-PM vs. Pout vs. Frequency

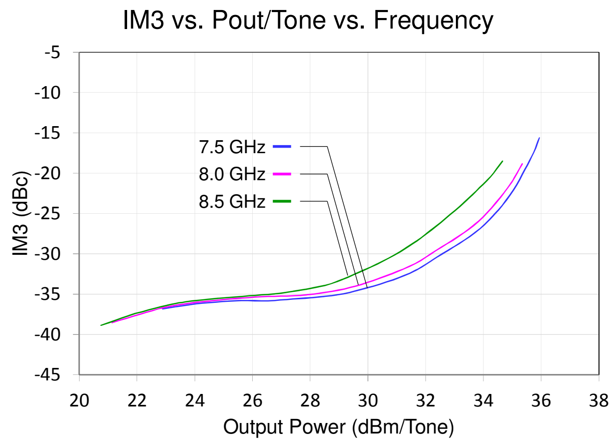


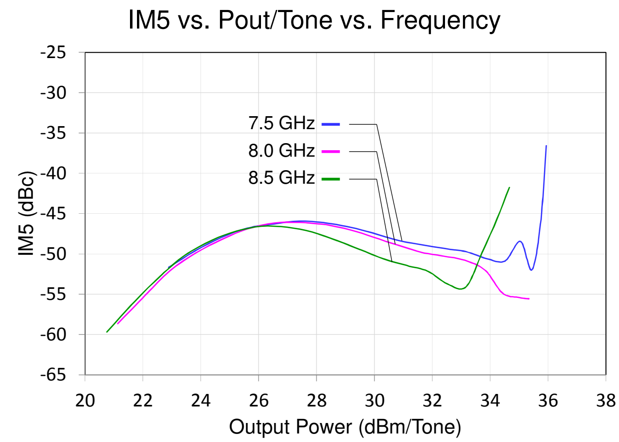
TOI vs. Frequency vs. Pout/Tone

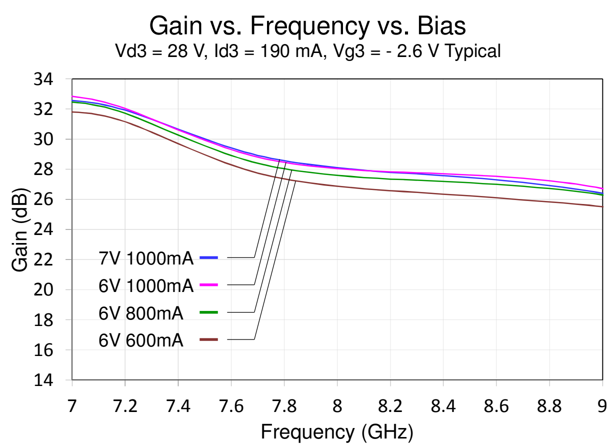


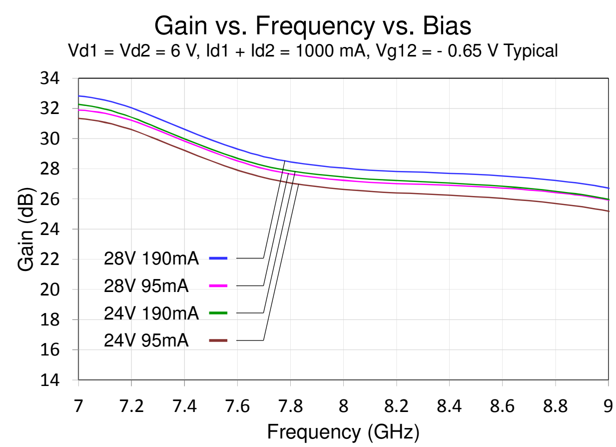
Performance Plots

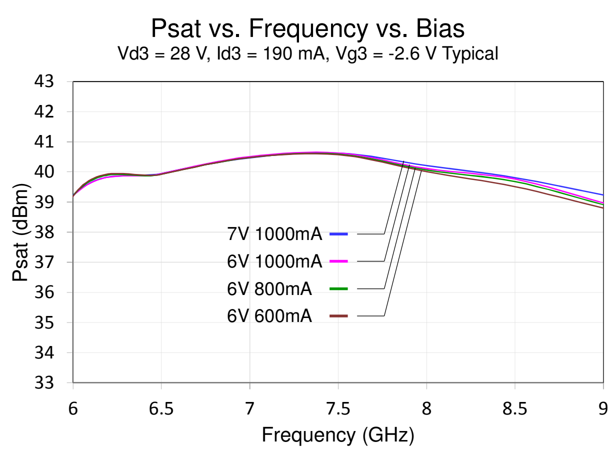
Test conditions unless otherwise noted: $V_{D1} = V_{D2} = +6$ V, $I_{D1} + I_{D2} = 1000$ mA, $V_{G1} = V_{G2} = -0.65$ V, $V_{D3-} = +28$ V, $I_{D3} = 190$ mA, $V_{G3} = -2.6$ V, Temp = +25 °C, $Z_0 = 50\ \Omega$

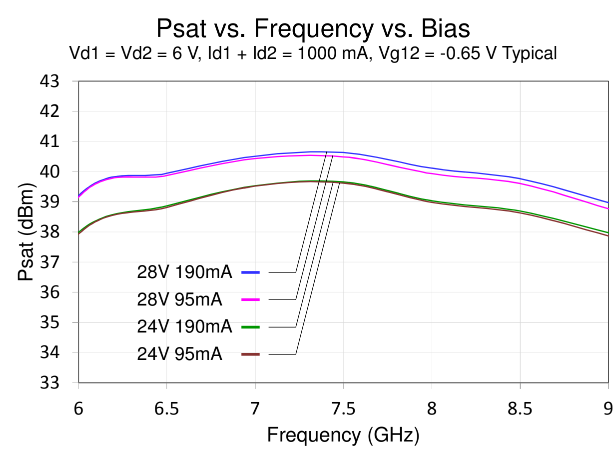






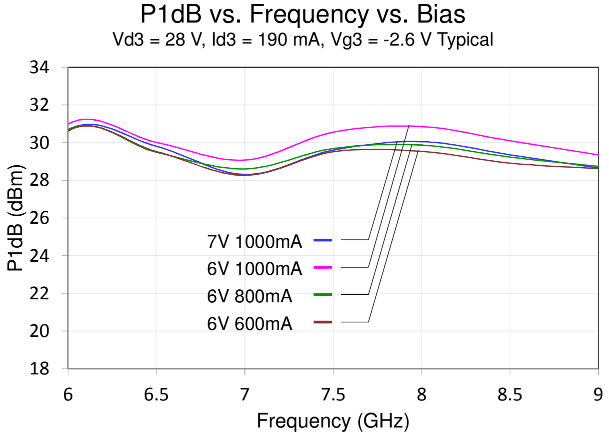


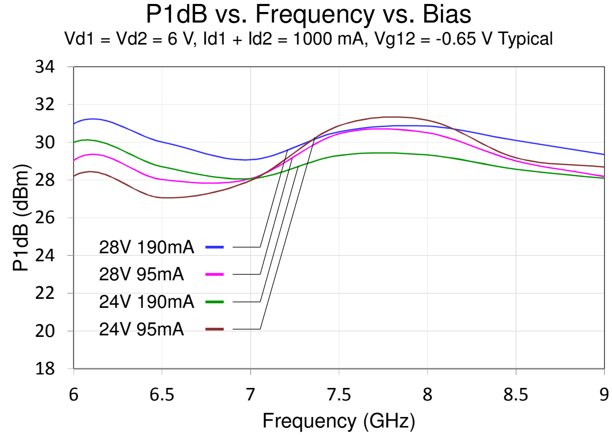


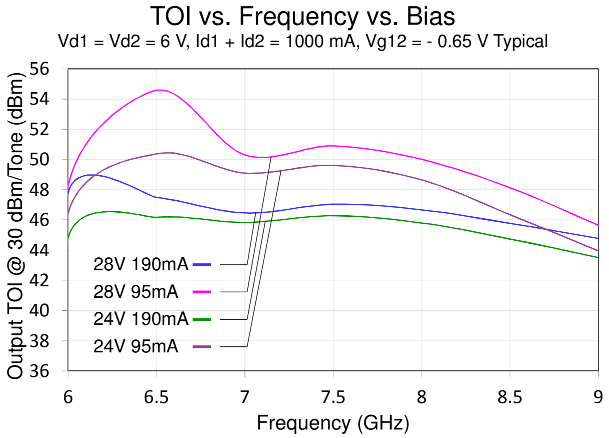


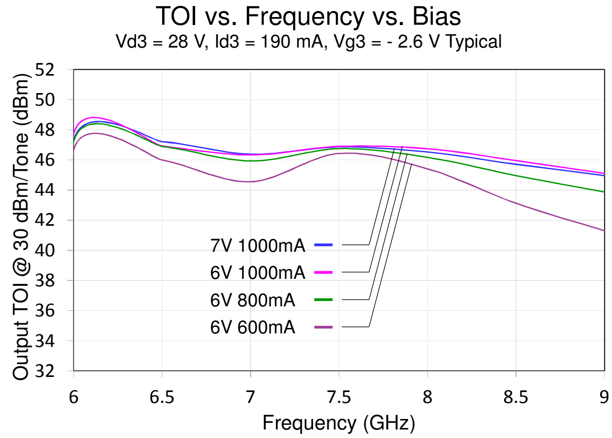
Performance Plots

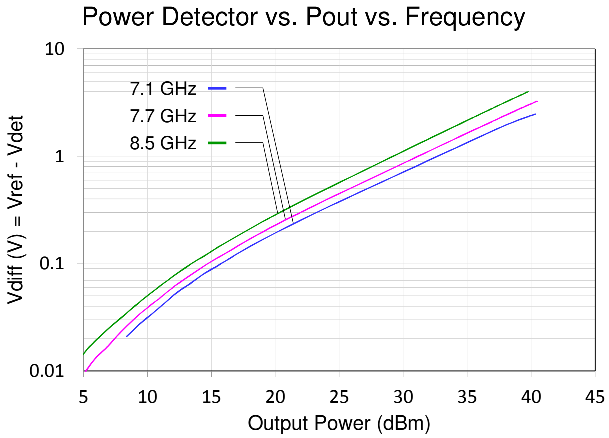
Test conditions unless otherwise noted: $V_{D1} = V_{D2} = +6$ V, $I_{D1} + I_{D2} = 1000$ mA, $V_{G1} = V_{G2} = −0.65$ V, V_{D3} = +28 V, $I_{D3} = 190$ mA, $V_{G3} = −2.6$ V, Temp = +25 °C, $Z_0 = 50\ \Omega$











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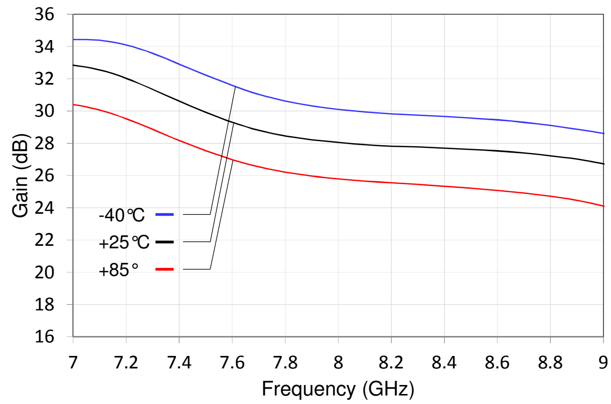
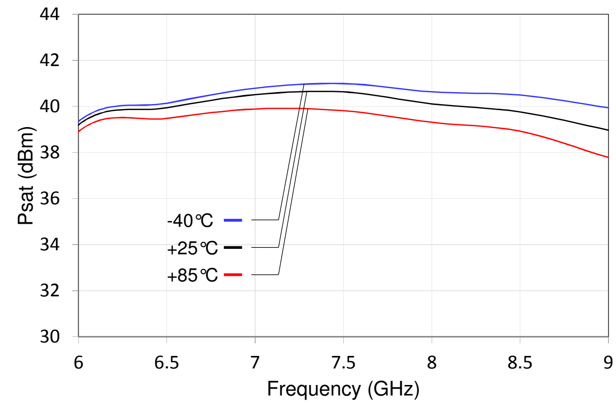
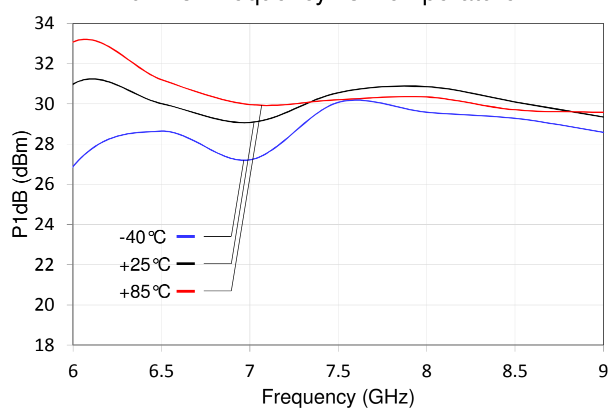
Gain vs. Frequency vs. Temperature



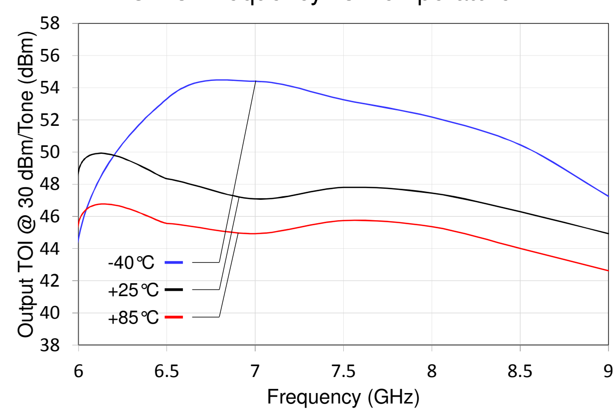
Psat vs. Frequency vs. Temperature



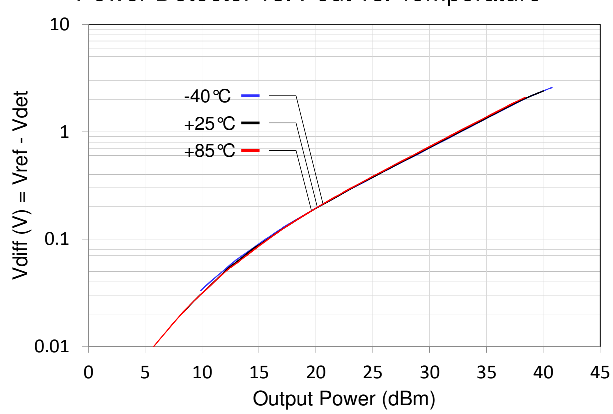
P1dB vs. Frequency vs. Temperature



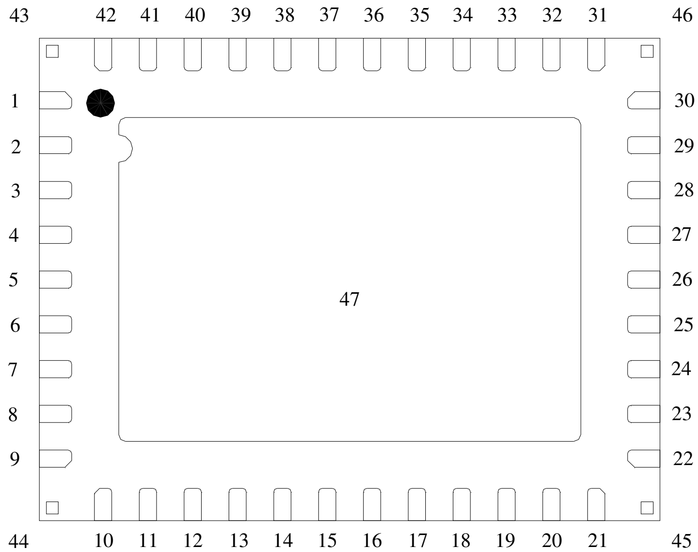
TOI vs. Frequency vs. Temperature



Power Detector vs. Pout vs. Temperature



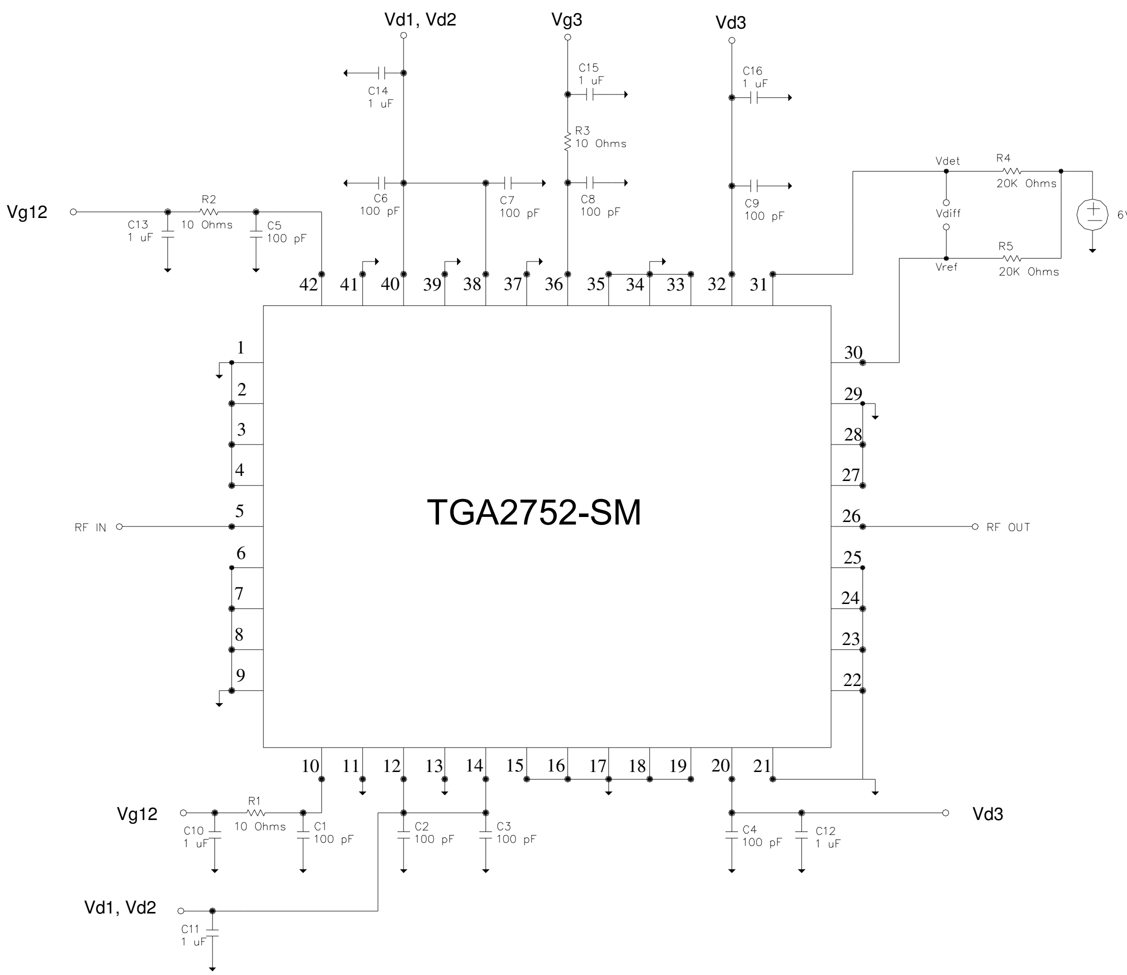
Pin Configuration and Description



Top View

Pad No.	Label	Description
1, 2, 3, 4, 6, 7, 8, 9,11, 13, 15, 16, 17 18, 19, 21, 22, 23, 24, 25, 27, 28, 29, 33, 34, 35, 37, 39, 41	NC	No internal connection; can be grounded on PCB.
5	RF IN	RF Input, matched to 50 Ω, AC Coupled.
10, 42	V_{G12}	Gate voltage. Bias network is required; can be biased from either pin, and non-biased pin can be left open; see Application Circuit on page 11 as an example.
12, 40	V_{D1}	Drain voltage. Bias network is required; see Application Circuit on page 11 as an example.
14, 38	V_{D2}	Drain voltage. Bias network is required; see Application Circuit on page 11 as an example.
20, 32	V_{D3}	Gate voltage. Bias network is required; can be biased from either pin, and non-biased pin can be left opened; see Application Circuit on page 11 as an example.
26	RF OUT	RF Output, matched to 50 ohms, AC Coupled.
30	V_{REF}	Reference diode output voltage.
31	V_{DET}	Detector diode output voltage. Varies with RF output power.
36	V_{G3}	Gate voltage. Bias network is required; see Application Circuit on page 11 as an example.
43, 44, 45, 46, 47	GND	Backside Paddle. Multiple vias should be employed to minimize inductance and thermal resistance; see Mounting Configuration on page 14 for suggested footprint.

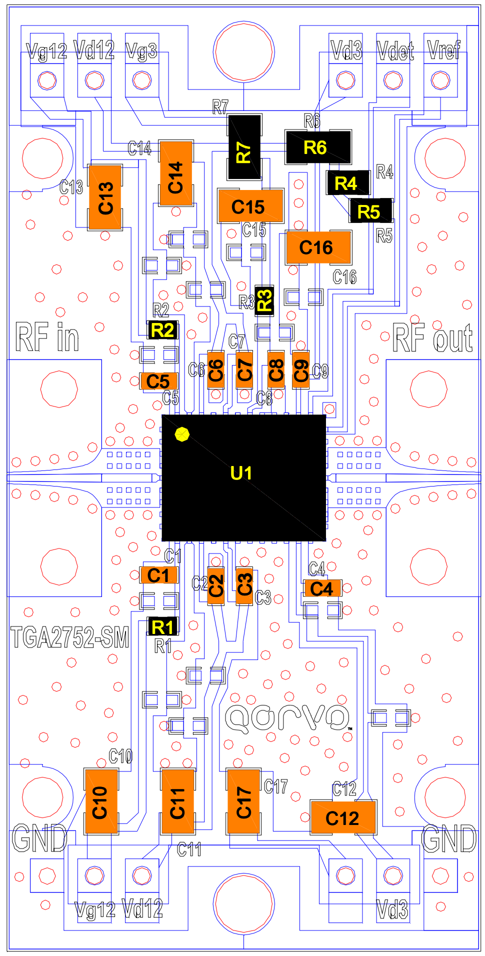
Application Circuit



V_{G12} can be biased from either side, and the non-biased side can be left open.
V_{D1}, V_{D2}, V_{D3}, must be biased from both sides.

Bias-up Procedure	Bias-down Procedure
V_{G12} set to –1.2 V	Turn off RF signal
V_{G3} set to –3.5 V	Reduce V_{G12} to –1.2 V. Ensure I_D ~ 0 mA
V_{D1}, V_{D2} set to +6 V	Reduce V_{G3} to –3.5 V. Ensure I_D ~ 0 mA
V_{D3} sets to +28 V	Turn V_{D1}, V_{D2}, V_{D3} to 0 V
Adjust V_{G12} more positive until quiescent I_D is 1000 mA. This will be ~ $V_G = -0.65$ V typical	Turn V_{G12}, V_{G3} to 0 V
Adjust V_{G3} more positive until quiescent I_D is 190 mA. This will be ~ $V_G = -2.6$ V typical	
Apply RF signal	

Application Evaluation Board



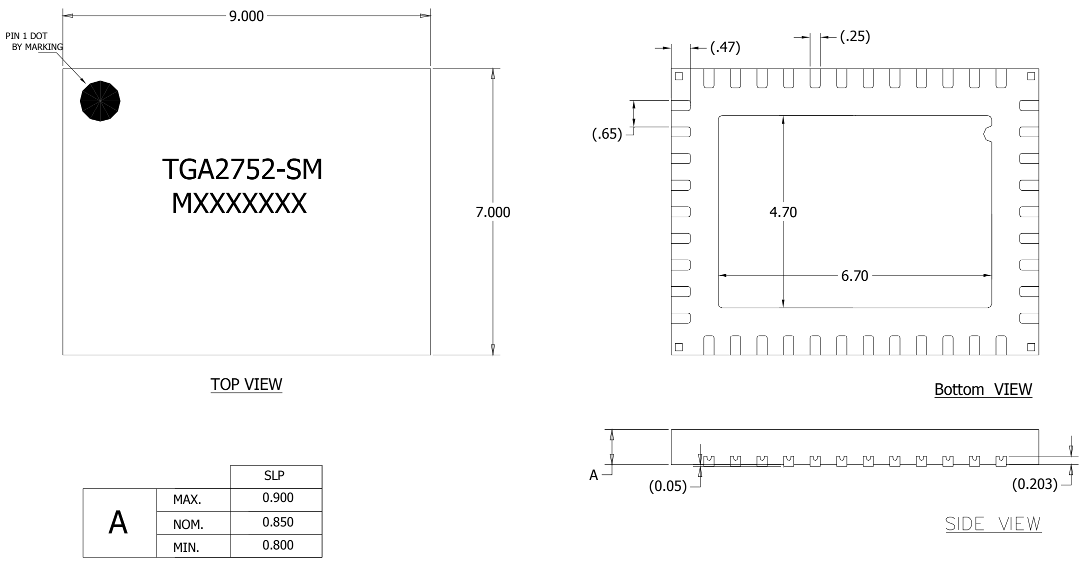
1. Board Material is RO4003 0.008” thickness with ½ oz. copper cladding

Bill of Material

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	Qorvo	
C1 – C9	100 pF	Cap, 0402, +50 V, 5%, COG	various	
C10 – C17	1 µF	Cap, 0603, +50 V, 5%, X5R	various	
R1 – R3	10 Ω	Res, 0402, 1/16W, 5%, SMD	various	
R4, R5	20 KΩ	Res, 0603, 1/16W, 5%, SMD	various	
R6, R7	0 Ω	Res, 0805, 1/16W, 5%, SMD	various	
U1		7.1 – 8.5 GHz Power Amplifier	Qorvo	TGA2752-SM

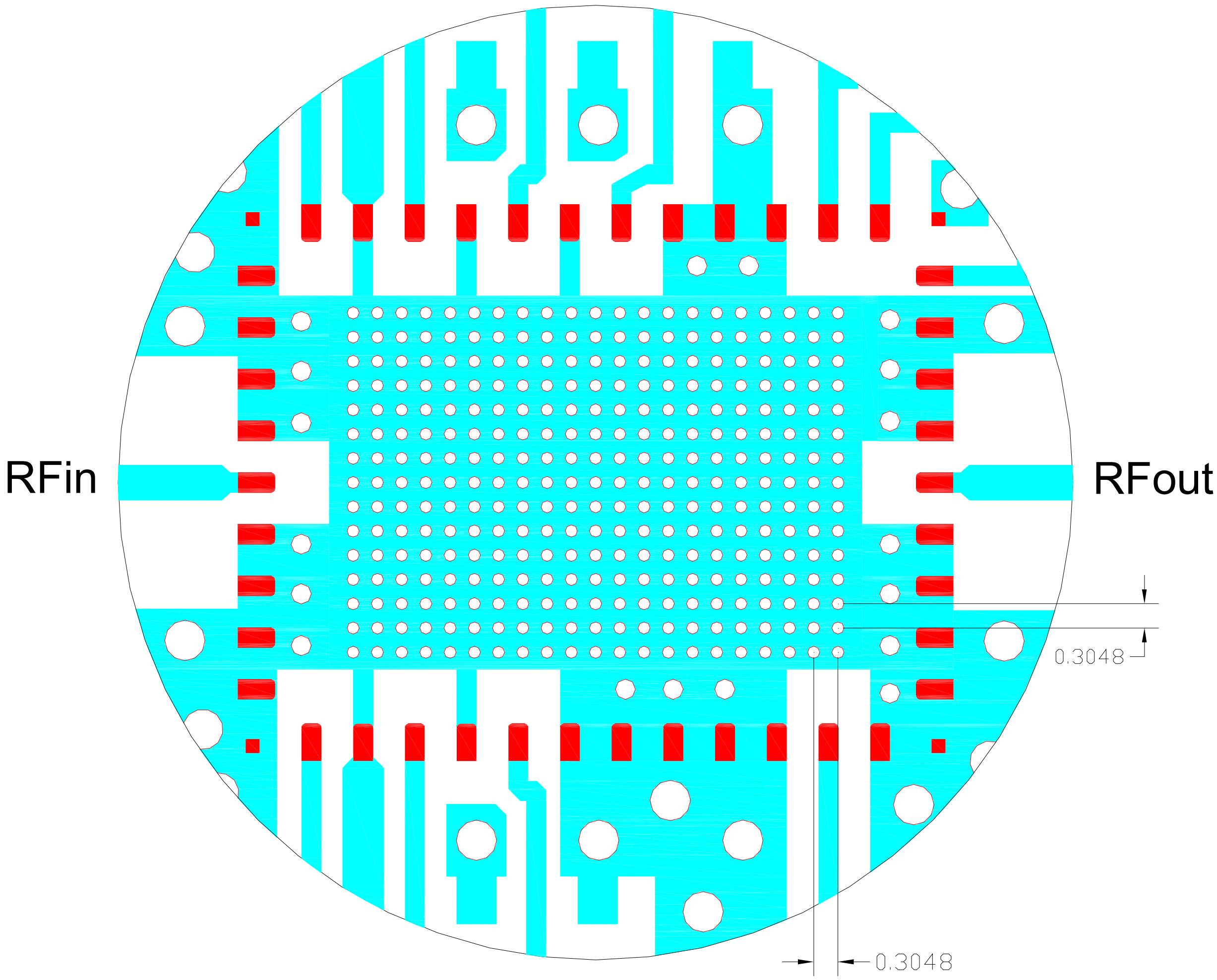
Package Marking and Dimensions

Marking: Part Number – TGA2752-SM
Lot Code – MXXXXXXX



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. This package is lead-free/RoHS-compliant with a copper alloy base (CDA194), and the plating material on the leads is NiPdAu. It is compatible with lead-free (maximum 260 °C reflow temperature) soldering process.

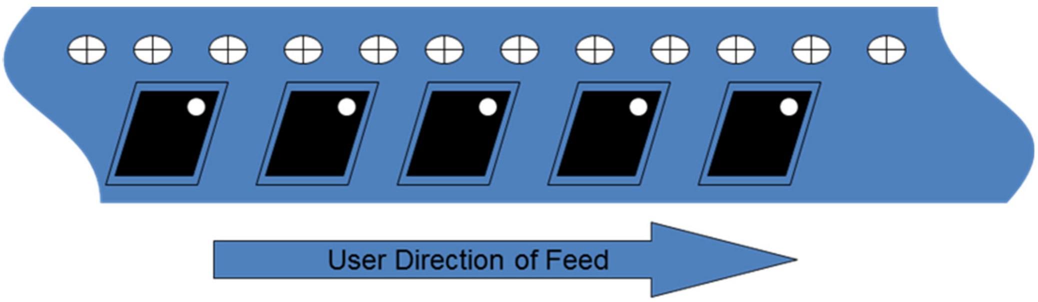
PCB Mounting Pattern

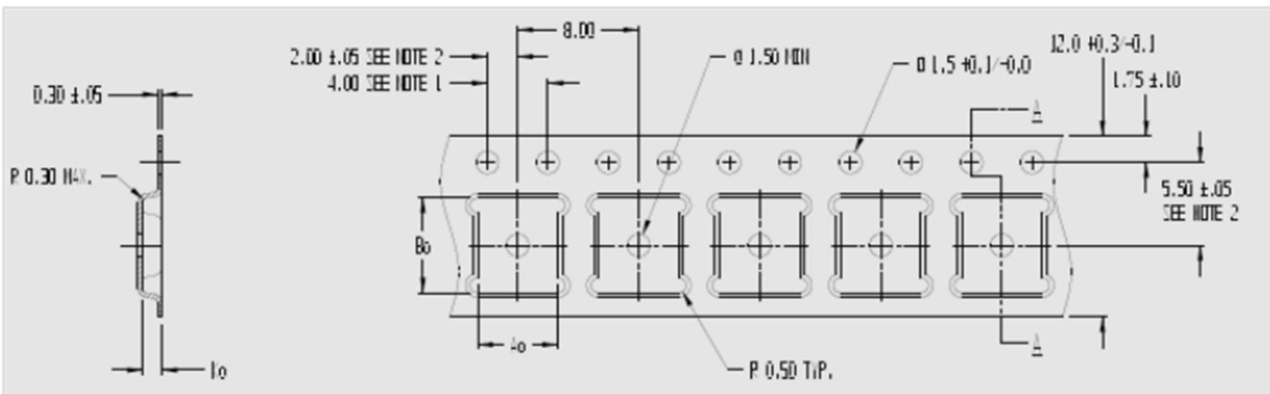


Notes:

1. The pad pattern shown has been developed and tested for optimized assembly at Qorvo. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.
2. Ground vias are critical for the proper performance of this device. Vias should have a final plated thru diameter of .1524 mm (.006").
3. For best thermal performance, vias under the ground paddle should be copper filled.

Tape and Reel Information





Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.366	9.3
	Width	B0	0.287	7.3
	Depth	K0	0.047	1.2
	Pitch	P1	0.472	12.0
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.0
	Cavity to Perforation - Width Direction	F	0.217	5.50
Cover Tape	Width	C	0.362	9.20
Carrier Tape	Width	W	0.630	16.0

Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.