TGA2958

13 – 18 GHz 2 W GaN Driver Amplifier

Product Description

Qorvo's TGA2958 is a driver amplifier fabricated on Qorvo's QGaN15 GaN on SiC process. The TGA2958 operates from 13 – 18 GHz and achieves 2 W of saturated output power with > 21 dB of large signal gain and at least 25% power-added efficiency.

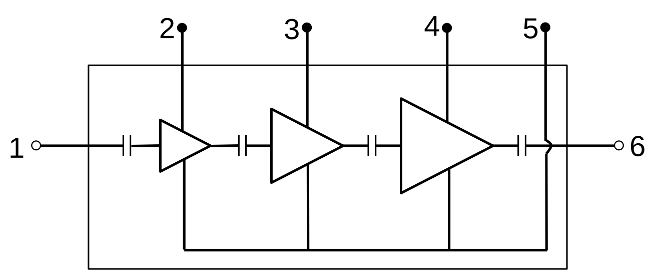
The TGA2958 is an ideal choice to drive Qorvo's high performing Ku-band GaN HPA's allowing the user to operate the driver and HPA off similar voltage rails.

Fully matched to 50 ohms with integrated DC blocking capacitors on both I/O ports, the TGA2958 is ideally suited for a variety of military and commercial radar and communications applications.

Lead free and RoHS compliant.

Evaluation Boards are available upon request.

Functional Block Diagram



Product Features

- Frequency Range: 13 - 18 GHz
- P_{SAT}: >33 dBm at P_{IN} = 12 dBm
- PAE: > 25 % at P_{IN} = 12 dBm
- Small Signal Gain: > 25 dB
- Input Return Loss: > 7 dB
- Output Return Loss: > 8 dB
- Bias: V_D = +20 V, I_{DQ} = 70 mA, V_G = −2.7 V Typical
- Chip Dimensions: 1.25 x 2.14 x 0.10 mm
- Performance under CW operation

Applications

- Satellite Communications
- Data Links
- Radar
- General Purpose

Ordering Information

Part No.	ECCN	Description
TGA2958	EAR99	13 – 18 GHz 2 W GaN Driver Amplifier

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	29.5 V
Gate Voltage Range (V_G)	-5 to 0 V
Drain Current – common drain - 1st Stage (I_{D1}) - 2nd Stage (I_{D2}) - 3rd Stage (I_{D3})	576 mA 72 mA 192 mA 384 mA
Gate Current at Tch = 200 °C: - 1st Stage (I_{G1}) - 2nd Stage (I_{G2}) - 3rd Stage (I_{G3})	 -0.2 to 1.2 mA -0.4 to 2.4 mA -0.8 to 2.4 mA
Power Dissipation (P_{DISS}), 85°C	13 W
Input Power (P_{IN}), CW, 50 Ω, V_D = 22 V, I_{DQ} = 70 mA, 85 °C	27 dBm
Input Power (P_{IN}), CW, VSWR 3:1, V_D = 22 V, I_{DQ} = 70 mA, 85 °C	20 dBm
Channel Temperature (T_{CH})	275 °C
Mounting Temperature (30 Seconds)	320 °C
Storage Temperature	-55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating

Parameter	Value / Range
Drain Voltage (V_D) CW	20 V
Drain Current (I_{DQ})	70 mA
Drain Current Under RF Drive (I_{D_DRIVE})	See plots p. 7
Gate Voltage (V_G)	−2.7 V (Typ.)
Gate Current Under RF Drive (I_{G_DRIVE})	See plots p. 7
Temperature (T_{BASE})	-40 to 85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Min	Typ	Max	Units
Operational Frequency Range	13		18	GHz
Small Signal Gain		> 25		dB
Input Return Loss		> 7		dB
Output Return Loss		> 8		dB
Output Power at P_{IN} = 12 dBm		> 33		dBm
Power Added Efficiency at P_{IN} = 12 dBm		> 25		%
Large Signal Gain at P_{IN} = 12 dBm		> 21		dB
IM3 (Pout/tone = 24 dBm, 1 MHz spacing)		-27		dBc
IM5 (Pout/tone = 24 dBm, 1 MHz spacing)		-33		dBc
Small Signal Gain Temperature Coefficient		-0.07		dB/°C
Output Power Temperature Coefficient - at P_{IN} = 0 dBm - at P_{IN} = 12 dBm		 -0.06 -0.01		dBm/°C
Recommended Operating Voltage		20	22	V

Test conditions unless otherwise noted: 25 °C, V_D = +20 V, I_{DQ} = 70 mA, V_G = −2.7 V Typical, CW.

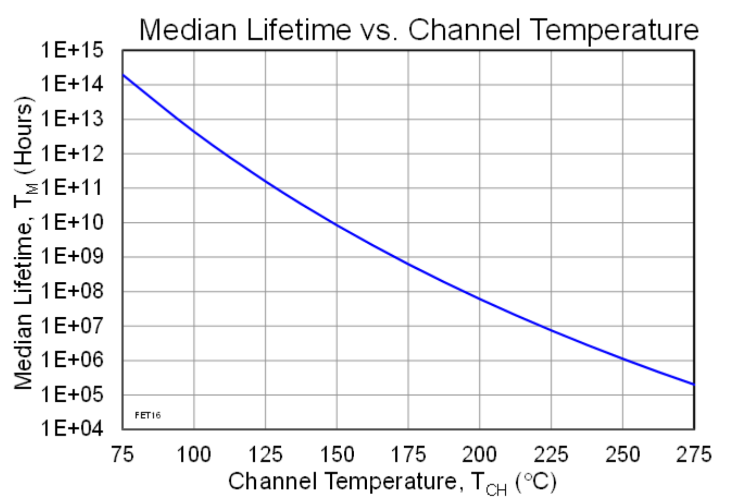
Thermal and Reliability Information

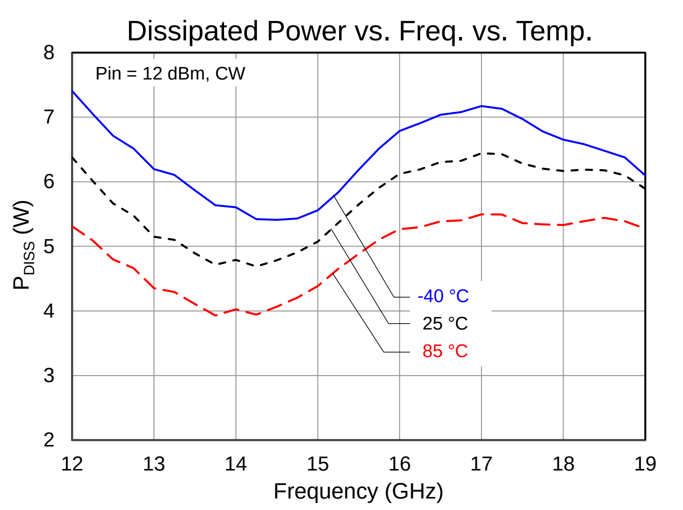
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85°C, V_D = 20 V (CW), I_{DQ} = 70 mA, P_{DISS} = 1.4 W	12.9	°C/W
Channel Temperature (T_{CH}) (Quiescent)		103	°C
Median Lifetime (T_M)		1.8 x 10^15	Hrs
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85°C, V_D = 20 V (CW), Freq = 17 GHz, I_{DQ} = 70 mA, P_{OUT} = 27 dBm, P_{DISS} = 3.2 W	15.6	°C/W
Channel Temperature (T_{CH}) (Under RF drive)		135	°C
Median Lifetime (T_M)		8.3 x 10^12	Hrs
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85°C, V_D = 20 V (CW), Freq = 17 GHz, I_{DQ} = 70 mA, P_{OUT} = 33.5 dBm, P_{DISS} = 7.9 W	14.8	°C/W
Channel Temperature (T_{CH}) (Under RF drive)		202	°C
Median Lifetime (T_M)		1.2 x 10^09	Hrs

Notes:
1. Thermal resistance measured to back of carrier plate. MMIC mounted on a 40 mil CuMo carrier using 1.5 mil 80/20 AuSn.

Median Lifetime

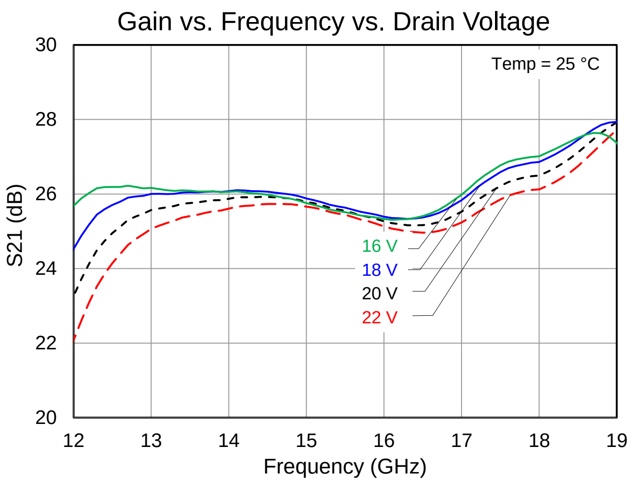
Test Conditions: V_D = +28 V; Failure Criteria = 10 % reduction in ID_MAX

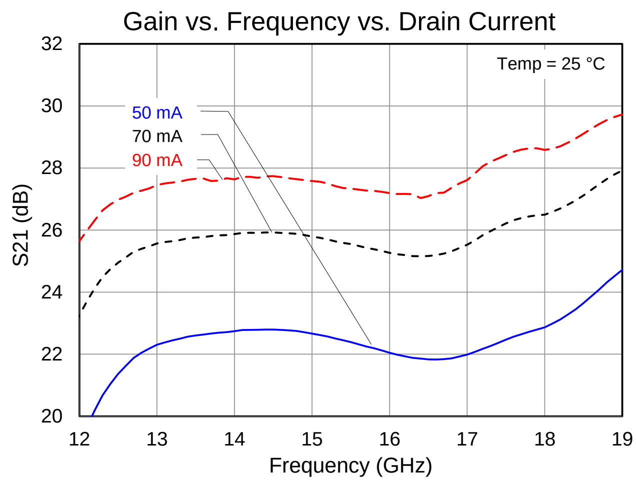


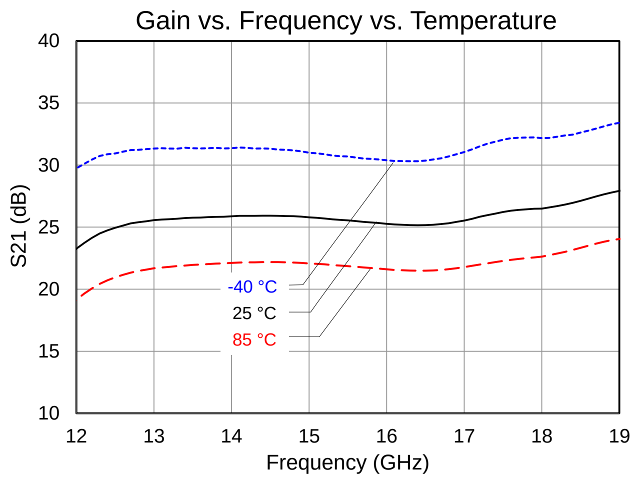


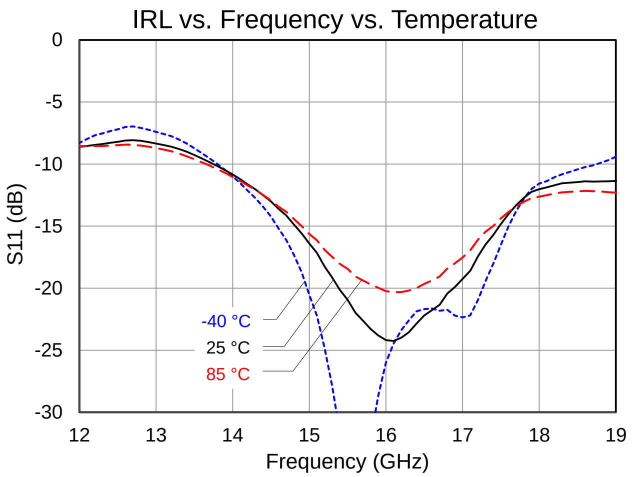
Performance Plots – Small Signal

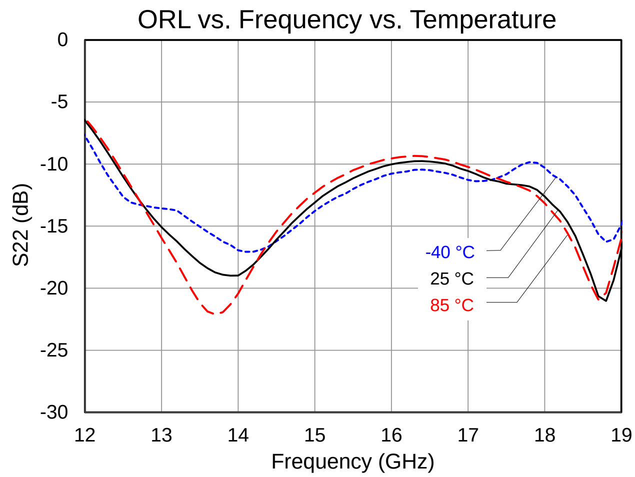
Conditions unless otherwise specified: V_D = +20 V, I_D = 70 mA, V_G = −2.7 V Typical, CW.





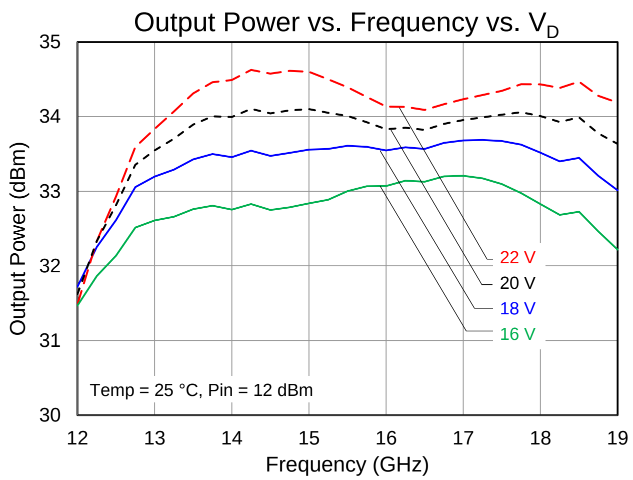


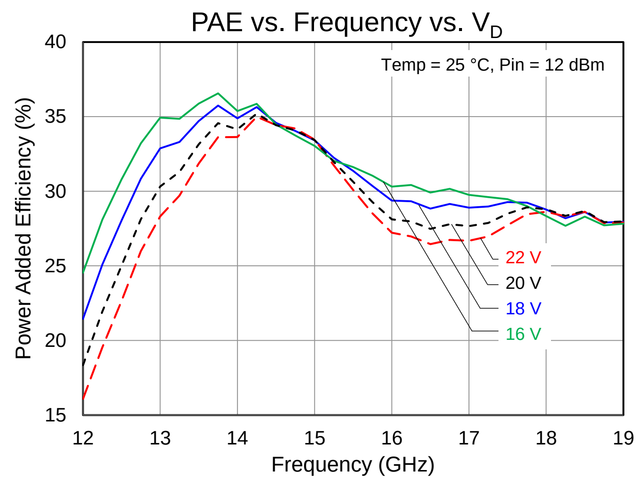


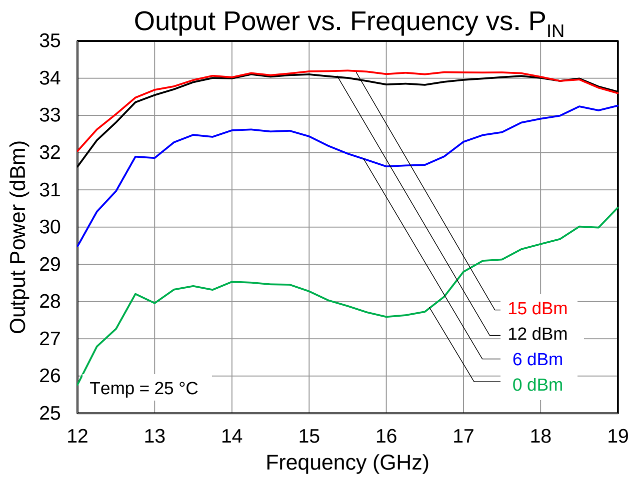


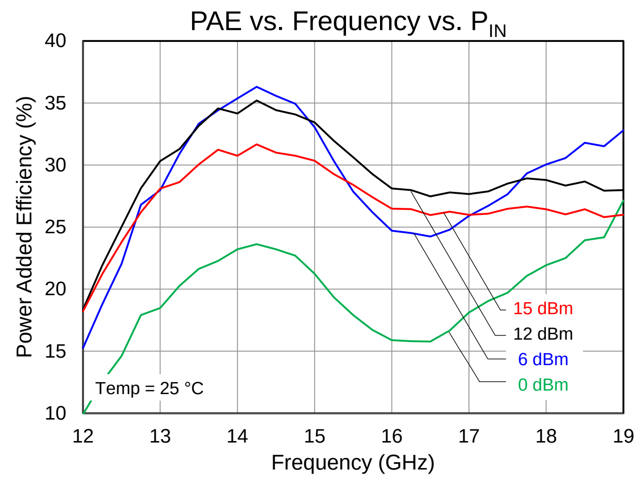
Performance Plots – Large Signal

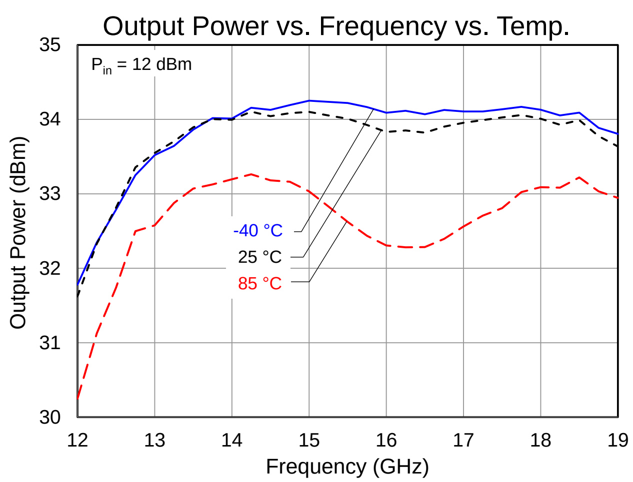
Conditions unless otherwise specified: V_D = +20 V, I_D = 70 mA, V_G = −2.7 V Typical, CW

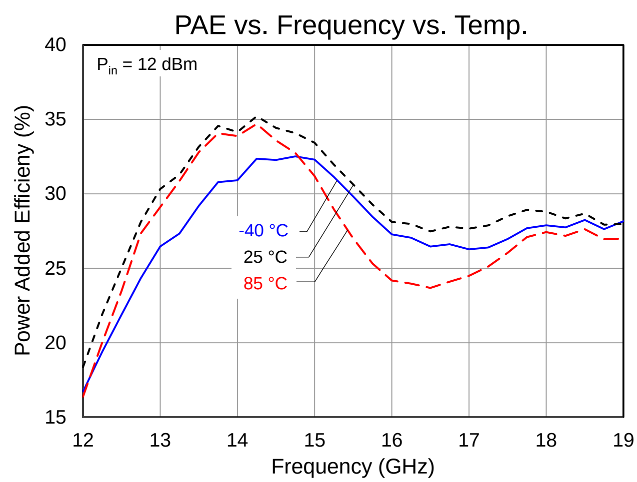






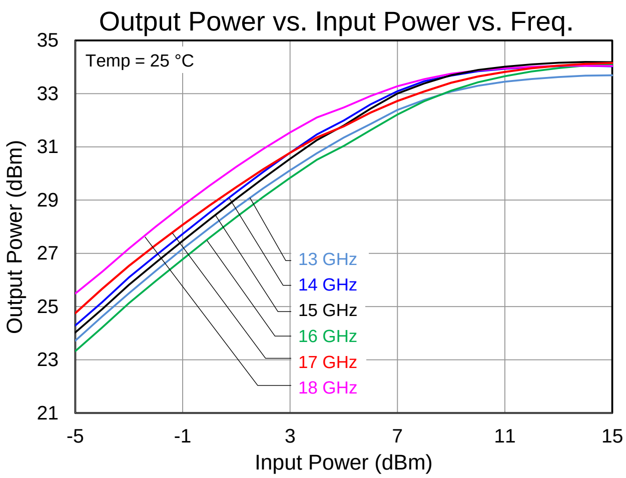


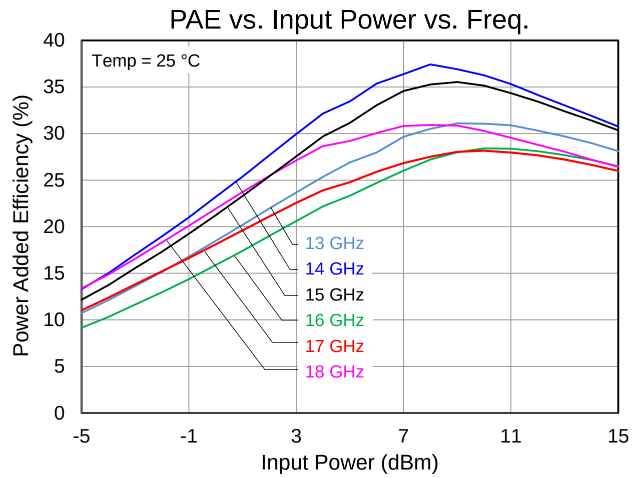


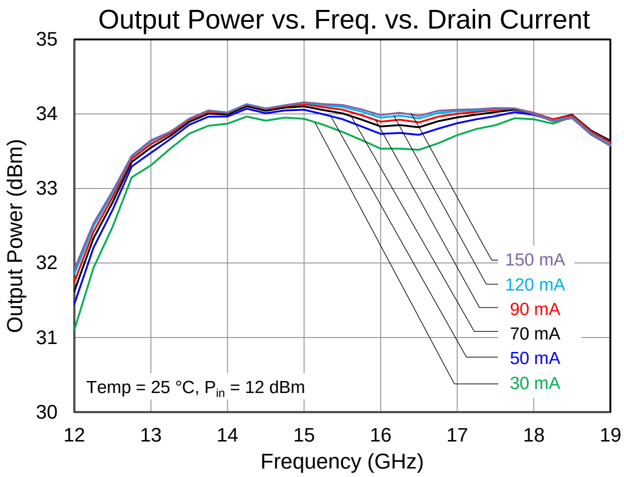


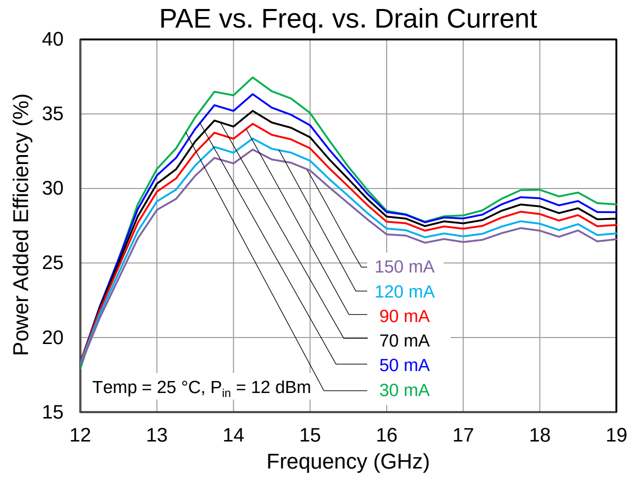
Performance Plots – Large Signal

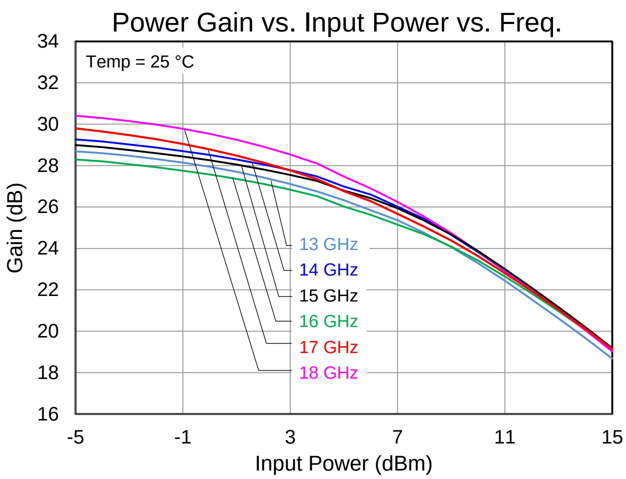
Conditions unless otherwise specified: V_D = +20 V, I_D = 70 mA, V_G = −2.7 V Typical, CW

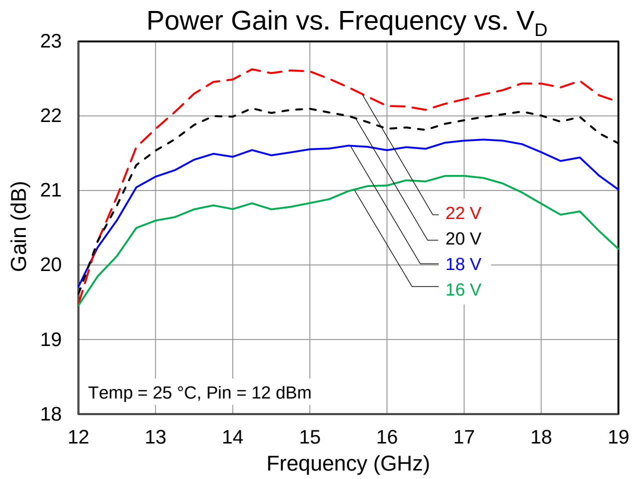






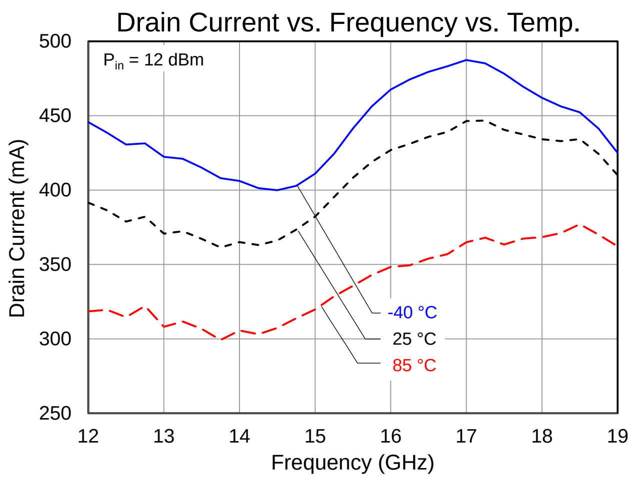


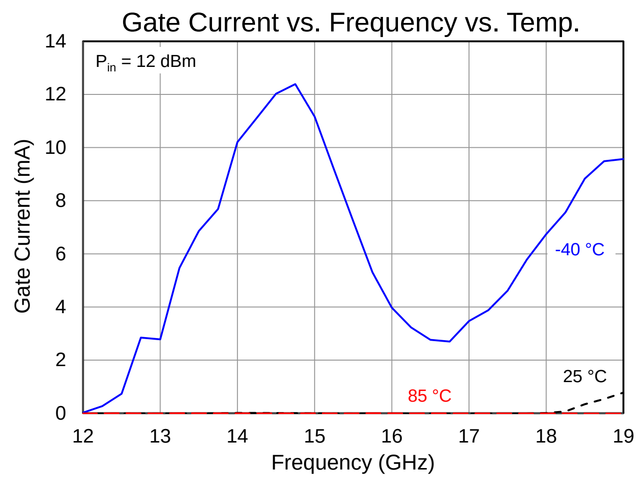


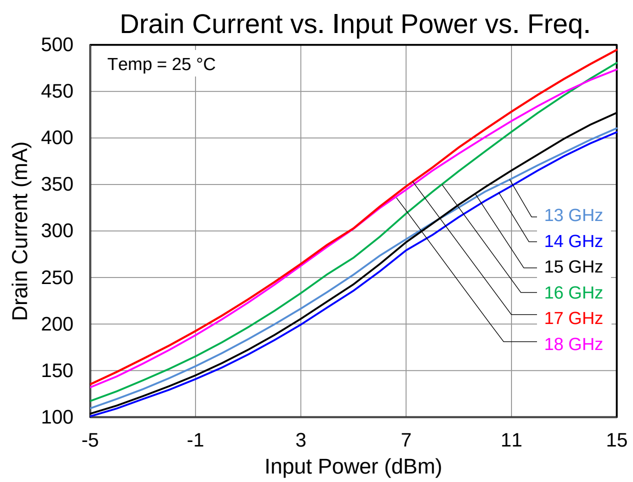


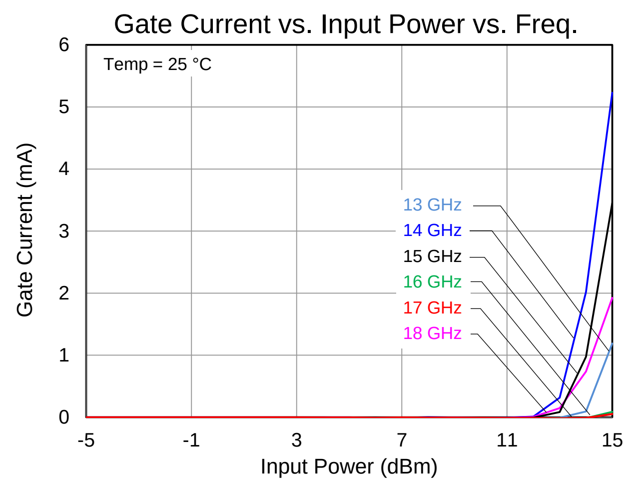
Performance Plots – Large Signal

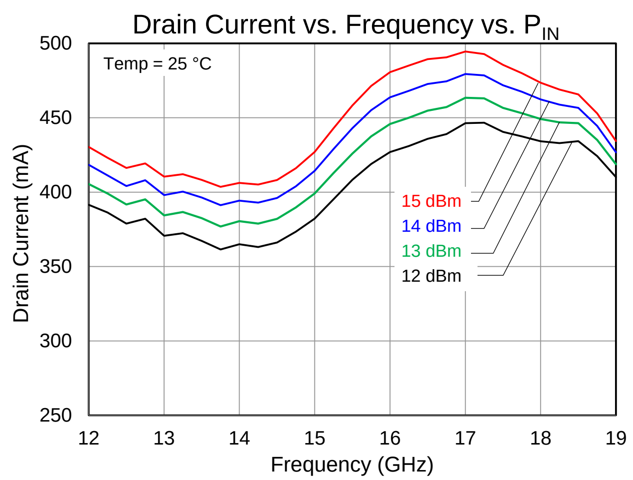
Conditions unless otherwise specified: V_D = +20 V, I_D = 70 mA, V_G = −2.7 V Typical, CW

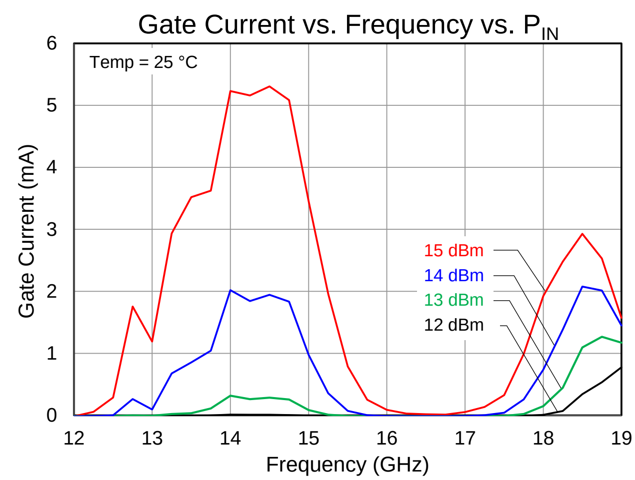






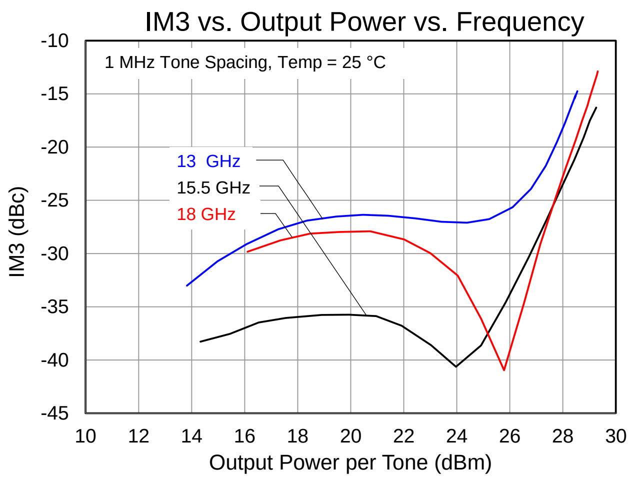


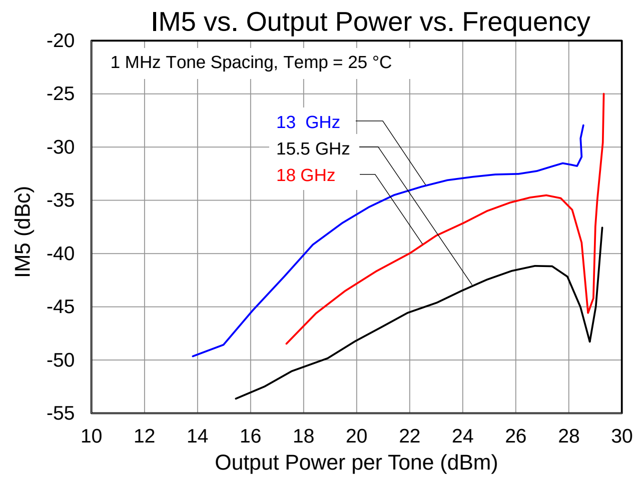


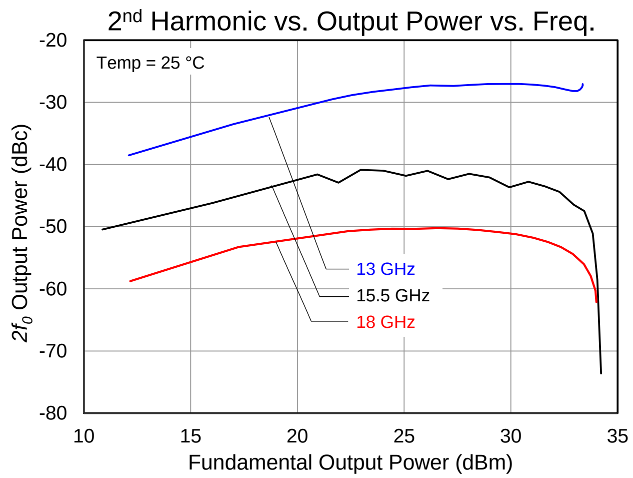


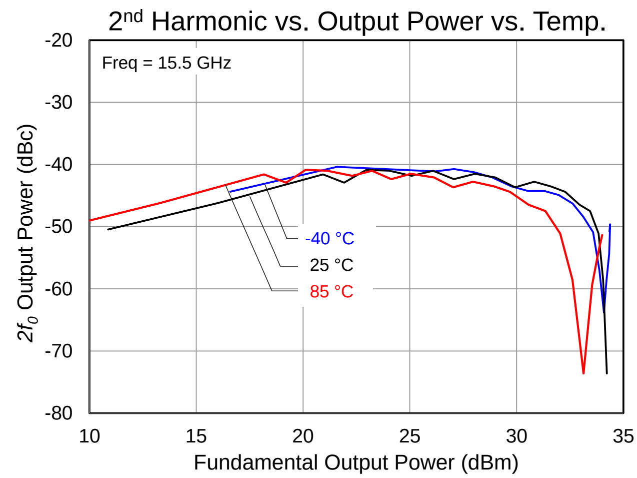
Performance Plots – Large Signal and Linearity

Conditions unless otherwise specified: V_D = +20 V, I_D = 70 mA, V_G = −2.7 V Typical, CW

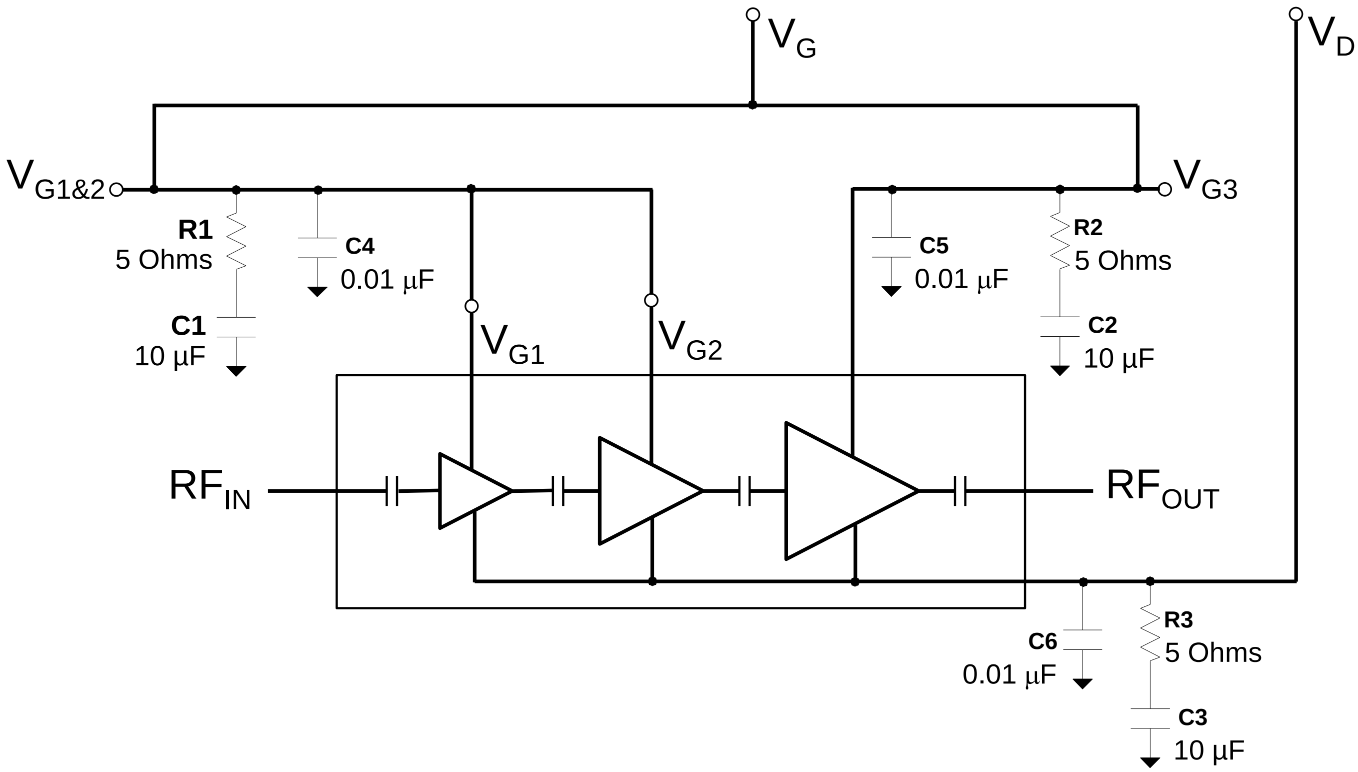








Applications Information and Pad Layout



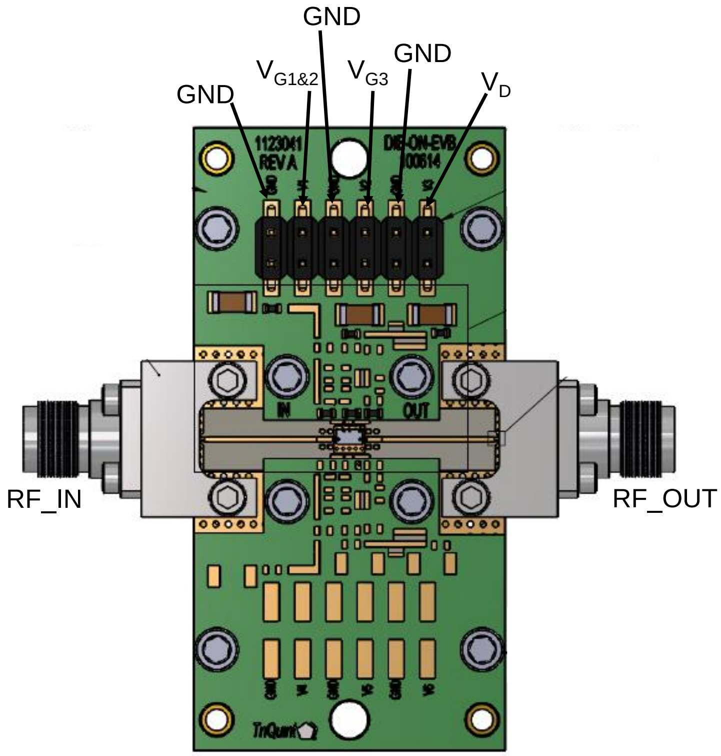
Bias Up Procedure

1. Set I_D limit to 500 mA, I_G limit to 13 mA
2. Apply −5 V to V_G
3. Apply +20 V to V_D ; ensure I_{DQ} is approx. 0 mA
4. Adjust V_G until I_{DQ} = 70 mA (V_G ~ −2.7 V Typ.).
5. Turn on RF signal generator

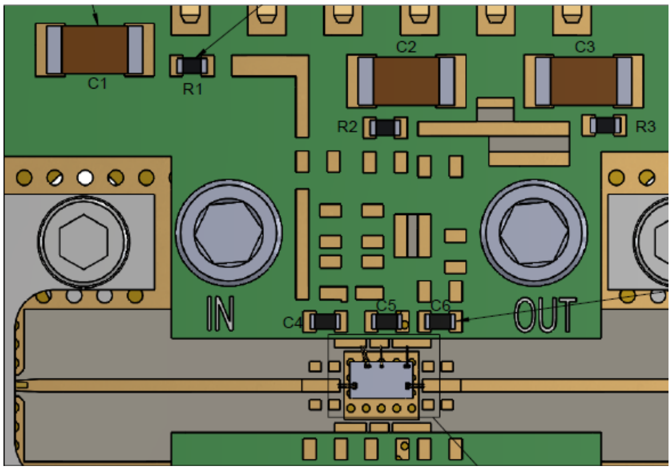
Bias Down Procedure

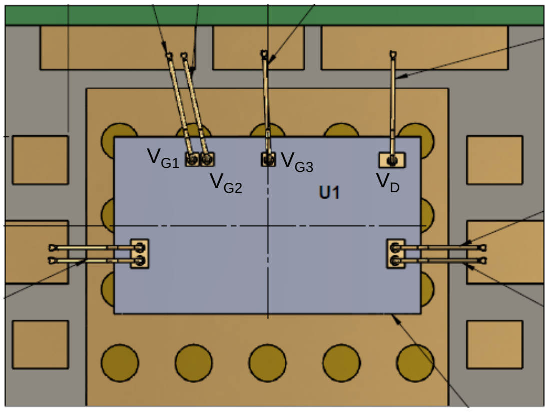
1. Turn off RF signal generator
2. Reduce V_G to −5 V; ensure I_{DQ} is approx. 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Evaluation Board



MMIC Bonding Detail:

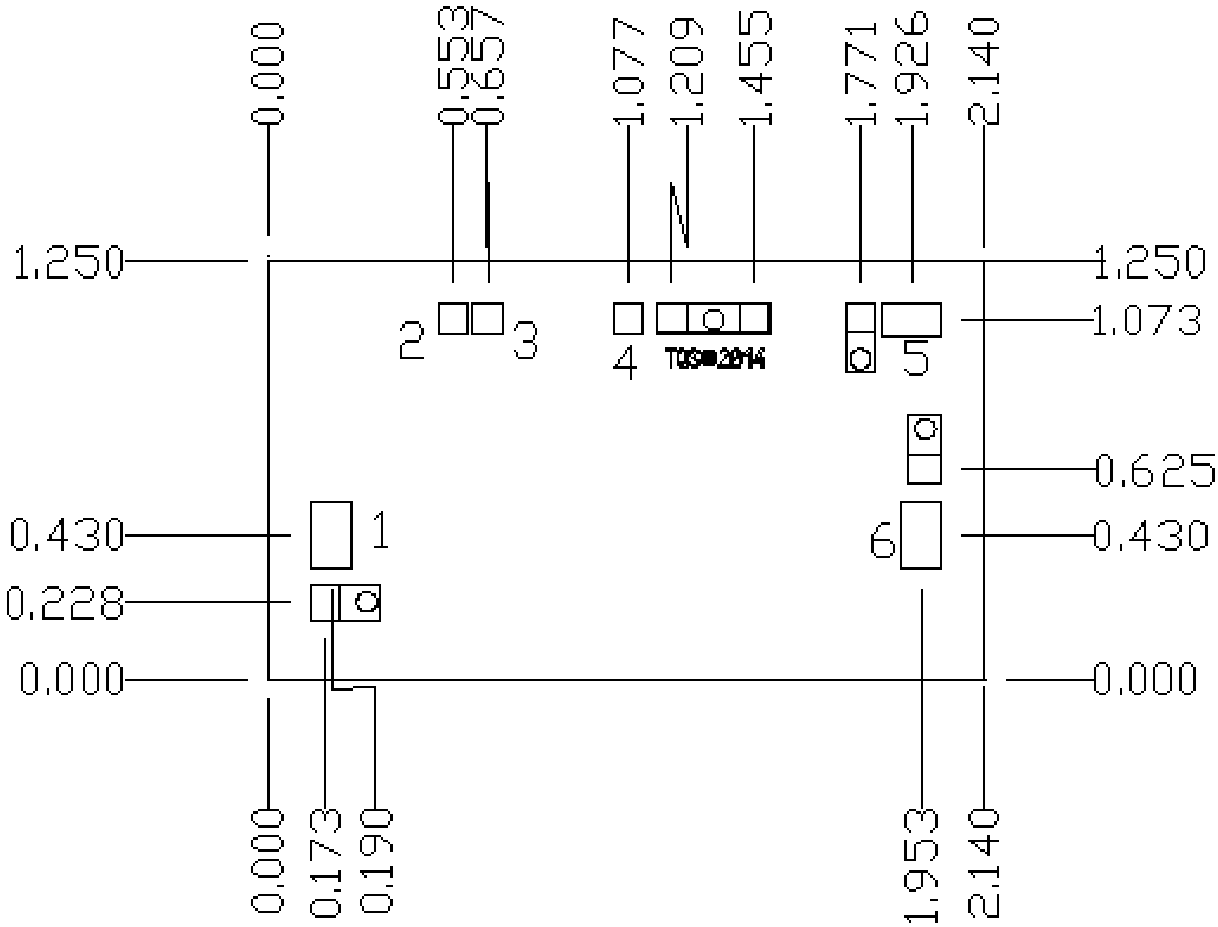




Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1, C2, C3	10 µF	Cap, 1206, 50V, 20%, X5R	Various	–
C4, C5, C6	0.01 µF	Cap, 0402, 50V, 10%, X7R	Various	–
R1, R2, R3	5.1 Ohms	Res, 0402, 5%	Various	–

Mechanical Information



Pad Description

Pad No.	Symbol	Description
1	RF_{IN}	Input; matched to 50 Ω; DC blocked
2	V_{G1} (1), (2)	Gate Voltage; Bias network is required; see recommended Application Information on page 9.
3	V_{G2} (1), (2)	Gate Voltage; Bias network is required; see recommended Application Information on page 9.
4	V_{G3} (2)	Gate Voltage; Bias network is required; see recommended Application Information on page 9.
5	V_D	Drain voltage; Bias network is required; see recommended Application Information page 9.
6	RF_{OUT}	Output; matched to 50 Ω; DC blocked

Notes:
1. Pads 2 & 3 are tied together off-chip.
2. Pads 2,3, & 4 may be tied together for biasing

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment (i.e. epoxy) can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300°C to 3-4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	TBD	JEDEC Standard JESD22 A114

Caution!
ESD-Sensitive Device

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260 °C

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Qorvo:

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