

Product Description

Qorvo's TGA2595 is a balanced Ka-band power amplifier fabricated on Qorvo's 0.15 um GaN on SiC process. The balanced configuration supports low return loss and improves robustness into non-ideal loads.

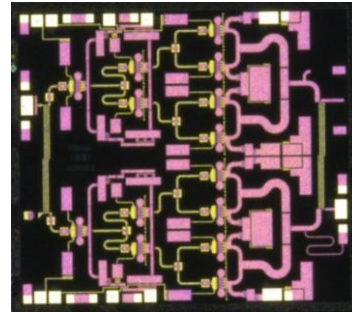
Operating from 27.5 to 31 GHz, it achieves 9W saturated output power, power-added efficiency of 24 % and 23 dB small signal gain. Along with excellent linear characteristics, the TGA2595 is ideally suited to support both commercial and defense related satellite communications.

To simplify system integration, the TGA2595 is fully matched to 50 Ω with integrated DC blocking caps on both I/O ports.

The TGA2595 is 100% DC and RF tested on-wafer to ensure compliance to electrical specifications.

Lead-free and RoHS compliant.

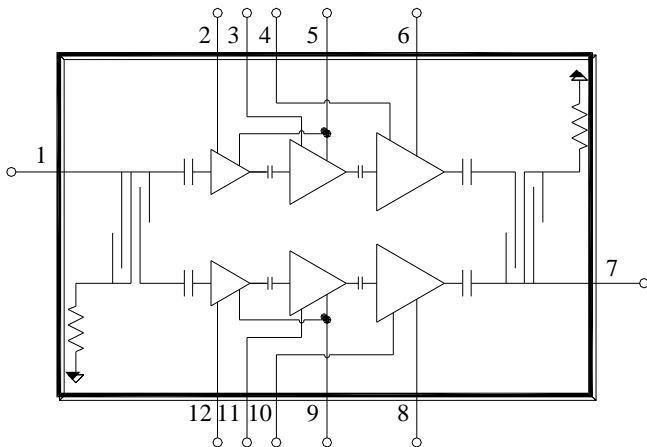
Evaluation Boards are available upon request.



Product Features

- Frequency Range: 27.5 to 31 GHz
- P_{OUT}: 39.5 dBm (P_{IN} = 22 dBm), CW
- PAE: 24 % (P_{IN} = 22 dBm), CW
- Small Signal Gain: 23 dB
- Return Loss: 20 dB
- IM3 @ 33 dBm/tone: -30 dBc
- IM5 @ 33 dBm/tone: -35 dBc
- Bias: V_D = +20 V, I_{DQ} = 280 mA, V_G = -3.0 V Typical
- Chip Dimensions: 3.60 x 3.24 x 0.10 mm

Functional Block Diagram



Applications

- Satellite Communications

Ordering Information

Part No.	ECCN	Description
TGA2595	3A001.b.2.c	27.5 – 31 GHz 9 W GaN Power Amplifier

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	+29.5 V
Gate Voltage Range (V_G)	-5 to 0 V
Drain Current (I_D)	2800 mA
Gate Current (I_G)	-5.5 to 33 mA
Power Dissipation, 85 °C, (P_{DISS})	44 W
Input Power, CW, 50 Ω , 85 °C, (P_{IN})	30 dBm
Input Power, CW, 10:1 VSWR, 25 °C, (P_{IN})	25 dBm
Channel temperature (T_{CH})	275 °C
Mounting Temperature (30 Seconds)	320 °C
Storage Temperature	-40 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating

Parameter	Value / Range
Drain Voltage (V_D)	+20V
Drain Current (I_{DQ})	280mA
Drain Current Under RF Drive (I_{D_Drive})	See page 6
Gate Voltage (V_G)	-3 V Typical

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Min	Typ	Max	Units
Operational Frequency Range	27.5	–	31	GHz
Small Signal Gain	–	23	–	dB
Input Return Loss	–	20	–	dB
Output Return Loss	–	20	–	dB
Output Power @ $P_{IN} = 22$ dBm	–	39.5	–	dBm
Power Added Efficiency @ $P_{IN} = 22$ dBm	–	25	–	%
IM3 @ $P_{out}/Tone = 33$ dBm	–	-30	–	dBc
IM5 @ $P_{out}/Tone = 33$ dBm	–	-35	–	dBc
Small Signal Gain Temperature Coefficient	–	-0.09	–	dB/°C
Output Power Temperature Coefficient	–	-0.01	–	dBm/°C

Test conditions unless otherwise noted: 25 °C, $V_D = +20$ V, $I_{DQ} = 280$ mA, $V_G = -3$ V Typical

Thermal and Reliability Information

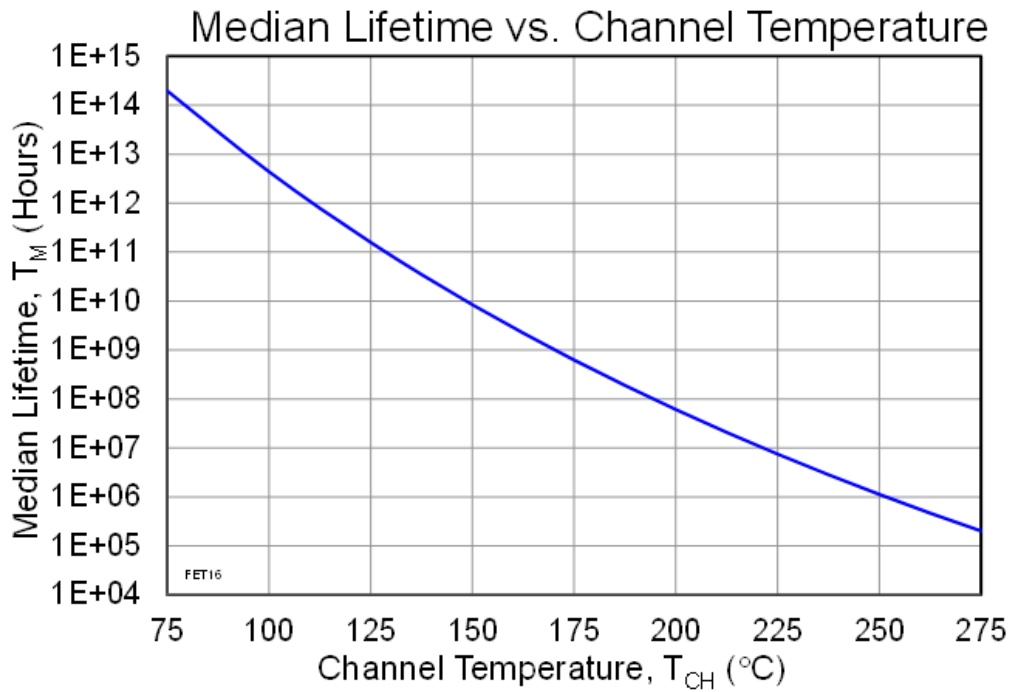
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) ⁽¹⁾	For $I_{DQ} = 280$ mA: $T_{BASE} = 85$ °C, $V_D = +20$ V, $I_{D_Drive} = 1600$ mA, $P_{IN} = 22$ dBm, $P_{OUT} = 39$ dBm, $P_{DISS} = 24$ W	4.35	°C/W
Channel Temperature (T_{CH}) under RF Drive		189	°C
Median Lifetime (T_M) under RF Drive		5.53×10^9	Hrs
Thermal Resistance (θ_{JC}) ⁽¹⁾	For $I_{DQ} = 560$ mA: $T_{BASE} = 85$ °C, $V_D = +20$ V, $I_{D_Drive} = 1780$ mA, $P_{IN} = 22$ dBm, $P_{OUT} = 39.5$ dBm, $P_{DISS} = 26.7$ W	4.35	°C/W
Channel Temperature (T_{CH}) under RF Drive		201	°C
Median Lifetime (T_M) under RF Drive		1.36×10^9	Hrs

Notes:

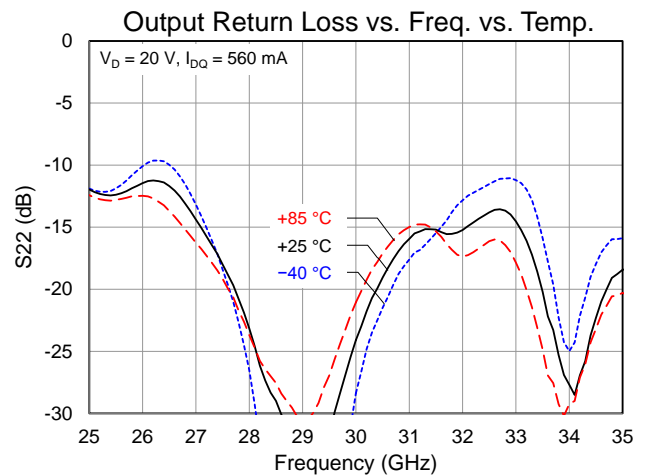
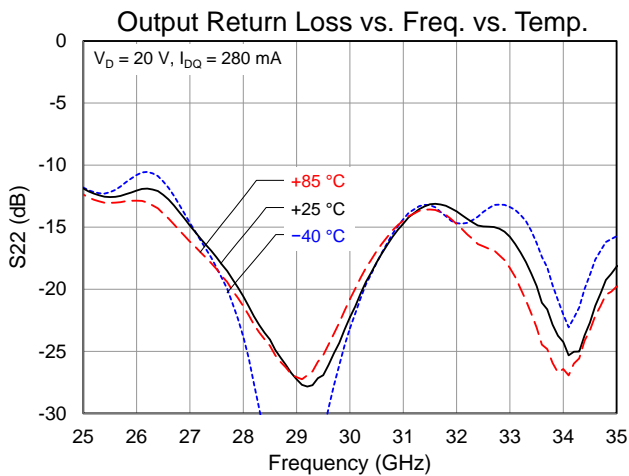
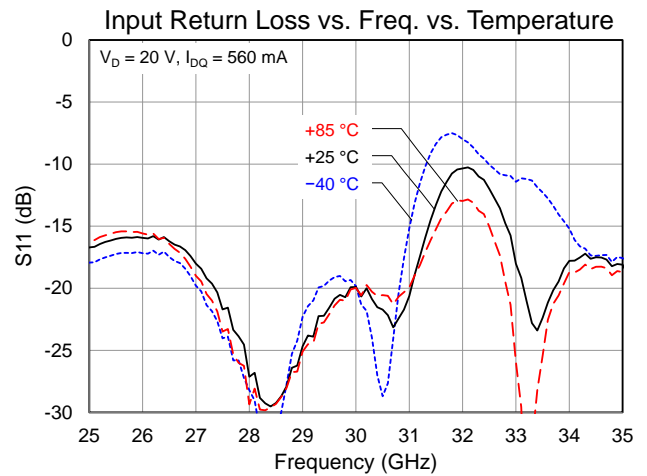
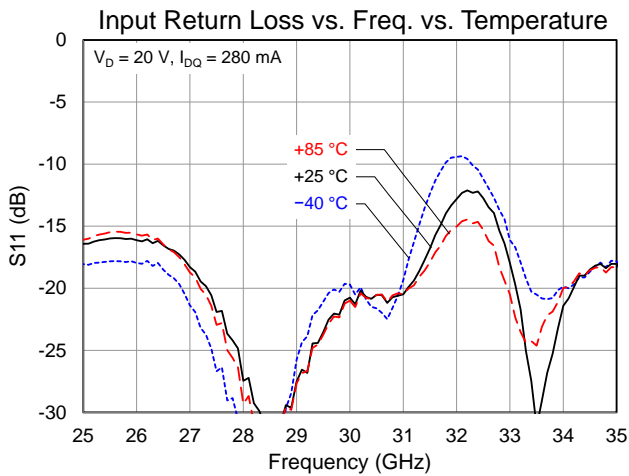
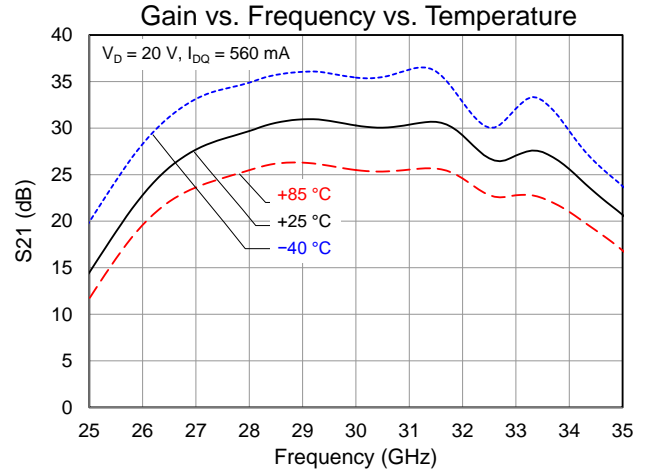
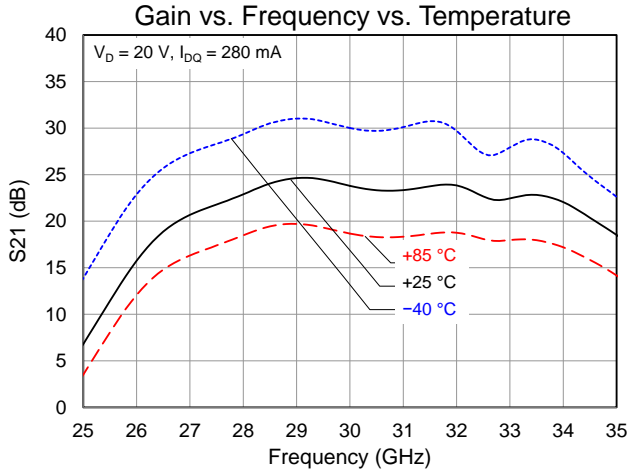
1. Thermal resistance measured to back of carrier plate. MMIC mounted on 20 mils CuMo carrier using 1.5 mil 80/20 AuSn.

Median Lifetime

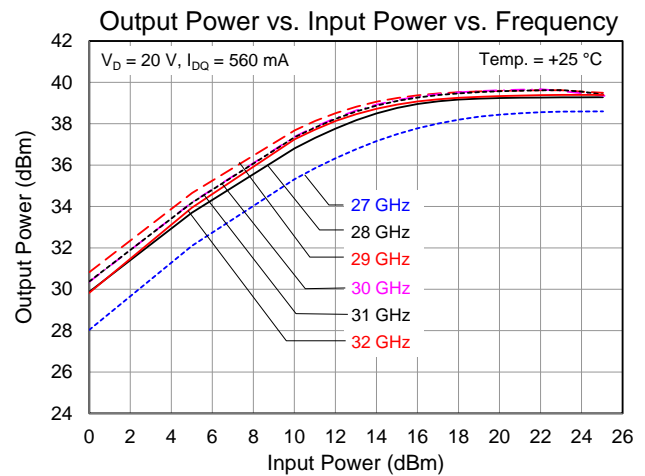
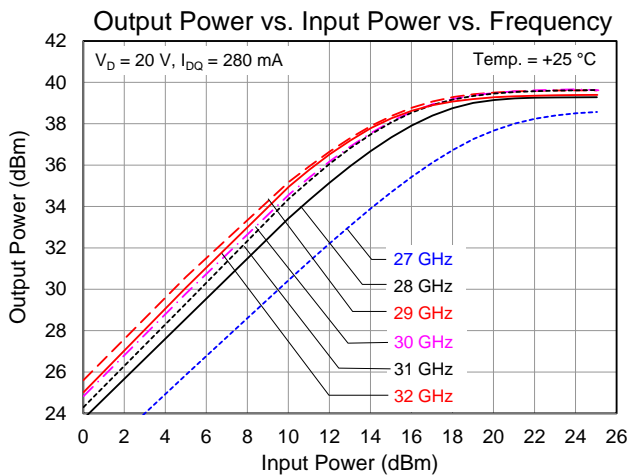
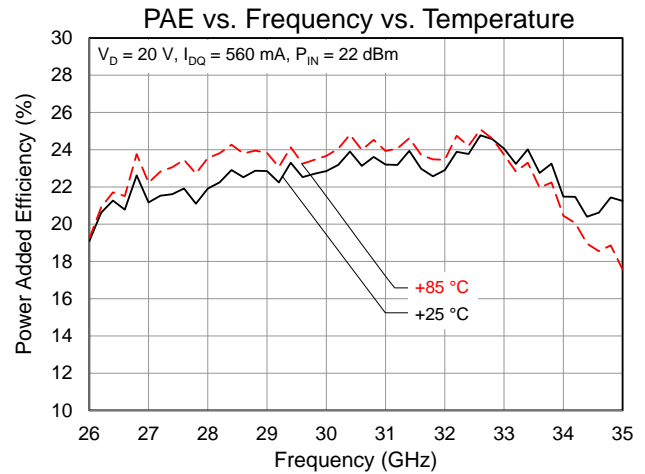
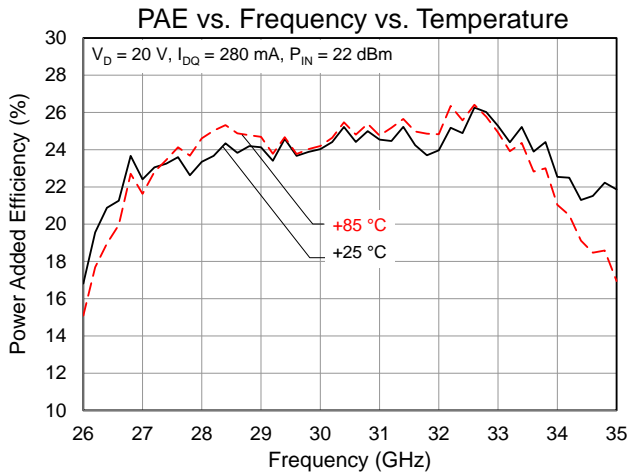
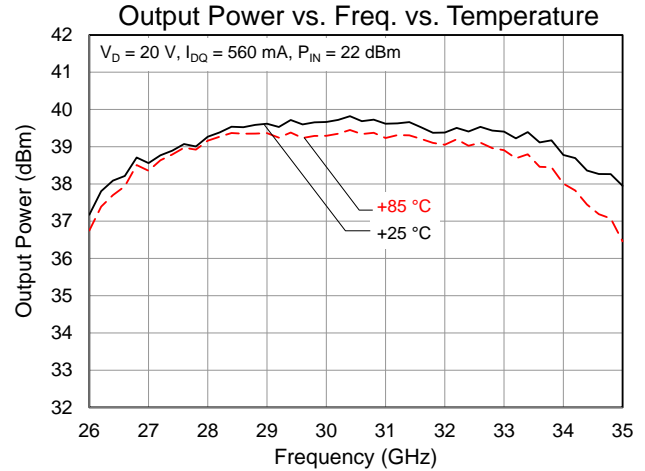
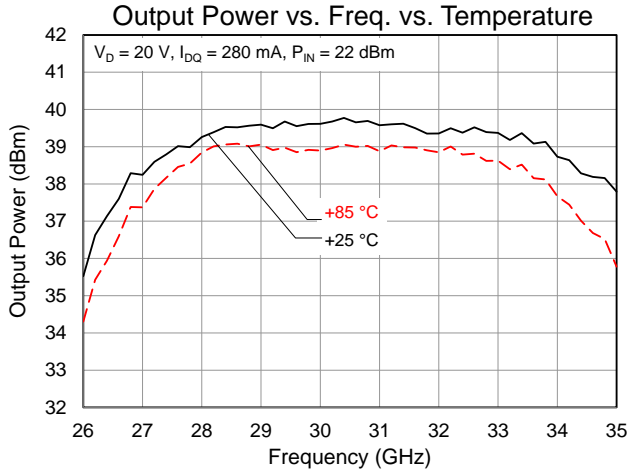
Test Conditions: $V_D = +28$ V; Failure Criteria = 10 % reduction in ID_MAX



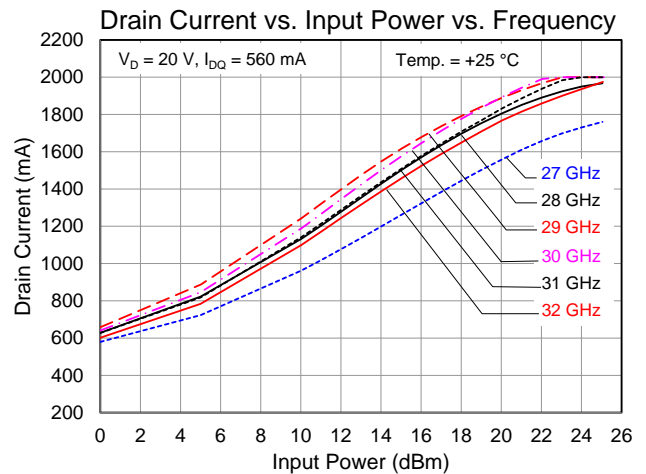
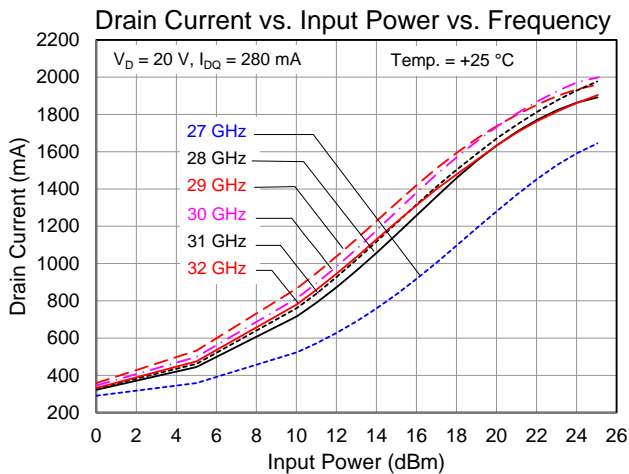
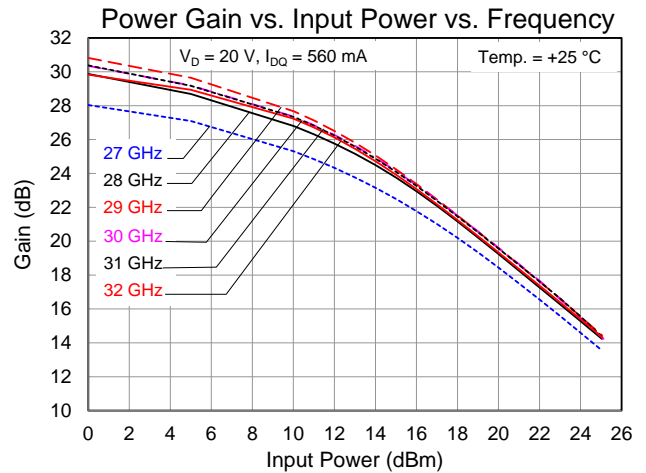
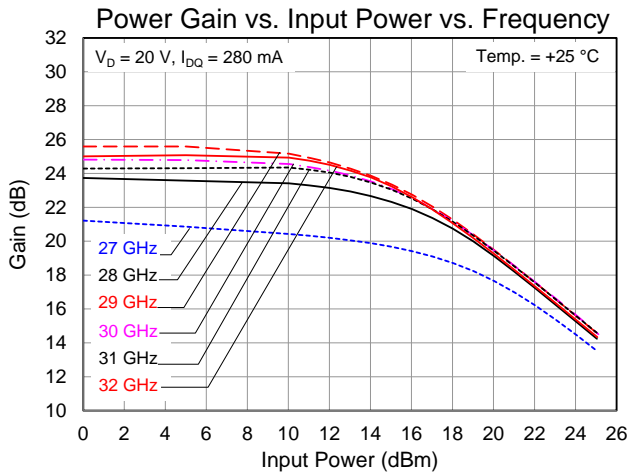
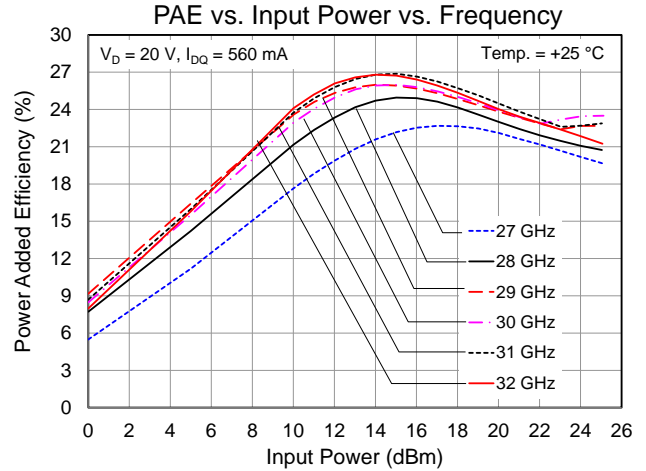
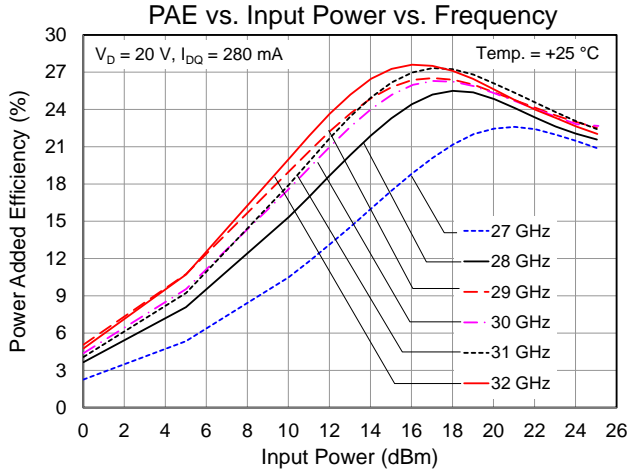
Typical Performance – Small Signal



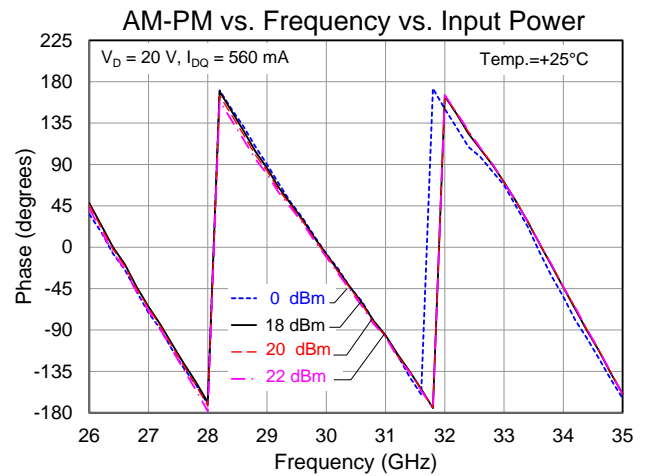
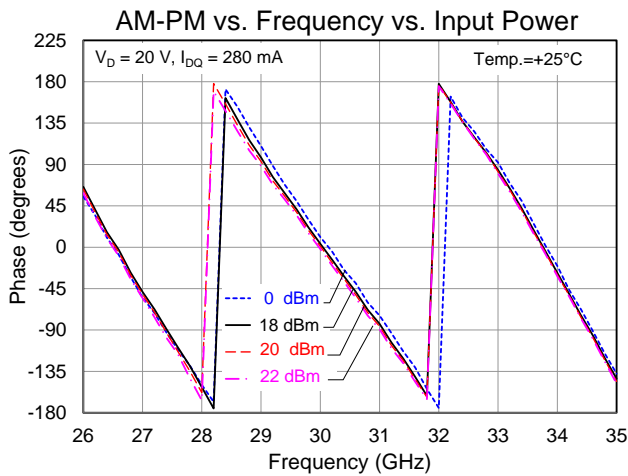
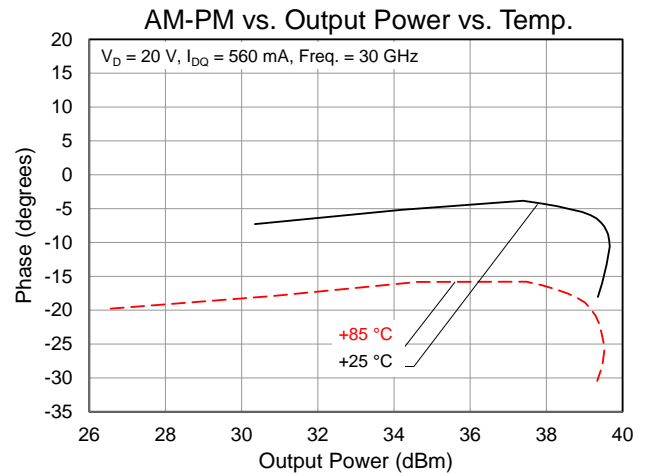
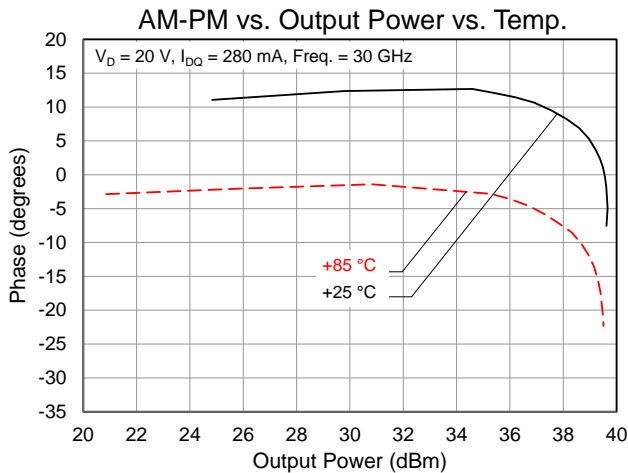
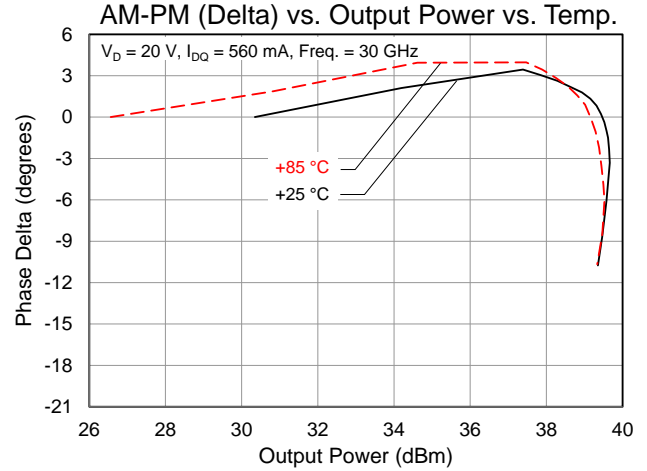
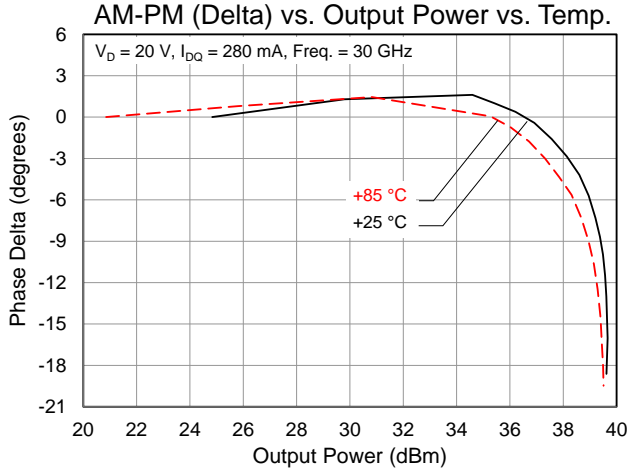
Typical Performance – Large Signal



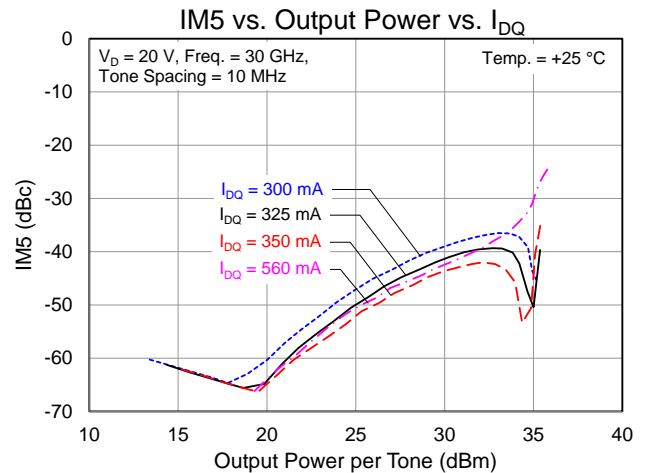
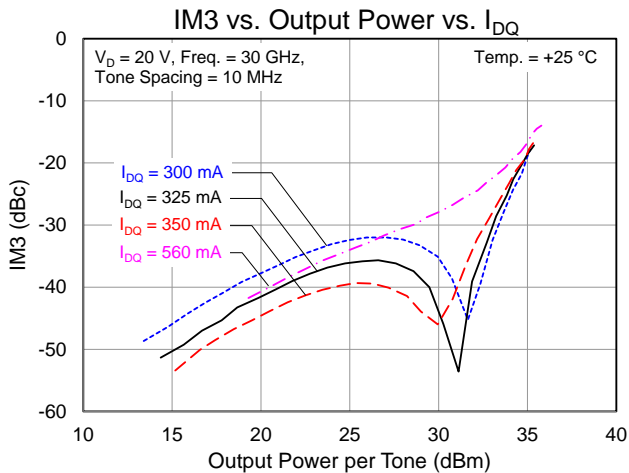
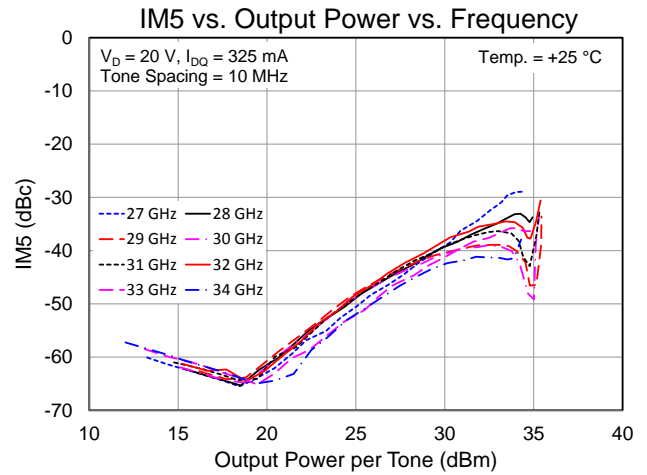
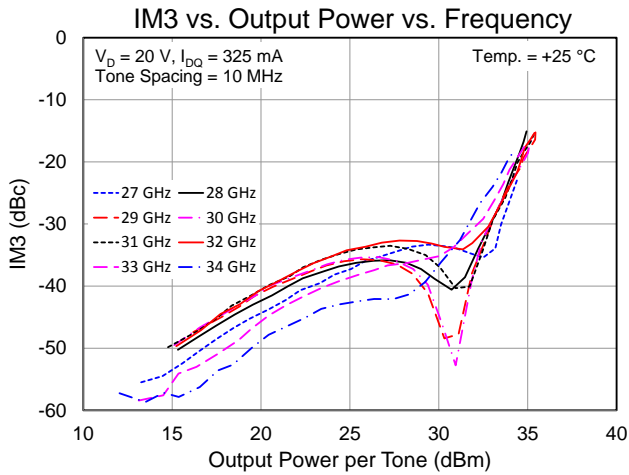
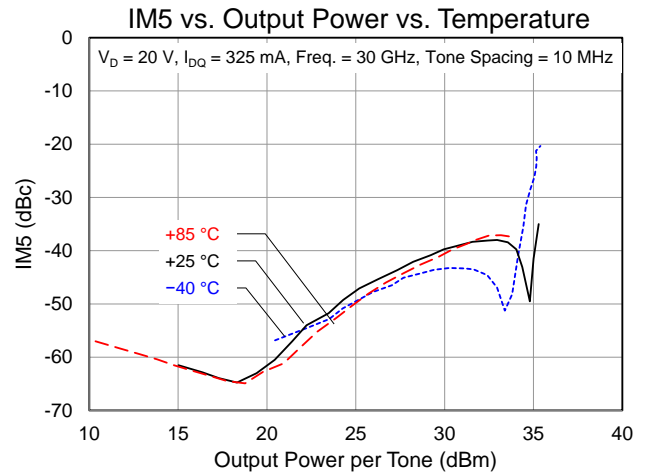
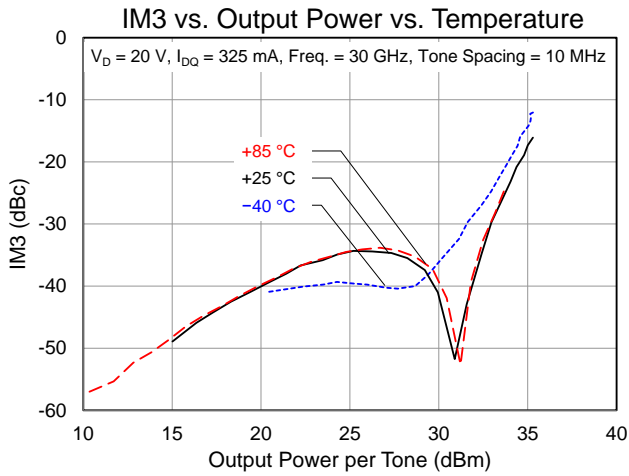
Typical Performance – Large Signal (cont.)



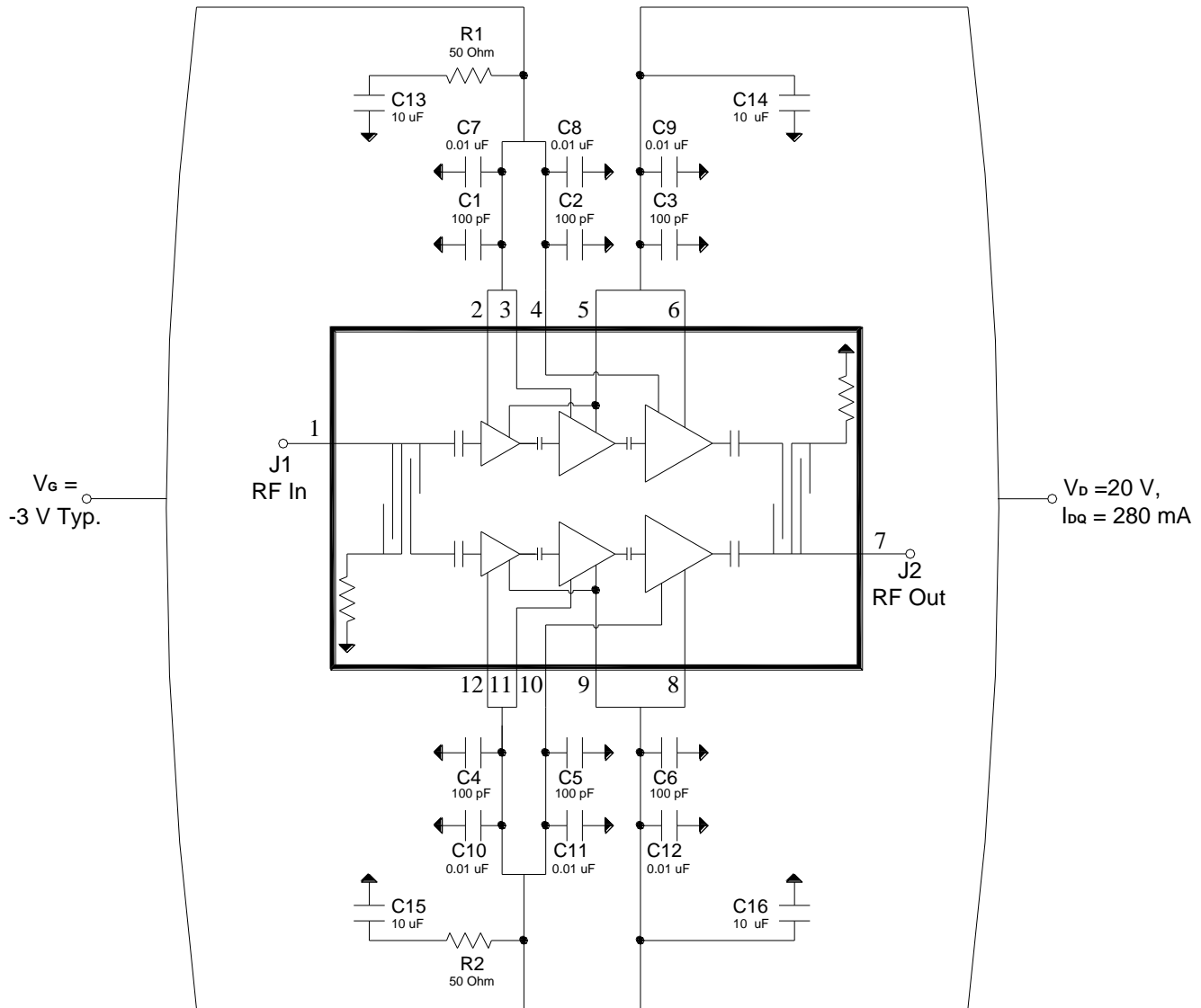
Typical Performance – Large Signal (Cont.)



Typical Performance – Linearity



Application Circuit



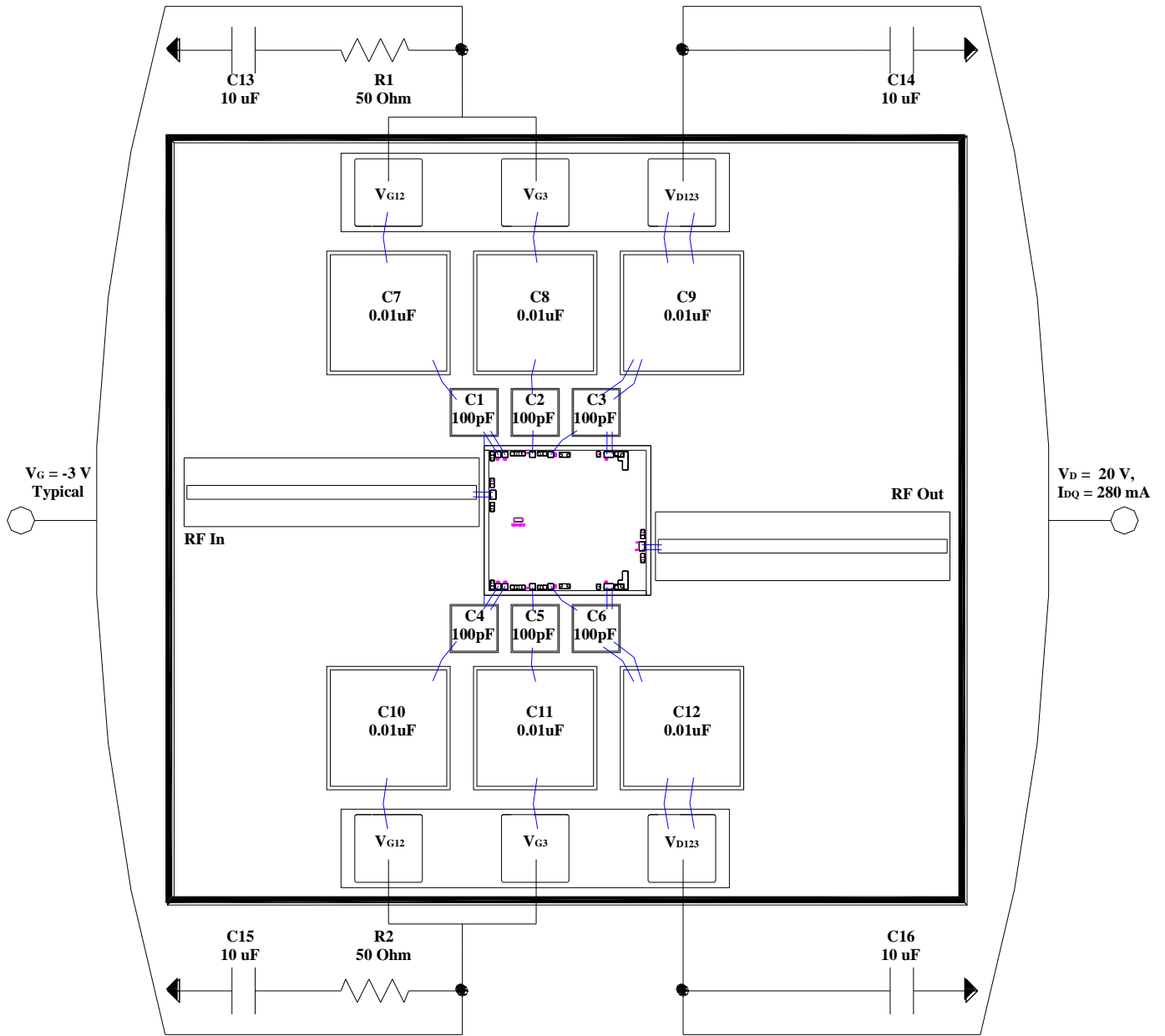
Bias Up Procedure

1. Set I_D limit to 2.2 A, I_G limit to 10 mA
2. Apply -5 V to V_G (Combine all V_G 's together)
3. Apply + 20 V to V_D (Combine all V_D 's together)
4. Adjust V_G until $I_{DQ} = 280$ mA ($V_G \sim -3$ V Typ.)
5. Apply RF signal

Bias Down Procedure

1. Turn off RF signal
2. Reduce V_G to -5 V; ensure I_{DQ} is approx. 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Assembly Drawing



Notes:

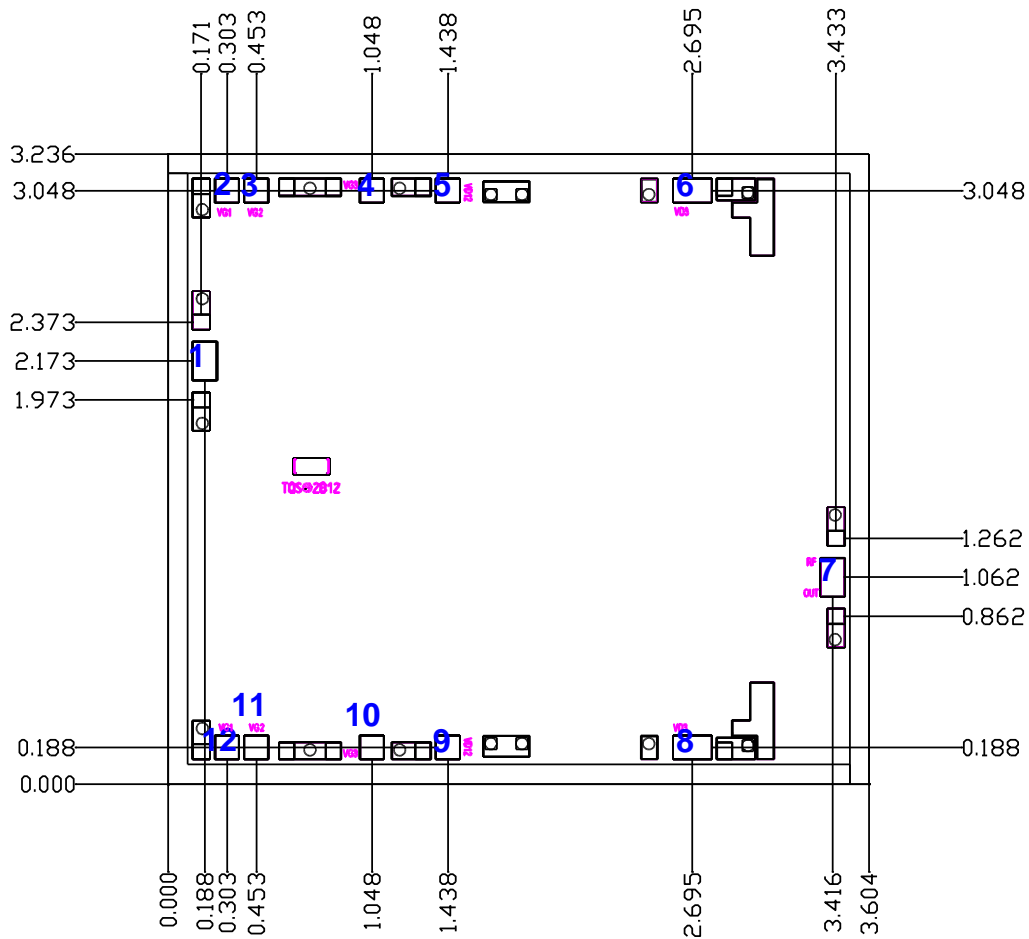
Amplifier must be biased from both sides.

Minimize RF wirebond lengths to achieve optimum return loss. Options in order of preference are:

1. Short w = 5mil ribbon bonds
2. Multiple short wedge or chisel bonds
3. Multiple ball bonds

Each set of chip capacitor 100 pF//0.01 uF (total 8 sets) can be replaced by one Presidio chip capacitor MVB3030x103M2H5C1F (RoHS compliant version).

Mechanical Drawing



Unit: millimeters
 Thickness: 0.10
 Die x, y size tolerance: ± 0.050
 Chip edge to bond pad dimensions are shown to center of pad
 Ground is backside of die

Bond Pad Description

Pad No.	Symbol	Pad Size	Description
1	RF In	0.125 x 0.200	Input; matched to 50 Ω ; DC blocked.
2, 12	V_{G1}	0.125 x 0.125	Gate voltage, V_{G1} top and bottom. Bias network is required; must be biased from both sides; see Application Circuit on page 9 as an example.
3, 11	V_{G2}	0.125 x 0.125	Gate voltage, V_{G2} top and bottom. Bias network is required; must be biased from both sides; see Application Circuit on page 9 as an example.
4, 10	V_{G3}	0.125 x 0.125	Gate voltage, V_{G1} top and bottom. Bias network is required; must be biased from both sides; see Application Circuit on page 9 as an example.
5, 9	V_{D12}	0.125 x 0.125	Drain voltage, V_{D12} top and bottom. Bias network is required; must be biased from both sides; see Application Circuit on page 9 as an example.
6, 8	V_{D3}	0.200 x 0.125	Drain voltage, V_{D3} top and bottom. Bias network is required; must be biased from both sides; see Application Circuit on page 9 as an example.
7	RF Out	0.125 x 0.200	Output; matched to 50 Ω ; DC blocked.

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment (i.e. epoxy) can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3–4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.