

### Product Description

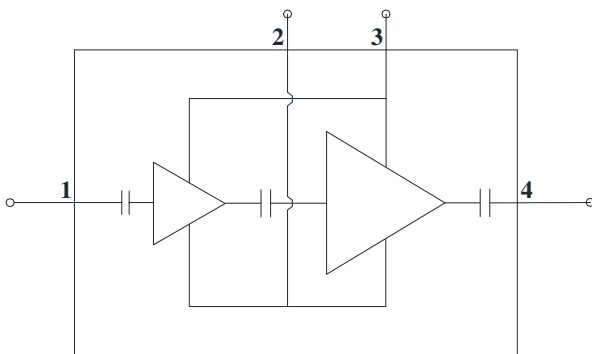
Qorvo's QPA1003D is a wideband high power MMIC amplifier fabricated on Qorvo's production 0.15um GaN on SiC process (QGaN15). The QPA1003D operates from 1 – 8 GHz and typically provides 10 W saturated output power with power-added efficiency of 30% and large-signal gain of 25 dB. This combination of wideband performance provides the flexibility designers are looking for to improve system performance while reducing size and cost.

The QPA1003D is matched to 50Ω with integrated DC blocking capacitors on both RF I/O ports simplifying system integration. The wideband performance makes it ideally suited in support of test instrumentation and electronic warfare, as well as, supporting multiple radar and communication bands.

The QPA1003D is 100% DC and RF tested on-wafer to ensure compliance to electrical specifications.

Lead-free and RoHS compliant.  
Evaluation boards are available upon request.

### Functional Block Diagram



### Product Features

- Frequency Range: 1 – 8 GHz
- P<sub>OUT</sub>: 40 dBm @ P<sub>IN</sub> = 15 dBm
- PAE: 30 % @ P<sub>IN</sub> = 15 dBm
- Large Signal Gain: 25 dB @ P<sub>IN</sub> = 15dBm
- Small Signal Gain: 30 dB
- Bias: V<sub>D</sub> = +28 V, I<sub>DQ</sub> = 650 mA, V<sub>G</sub> = -2.2 V Typical
- Chip Dimensions: 3.3 x 3.55 x 0.10 mm
- Process Technology: QGaN15

*Performance is typical across frequency. Please reference electrical specification table and data plots for more details.*

### Applications

- Electronic Warfare (EW)
- Radar
- Communications
- Test Instrumentation

### Ordering Information

Part No.	ECCN	Description
QPA1003D	3A001.b.2.b.1	1 – 8 GHz 10 W GaN Power Amplifier



## Electrical Specifications

Test conditions unless otherwise noted: 25 °C,  $V_D = +28\text{ V}$ ,  $I_{DQ} = 650\text{ mA}$ ,  $V_G = -2.2\text{ V}$  Typical, CW.

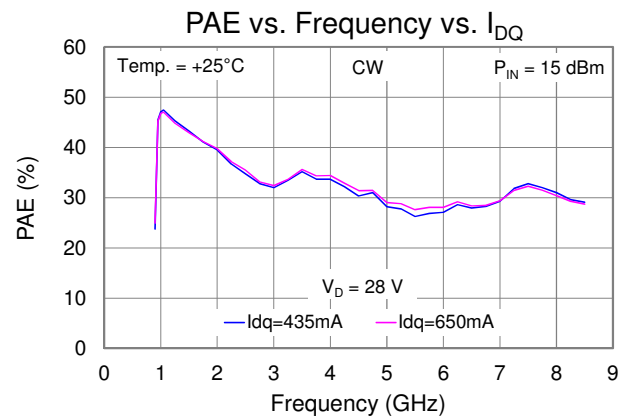
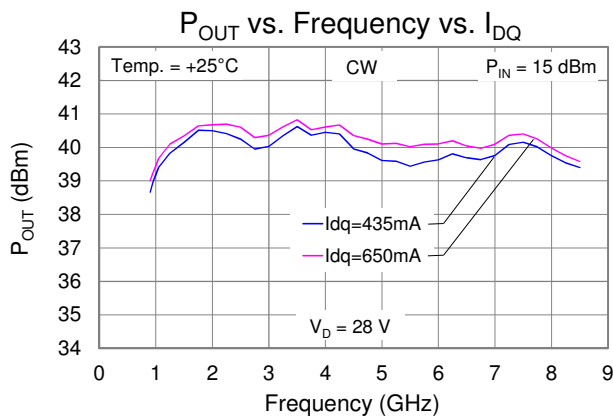
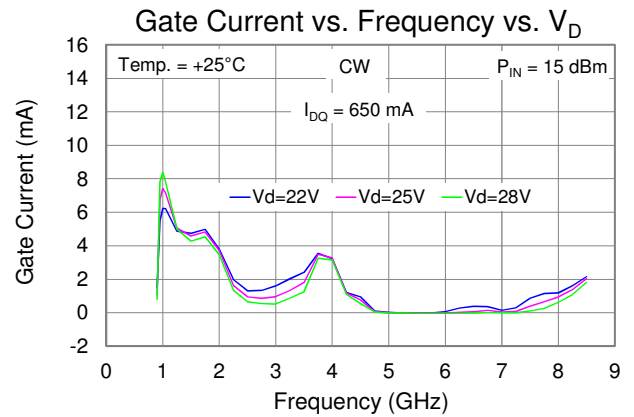
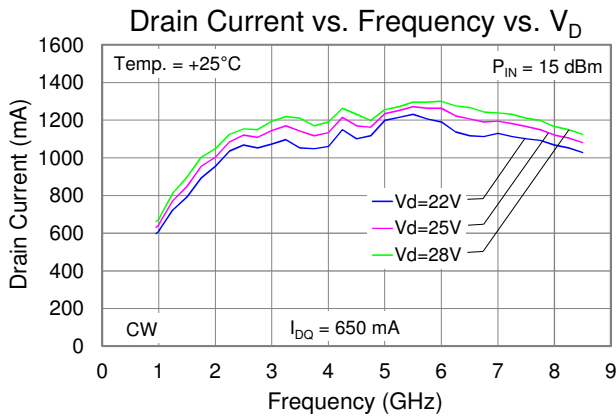
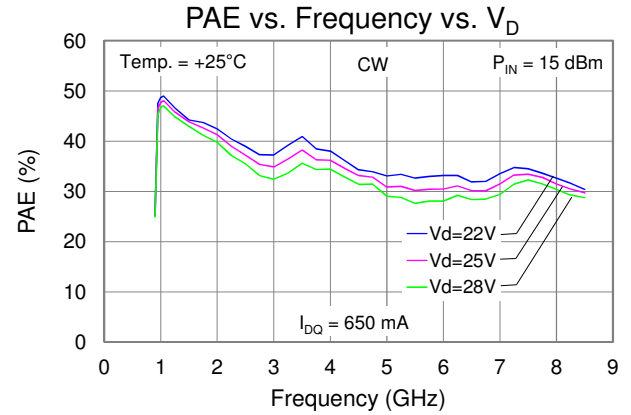
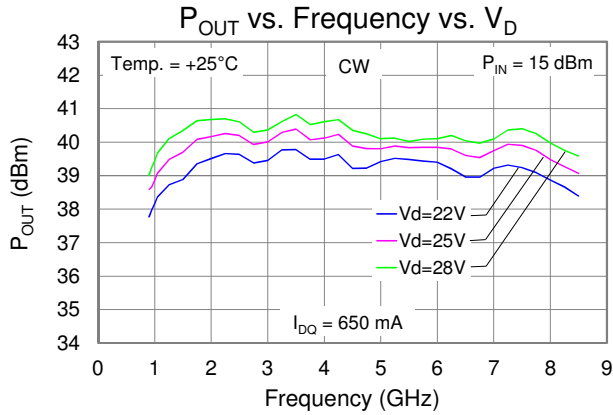
Parameter	Min	Typ	Max	Units
Operational Frequency Range	1	–	8	GHz
Output Power @ $P_{IN} = 15\text{ dBm}$	Frequency = 1 GHz	39.4	–	dBm
	Frequency = 4 GHz	40.6	–	
	Frequency = 8 GHz	40	–	
Power Added Efficiency @ $P_{IN} = 15\text{ dBm}$	Frequency = 1 GHz	46.8	–	%
	Frequency = 4 GHz	34.4	–	
	Frequency = 8 GHz	30.4	–	
Small Signal Gain	Frequency = 1 GHz	31.5	–	dB
	Frequency = 4 GHz	32.6	–	
	Frequency = 8 GHz	31	–	
Input Return Loss	Frequency = 1 GHz	13.2	–	dB
	Frequency = 4 GHz	14.7	–	
	Frequency = 8 GHz	14.4	–	
Output Return Loss	Frequency = 1 GHz	16.7	–	dB
	Frequency = 4 GHz	11	–	
	Frequency = 8 GHz	21	–	
Small Signal Gain Temperature Coefficient	–	-0.04	–	dB/°C
Output Power Temperature Coefficient	–	-0.012	–	dBm/°C

## Recommended Operating Conditions

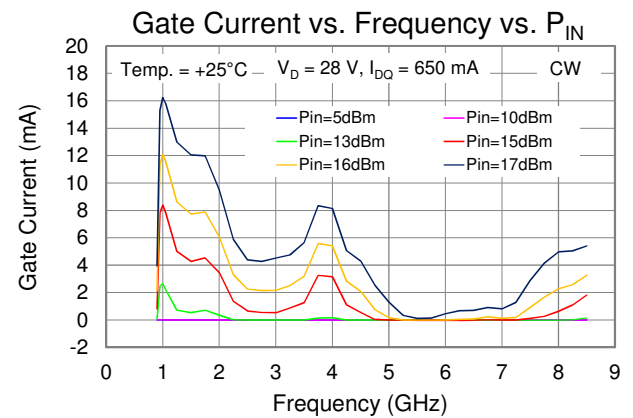
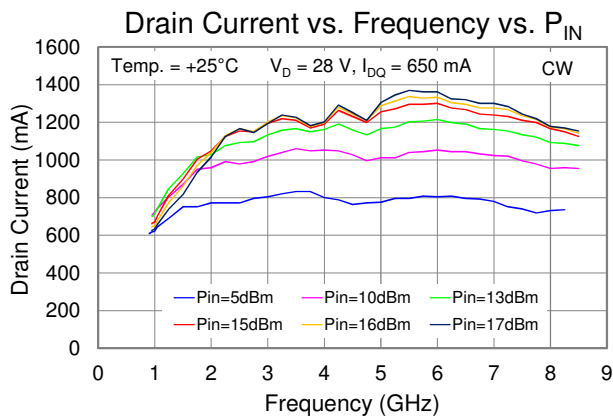
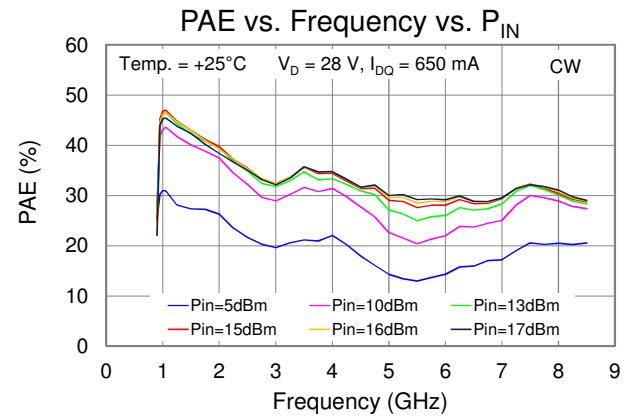
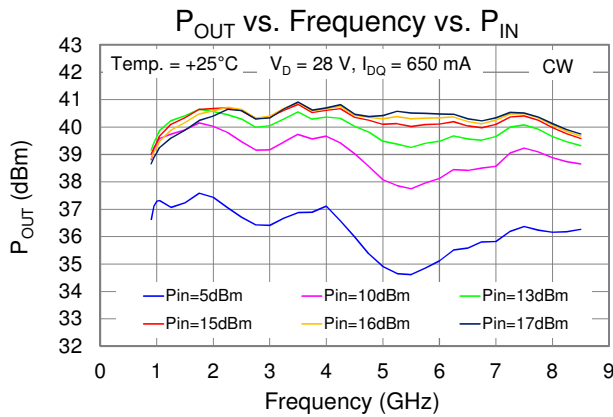
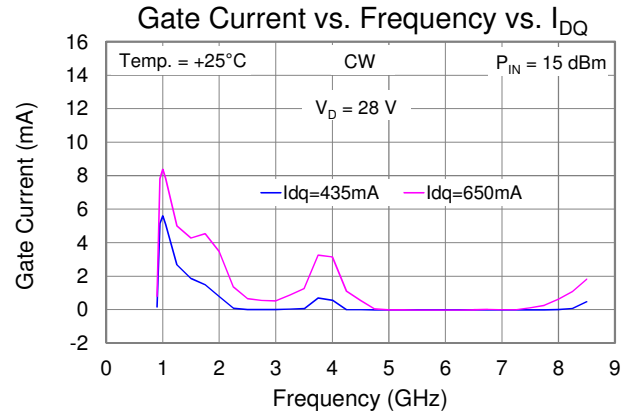
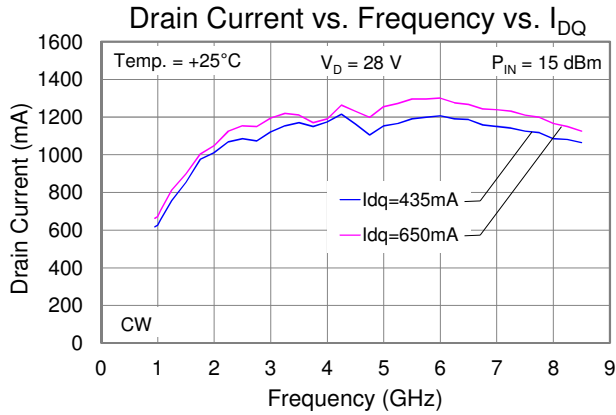
Parameter	Value / Range
Drain Voltage ( $V_D$ )	+28 V
Drain Current ( $I_{DQ}$ )	650 mA
Gate Voltage ( $V_G$ )	-2.2 V (Typ.)
Temperature ( $T_{BASE}$ )	-40 to 85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

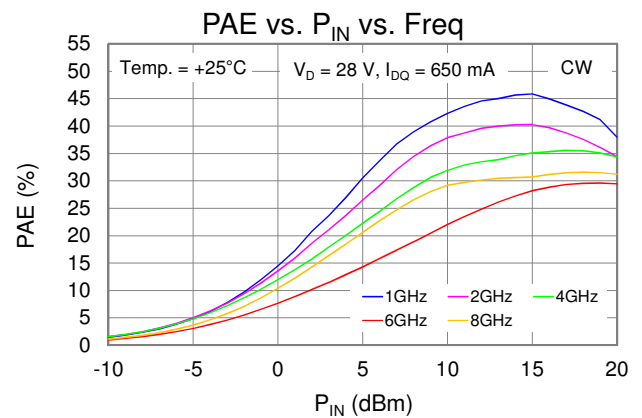
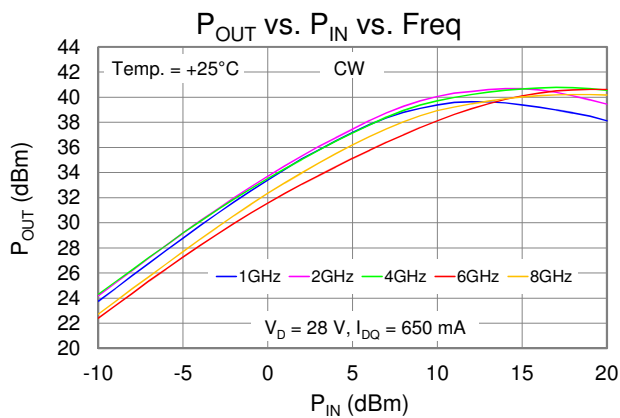
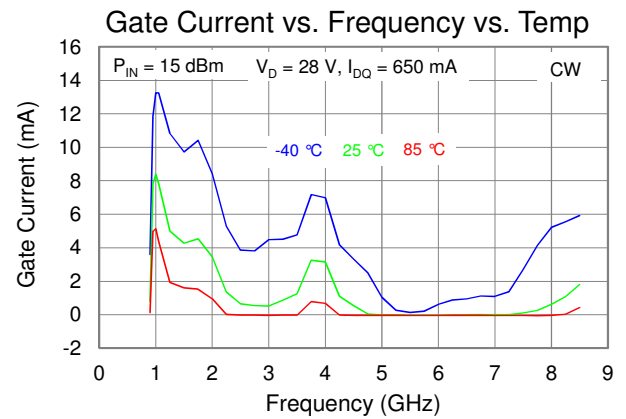
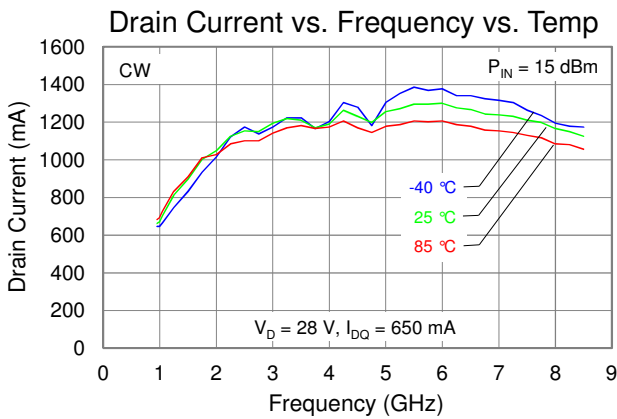
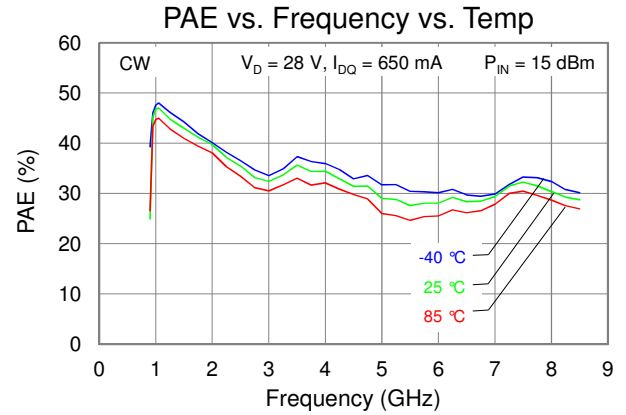
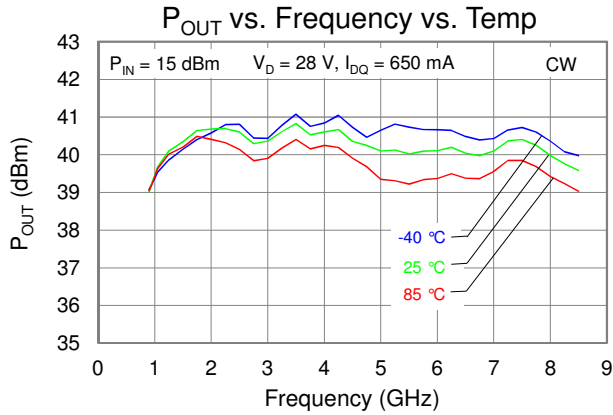
### Performance Plots – Large Signal (CW)



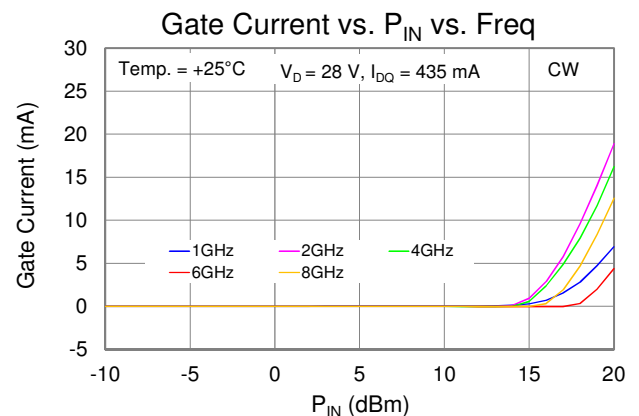
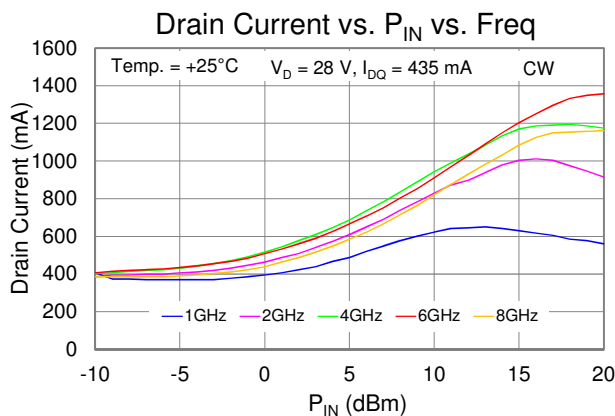
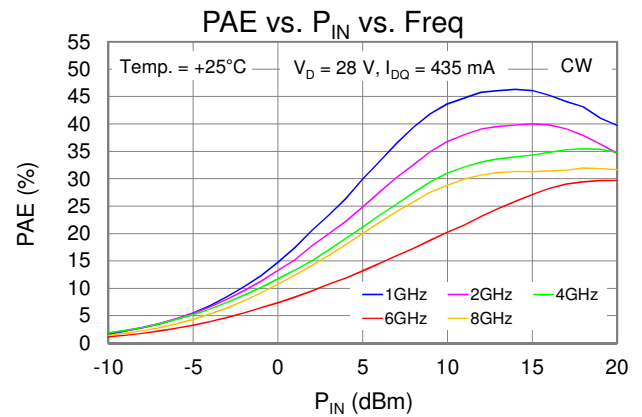
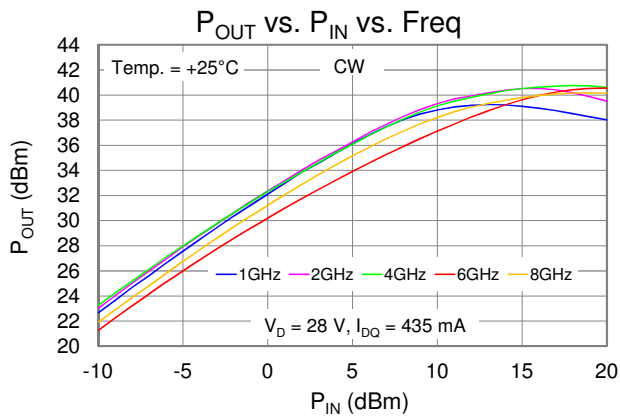
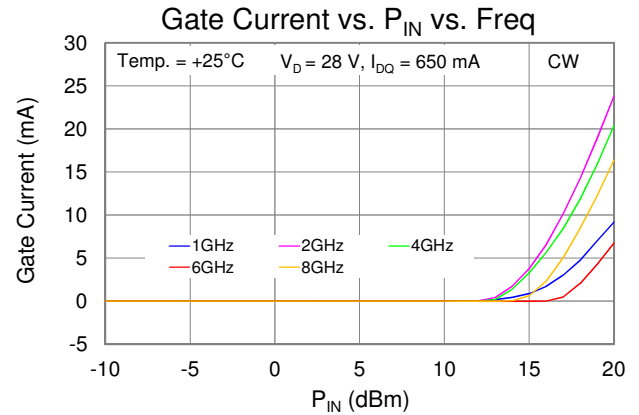
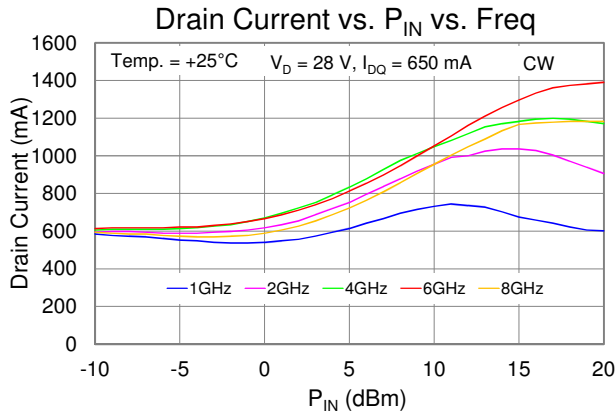
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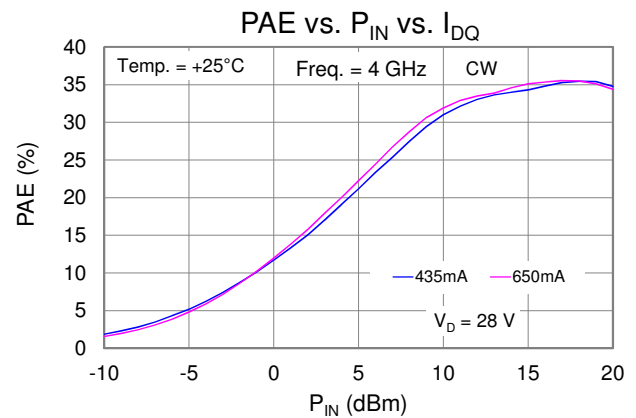
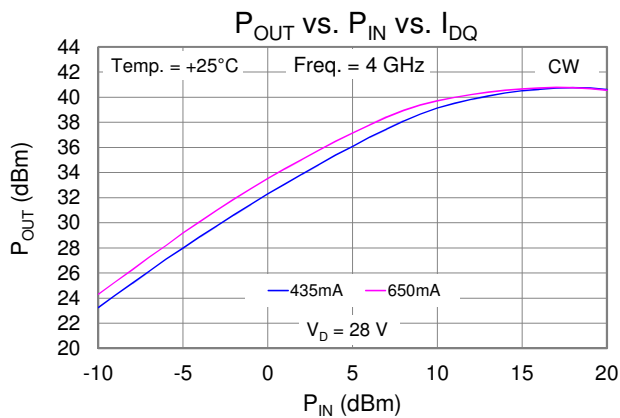
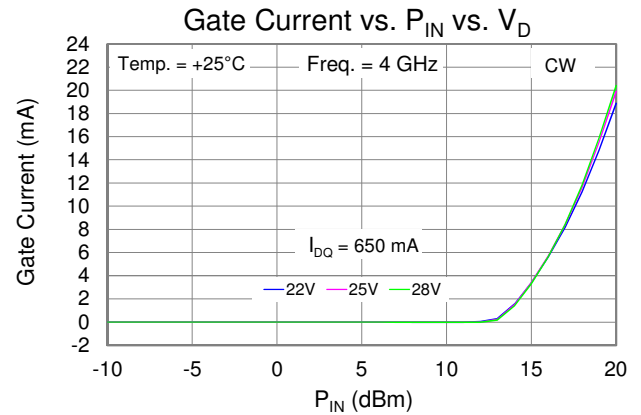
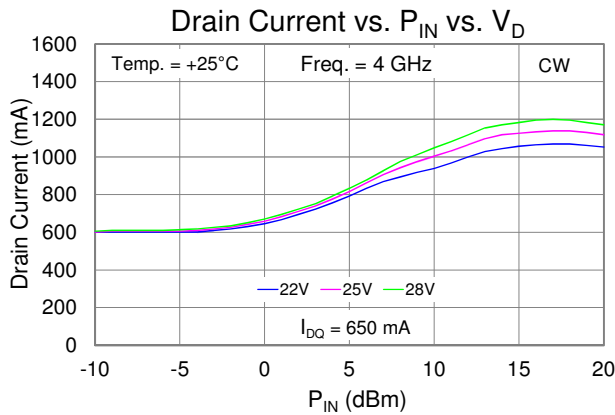
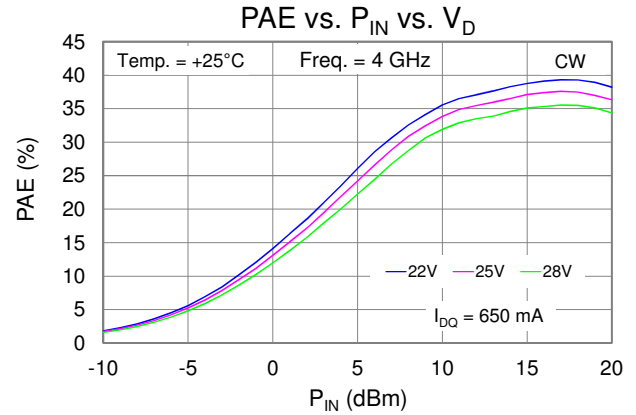
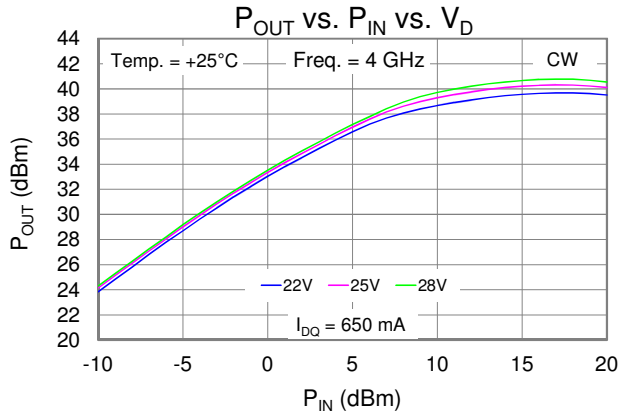
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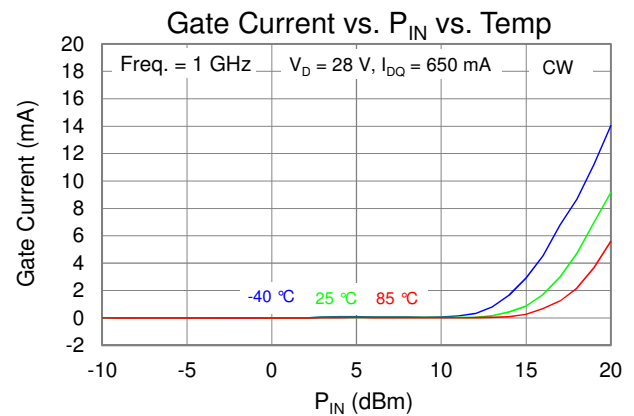
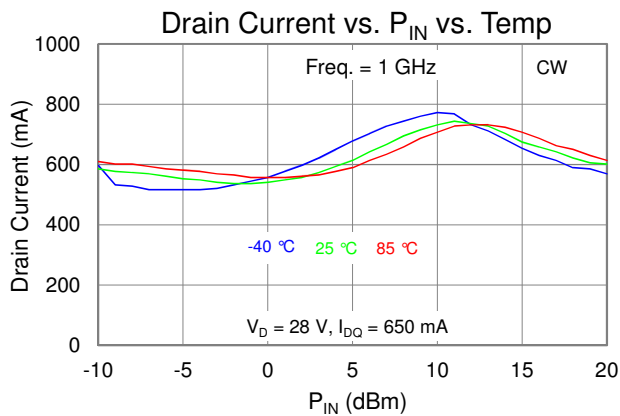
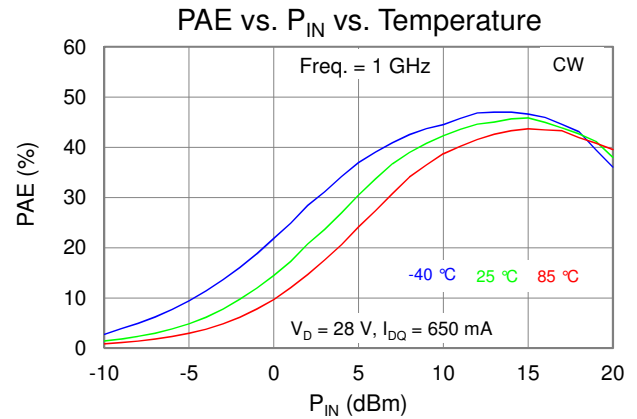
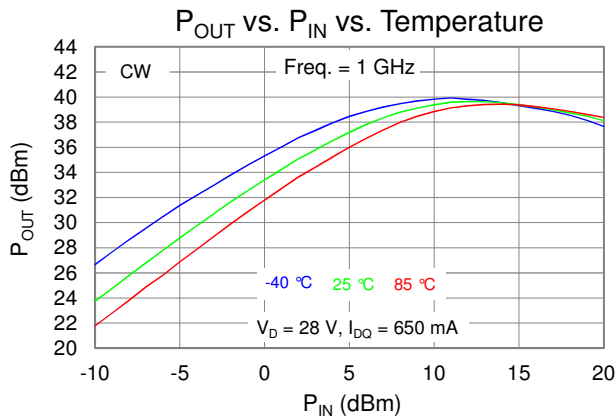
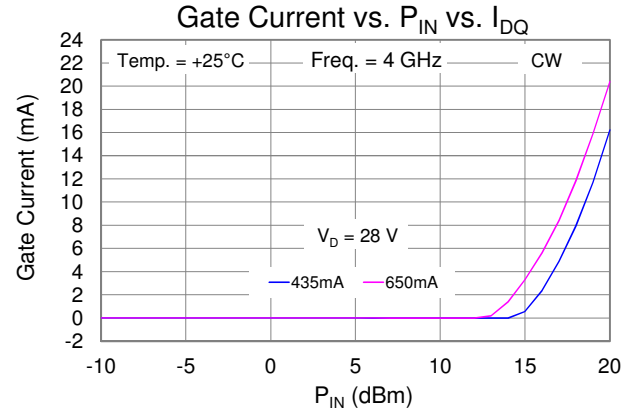
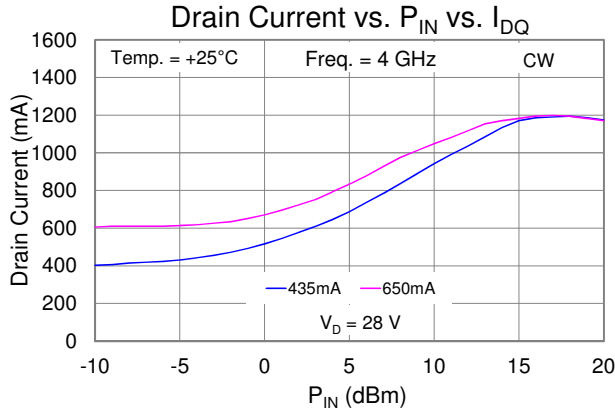
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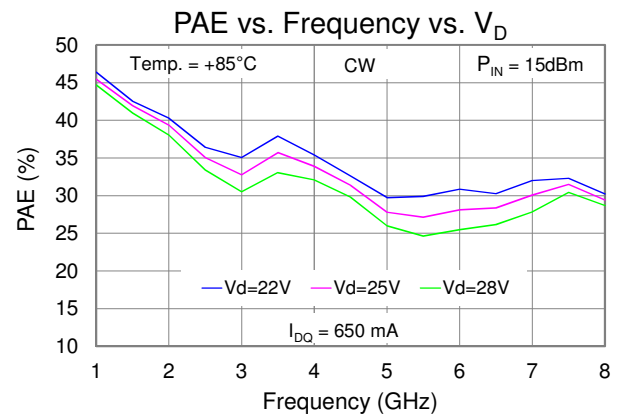
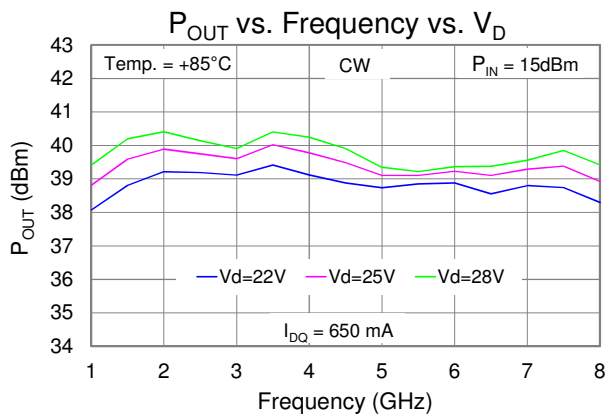
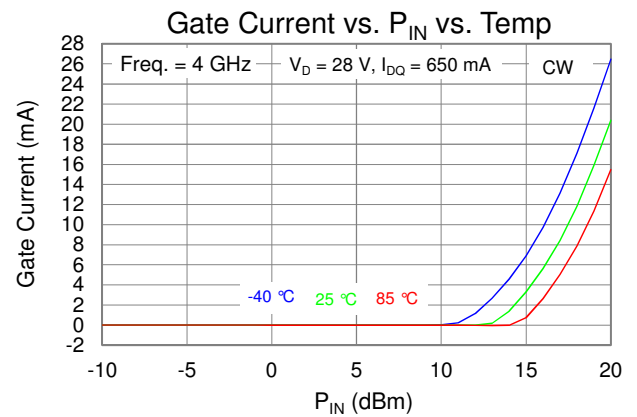
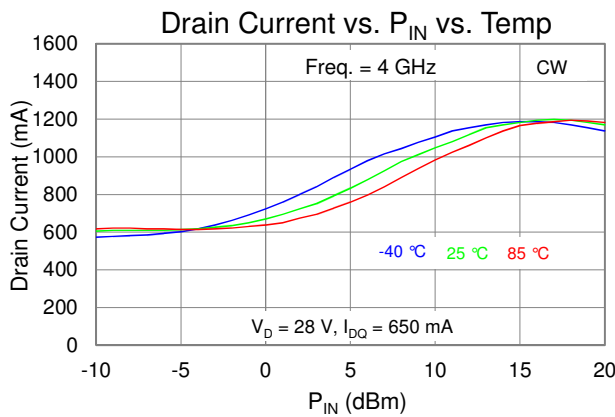
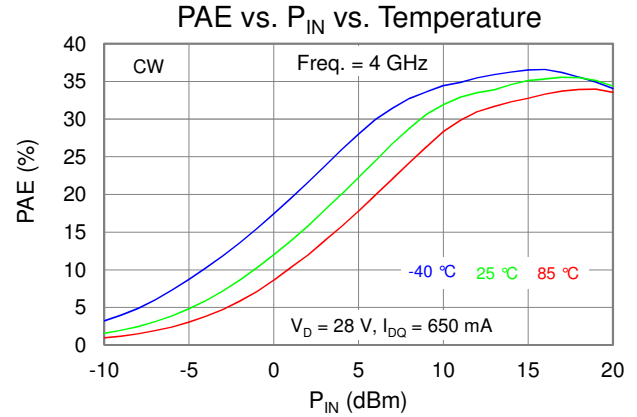
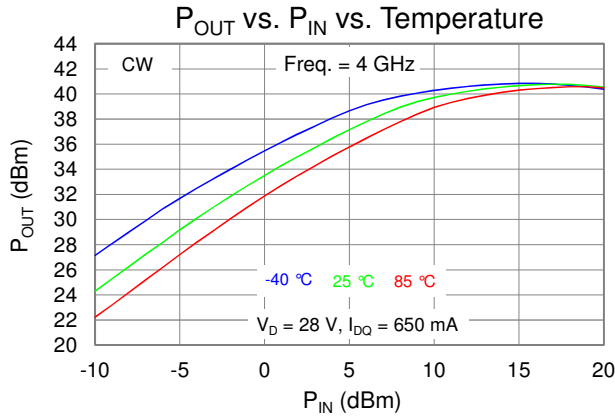


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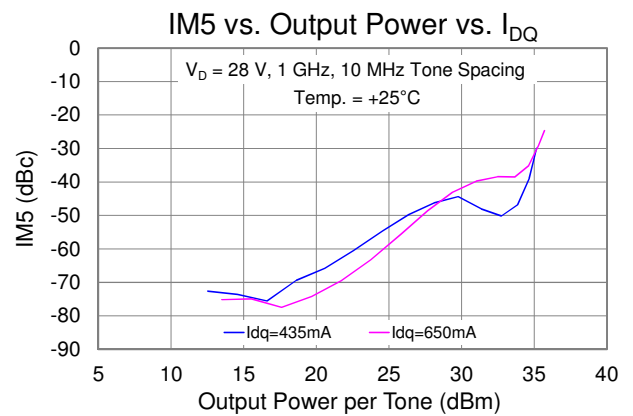
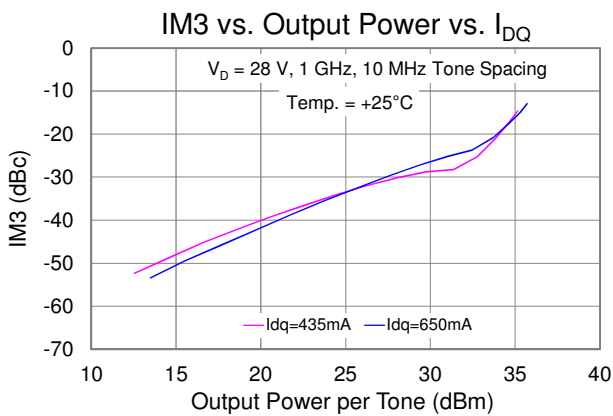
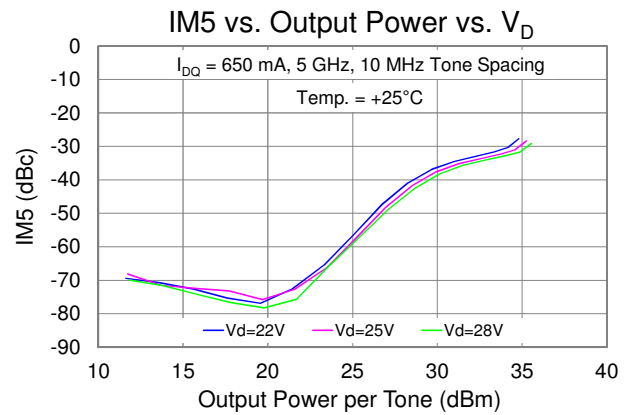
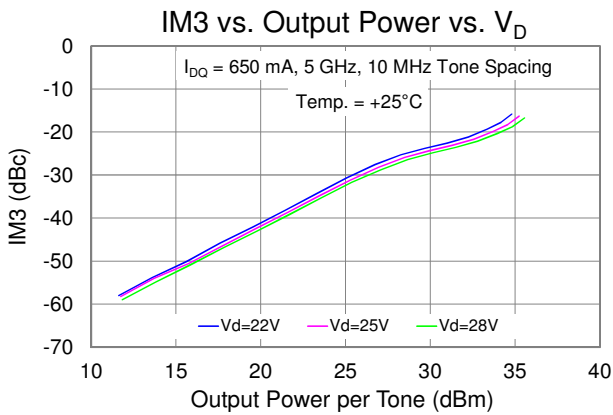
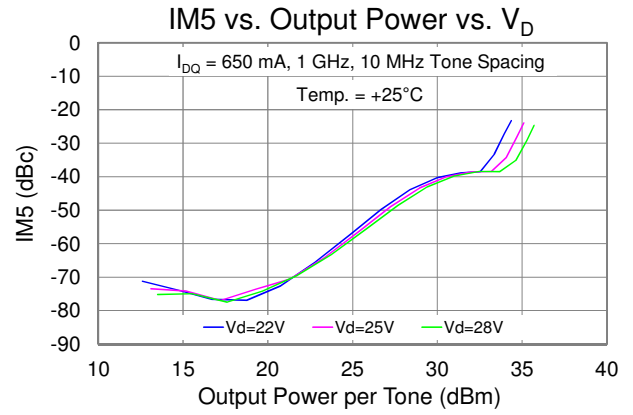
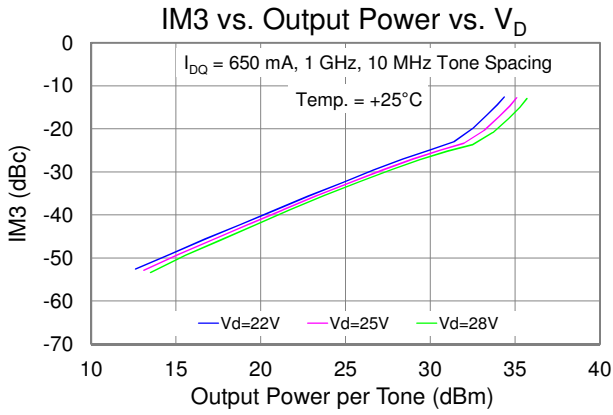




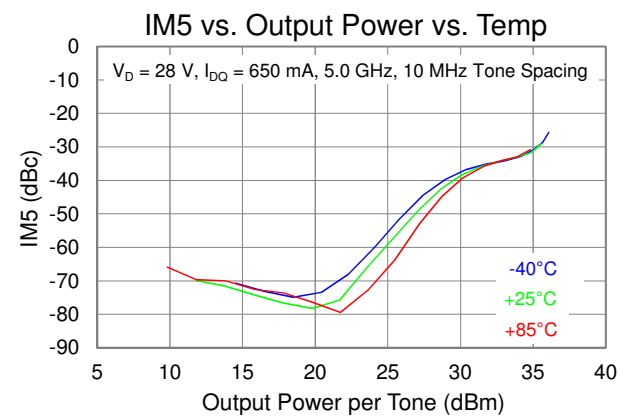
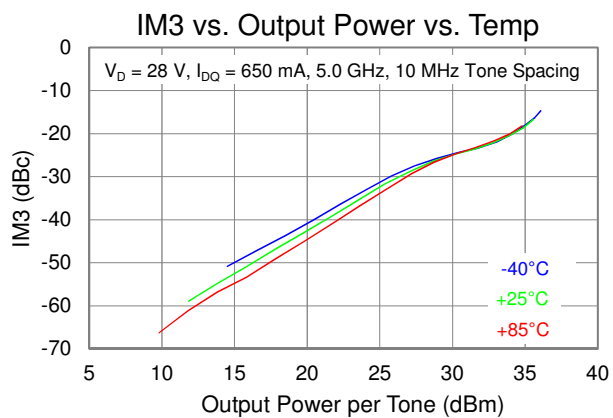
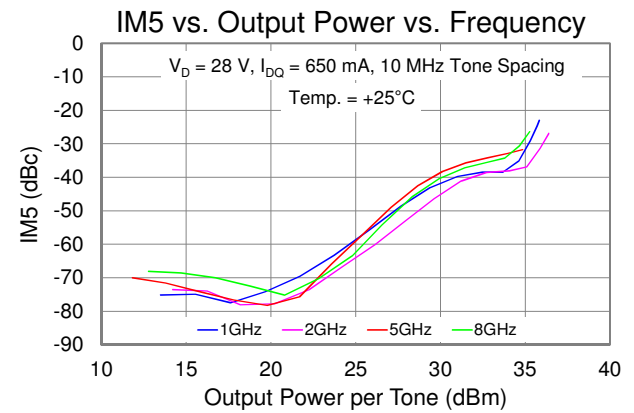
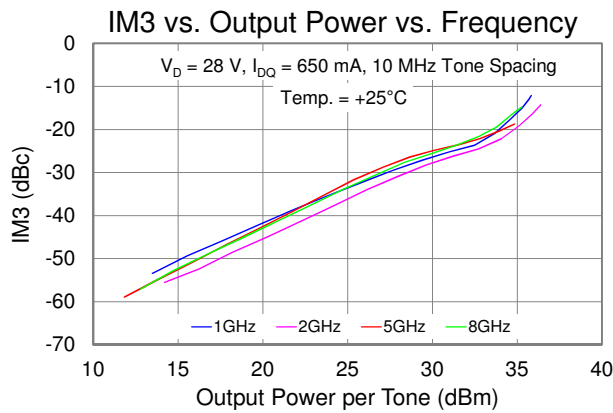
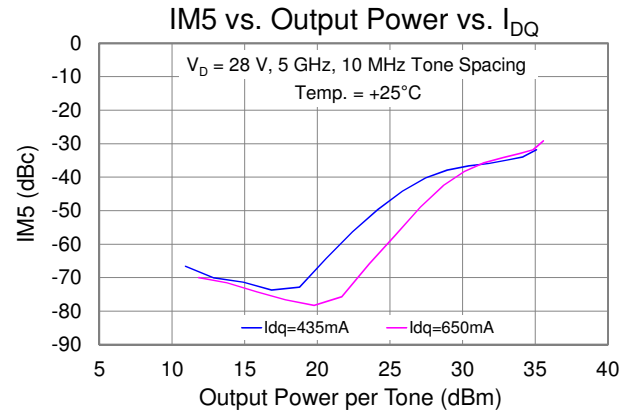
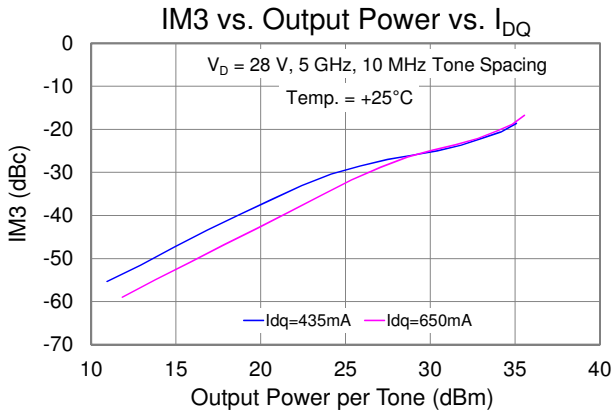
### Performance Plots – Large Signal (CW)



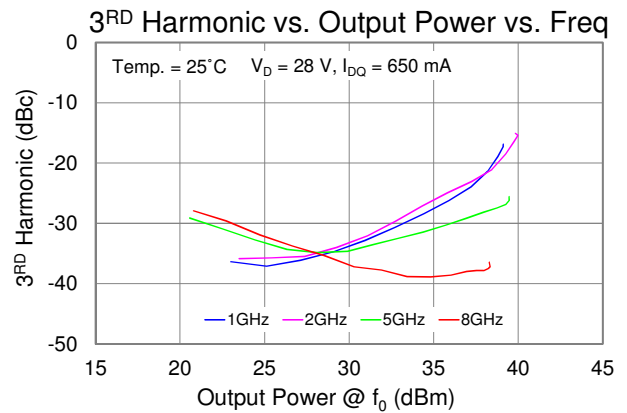
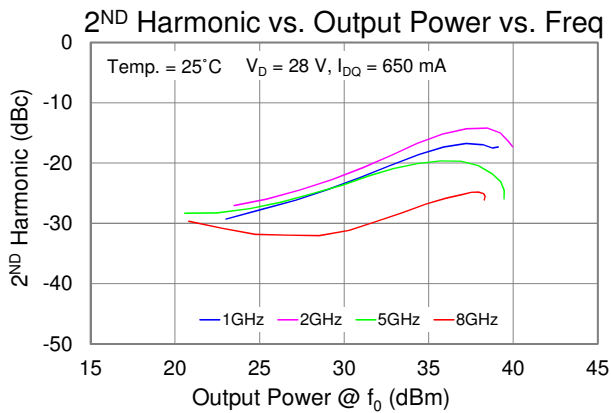
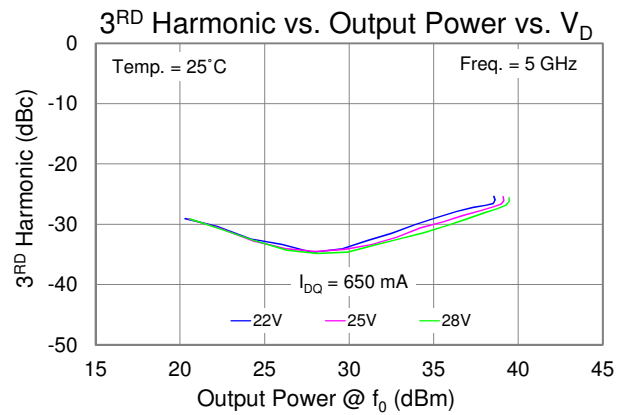
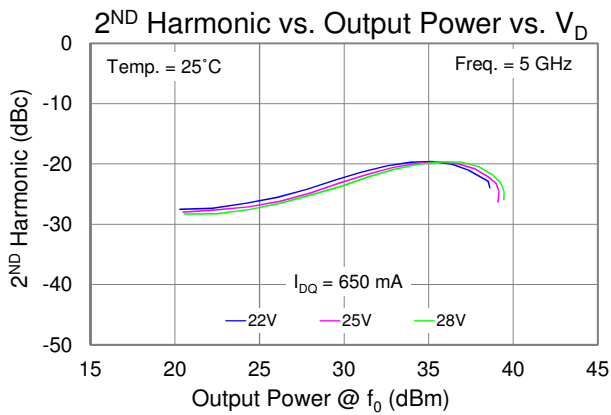
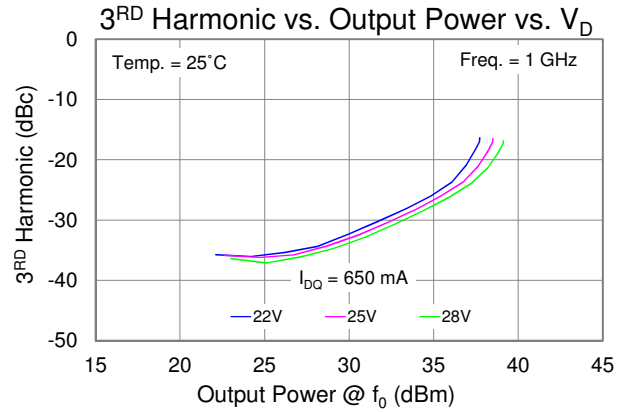
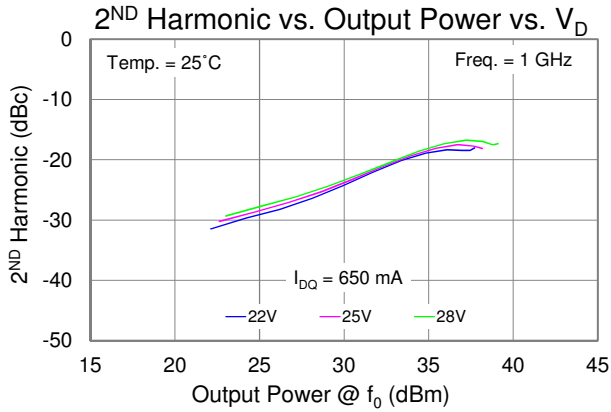
### Performance Plots – Linearity



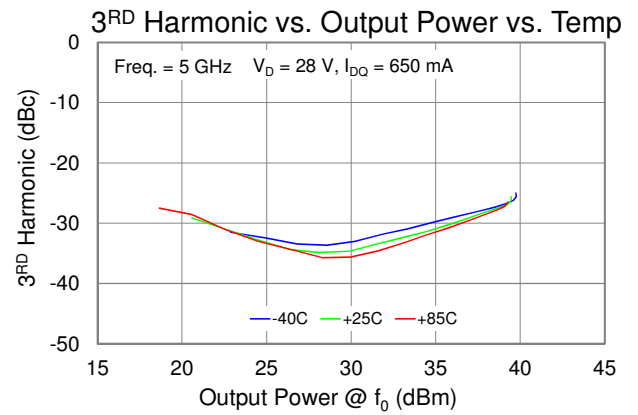
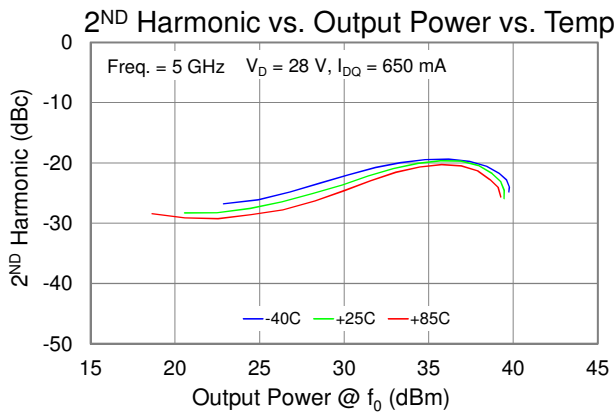
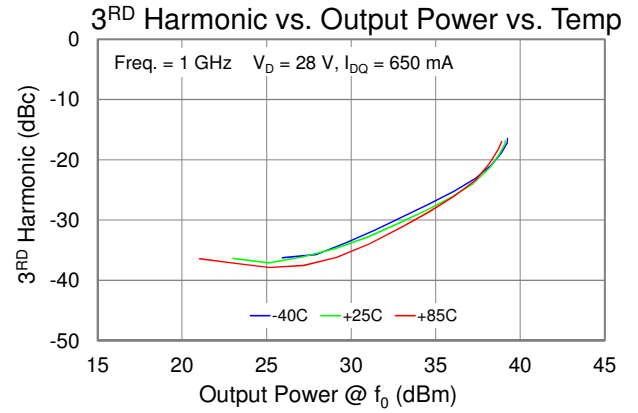
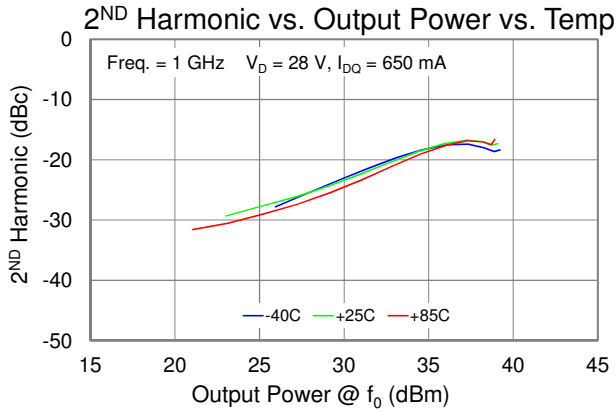
### Performance Plots – Linearity



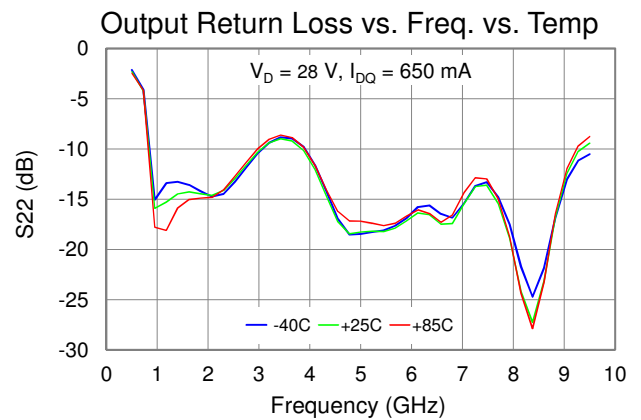
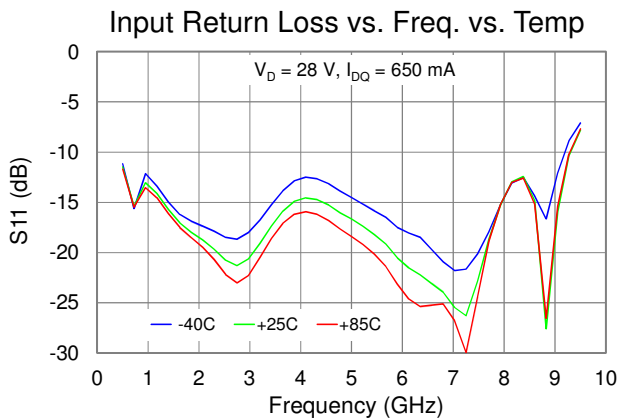
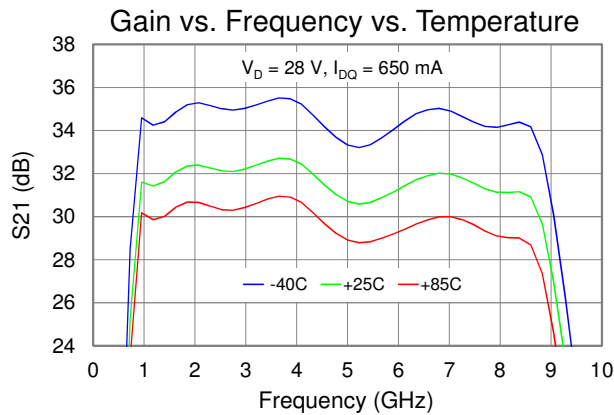
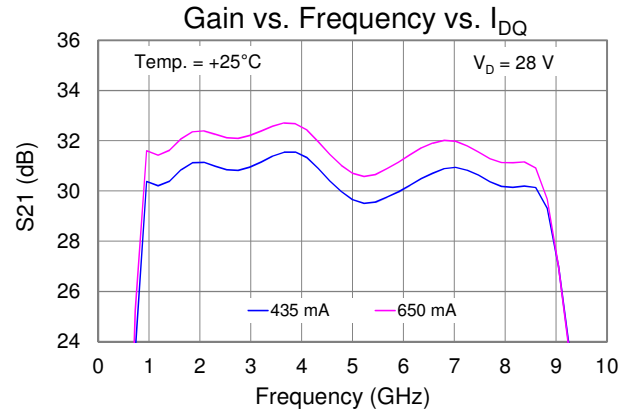
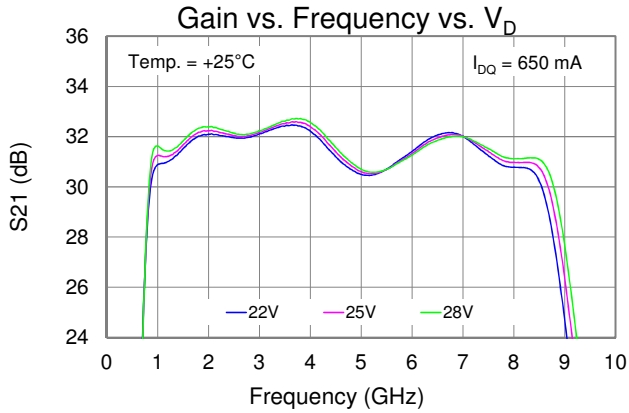
**Performance Plots – Linearity**



**Performance Plots – Linearity**



### Performance Plots – Small Signal



### Thermal and Reliability Information

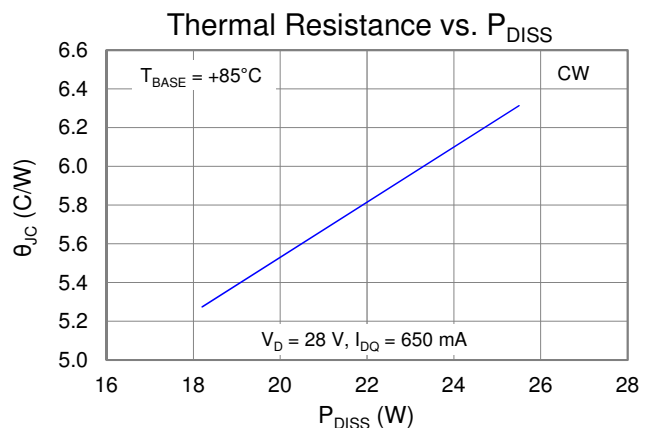
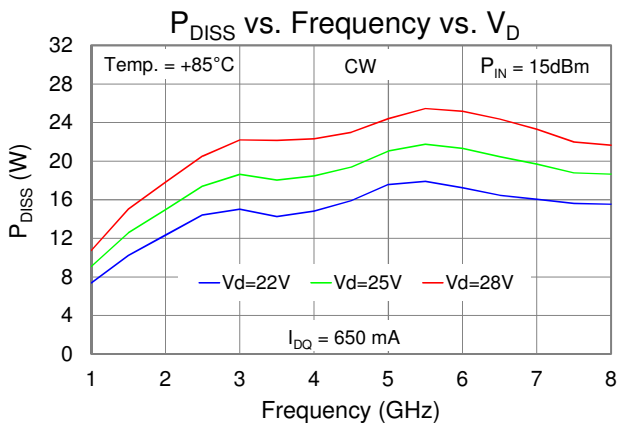
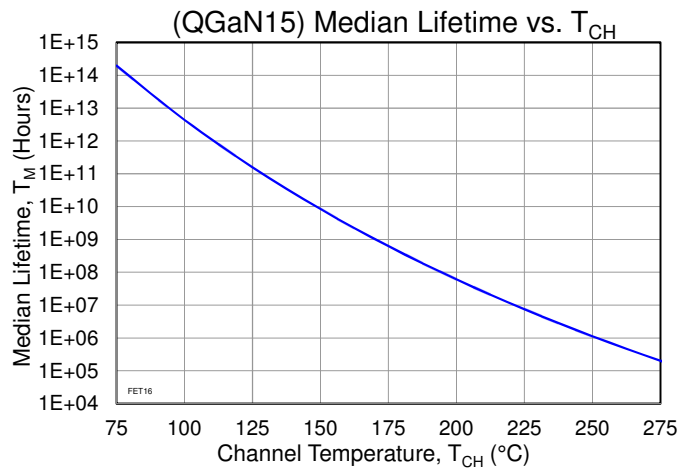
Parameter	Test Conditions	Value	Units
Thermal Resistance ( $\theta_{JC}$ ) <sup>(1)</sup>	$T_{BASE} = 85^\circ\text{C}$ , $V_D = +28\text{ V}$ (CW) At $I_{DQ} = 650\text{ mA}$ , $P_{DISS} = 18.2\text{ W}$	5.28	$^\circ\text{C/W}$
Channel Temperature ( $T_{CH}$ ) (Quiescent)		181	$^\circ\text{C}$
Median Lifetime ( $T_M$ )		3.5E+8	Hrs
Thermal Resistance ( $\theta_{JC}$ ) <sup>(1)</sup>	$T_{BASE} = 85^\circ\text{C}$ , $V_D = +25\text{ V}$ (CW) At Freq = 5.5 GHz, $P_{IN} = 15\text{ dBm}$ : $I_{DQ} = 650\text{ mA}$ , $I_{D\_Drive} = 1.2\text{ A}$ $P_{OUT} = 39\text{ dBm}$ , $P_{DISS} = 22\text{ W}$	6.05	$^\circ\text{C/W}$
Channel Temperature ( $T_{CH}$ ) (Under RF drive)		218	$^\circ\text{C}$
Median Lifetime ( $T_M$ )		1.3E+7	Hrs
Thermal Resistance ( $\theta_{JC}$ ) <sup>(1)</sup>	$T_{BASE} = 85^\circ\text{C}$ , $V_D = +28\text{ V}$ (CW) At Freq = 5.5 GHz, $P_{IN} = 15\text{ dBm}$ : $I_{DQ} = 650\text{ mA}$ , $I_{D\_Drive} = 1.2\text{ A}$ $P_{OUT} = 39\text{ dBm}$ , $P_{DISS} = 25.5\text{ W}$	6.31	$^\circ\text{C/W}$
Channel Temperature ( $T_{CH}$ ) (Under RF drive)		246	$^\circ\text{C}$
Median Lifetime ( $T_M$ )		1.5E+6	Hrs

**Notes:**

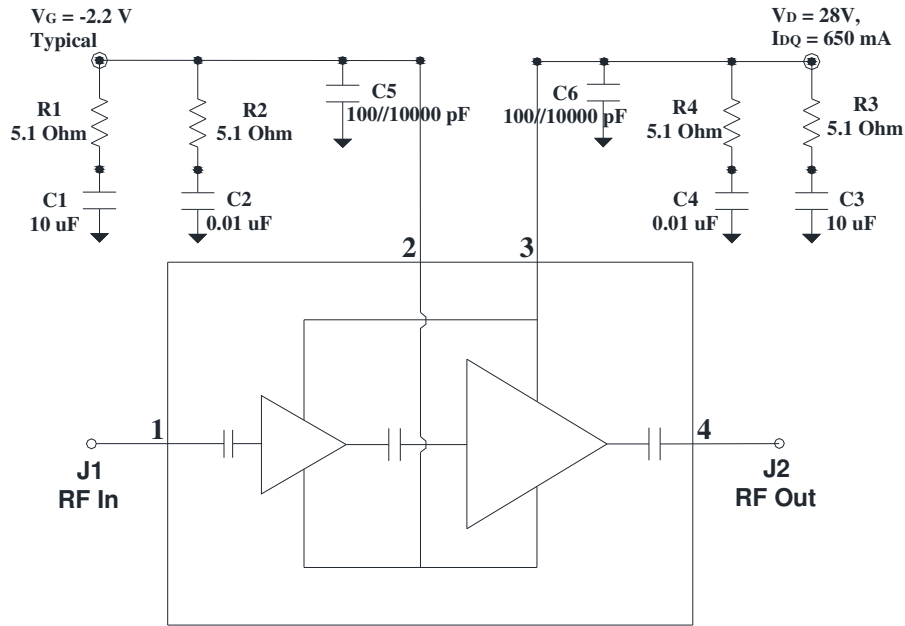
- Thermal resistance measured to back of carrier plate. MMIC mounted to 20 mil CuMo (75/25) carrier using 1.5 mil AuSn.

### Median Lifetime

Test Conditions:  $V_D = +28\text{ V}$ ; Failure Criteria = 10% reduction in  $I_{D\_MAX}$  during DC Life Testing



**Applications Information and Pad Layout**



**Bias Up Procedure**

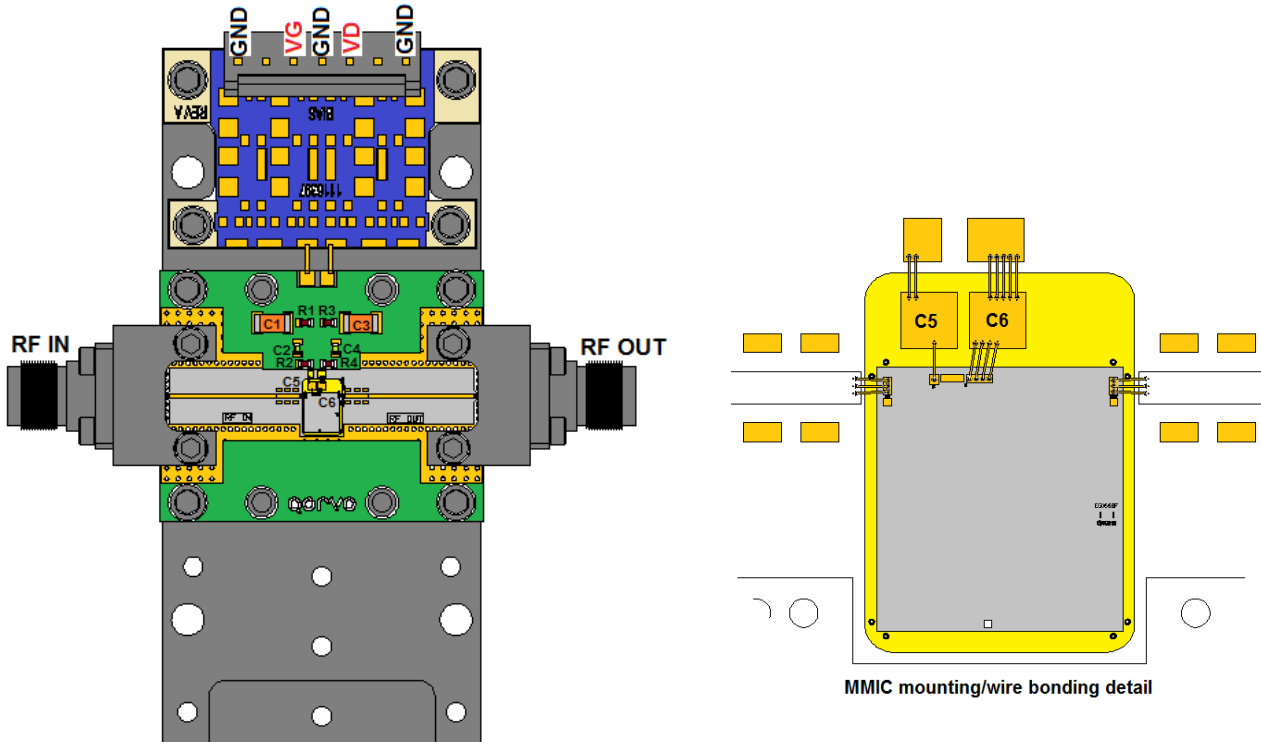
1. Set  $I_D$  limit to 1.3 A,  $I_G$  limit to 6 mA
2. Apply  $-5\text{ V}$  to  $V_G$
3. Apply  $+28\text{ V}$  to  $V_D$ ; ensure  $I_{DQ}$  is approx. 0 mA
4. Adjust  $V_G$  until  $I_{DQ} = 650\text{ mA}$  ( $V_G \sim -2.2\text{ V Typ.}$ ).
5. Turn on RF supply

**Bias Down Procedure**

1. Turn off RF supply
2. Reduce  $V_G$  to  $-5\text{ V}$ ; ensure  $I_{DQ}$  is approx. 0 mA
3. Set  $V_D$  to 0 V
4. Turn off  $V_D$  supply
5. Turn off  $V_G$  supply



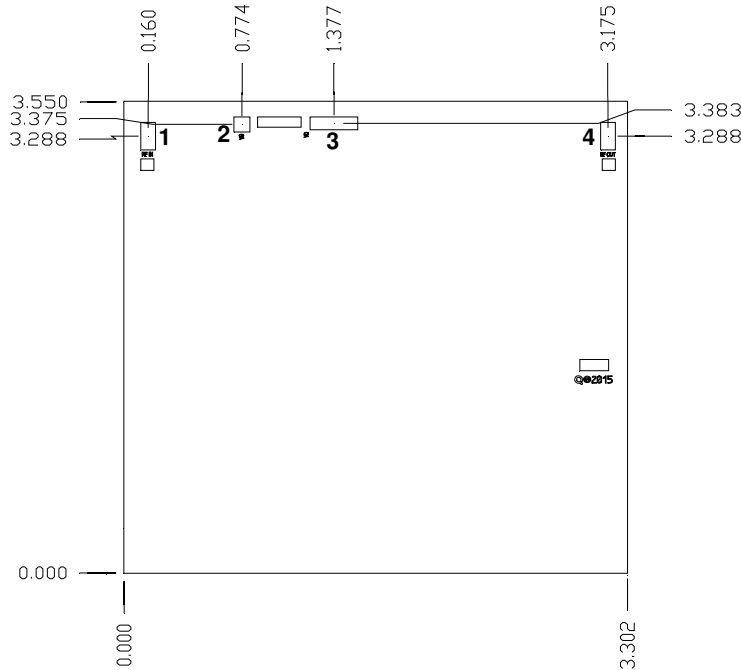
**Evaluation Board (EVB) Layout Assembly**



**Bill of Materials**

Reference Des.	Value	Description	Manuf.	Part Number
C1, C3	10 $\mu$ F	Cap, 1205, 50 V, 20 %, X7R	Various	–
C2, C4	0.01 $\mu$ F	Cap, 0402, 50 V, 10 %, X5R	Various	–
C5, C6	100pF/10000 pF	Cap, 30 x 30, 50V, Single Layer	Various	–
R1, R2, R3, R4	5.1 Ohm	Res, 0402, 50 V, 5 %	Various	–

**Mechanical Information**



Units: millimeters  
 Thickness: 0.10  
 Die x,y size tolerance:  $\pm 0.050$   
 Ground is backside of die

**Bond Pad Description**

Pad No.	Symbol	Pad Size (mm)	Description
1	RF In	0.097 x 0.207	RF Input; matched to 50 $\Omega$ , DC blocked
2	VG	0.105 x 0.112	Gate voltage, bias network is required; see Application Circuit on page 16 as an example.
3	VD	0.312 x 0.096	Drain voltage, bias network is required; see Application Circuit on page 16 as an example.
4	RF Out	0.097 x 0.207	RF Output; matched to 50 $\Omega$ , DC blocked

## Assembly Notes

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Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment (i.e. epoxy) can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3–4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

### Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage ( $V_D$ )	+29.5 V
Gate Voltage Range ( $V_G$ )	-8 to 0 V
Drain Current	1300 mA
Forward Gate Current ( $I_G$ )	See $I_{G\_MAX}$ plot
Power Dissipation ( $P_{DISS}$ ), 85 °C, CW	30 W
Input Power, CW, 50 $\Omega$ , ( $P_{IN}$ ), $V_D = +28$ V, $I_{DQ} = 650$ mA, 85 °C,	18 dBm
Input Power, CW, VSWR 3:1, ( $P_{IN}$ ) $V_D = +28$ V, $I_{DQ} = 650$ mA, 85 °C	18 dBm
Channel Temperature ( $T_{CH}$ )	275 °C
Mounting Temperature (30 Seconds)	260 °C
Storage Temperature	-55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

