TGA2214-CP

2 – 18 GHz 4 W GaN Power Amplifier

Product Description

Qorvo's TGA2214-CP is a packaged wideband power amplifier fabricated on Qorvo's QGaN15 0.15 µm GaN on SiC process. Operating from 2 to 18 GHz, the TGA2214-CP generates > 4 W saturated output power with a power-added efficiency of > 15 %, and > 14 dB large signal gain across the entire operational band.

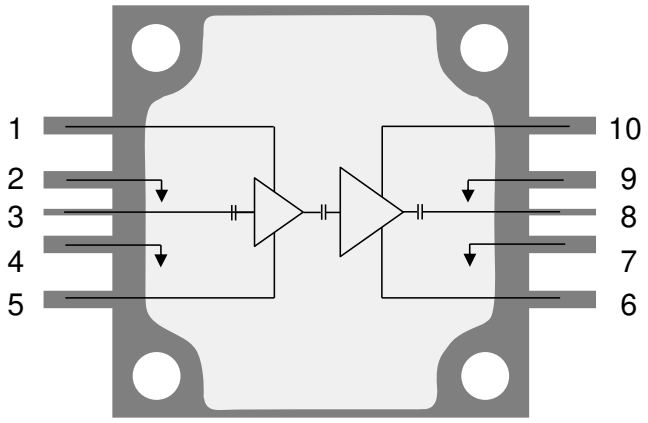
The TGA2214-CP is offered in a 10-lead 15 x 15 mm bolt-down package. The package has a pure Cu base, offering superior thermal management. The TGA2214-CP is ideally suited to support, both in the commercial and the defense arenas, applications requiring either wideband or multi-band frequency performance.

Both RF ports have integrated DC blocking capacitors and are fully matched to 50 Ohms.

Lead free and RoHS compliant.

Evaluation Boards are available upon request.

Functional Block Diagram



Product Features

- Frequency Range: 2 – 18 GHz
- P_{OUT}: > 36 dBm at P_{IN} = 23 dBm
- PAE: > 15 % CW at P_{IN} = 23 dBm
- Small Signal Gain: > 22 dB
- IM3: < –17 dBc at 30 dBm P_{OUT} / Tone
- Bias: V_D = +22 V, I_{DQ} = 600 mA, V_G = –2.3 V Typical
- Package Dimensions: 15.2 x 15.2 x 3.5 mm
- Package base is pure Cu offering superior thermal management

Applications

- Test Equipment
- Electronic Warfare
- Military and Commercial Radar

Ordering Information

Part No.	ECCN	Description
TGA2214-CP	3A001.b.2.c	2 – 18 GHz 4 W GaN Power Amplifier

Absolute Maximum Ratings

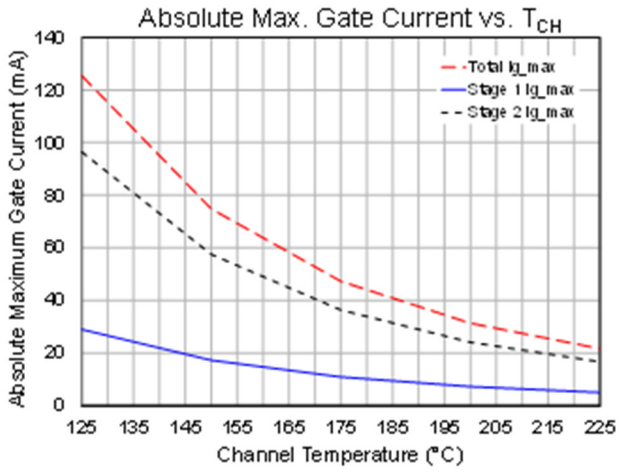
Parameter	Value / Range
Drain Voltage (V_D)	+29.5 V
Gate Voltage Range (V_G)	–5 to 0 V
Drain Current (I_D) 1st stage 2nd stage	 0.5 A 1.0 A
Forward Gate Current (I_G)	See graph this page
Power Dissipation (P_{DISS}), 85 °C	31 W
Input Power, CW, 50 Ω, (P_{IN})	31 dBm
Input Power, CW, VSWR 3:1, V_D = +30 V, 85 °C, (P_{IN})	31 dBm
Channel Temperature (T_{CH})	275 °C
Mounting Temperature (30 Seconds)	260 °C
Storage Temperature	–55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating

Parameter	Value / Range
Drain Voltage (V_D)	+22 V
Drain Current (I_{DQ})	600 mA
Drain Current Under RF Drive (I_{D_DRIVE})	See plots p. 7
Gate Voltage (V_G)	–2.3 V (Typ.)
Gate Current Under RF Drive (I_{G_DRIVE})	See plots p. 7
Temperature (T_{BASE})	–40 to 85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.



Electrical Specifications

Parameter	Min	Typ	Max	Units
Operational Frequency Range	2	–	18	GHz
Small Signal Gain	–	> 22	–	dB
Input Return Loss	–	> 8	–	dB
Output Return Loss	–	> 11	–	dB
Output Power at P_{IN} = 23 dBm	–	> 36	–	dBm
Power Added Efficiency at P_{IN} = 23 dBm	–	> 15	–	%
IM3 (P_{OUT} / Tone = 30 dBm/Tone)	–	< –17	–	dBc
IM5 (P_{OUT} / Tone = 30 dBm/Tone)	–	< –29	–	dBc
Small Signal Gain Temperature Coefficient	–	-0.04	–	dB/°C
Output Power Temperature Coefficient (25 to 85 °C)	–	–0.005	–	dBm/°C
Recommended Operating Voltage	–	+22	+22	V

Test conditions unless otherwise noted: 25 °C, V_D = +22 V, I_{DQ} = 600 mA, V_G = –2.3 V Typ, CW.

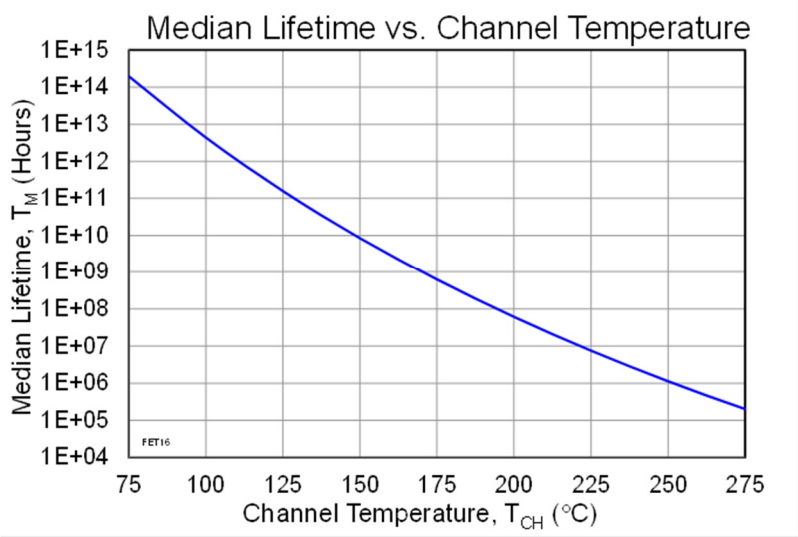
Thermal and Reliability Information

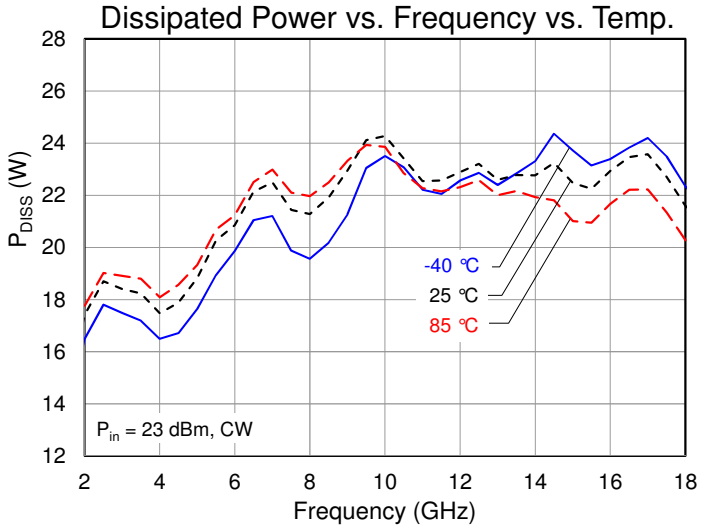
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85 °C, V_D = +22 V (CW) At Freq = 10 GHz, P_{IN} = 23 dBm: I_{DQ} = 600 mA, I_{D_Drive} = 1.3 A P_{OUT} = 37 dBm, P_{DISS} = 23.6 W	6.2	°C/W
Channel Temperature (T_{CH}) (Under RF drive)		232	°C
Median Lifetime (T_M)		4.4E+6	Hrs

Notes:
1. Thermal resistance measured to back of package.

Median Lifetime

Test Conditions: V_D = +28 V; Failure Criteria = 10 % reduction in ID_MAX

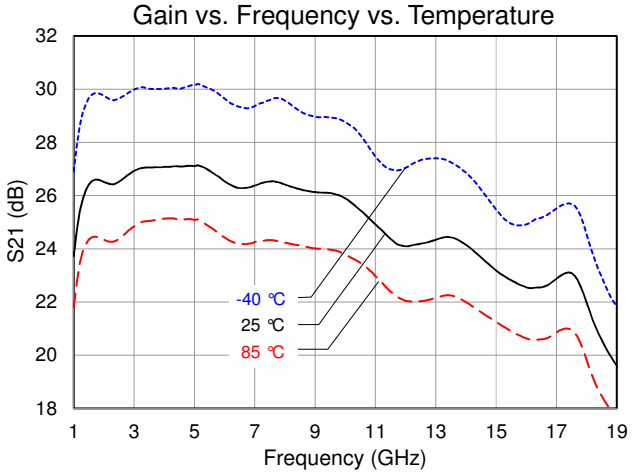




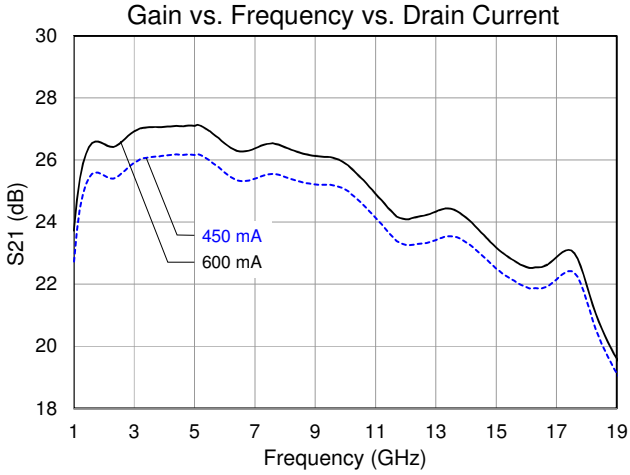
Performance Plots – Small Signal

Conditions unless otherwise specified: V_D = +22 V, I_{DQ} = 600 mA, V_G = –2.3 V Typical, CW.

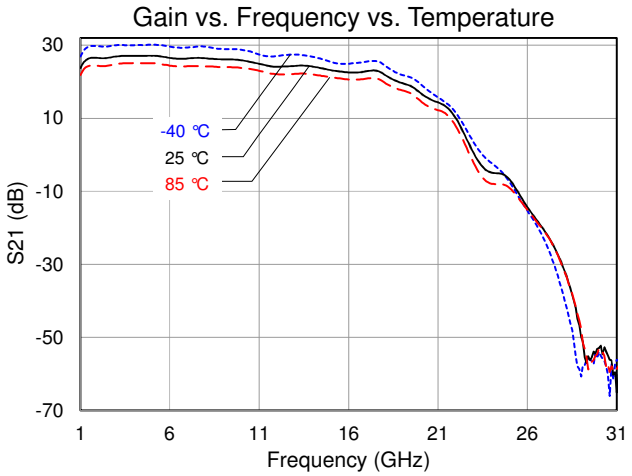
Gain vs. Frequency vs. Temperature



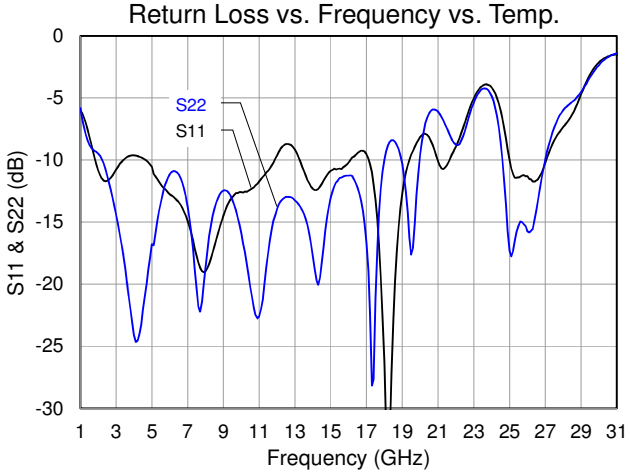
Gain vs. Frequency vs. Drain Current



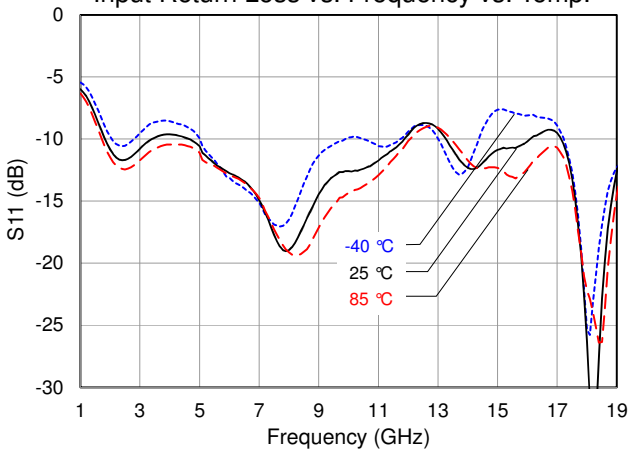
Gain vs. Frequency vs. Temperature



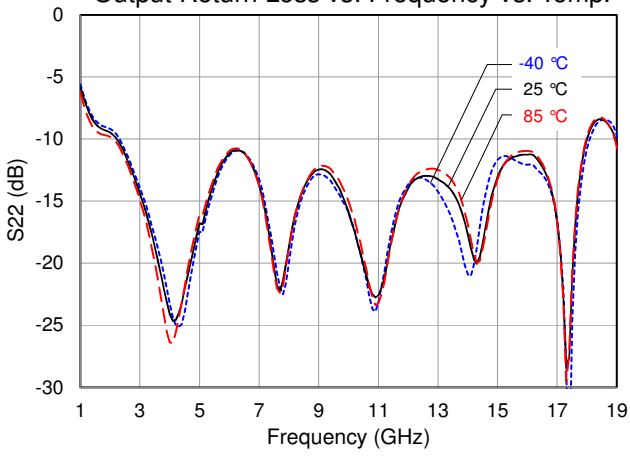
Return Loss vs. Frequency vs. Temp.



Input Return Loss vs. Frequency vs. Temp.

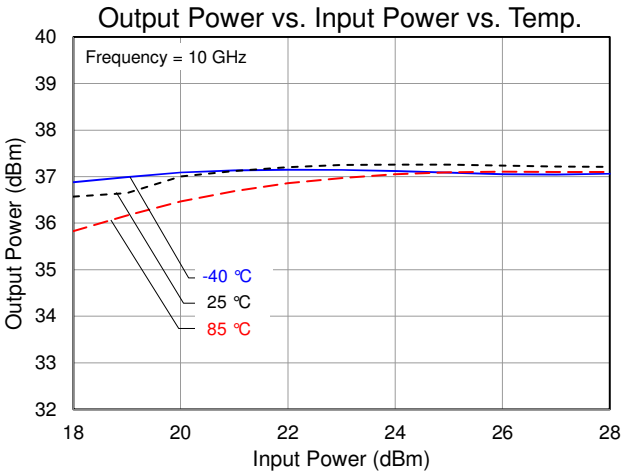


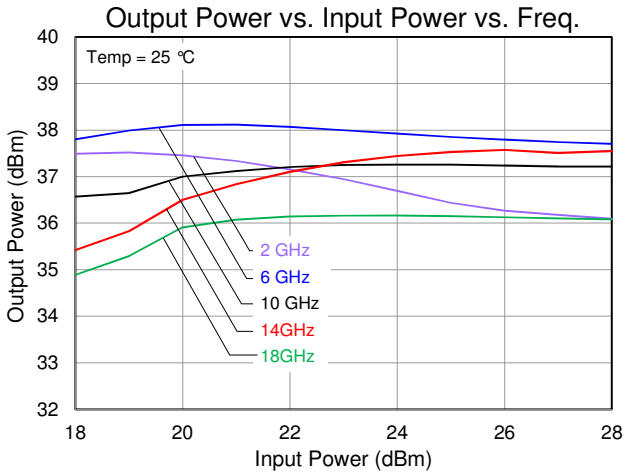
Output Return Loss vs. Frequency vs. Temp.

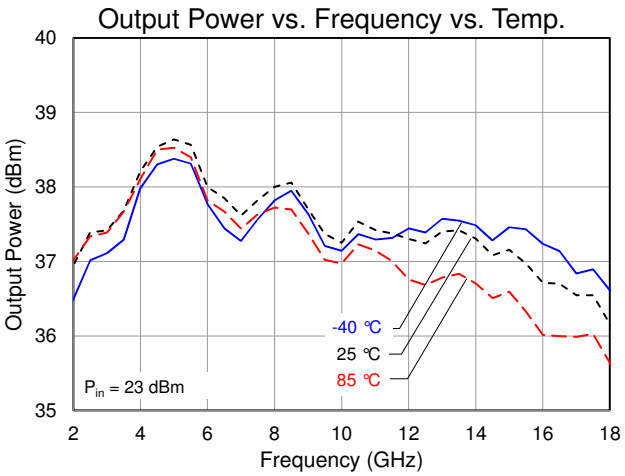


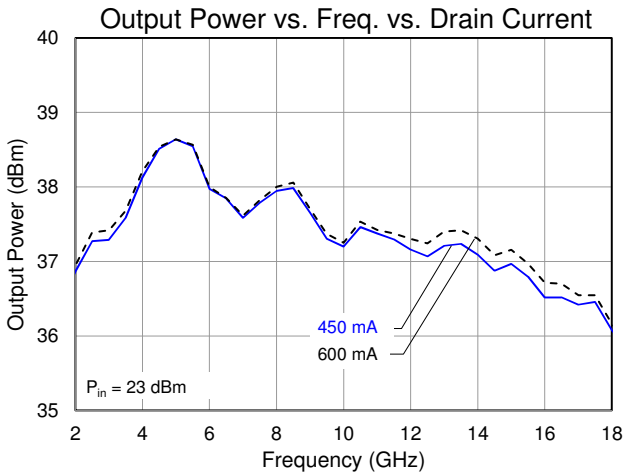
Performance Plots – Large Signal

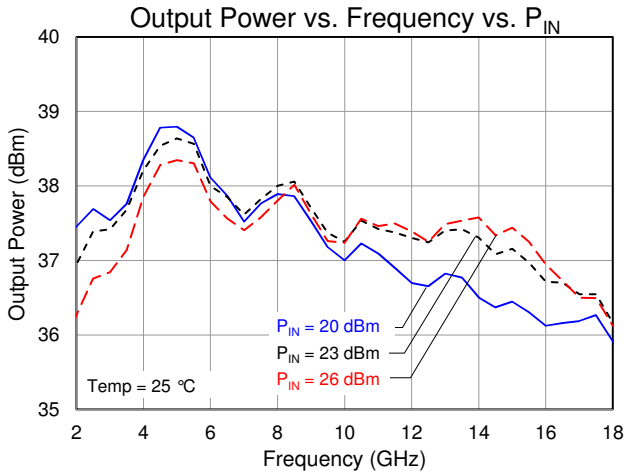
Conditions unless otherwise specified: V_D = +22 V, I_{DQ} = 600 mA, V_G = –2.3 V Typical, CW.







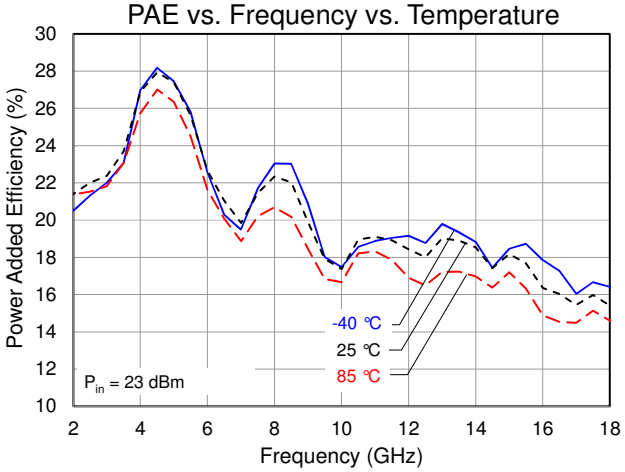




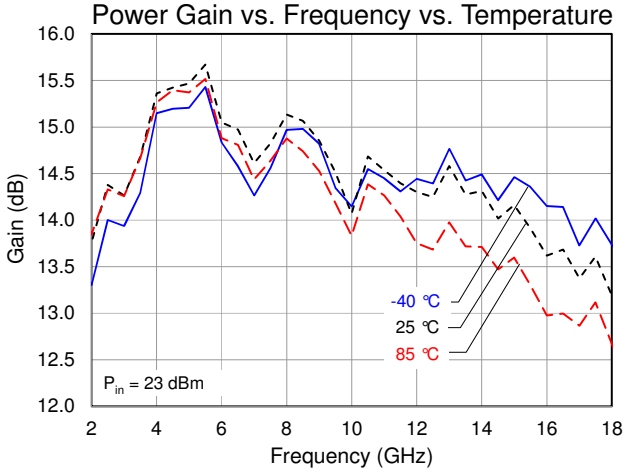
Performance Plots – Large Signal

Conditions unless otherwise specified: V_D = +22 V, I_{DQ} = 600 mA, V_G = –2.3 V Typical, CW.

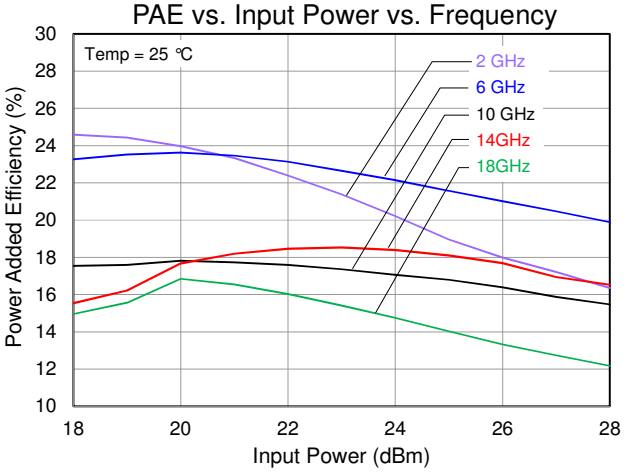
PAE vs. Frequency vs. Temperature



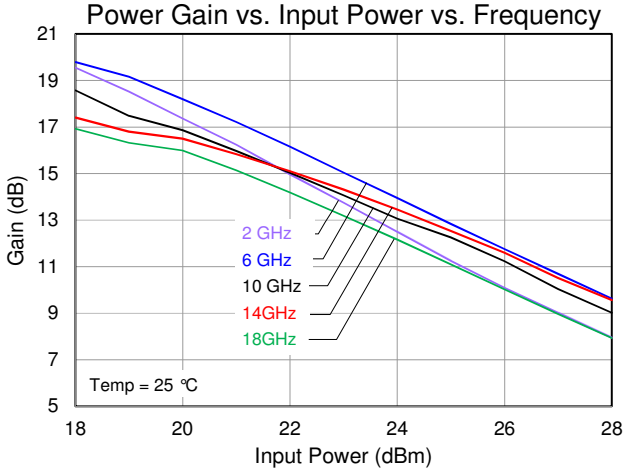
Power Gain vs. Frequency vs. Temperature



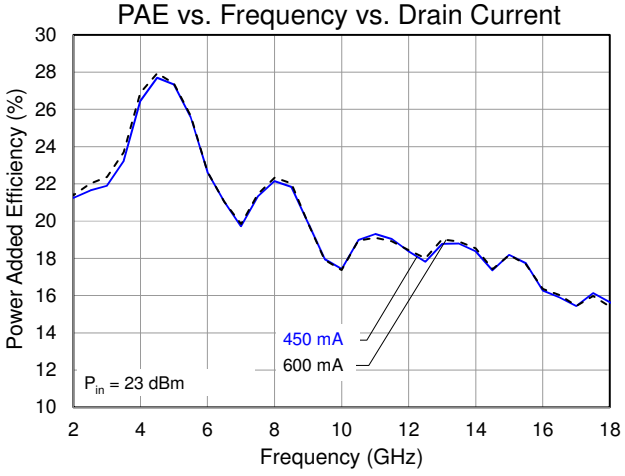
PAE vs. Input Power vs. Frequency



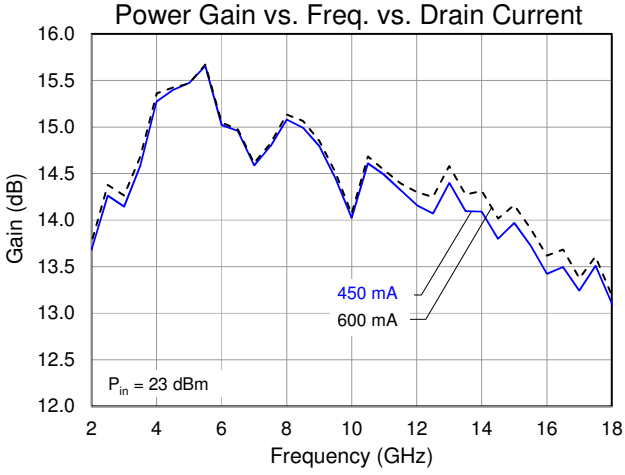
Power Gain vs. Input Power vs. Frequency



PAE vs. Frequency vs. Drain Current

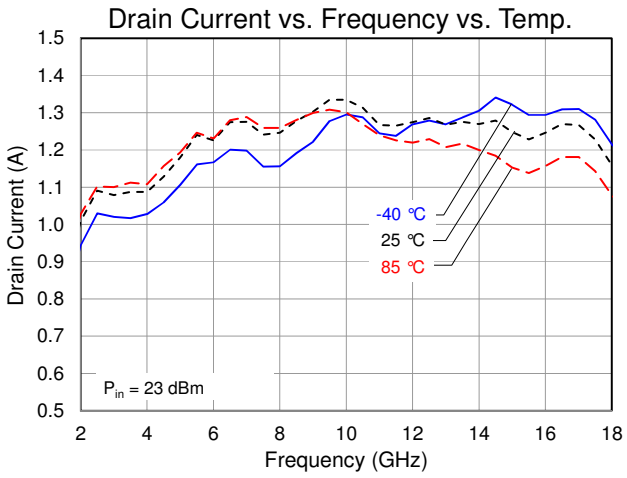


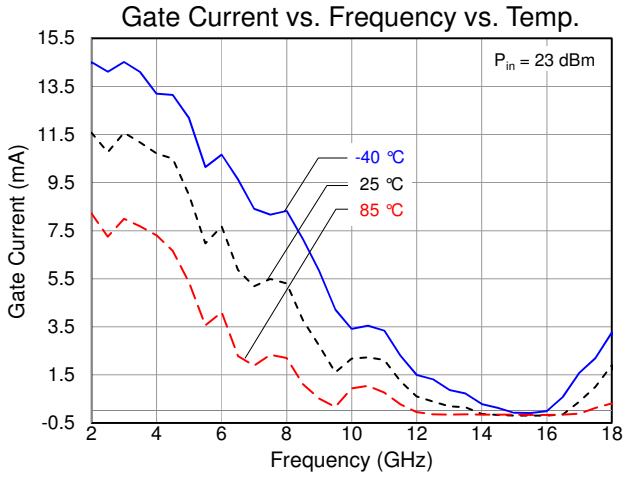
Power Gain vs. Freq. vs. Drain Current

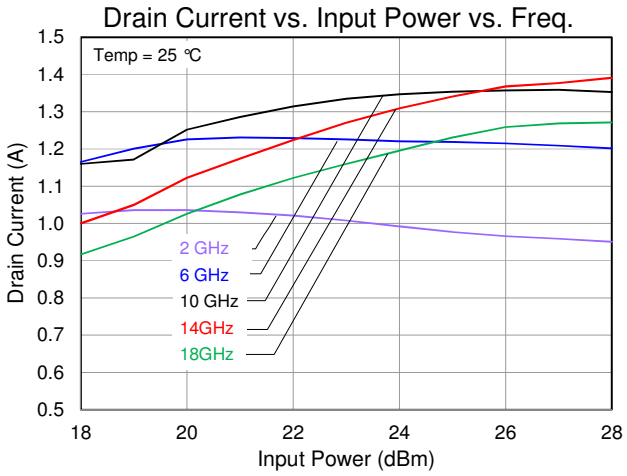


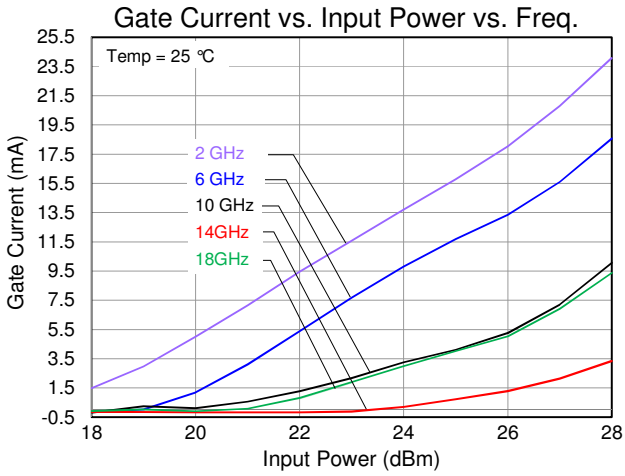
Performance Plots – Large Signal

Conditions unless otherwise specified: V_D = +22 V, I_{DQ} = 600 mA, V_G = –2.3 V Typical, CW.





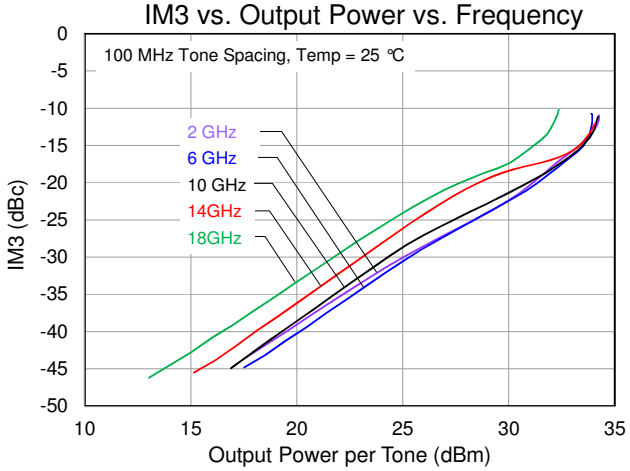




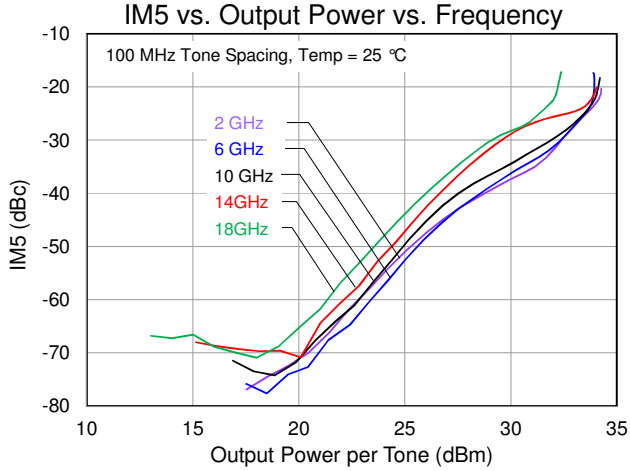
Performance Plots – Linearity

Conditions unless otherwise specified: V_D = +22 V, I_{DQ} = 600 mA, V_G = –2.3 V Typical, CW.

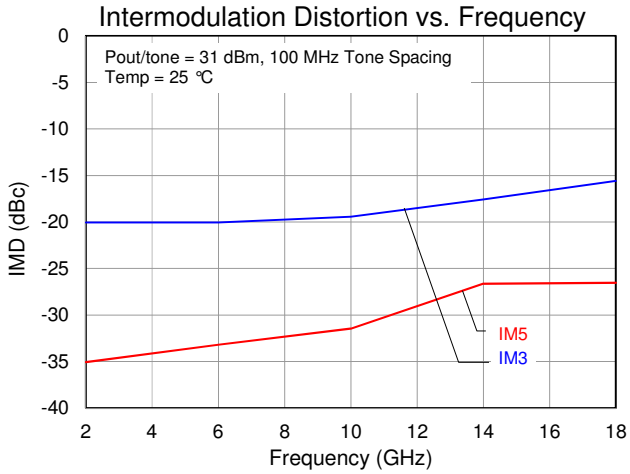
IM3 vs. Output Power vs. Frequency



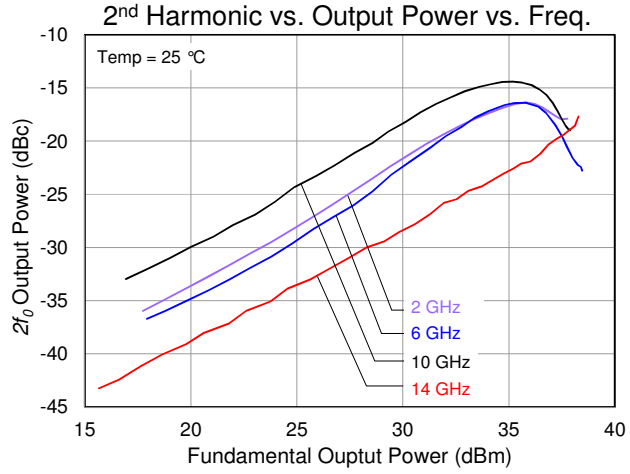
IM5 vs. Output Power vs. Frequency



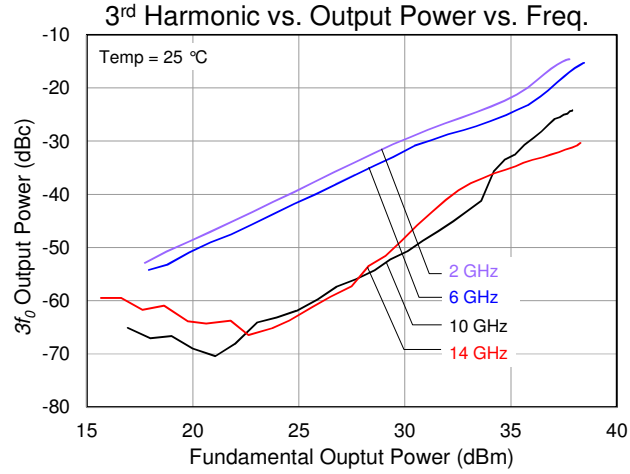
Intermodulation Distortion vs. Frequency



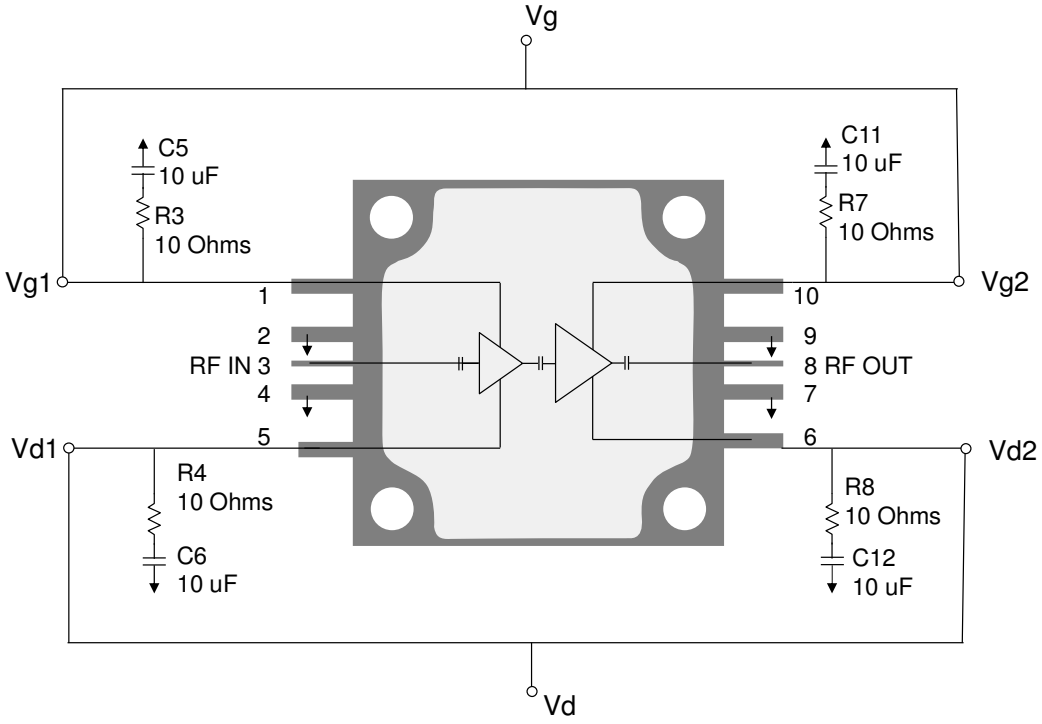
2nd Harmonic vs. Output Power vs. Freq.



3rd Harmonic vs. Output Power vs. Freq.



Applications Information and Pin Layout



Bias Up Procedure

1. Set I_D limit to 1.5 A, I_G limit to 26 mA
2. Apply –5 V to V_G
3. Apply +22 V to V_D; ensure I_{DQ} is approx. 0 mA
4. Adjust V_G until I_{DQ} = 600 mA (V_G ~ –2.3 V Typ.).
5. Turn on RF supply

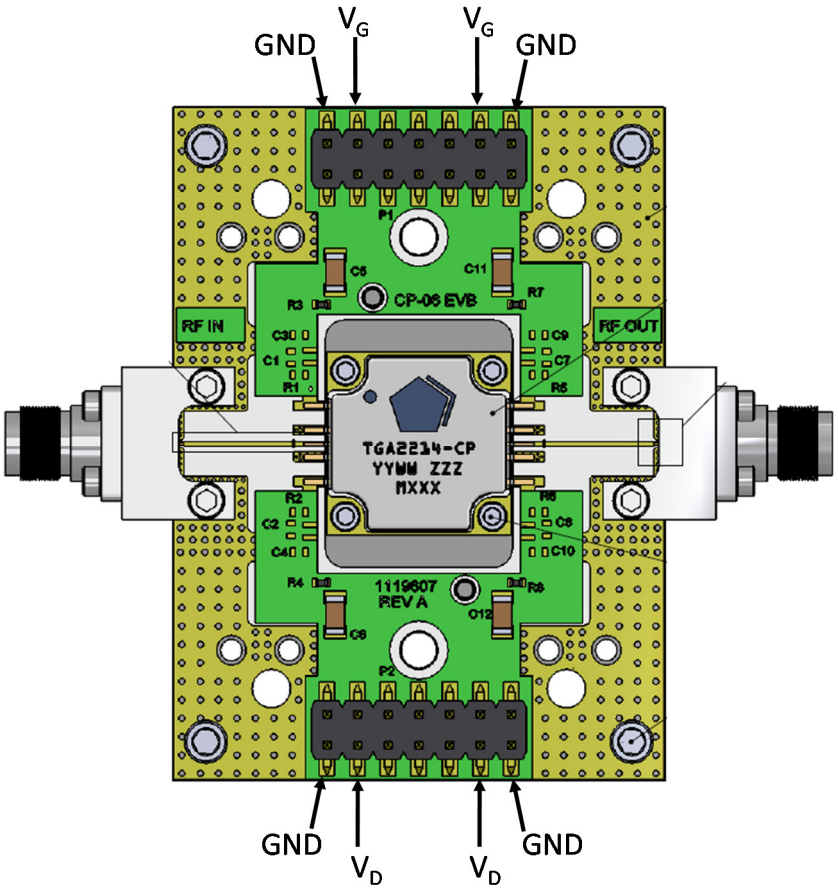
Bias Down Procedure

1. Turn off RF supply
2. Reduce V_G to –5 V; ensure I_{DQ} is approx. 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Pad Description

Pin No.	Symbol	Description
1,10	V_{G1}, V_{G2} (respectively)	Gate Voltage; Bias network is required; must be biased from both sides; see recommended Application Information above.
3	RF_{IN}	Output; matched to 50 Ω; DC blocked
2,4,7,9	GND	Must be grounded on the PCB.
5,6	V_{D1}, V_{D2} (respectively)	Drain voltage; Bias network is required; must be biased from both sides; see recommended Application Information above.
8	RF_{OUT}	Input; matched to 50 Ω; DC blocked

Evaluation Board



Notes:
1. Both V_D and V_G pins must be biased.

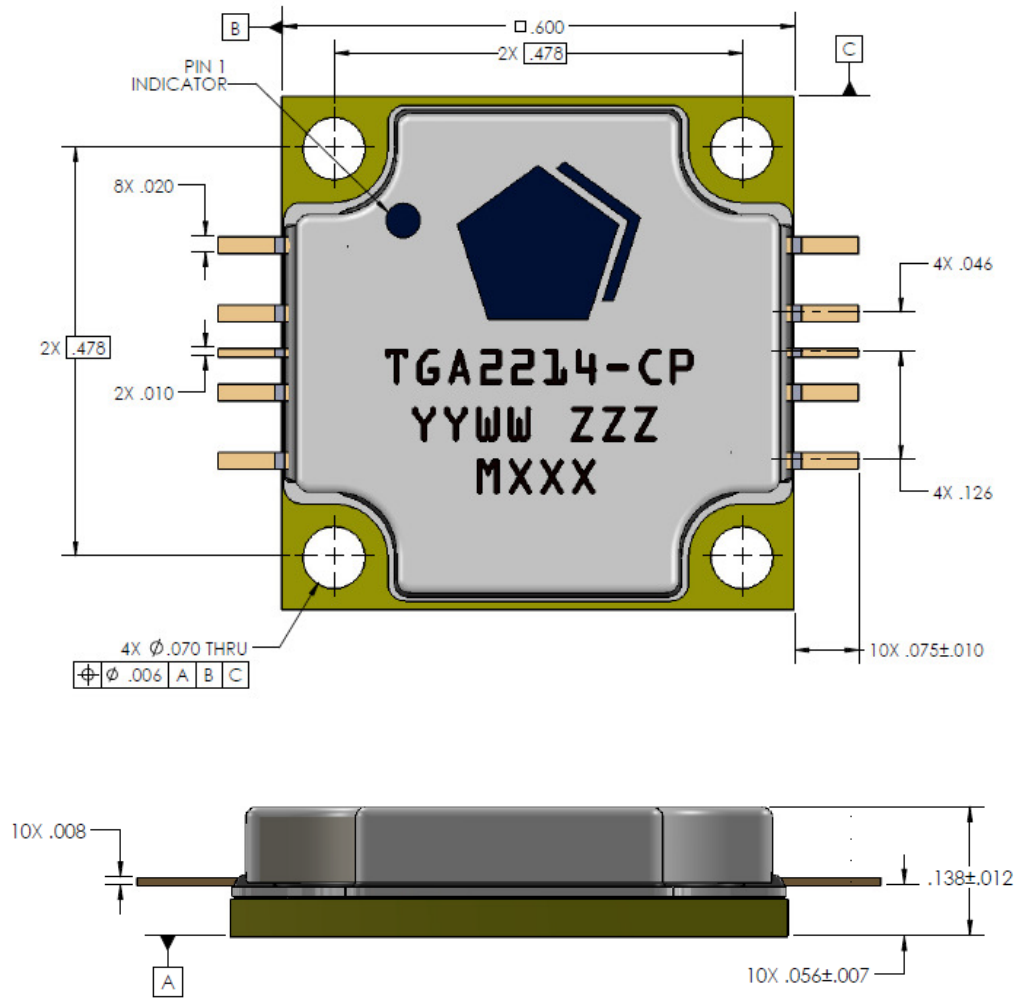
Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C5, C6, C11, C12	10 µF	Cap, 1206, +50 V, 20 %, X5R	Various	–
R3, R4, R7, R8	10 Ohm	Res, 0402, 5 %	Various	–

Assembly Notes

1. Clean the board or module with alcohol. Allow it to dry fully.
2. Nylock screws are recommended for mounting the TGA2214-CP to the board.
3. To improve the thermal and RF performance, we recommend the following:
   a. Apply thermal compound or 4 mils indium shim between the package and the board.
   b. Attach a heat sink to the bottom of the board and apply thermal compound or 4 mils indium shim between the heat sink and the board.
4. Apply solder to each pin of the TGA2214-CP.
5. Clean the assembly with alcohol.

Mechanical Information



Units: inches
Tolerances: unless specified
x.xx = ± 0.01
x.xxx = ± 0.005
Materials:
Base: Copper
Lid: Plastic
All metalized features are gold plated
Part is epoxy sealed
Marking:
2214: Part number
YY: Part Assembly year
WW: Part Assembly week
ZZZ: Serial Number
MXXX: Batch ID