TGA2597-SM

2 – 6 GHz GaN Driver Amplifier

Product Description

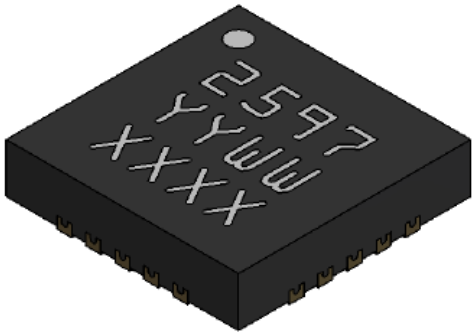
Qorvo's TGA2597-SM is a packaged driver amplifier fabricated on Qorvo's QGaN25 0.25um GaN on SiC production process. The TGA2597-SM operates from 2.0 to 6.0GHz and provides 32 dBm of output power with14 dB of large signal gain and 31 % power-added efficiency.

Using GaN MMIC technology and plastic packaging, the TGA2597-SM provides a low cost driver solution that provides the added benefit of operating on the same voltage rail as the corresponding GaN HPA. It can also serve as the output power amplifier in lower power architectures.

The TGA2597-SM is offered in a 4x4 mm plastic overmold QFN. It is internally matched to 50 ohms and includes integrated DC blocking caps on both RF ports allowing for simple system integration.

Lead–Free and RoHS compliant.

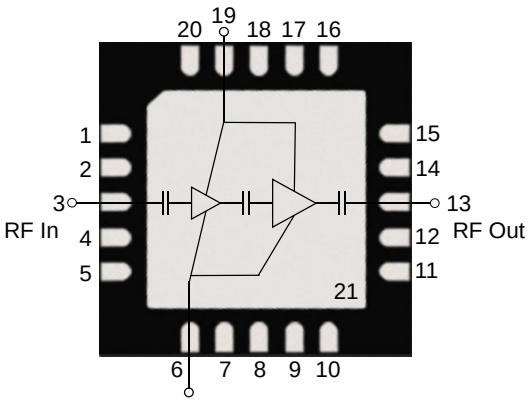
Evaluation boards are available upon request.



Product Features

- Frequency Range: 2 – 6 GHz
- Small Signal Gain: > 24 dB
- Power: > 32 dBm
- PAE: > 31 %
- IM3: < -24 dBc
- Bias: V_D = 25 V, I_{DQ} = 40 mA
- Package Dimensions: 4.0 x 4.0 x 0.85 mm

Functional Block Diagram



Applications

- Commercial & Military Radar
- Communications
- Electronic Warfare (EW)

Ordering Information

Part No.	ECCN	Description
TGA2597-SM	EAR99	2 – 6 GHz GaN Driver Amplifier

Absolute Maximum Ratings

Parameter	Range / Value	Units
Drain Voltage (V_D)	+40	V
Gate Voltage (V_G)	−5 to 0	V
Drain Current (I_D)	400	mA
Gate Current (I_G)	See graph on page 3	–
Power Dissipation, 85 °C (P_{DISS})	5.4	W
RF Input Power, CW, 50 Ω [1]	24	dBm
RF Input Power, CW, VSWR 3:1[1]	24	dBm
Channel Temperature (T_{CH})	+275	°C
Mounting Temperature (30 seconds maximum)	+260	°C
Storage Temperature	−55 to +150	°C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

(1) V_D = 25V, I_{DQ} = 40mA, T_B = 85 °C

Recommended Operating Conditions

Parameter	
Drain Voltage (V_D)	25 V
Gate Voltage (V_G)	-2.5 V
Quiescent Drain Current (I_{DQ})	40 mA
Operating Drain Current (I_{D_DRIVE})	250 mA

Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		2		6	GHz
Output Power	P_{IN} = 18 dBm		> 32		dBm
Power Added Efficiency	P_{IN} = 18 dBm		> 31		%
Small Signal Gain			> 24		dB
Input Return Loss			20		dB
Output Return Loss			> 5		dB
IM3	P_{OUT} / Tone ≤ 24 dBm, Δf = 10 MHz		<−24		dBc
Small Signal Gain Temperature Coefficient			−0.050		dB / °C
Output Power Temperature Coefficient			-0.009		dB / °C

Test conditions unless otherwise noted: T_{BASE} = +25 °C, V_D = 25 V, V_G = −2.5 V, CW, Part mounted to EVB (page 11)

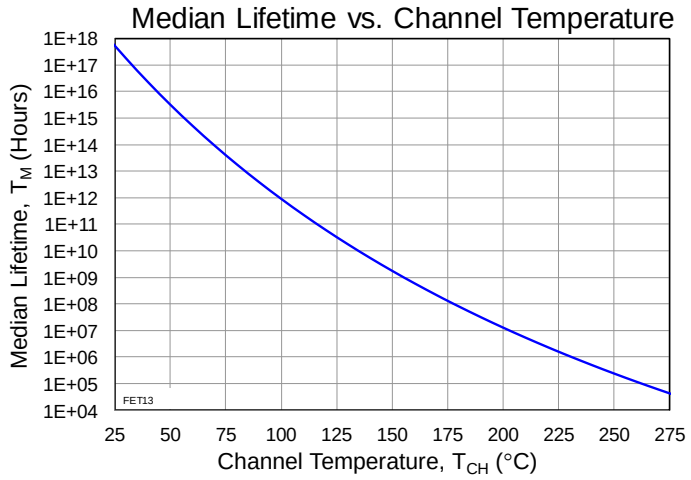
Thermal and Reliability Information

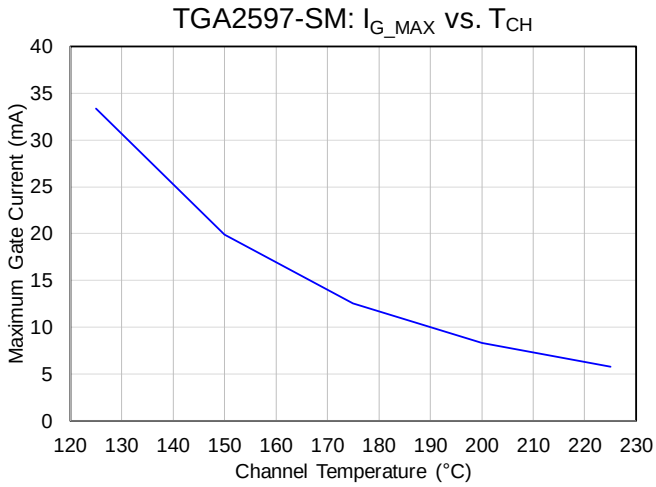
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = +85 °C, V_D = 25 V, I_{DQ} = 40 mA, I_{D_DRIVE} = 206 mA, P_{IN} = 18 dBm, P_{OUT} = 31.8 dBm, P_{DISS} = 3.7 W	24.6	°C/W
Channel Temperature (T_{CH}) (1)		176	°C
Median Lifetime (T_M)		1.18E+8	Hrs.

Notes:
1. Package backside temperature fixed at 85 °C.

Median Lifetime

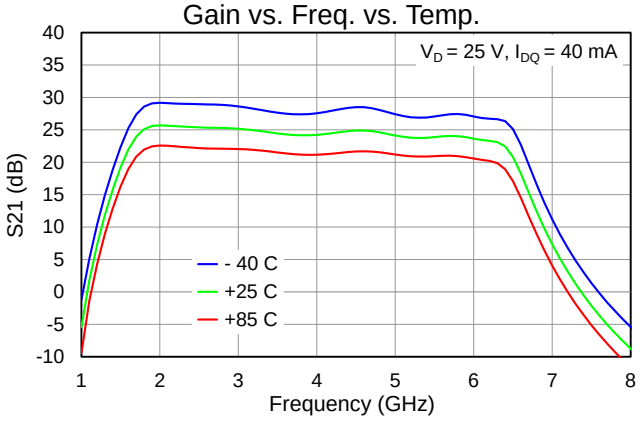
Test Conditions: V_D = 40 V; Failure Criterion = 10% reduction in $I_{D\ MAX}$



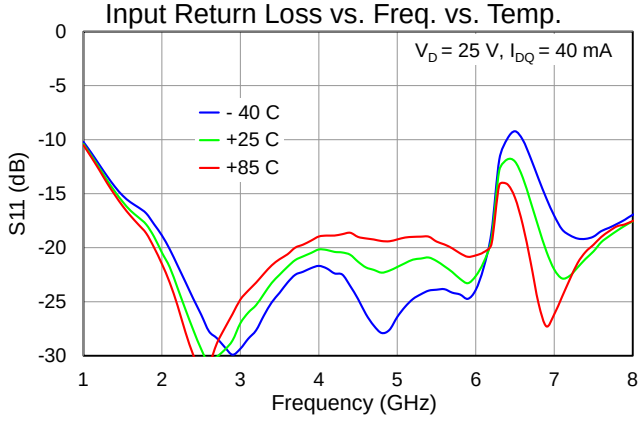


Performance Plots – Small Signal

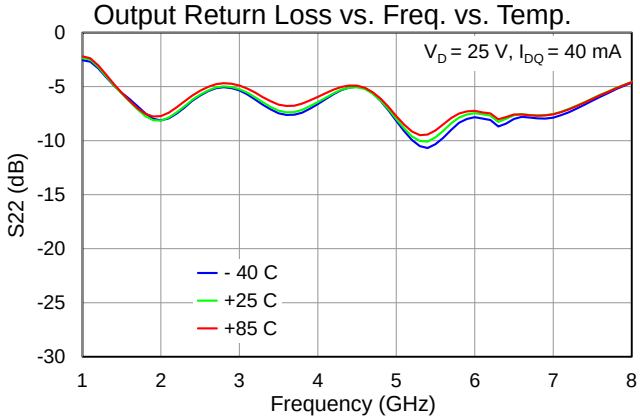
Gain vs. Freq. vs. Temp.



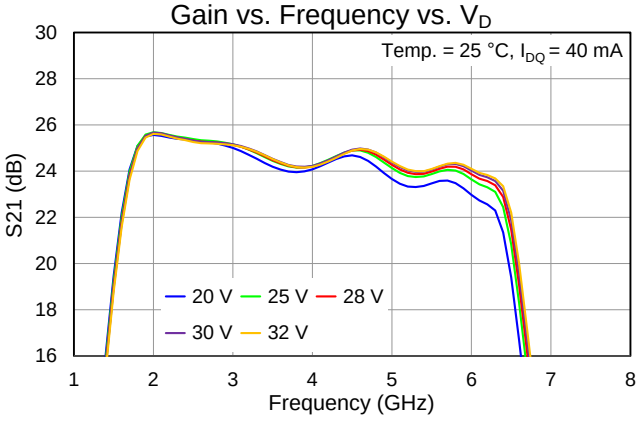
Input Return Loss vs. Freq. vs. Temp.



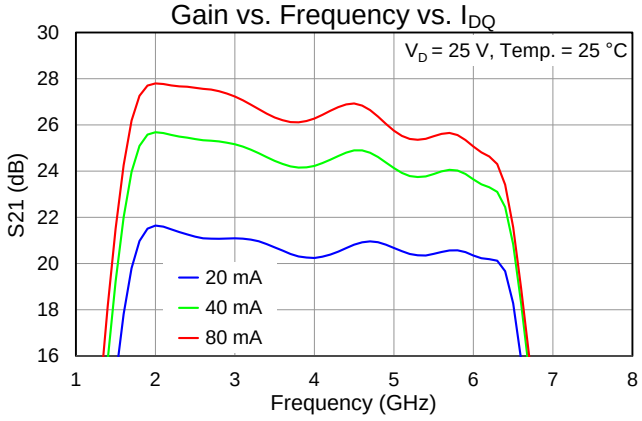
Output Return Loss vs. Freq. vs. Temp.



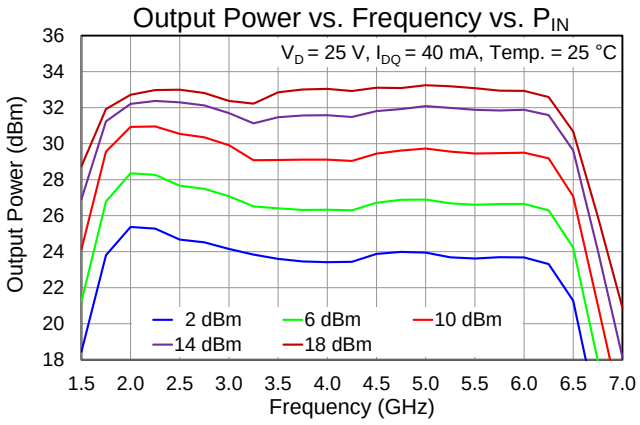
Gain vs. Frequency vs. V_D

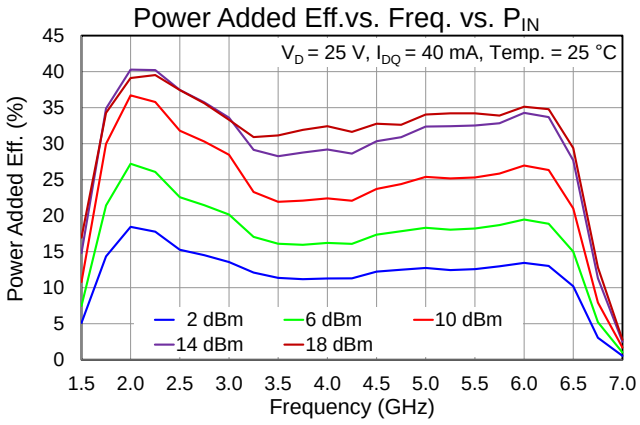


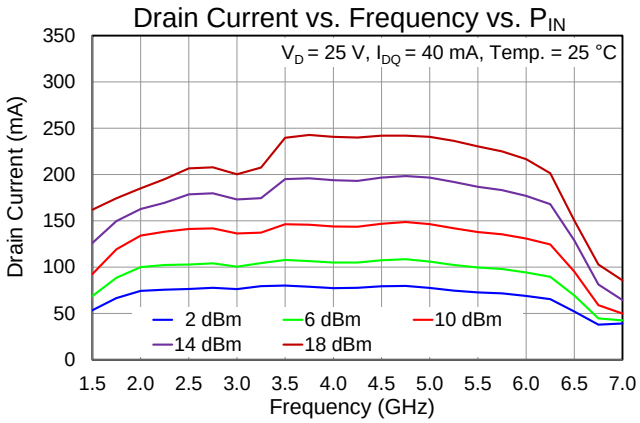
Gain vs. Frequency vs. I_{DQ}

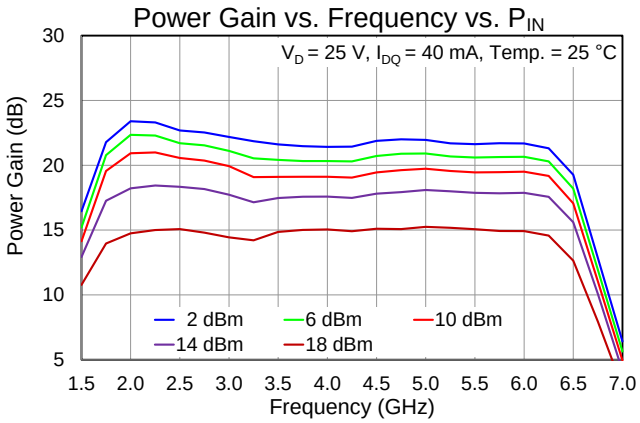


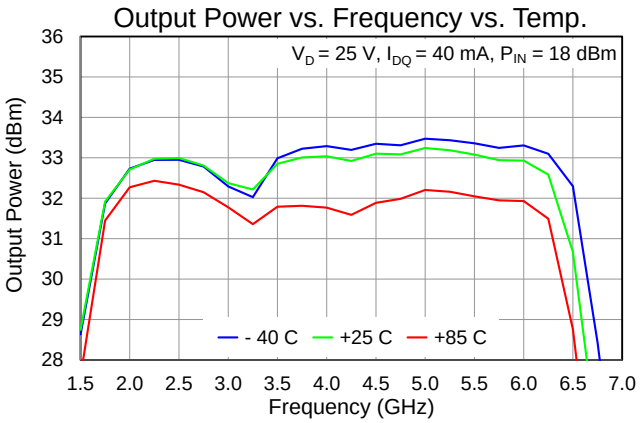
Performance Plots – Large Signal

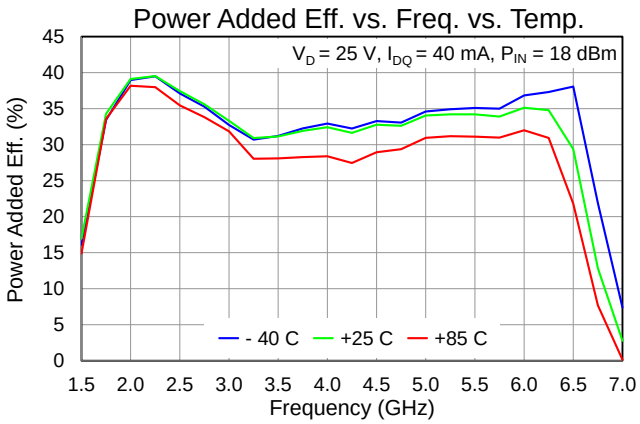






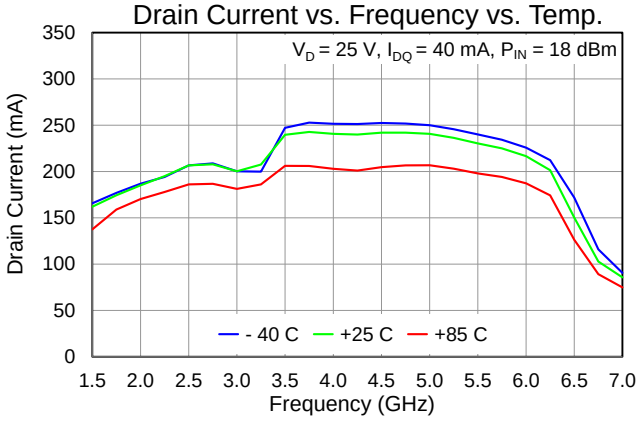




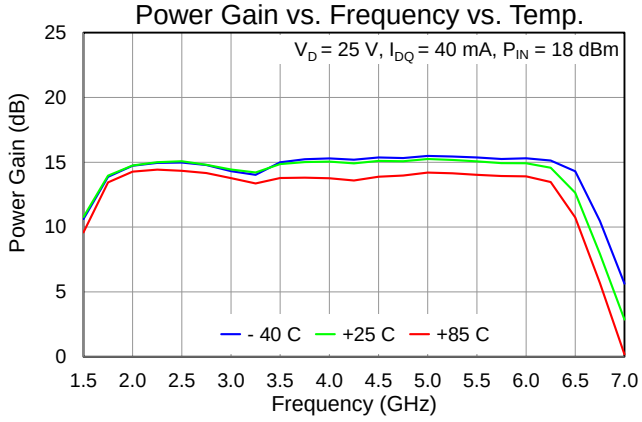


Performance Plots – Large Signal

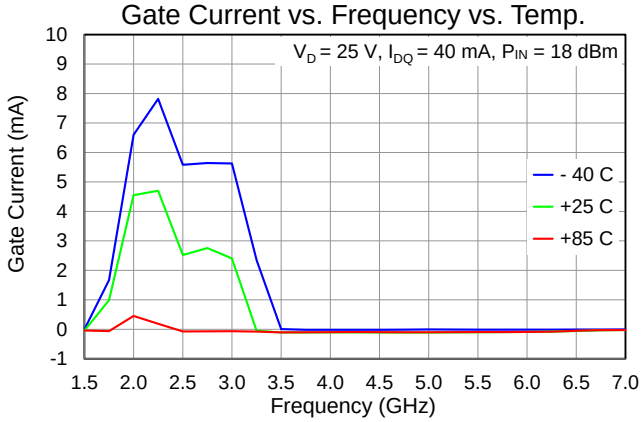
Drain Current vs. Frequency vs. Temp.



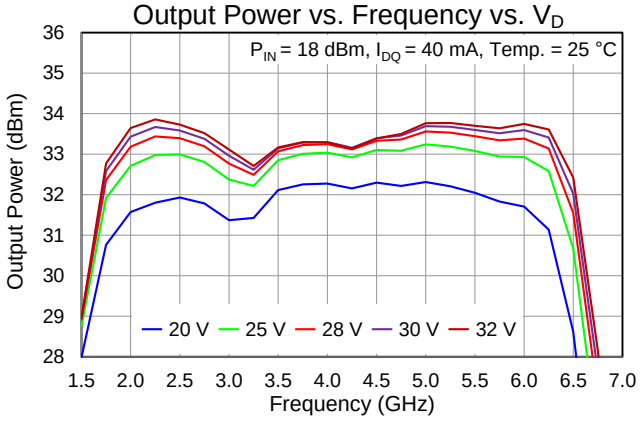
Power Gain vs. Frequency vs. Temp.



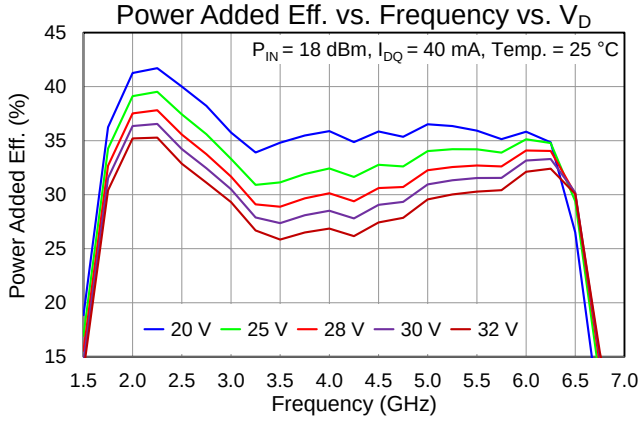
Gate Current vs. Frequency vs. Temp.



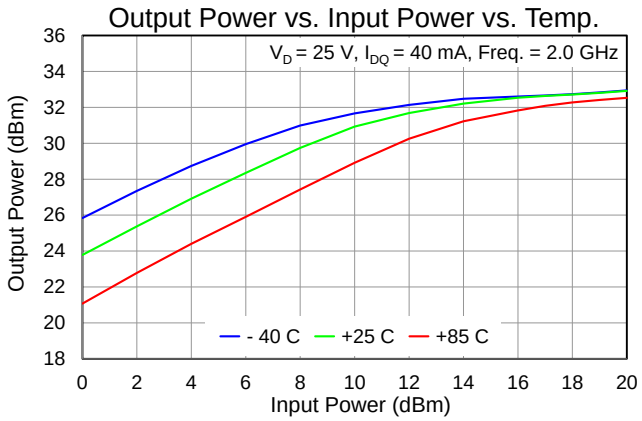
Output Power vs. Frequency vs. V_D

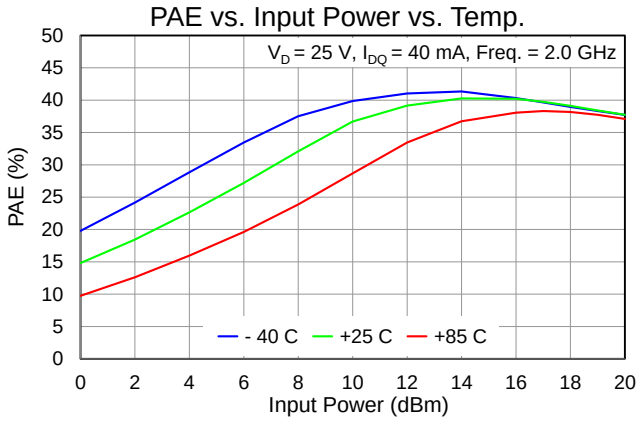


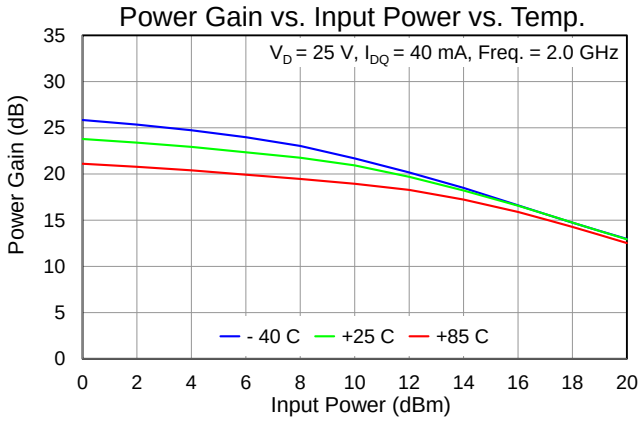
Power Added Eff. vs. Frequency vs. V_D

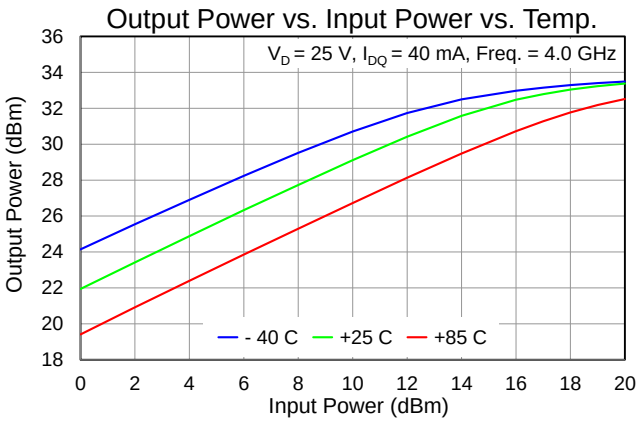


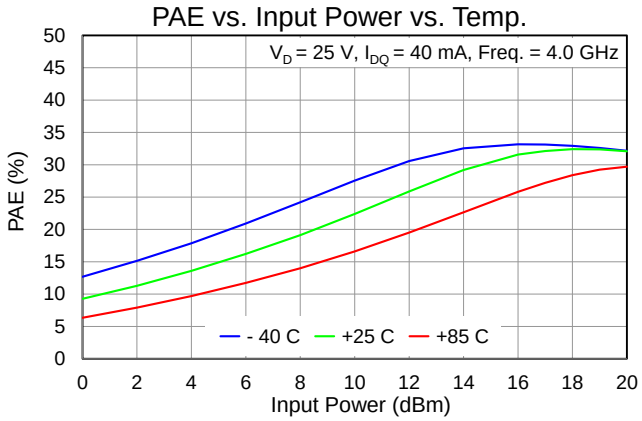
Performance Plots – Large Signal

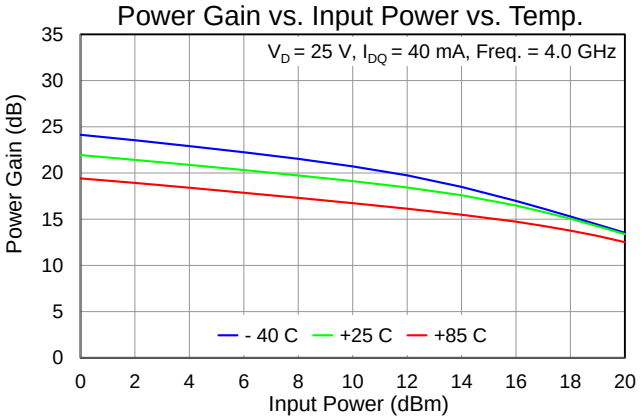




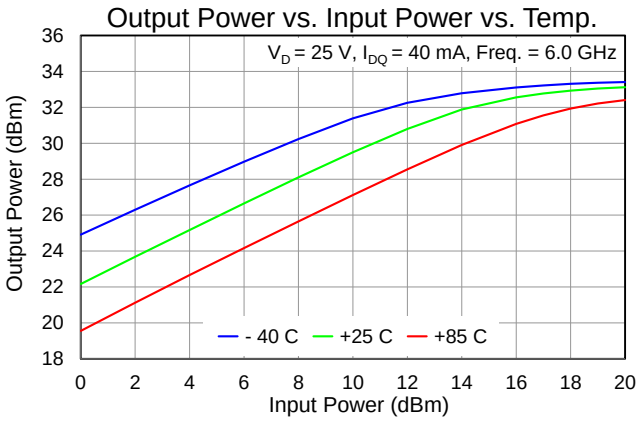


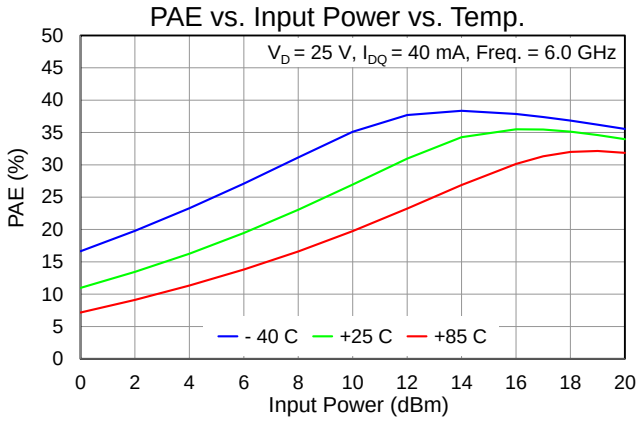


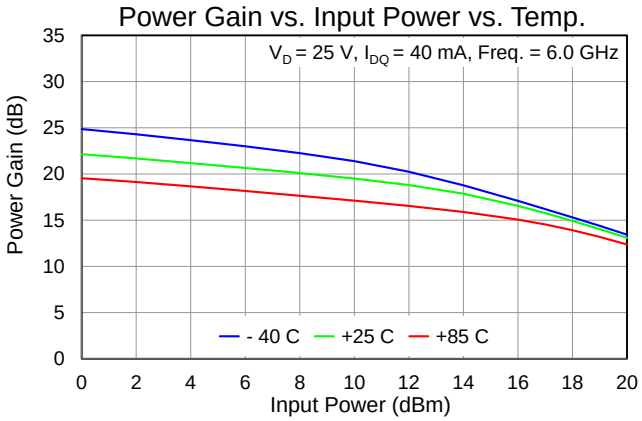


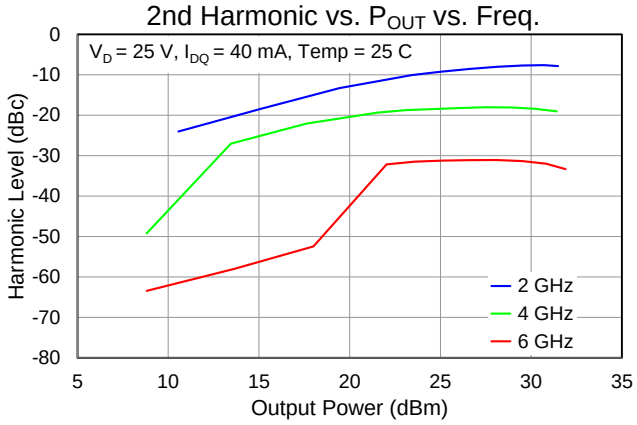


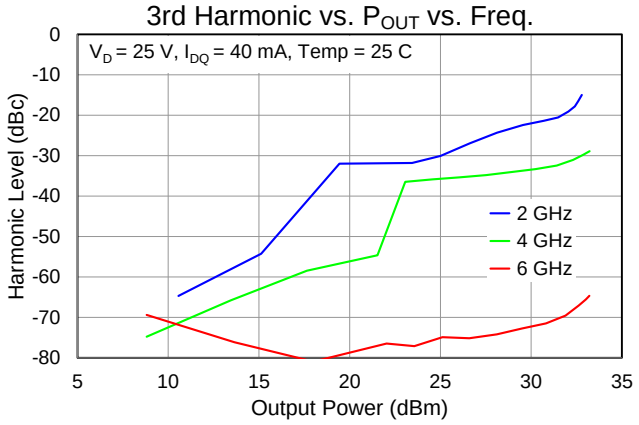
Performance Plots – Large Signal





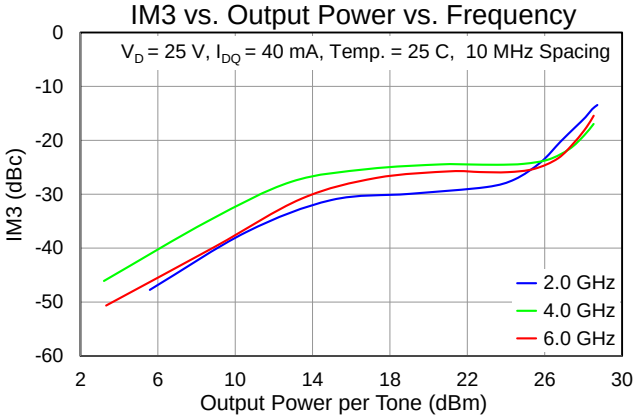




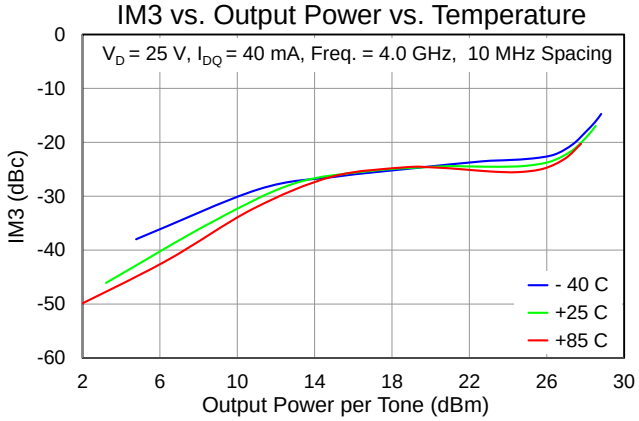


Performance Plots – Linearity & Harmonic

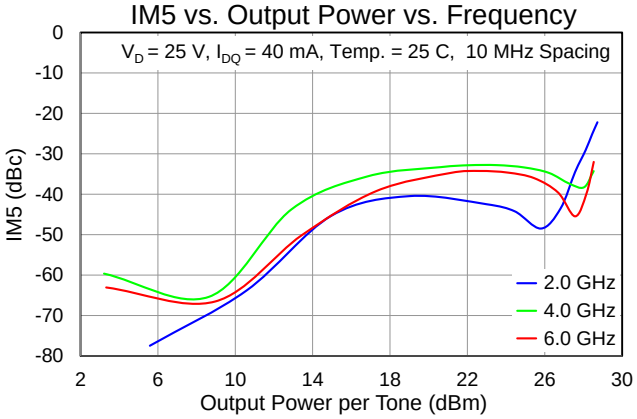
IM3 vs. Output Power vs. Frequency



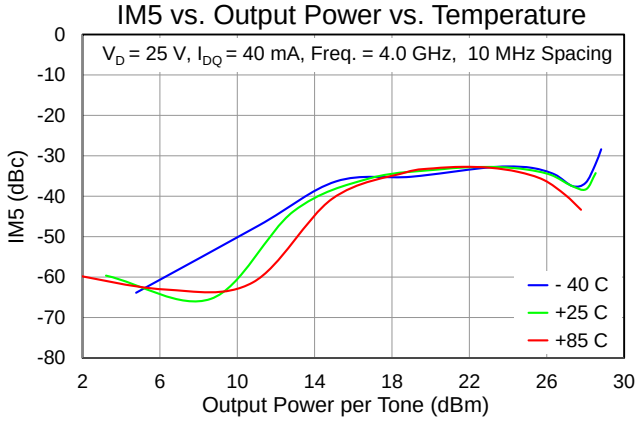
IM3 vs. Output Power vs. Temperature



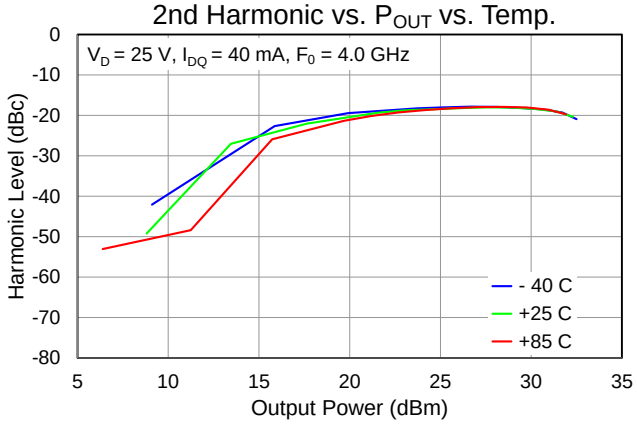
IM5 vs. Output Power vs. Frequency



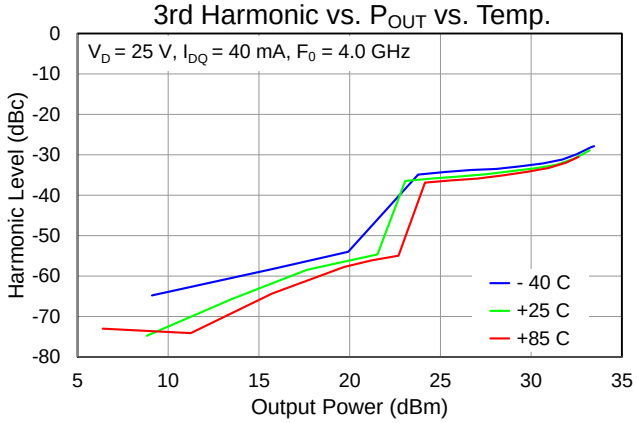
IM5 vs. Output Power vs. Temperature



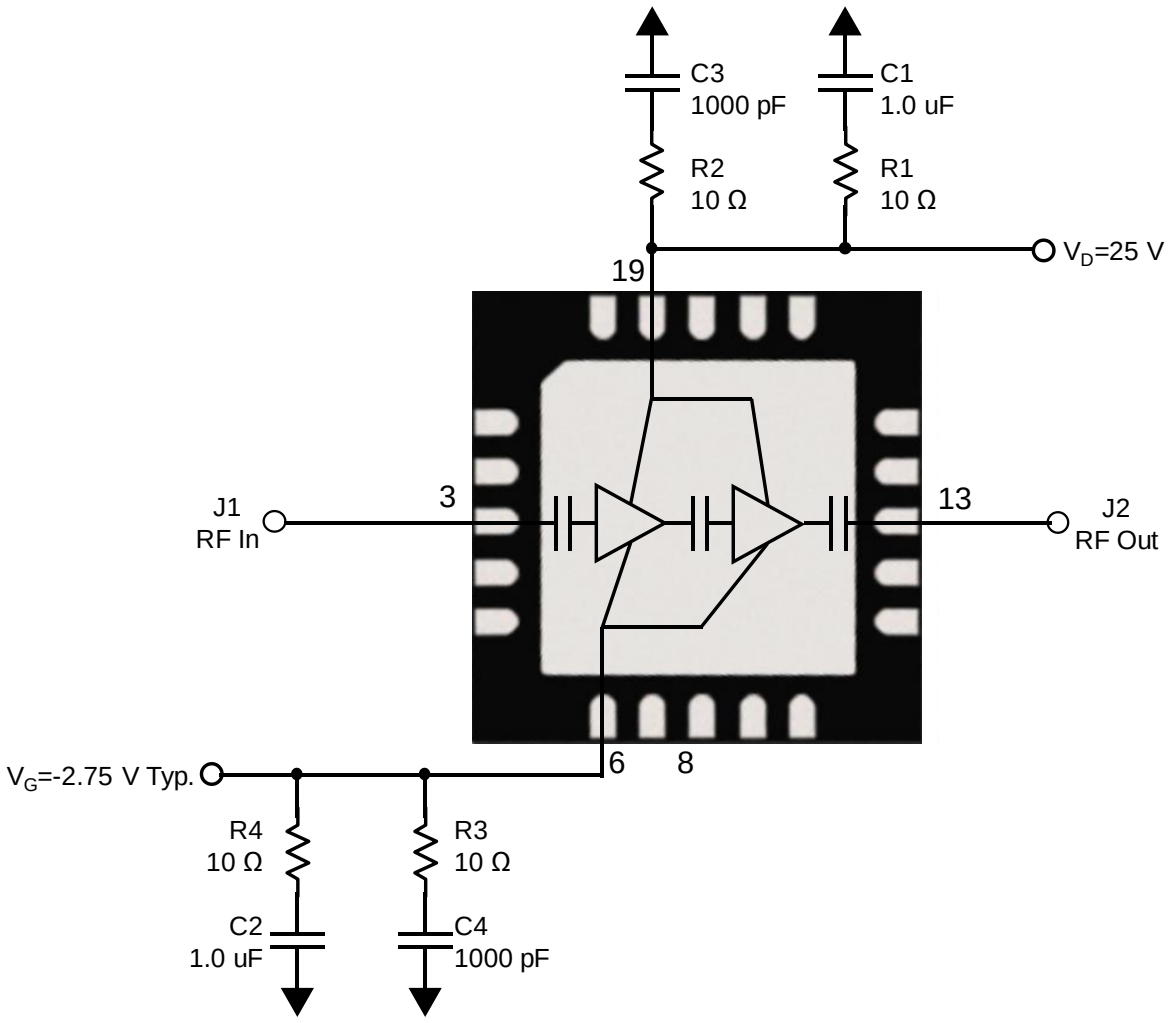
2nd Harmonic vs. P_{OUT} vs. Temp.



3rd Harmonic vs. P_{OUT} vs. Temp.



Application Circuit



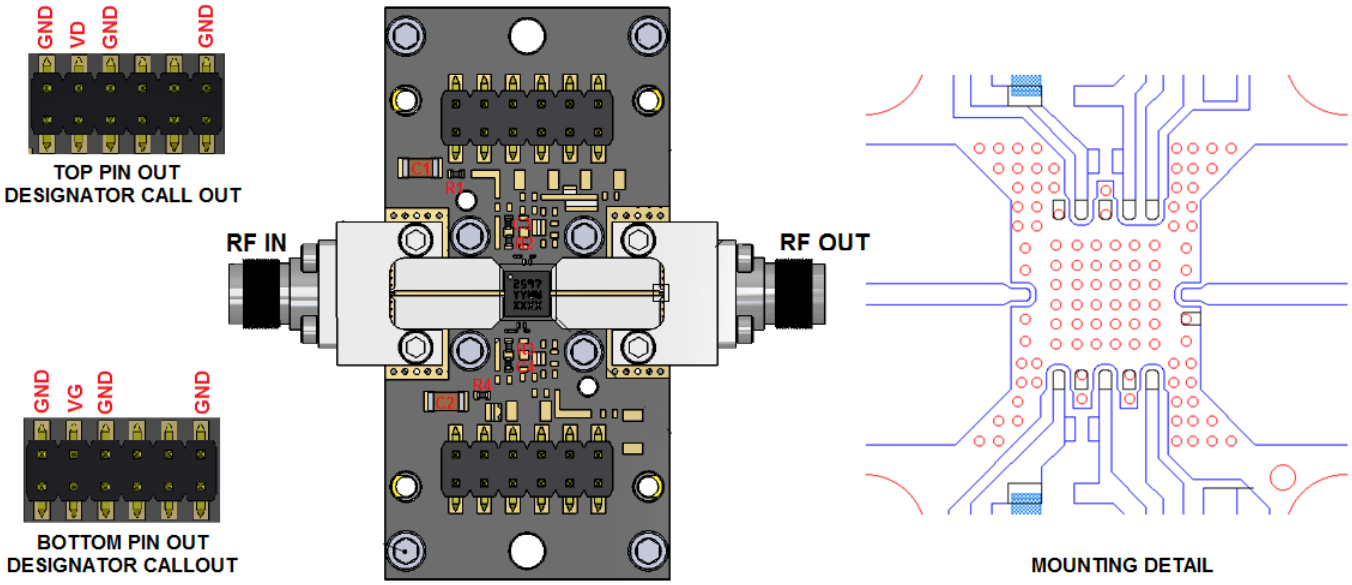
Bias Up Procedure

1. Set I_D limit to 400 mA, I_G limit to 4.5 mA
2. Set V_G to -5.0V
3. Set V_D +25V
4. Adjust V_G more positive until I_{DQ} = 40 mA.
5. Apply RF signal

Bias Down Procedure

1. Turn off RF signal
2. Set V_G to -5.0V. Ensure I_{DQ} ~ 0mA
3. Set V_D to 0V
4. Turn off V_D supply
5. Turn off V_G supply

Evaluation Board Layout



RF Layer is 0.008" thick Rogers Corp. RO4003C, ε_r = 3.38. Metal layers are 0.5 oz. copper. The microstrip line at the connector interface is optimized for the Southwest Microwave end launch connector 1092-01A-5.

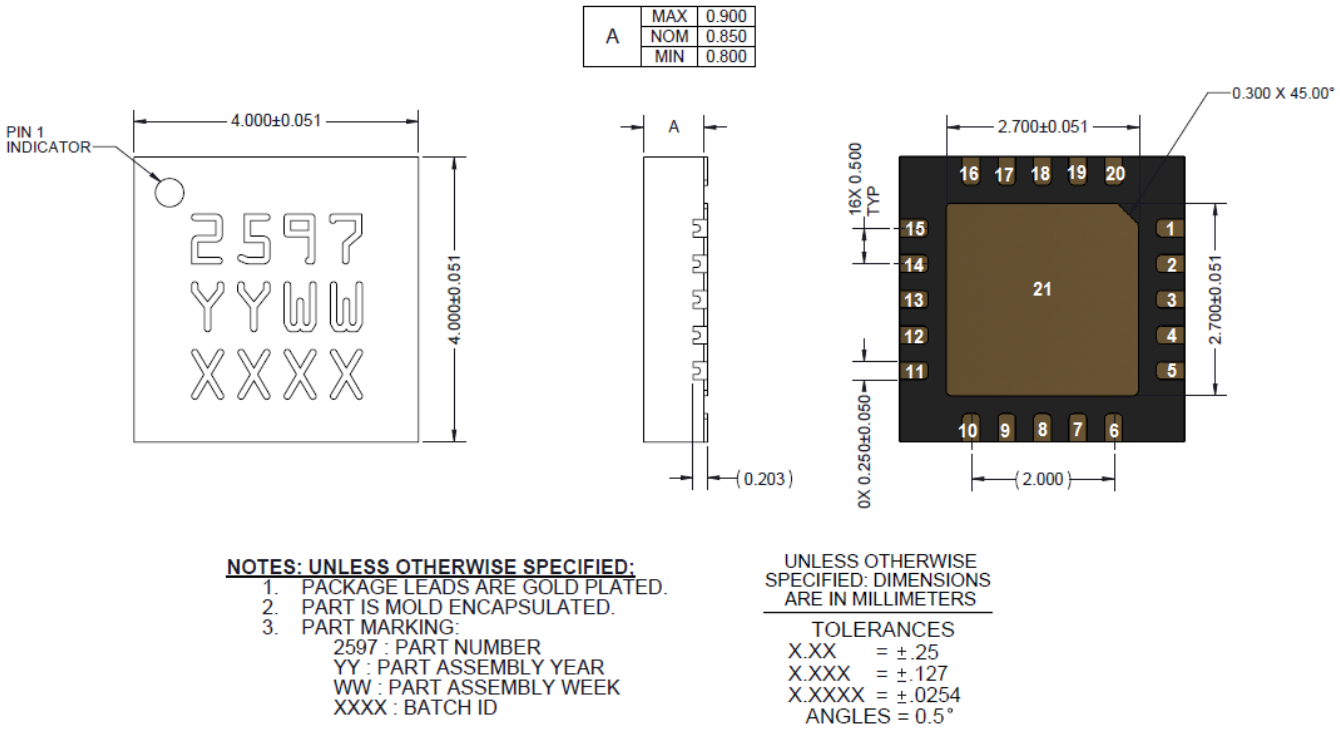
The pad pattern shown has been developed and tested for optimized assembly at Qorvo. The PCB land pattern has been developed to accommodate lead tolerances. Since processes vary from company to company, careful process development is recommended

Multiple vias should be employed under the package center paddle to minimize inductance resistance.

Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1, C2	1 uF, 50 V, 20 %	CAP X5R 1206	Various	–
C3, C4	1000 pF, 100 V, 10 %	CAP X7R 0402	Various	–
R1 – R4	10 Ohm, 1 %, 1/16 W	RES 0402 case	Various	–

Mechanical Information, Pin Configuration and Description



NOTES: UNLESS OTHERWISE SPECIFIED:

1. PACKAGE LEADS ARE GOLD PLATED.
2. PART IS MOLD ENCAPSULATED.
3. PART MARKING:
   2597 : PART NUMBER
   YY : PART ASSEMBLY YEAR
   WW : PART ASSEMBLY WEEK
   XXXX : BATCH ID

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS

TOLERANCES
X.XX = ± .25
X.XXX = ± .127
X.XXXX = ± .0254
ANGLES = 0.5°

Pin No.	Label	Description
1-2, 4-5, 7-12, 14-18, 20	GND	Connected to ground paddle (21); recommend grounding on PCB for improved package isolation.
3	RF Input	RF input, matched to 50 Ω, DC blocked
6	V_G	Gate voltage. Bias network required
13	RF Output	RF output, matched to 50 Ω, DC blocked
19	V_D	Drain voltage. Bias network required.
21	Slut (GND)	Backside paddle. Multiple vias should be employed to minimize inductance and thermal resistance. Copper-filled vias recommended for best thermal performance.

Recommended Soldering Temperature Profile