TriQuint

TGA2216
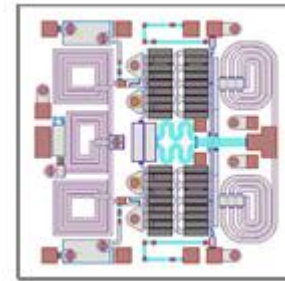## 0.1 – 3.0GHz 12W GaN Power Amplifier

Applications

- Commercial and military radar
- Communications
- Electronic Warfare

Product Features

- Frequency Range: 0.1 – 3.0GHz
- P_{SAT}: 41dBm at P_{IN} = 27dBm
- P1dB: >34dBm
- PAE: >40%
- Large Signal Gain: 14dB
- Small Signal Gain: 22dB
- IM3 @ 120mA P_{OUT}< 33dBm/tone: -30dBc
- IM5 @ 120mA P_{OUT}< 33dBm/tone: -35dBc
- Bias: V_D = 48V, I_{DQ} = 360mA, V_{G1} = -2.3V Typical, V_{G2} = +21.7V Typical
- Wideband Flat Gain and Power
- Chip Dimensions: 1.8 x 1.8 x 0.10 mm

Functional Block Diagram
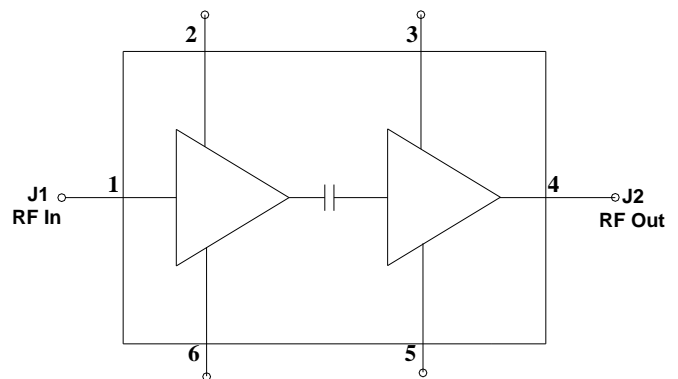
General Description

TriQuint's TGA2216 is a wideband cascode amplifier fabricated on TriQuint's production 0.25um GaN on SiC process. The cascode configuration offers exceptional wideband performance as well as supporting 48V operation. The TGA2216 operates from 0.1 - 3.0GHz and provides 12W of saturated output power with 14dB of large signal gain and greater than 40% power-added efficiency.

The broadband performance supports both radar and communication applications across defense and commercial markets as well as electronic warfare. The TGA2216 is fully matched to 50Ω at both RF ports allowing for simple system integration. DC blocks are required on both RF ports and the drain voltage must be injected through an off chip bias-tee on the RF output port.

Lead-free and RoHS compliant.

Evaluation boards are available upon request.

Pad Configuration

Pad No.	Symbol
1	RF In, V_{G1}
2, 6	V_{G1}
3, 5	V_{G2}
4	RF Out, V_D

Ordering Information

Part	ECCN	Description
TGA2216	EAR99	0.1 – 3.0GHz 12W GaN Power Amplifier

Absolute Maximum Ratings

Parameter	Value
Drain Voltage (V$_D$)	80V
Gate Voltage Range (V$_{G1}$)	-8 to 0V
Gate Voltage Range (V$_{G2}$)	0 to 40V
Drain Current (I$_D$)	760mA
Gate Current (I$_{G1}$)	-5 to 5.6mA
Gate Current (I$_{G2}$)	-5 to 5.6mA
Power Dissipation (P$_{DISS}$), 85°C	28W
Input Power (P$_{IN}$), CW, 50 Ω, 85°C,	33dBm
Input Power (P$_{IN}$), CW, VSWR 10:1, V$_D$ = 48V, 85°C	30dBm
Channel Temperature (T$_{CH}$)	275°C
Mounting Temperature (30 Seconds)	320°C
Storage Temperature	-55 to 150°C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value
Drain Voltage (V$_D$)	48V
Drain Current (I$_{DQ}$)	360mA
Drain Current Under RF Drive (I$_{D\_Drive}$)	710mA
Gate Voltage (V$_{G1}$)	-2.3V (Typ.)
Gate Voltage (V$_{G2}$)	+21.7V (Typ.)

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: 25^{0}C, V$_D$ = 48V, I$_{DQ}$ = 360mA, V$_{G1}$ = -2.3V Typical, V$_{G2}$ = +21.7V Typical

Parameter	Min	Typical	Max	Units
Operational Frequency Range	0.1		3.0	GHz
Small Signal Gain		22		dB
Input Return Loss		10 (mid band)		dB
Output Return Loss		10 (mid band)		dB
Output Power (Pin = 27dBm)		41		dBm
Power Added Efficiency (Pin = 27dBm)		> 40		%
Power @ 1dB Compression (P1dB)		> 34		dB
IM3 @ 120mA P$_{OUT}$/Tone < 33dBm		-30		dBc
IM5 @ 120mA P$_{OUT}$/Tone < 33dBm		-35		dBc
Small Signal Gain Temperature Coefficient		-0.02		dB/°C
Output Power Temperature Coefficient		-0.005		dBm/°C
Recommended Operating Voltage:	40	48	50	V

Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) [1]	T_{base} = 85°C, $\mathbf{V_D}$[2] **= 40V**, I_{DQ} = 360mA	6.56	ºC/W
Channel Temperature (T_{CH}) (Under RF drive)	T_{base} = 85°C, $\mathbf{V_D}$[2] **= 40V**, I_{D_Drive} = 635mA, P_{OUT} = 40dBm, P_{DISS} = 15W	183	°C
Median Lifetime (T_M)		6 x 10^8	Hrs
Thermal Resistance (θ_{JC}) [1]	T_{base} = 85°C, $\mathbf{V_D}$[2] **= 48V**, I_{DQ} = 360mA,	6.85	ºC/W
Channel Temperature (T_{CH}) (Under RF drive)	T_{base} = 85°C, $\mathbf{V_D}$[2] **= 48V**, I_{D_Drive} = 675mA, P_{OUT} = 40.8dBm, P_{DISS} = 20W	222	°C
Median Lifetime (T_M)		1.99 x 10^6	Hrs

Notes:
1. Thermal resistance measured to back of carrier plate. MMIC mounted on 40 mils CuMo (80/20) carrier using 1.5 mil AuSn.
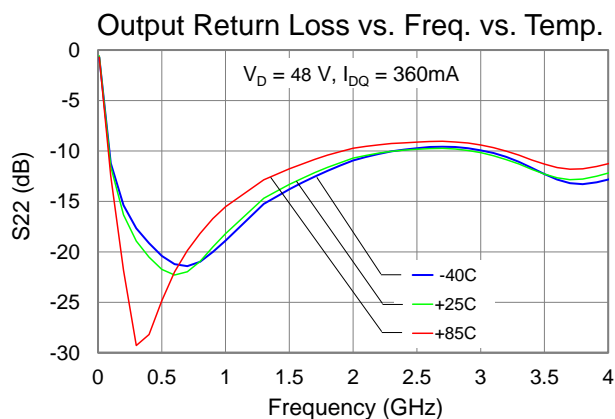2. The drain voltage for Cascode amplifier transistor is ½ of the V_D.
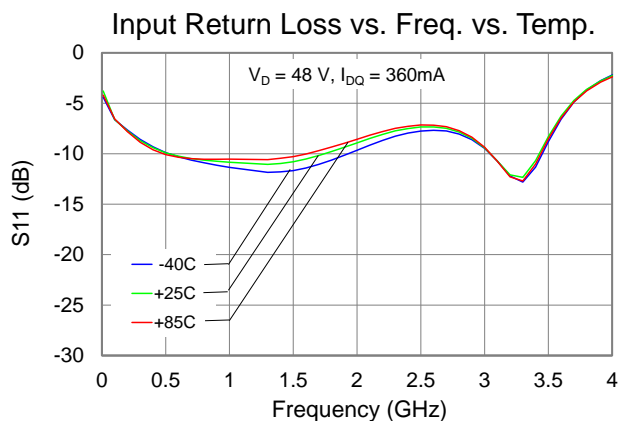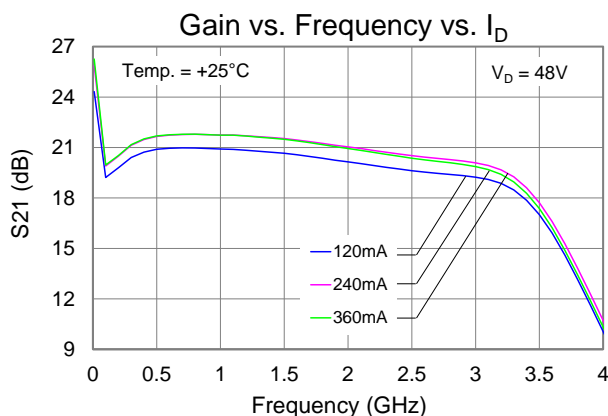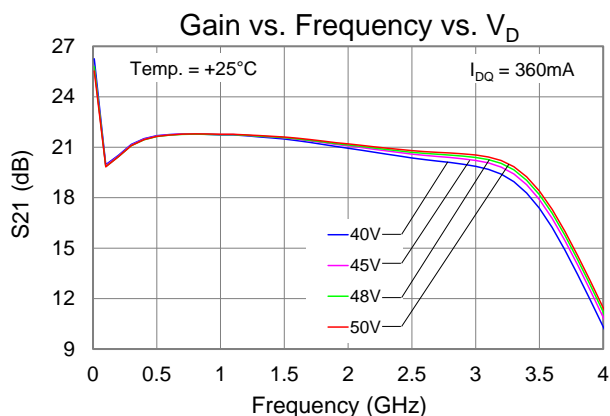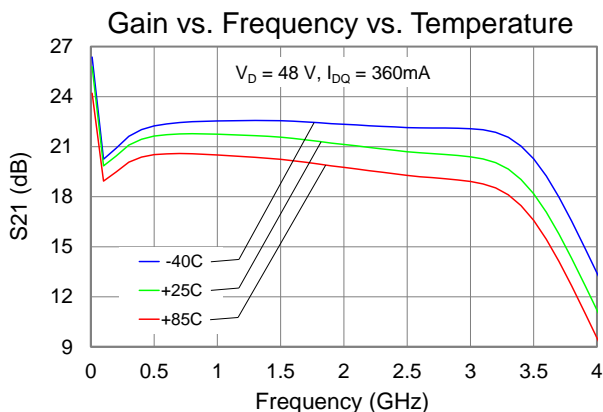
Median Lifetime

Test Conditions: V_D = 40 V; Failure Criteria = 10% reduction in I_{D_MAX}

Median Lifetime vs. Channel Temperature

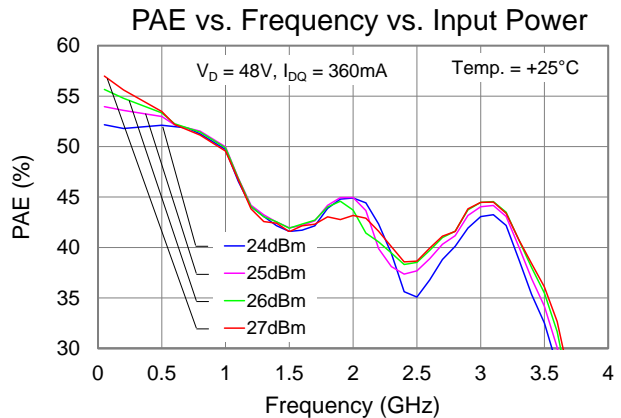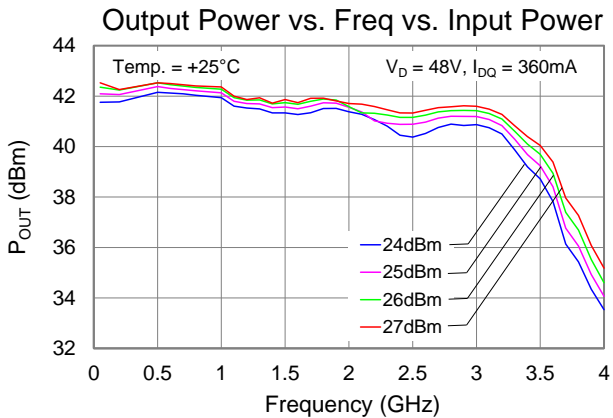## Typical Performance

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 10)

Gain vs. Frequency vs. Temperature

V_D = 48 V, I_{DQ} = 360mA

- -40C
- +25C
- +85C

Gain vs. Frequency vs. V_D

Temp. = +25°C I_{DQ} = 360mA

- 40V
- 45V
- 48V
- 50V

Gain vs. Frequency vs. I_D

Temp. = +25°C V_D = 48V

- 120mA
- 240mA
- 360mA

Input Return Loss vs. Freq. vs. Temp.

V_D = 48 V, I_{DQ} = 360mA

- -40C
- +25C
- +85C

Output Return Loss vs. Freq. vs. Temp.

V_D = 48 V, I_{DQ} = 360mA
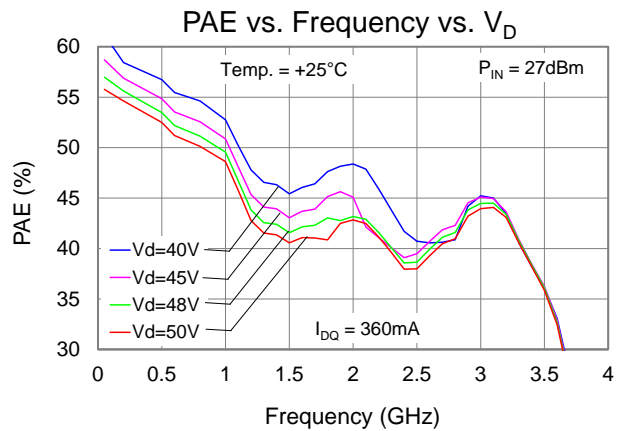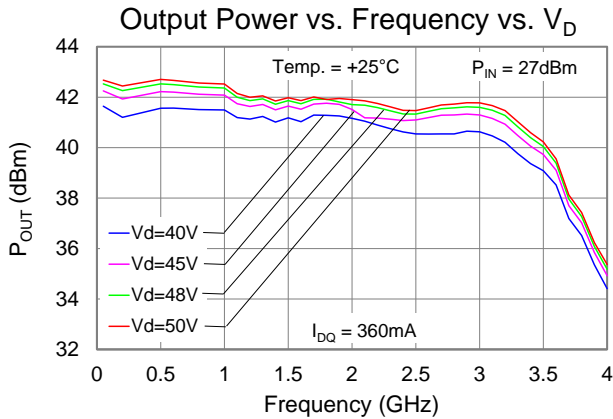
- -40C
- +25C
- +85C

Typical Performance

The plots reflect performance measured with an external coaxial bias tee and DC blocks
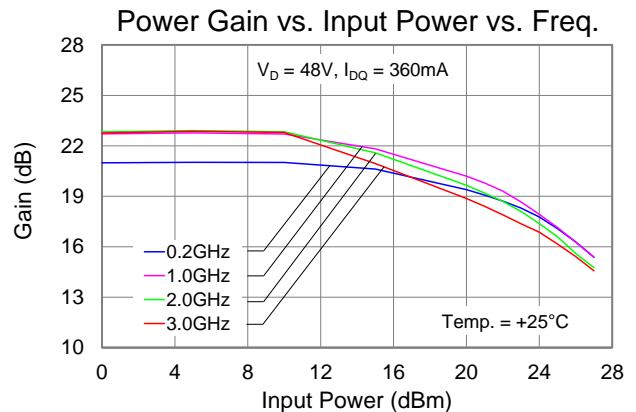(See application circuit on page 10)

Output Power vs. Frequency vs. V_D

PAE vs. Frequency vs. V_D

Output Power vs. Freq vs. Input Power

PAE vs. Frequency vs. Input Power

Output Power vs. Frequency vs. Temp.

PAE vs. Frequency vs. Temperature

Typical Performance

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 10)

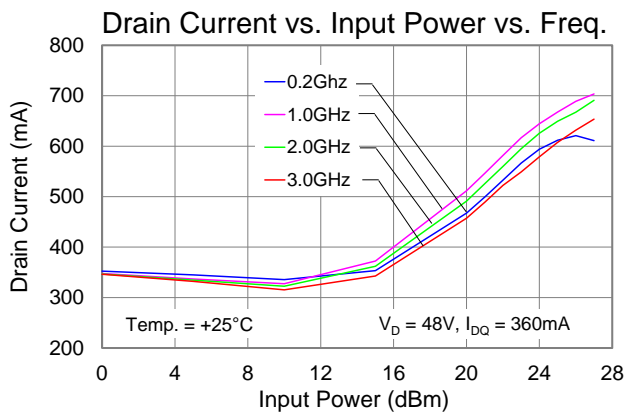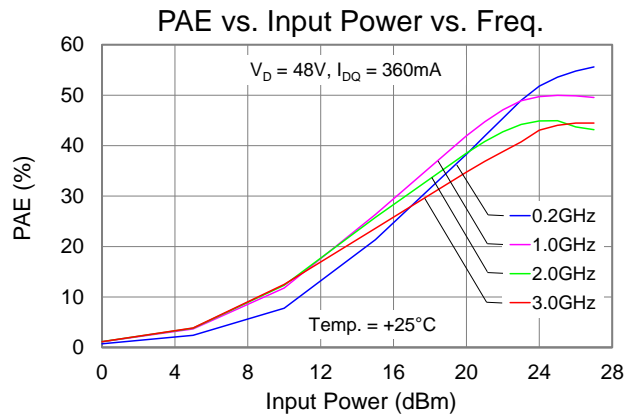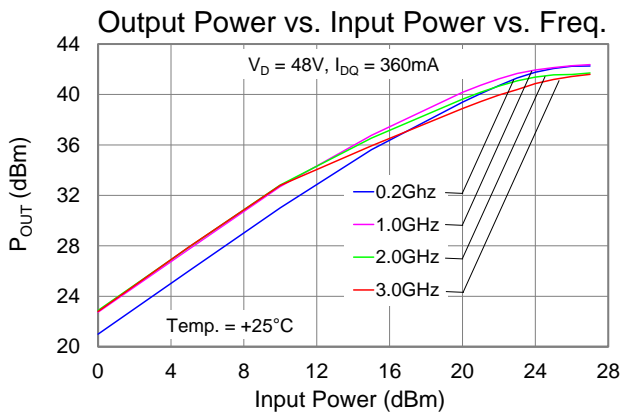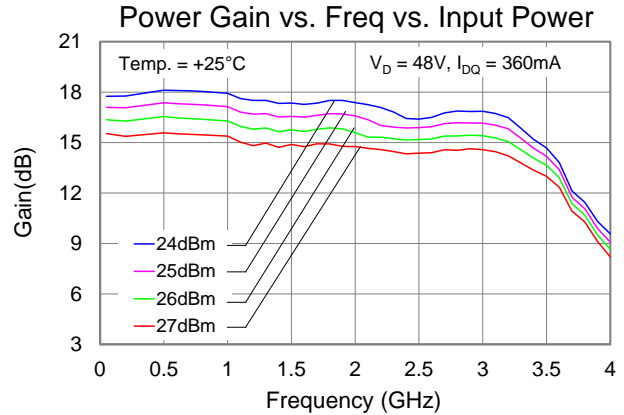Drain Current vs. Frequency vs. Temp.
P_{IN} = 27dBm
-40C
+25C
+85C
V_D = 48V, I_{DQ} = 360mA

Power Gain vs. Freq vs. Input Power
Temp. = +25°C
V_D = 48V, I_{DQ} = 360mA
24dBm
25dBm
26dBm
27dBm

Output Power vs. Input Power vs. Freq.
V_D = 48V, I_{DQ} = 360mA
0.2Ghz
1.0GHz
2.0GHz
3.0GHz
Temp. = +25°C

PAE vs. Input Power vs. Freq.
V_D = 48V, I_{DQ} = 360mA
0.2GHz
1.0GHz
2.0GHz
3.0GHz
Temp. = +25°C

Drain Current vs. Input Power vs. Freq.
0.2Ghz
1.0GHz
2.0GHz
3.0GHz
Temp. = +25°C
V_D = 48V, I_{DQ} = 360mA

Power Gain vs. Input Power vs. Freq.
V_D = 48V, I_{DQ} = 360mA
0.2GHz
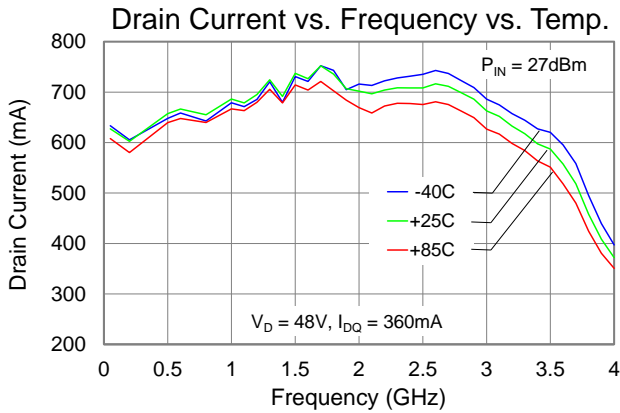1.0GHz
2.0GHz
3.0GHz
Temp. = +25°C

Typical Performance

The plots reflect performance measured with an external coaxial bias tee and DC blocks
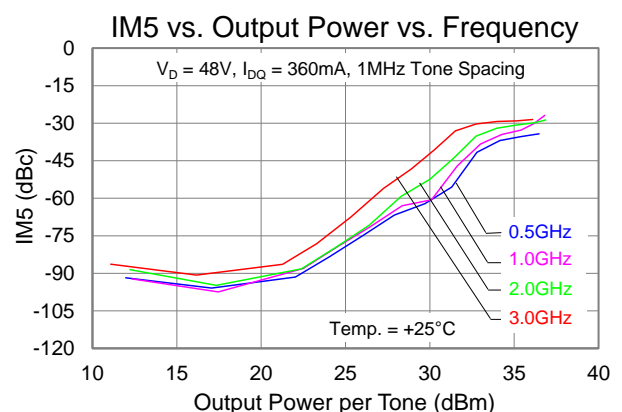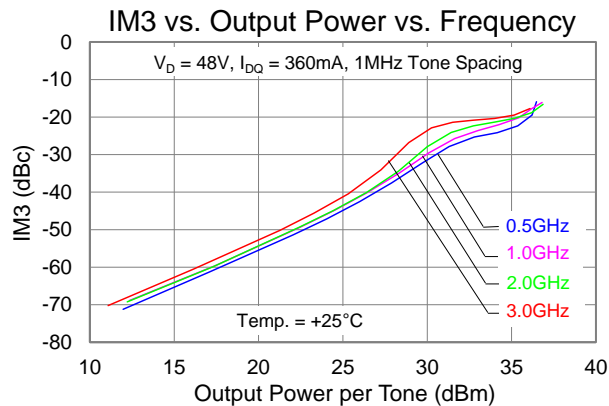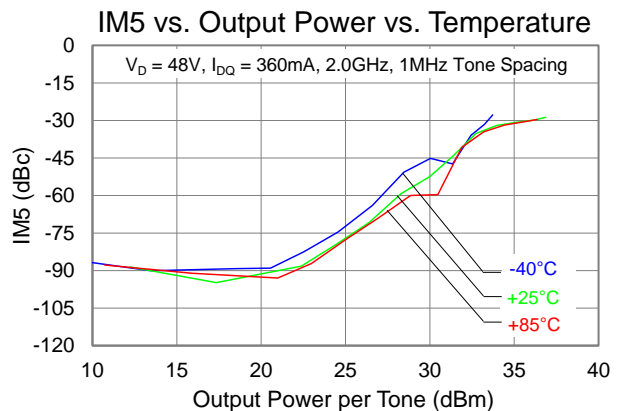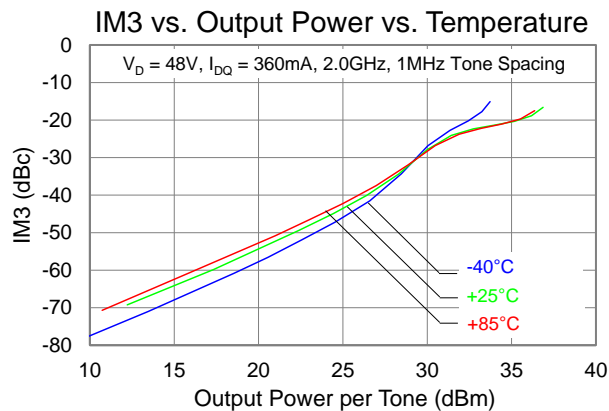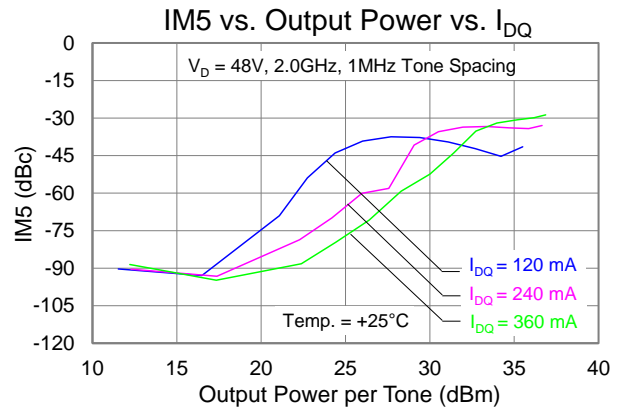(See application circuit on page 10)

IM3 vs. Output Power vs. I_{DQ}

V_D = 48V, 2.0GHz, 1MHz Tone Spacing

IM3 (dBc) vs. Output Power per Tone (dBm)

I_{DQ} = 120 mA
I_{DQ} = 240 mA
I_{DQ} = 360 mA

Temp. = +25°C

IM5 vs. Output Power vs. I_{DQ}

V_D = 48V, 2.0GHz, 1MHz Tone Spacing

IM5 (dBc) vs. Output Power per Tone (dBm)

I_{DQ} = 120 mA
I_{DQ} = 240 mA
I_{DQ} = 360 mA

Temp. = +25°C

IM3 vs. Output Power vs. Temperature

V_D = 48V, I_{DQ} = 360mA, 2.0GHz, 1MHz Tone Spacing

IM3 (dBc) vs. Output Power per Tone (dBm)

-40°C
+25°C
+85°C

IM5 vs. Output Power vs. Temperature

V_D = 48V, I_{DQ} = 360mA, 2.0GHz, 1MHz Tone Spacing

IM5 (dBc) vs. Output Power per Tone (dBm)

-40°C
+25°C
+85°C

IM3 vs. Output Power vs. Frequency

V_D = 48V, I_{DQ} = 360mA, 1MHz Tone Spacing

IM3 (dBc) vs. Output Power per Tone (dBm)

0.5GHz
1.0GHz
2.0GHz
3.0GHz

Temp. = +25°C

IM5 vs. Output Power vs. Frequency

V_D = 48V, I_{DQ} = 360mA, 1MHz Tone Spacing

IM5 (dBc) vs. Output Power per Tone (dBm)

0.5GHz
1.0GHz
2.0GHz
3.0GHz

Temp. = +25°C

Disclaimer: Subject to change without notice
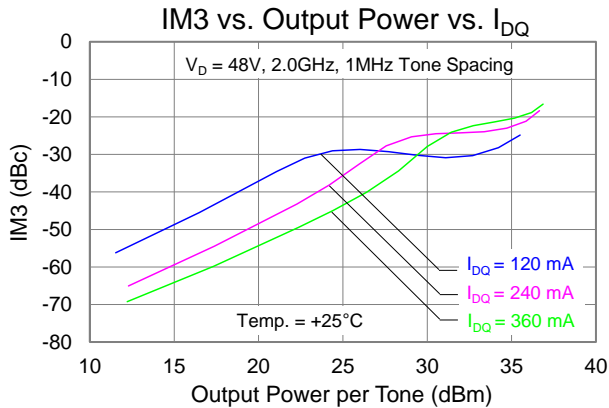www.triquint.com

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Typical Performance

The plots reflect performance measured with an external coaxial bias tee and DC blocks
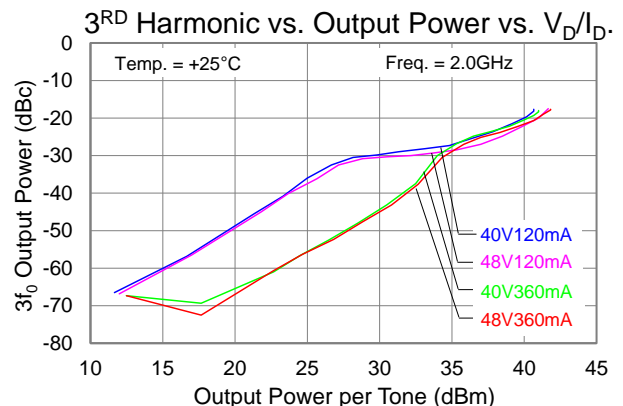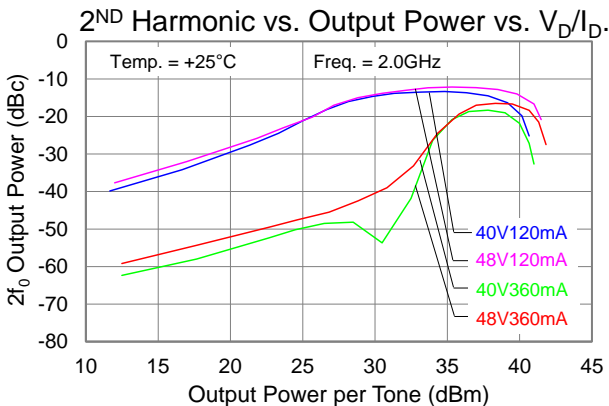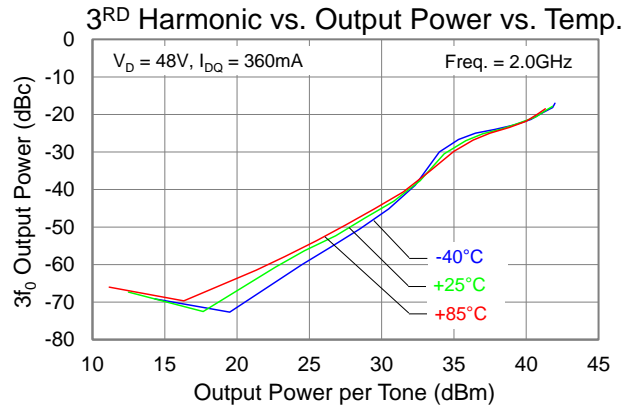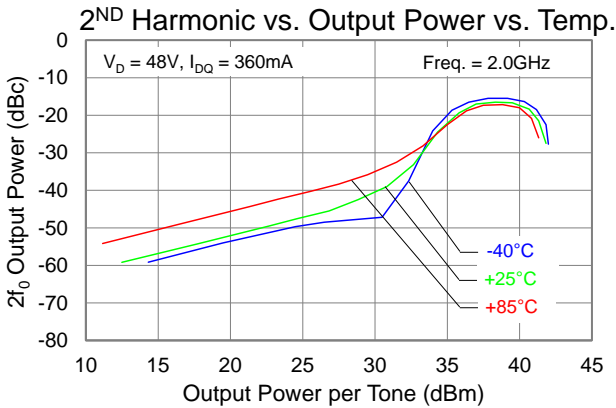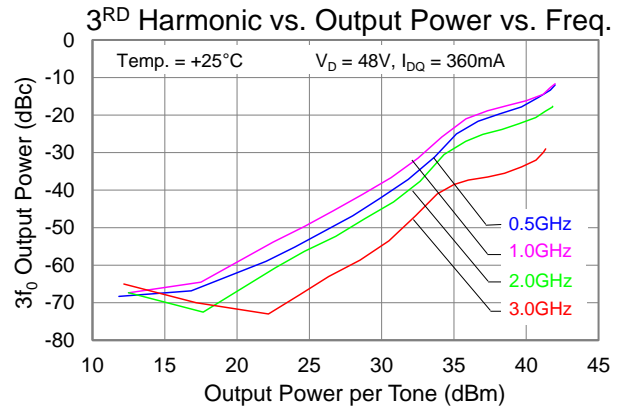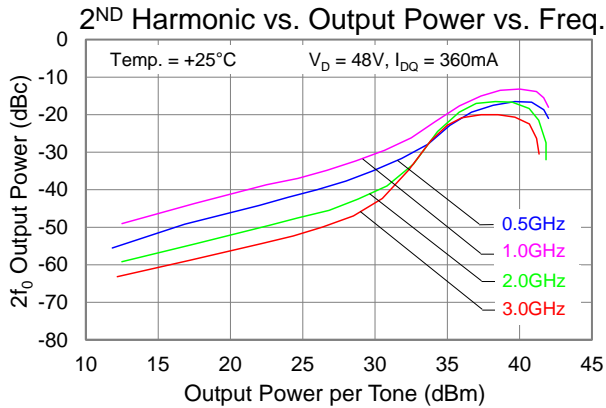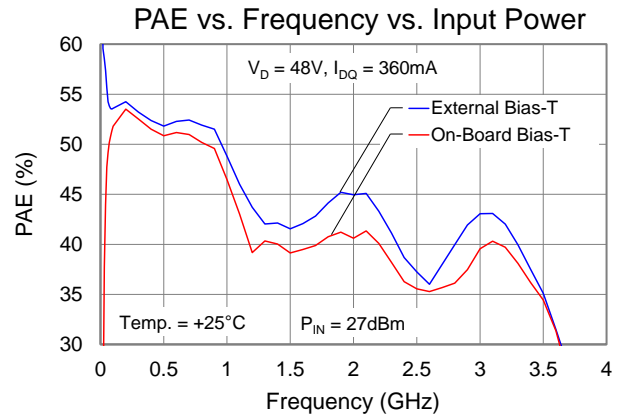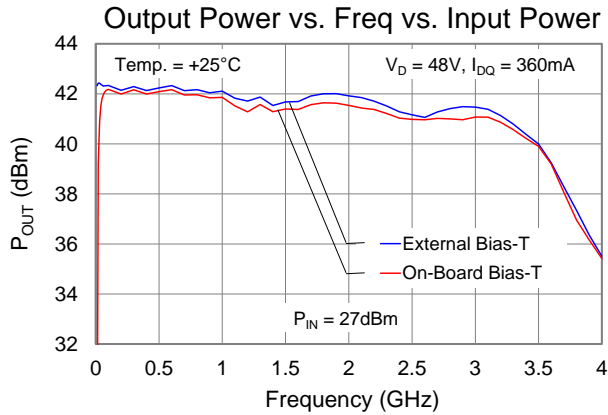(See application circuit on page 10)

2ND Harmonic vs. Output Power vs. Freq.

3RD Harmonic vs. Output Power vs. Freq.

2ND Harmonic vs. Output Power vs. Temp.

3RD Harmonic vs. Output Power vs. Temp.

2ND Harmonic vs. Output Power vs. V_D/I_D.

3RD Harmonic vs. Output Power vs. V_D/I_D.

Typical Performance

The plots below reflect performance measured between external bias tee and on-board bias tee
(See application circuit on pages 10 and 12)

Output Power vs. Freq vs. Input Power

Temp. = +25°C $V_D = 48V$, $I_{DQ} = 360mA$

- External Bias-T
- On-Board Bias-T

$P_{IN} = 27dBm$

P_{OUT} (dBm) vs. Frequency (GHz)

PAE vs. Frequency vs. Input Power

$V_D = 48V$, $I_{DQ} = 360mA$

- External Bias-T
- On-Board Bias-T

Temp. = +25°C $P_{IN} = 27dBm$

PAE (%) vs. Frequency (GHz)

Application Circuit (Coaxial input DC block and coaxial output bias tee)
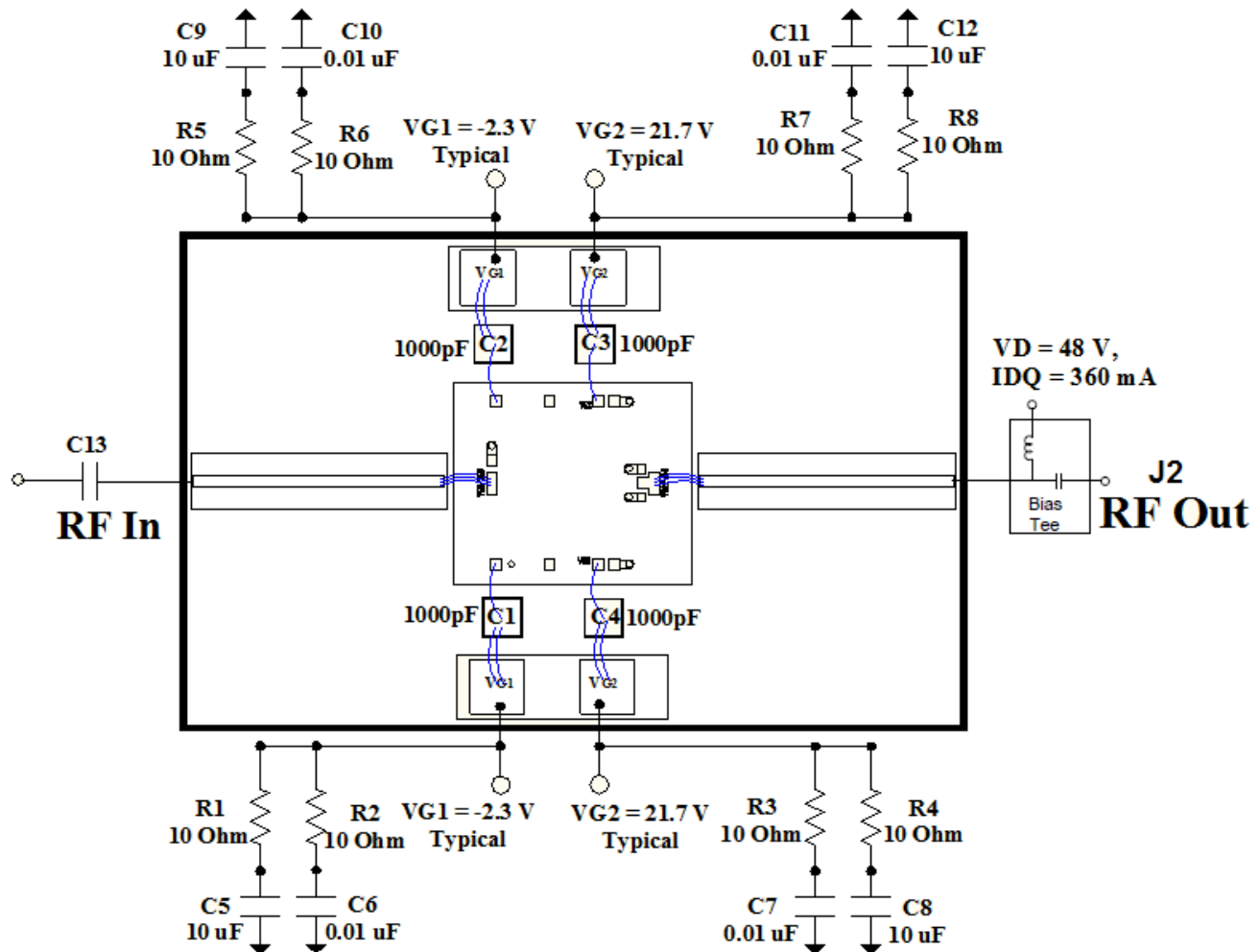
Notes:
1. V_{G1} & V_{G2} can be biased from either side (Top or Bottom.)
2. Coaxial input DC block (C13) is used for input port (RF In.)
3. External wide bandwidth Bias-Tee is used for output port (RF Out). V_D is applied through the output Bias-Tee.

Bias-up Procedure

1. Set I_D limit to 720mA, $I_{G1\ \&}\ I_{G2}$ limit to 5mA

2. Set V_{G1} to -5.0V

3. Set V_{G2} to (V_D/2) - 2.7V or 48V/2 - 2.7V = 21.3V

4. Set V_D +48V

5. Adjust V_{G1} more positive until I_{DQ} = 360mA (V_{G1} ~ -2.3V Typical)

6. Adjust V_{G2} to (V_D/2) + V_{G1}; (V_{G2} ~ 21.7V Typical)

7. Apply RF signal

Bias-down Procedure

1. Turn off RF signal

2. Reduce V_{G1} to -5.0V. Ensure I_{DQ} ~ 0mA

3. Reduce V_{G2} to 0V.

4. Set V_D to 0V

5. Turn off V_D supply

6. Turn off V_{G2} supply

7. Turn off V_{G1} supply

Assembly Drawing (Coaxial input DC block and coaxial output bias tee)
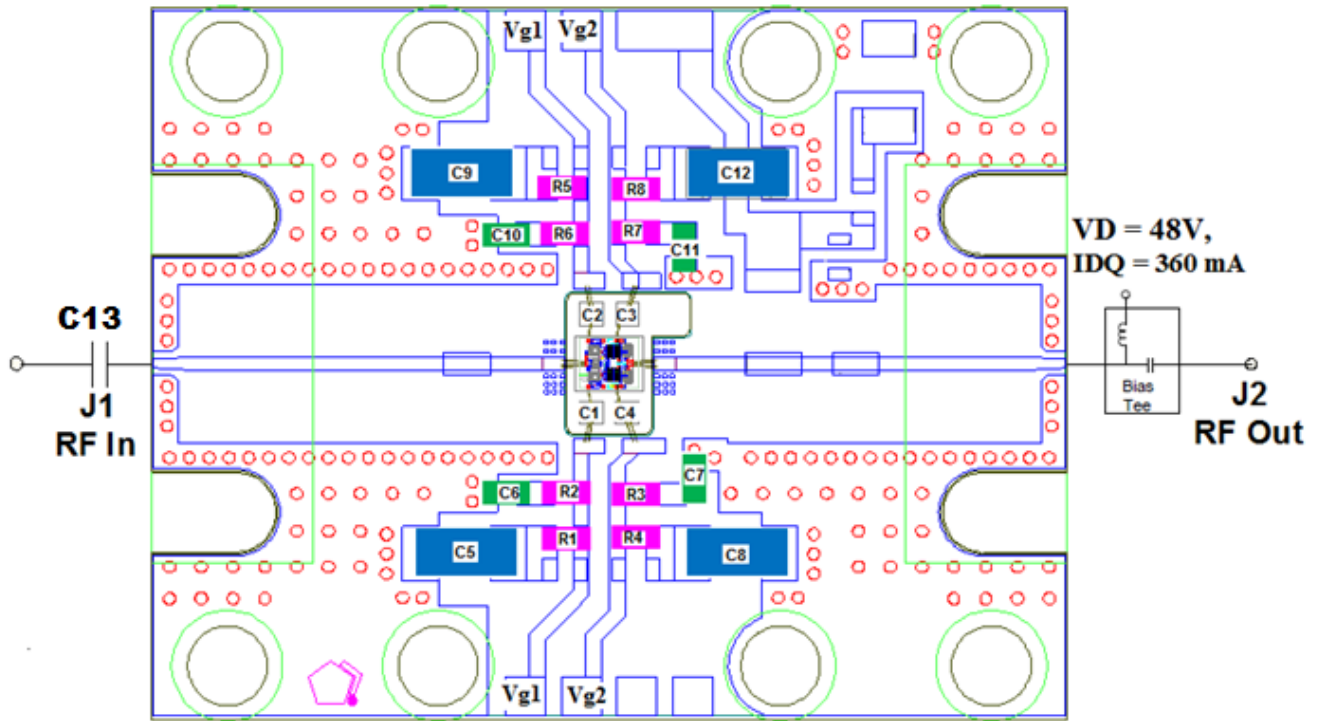
Bill of Materials

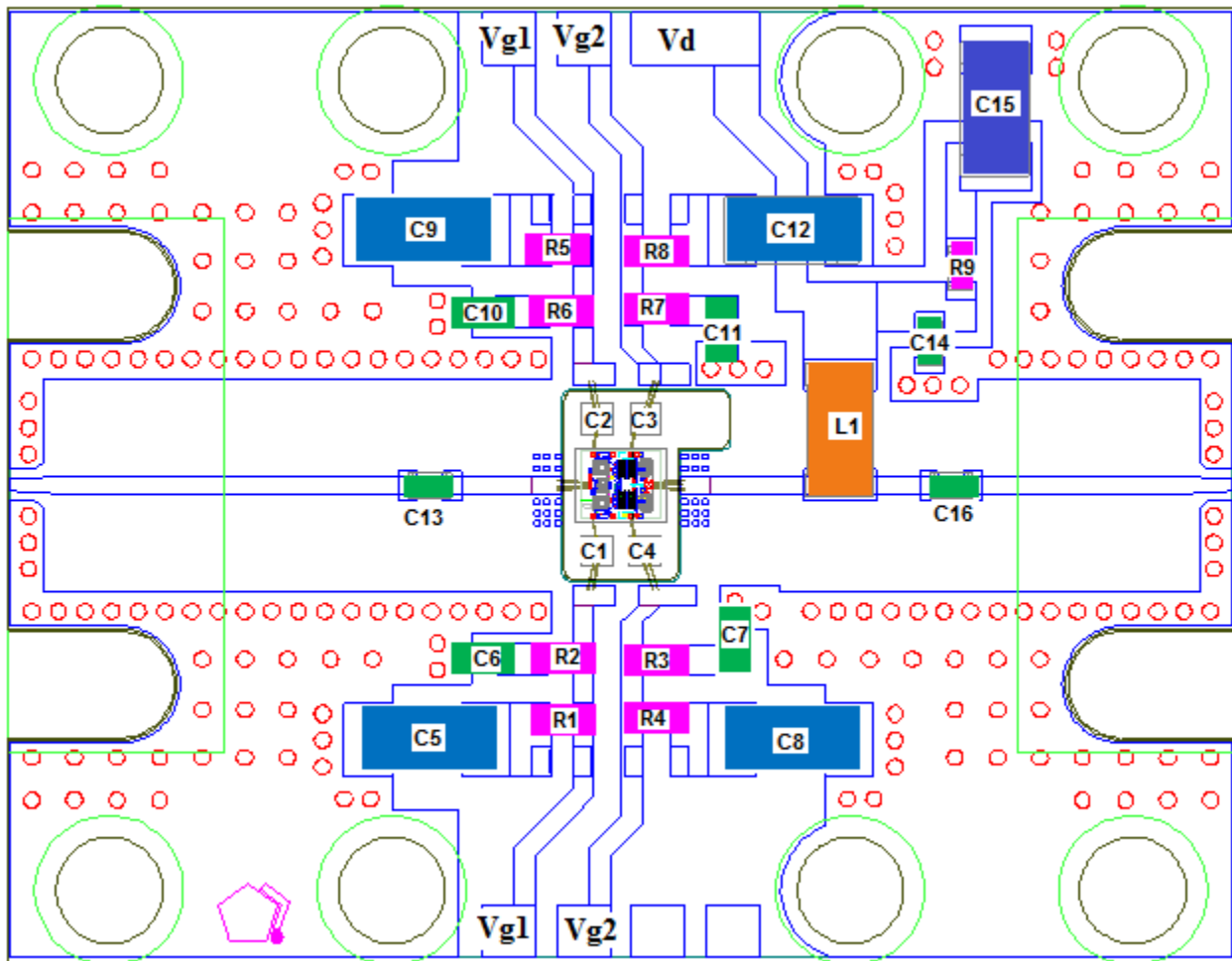| Reference Design	Value	Description	Manufacturer	Part Number
C1 – C4	1000pF	SLC, 50V	Various	
C5, C8, C9, C12	10uF	Cap, 1206, 50V, 10%, X7R	Various	
C6, C7, C10, C11	0.01uF	Cap, 0402, 50V, 10%, X7R	Various	
C13		DC Block	Various	
R1 – R8	10Ω	Res, 0402	Various	

Application Circuit (Option with board-level DC blocks and output bias tee)
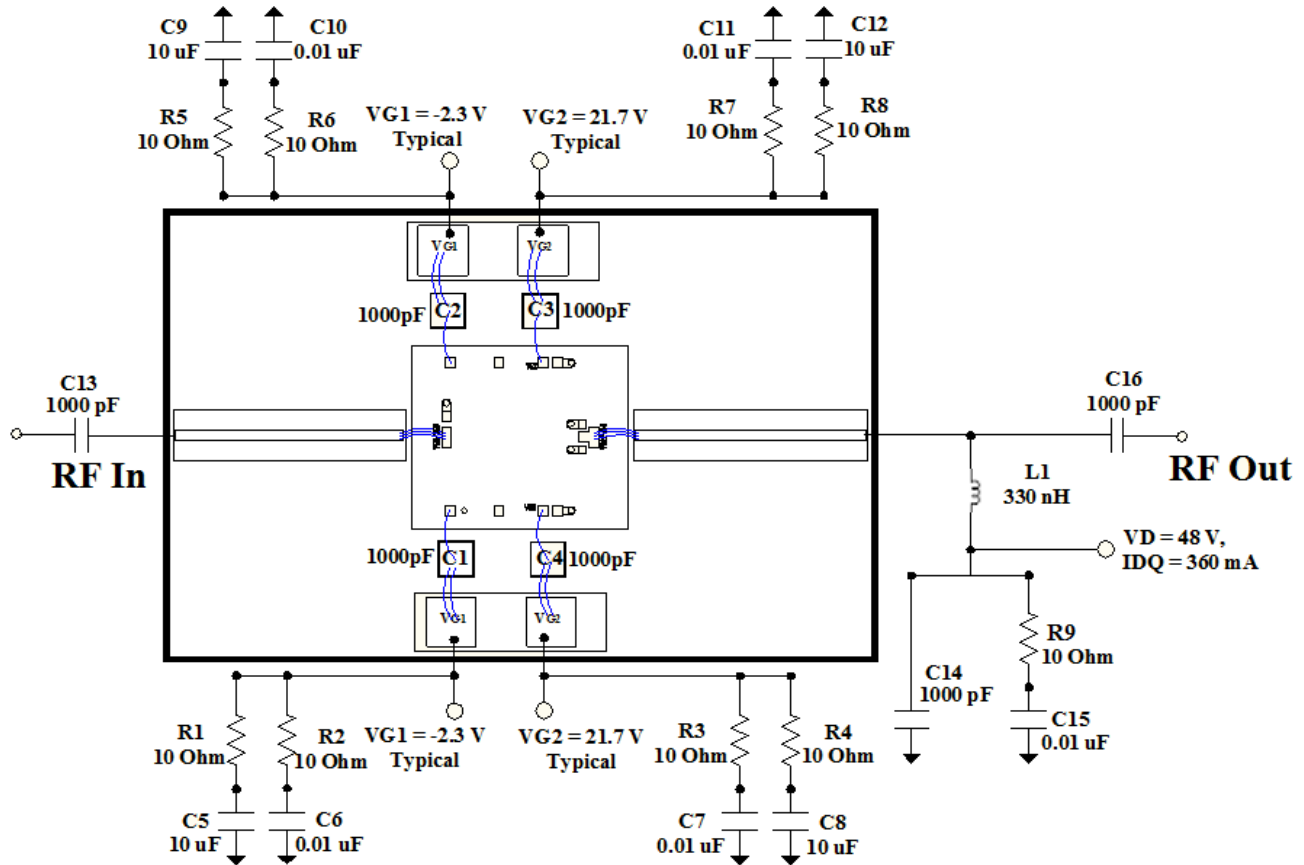
Notes:
1. Performance of the MMIC with surface mount DC blocks and bias tee components may be degraded relative to the coaxial option. These components should be optimized for the desired operational bandwidth.
2. V_{G1} & V_{G2} can be biased from either side (Top or Bottom.)

Evaluation Board Layout with On-Board DC Blocks and Output Bias-T Option

Bill of Materials For On-Board Bias-Tee

Reference Design	Value	Description	Manufacturer	Part Number
C13, C14, C16	1000pF	Cap, 0402, 100V, 10%, X7R	Various	
C15	0.01uF	Cap, 1206, 100V, 10%, X7R	Various	
L1	330nH	Ind, 1206, 100V, 10%, X7R	Various	
R9	10Ω	Res, 0402	Various	

Mechanical Drawing & Bond Pad Description
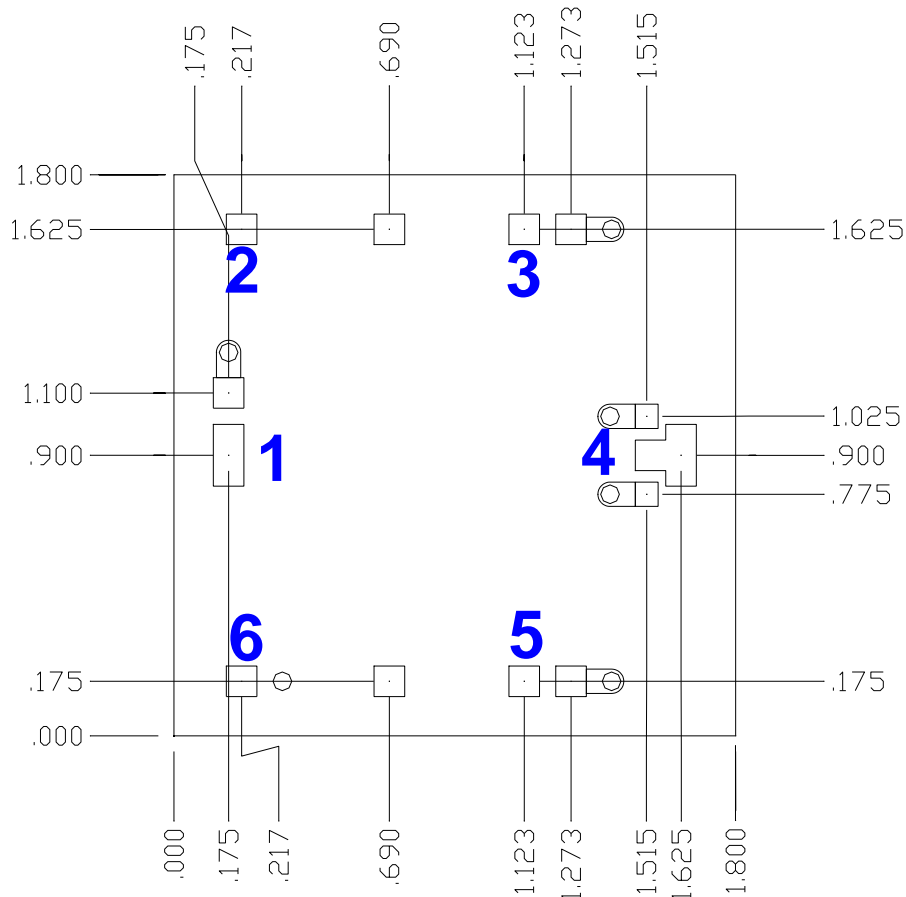
Unit: millimeters
Thickness: 0.10
Die x, y size tolerance: +/- 0.050
Chip edge to bond pad dimensions are shown to center of pad
Ground is backside of die

Bond Pad	Symbol	Pad Size	Description
1	RF In/ V_{G1}	0.098 x 0.198	RF Input; VG1 gate voltage is present here, DC block is required.
2, 6	V_{G1}	0.098 x 0.098	Gate voltage 1, bias network is required; see Application Circuit on pages 10 and 12 as an example.
3, 5	V_{G2}	0.098 x 0.098	Gate voltage 2, bias network is required; see Application Circuit on pages 10 and 12 as an example.
4	RF Out/ V_D	0.098 x 0.198	Output; Drain voltage, bias network is required; see Application Circuit on pages 10 and 12 as an example.

Assembly Notes

Component placement and adhesive attachment assembly notes:
- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment (i.e. epoxy) can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.

Reflow process assembly notes:
- Use AuSn (80/20) solder and limit exposure to temperatures above 300°C to 3-4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:
- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.