TGA2218

13.4 – 16.5 GHz 12 W GaN Power Amplifier

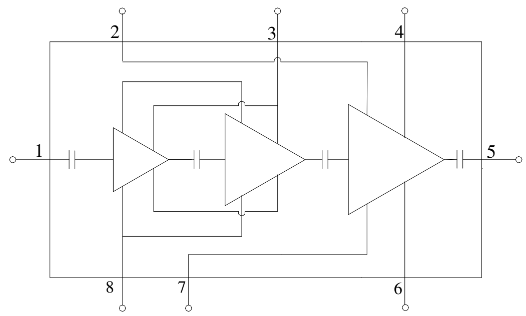
Applications

- Satellite Communications
- Data Link
- Radar

Product Features

- Frequency Range: 13.4 – 16.5 GHz
- P_{SAT}: 41 dBm @ P_{IN} = 18 dBm
- PAE: >28% @ P_{IN} = 18 dBm
- Large Signal Gain: 23 dB
- Small Signal Gain: >26 dB
- Bias: V_D = 28 V, I_{DQ} = 225 mA, V_G = -2.6 V Typical
- Process Technology: TQGaN15
- Chip Dimensions: 3.7 x 1.73 x 0.10 mm
- Performance Under CW Operation

Functional Block Diagram



General Description

TriQuint's TGA2218 is a Ku-band, high power MMIC amplifier fabricated on TriQuint's production 0.15um GaN on SiC process. The TGA2218 operates from 13.4 – 16.5 GHz and provides greater than 12 W of saturated output power with 23 dB of large signal gain and greater than 28% power-added efficiency.

This high performance combination provides system designers the flexibility to improve system performance while reducing size and cost.

The TGA2218 is fully matched to 50 Ohms with integrated DC blocking capacitors on RF ports simplifying system integration. It is ideally suited for military and commercial Ku-band radar and satellite communication systems.

Lead-free and RoHS compliant.

Evaluation boards are available upon request.

Pad Configuration

Pad No.	Symbol
1	RF In
2, 7	V_{G3}
3	V_{D12}
4, 6	V_{D3}
5	RF Out
8	V_{G12}

Ordering Information

Part	ECCN	Description
TGA2218	3A001.b.2.c	13.4 – 16.5 GHz 12 W GaN Power Amplifier

Absolute Maximum Ratings

Parameter	Value
Drain Voltage (V_D)	29.5 V
Gate Voltage Range (V_G)	-8 to -0 V
Drain Current (I_{D1-2})	1.15 A
Drain Current (I_{D3})	1.03 A
Gate Current	See plot on page 3
Power Dissipation (P_{DISS}), 85°C, CW	35 W
Input Power (P_{IN}), CW, 50Ω, V_D = 28 V, I_{DQ} = 225 mA, 85°C	30 dBm
Input Power (P_{IN}), CW, VSWR 3:1, V_D = 28 V, I_{DQ} = 225 mA, 85°C	27 dBm
Channel Temperature (T_{CH})	275°C
Mounting Temperature (30 seconds)	320°C
Storage Temperature	-40 to 150°C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value
Drain Voltage (V_D)	28 V
Drain Current (I_{DQ})	225 mA (Total)
Gate Voltage (V_G)	-2.6 V (Typ.)

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: 25°C , V_D = 28 V, I_{DQ} = 225 mA, V_G = -2.6 V Typical, CW

Parameter	Min	Typical	Max	Units
Operational Frequency Range	13.4		16.5	GHz
Small Signal Gain		>26		dB
Input Return Loss		>13		dB
Output Return Loss		>3		dB
Power Gain (Pin = 18dBm)		23		dB
Output Power (Pin = 18dBm)		41		dBm
Power Added Efficiency (Pin = 18dBm)		>28		%
Small Signal Gain Temperature Coefficient		-0.06		dB/°C
Output Power Temperature Coefficient (Temp: 25°C – 85°C @ Pin = 18dBm)		-0.01		dB/°C
Recommended Operating Voltage		20 to 28	28	V

Thermal and Reliability Information

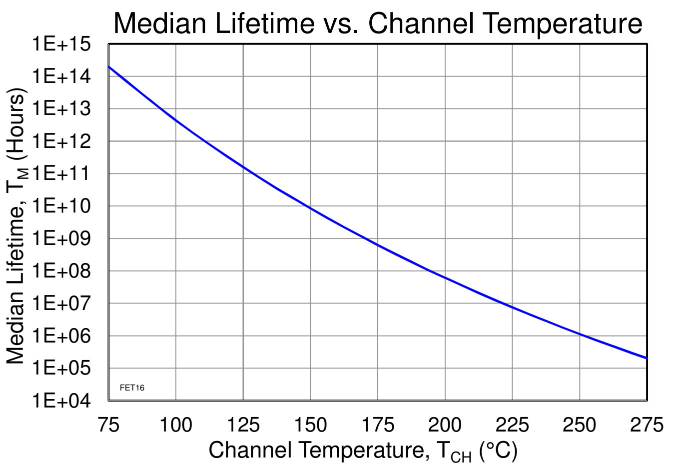
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) [1]	T_{base} = 85°C	4.93	ºC/W
Channel Temperature (T_{CH}) (No RF drive)	V_D = 28 V, I_{DQ} = 225 mA	116	°C
Median Lifetime (T_M)	P_{DISS} = 6.3 W	4.9 x 10^11	Hrs

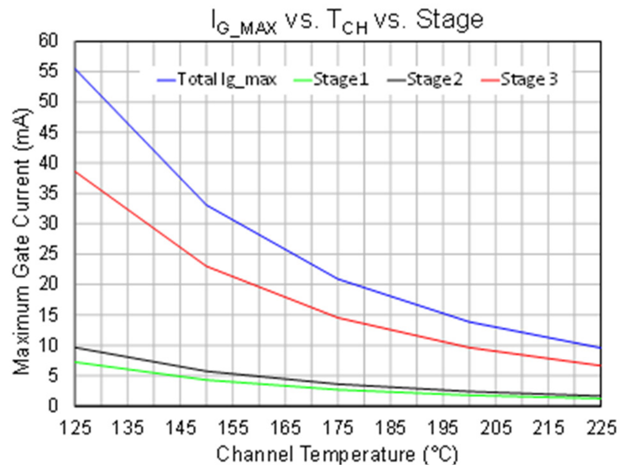
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) [1]	T_{base} = 85°C, CW , V_D = 28 V, I_{DQ} = 225 mA	5.36	ºC/W
Channel Temperature (T_{CH}) (Under RF drive)	Freq = 14.75 GHz, I_{D_Drive} = 1.45 A,	245	°C
Median Lifetime (T_M)	P_{IN} = 20 dBm, P_{OUT} = 40.5 dBm, P_{DISS} = 29.8 W	1.6 x 10^6	Hrs

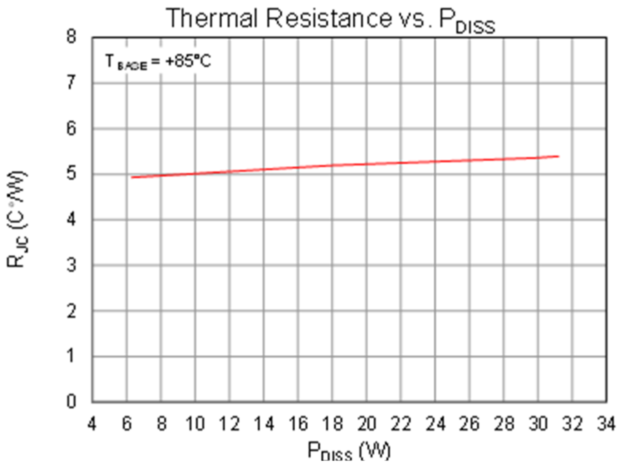
Notes:
1. Thermal resistance measured to back of carrier plate. MMIC mounted on 40 mils CuMo (75/25) carrier using 1.5 mil AuSn.

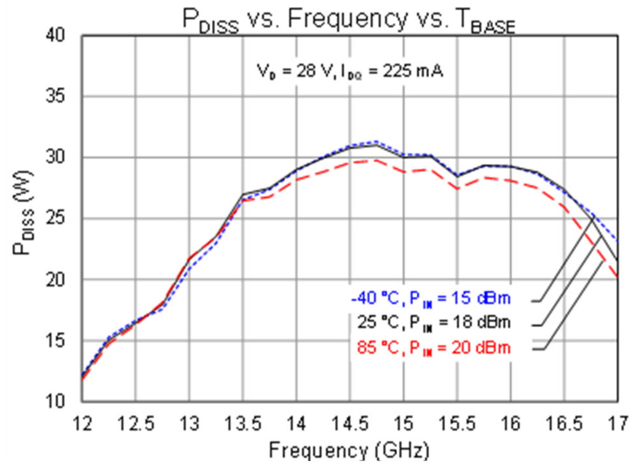
Median Lifetime

Test Conditions: V_D = +28 V; Failure Criteria = 10% reduction in ID_MAX During DC Life Testing

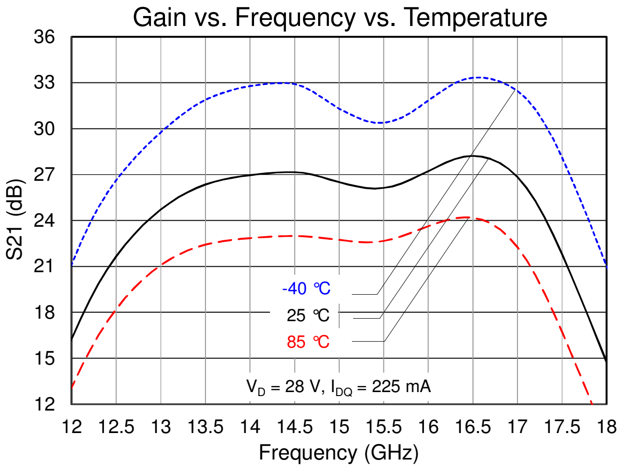


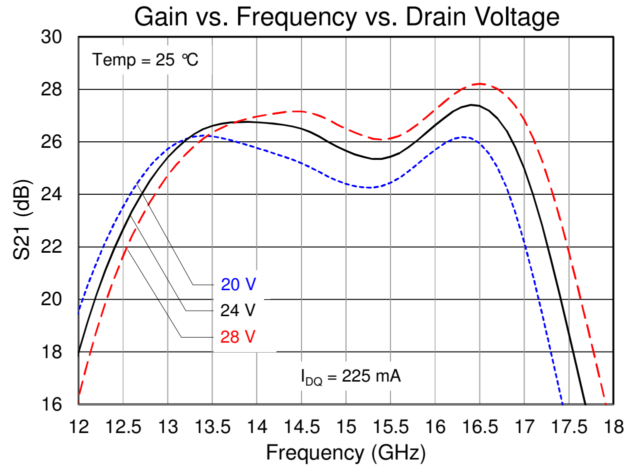


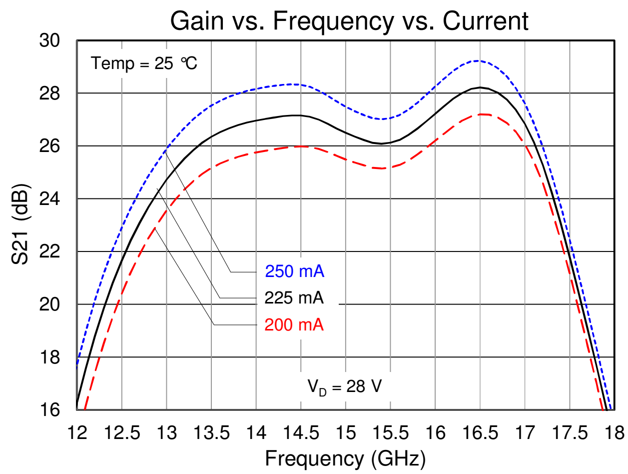


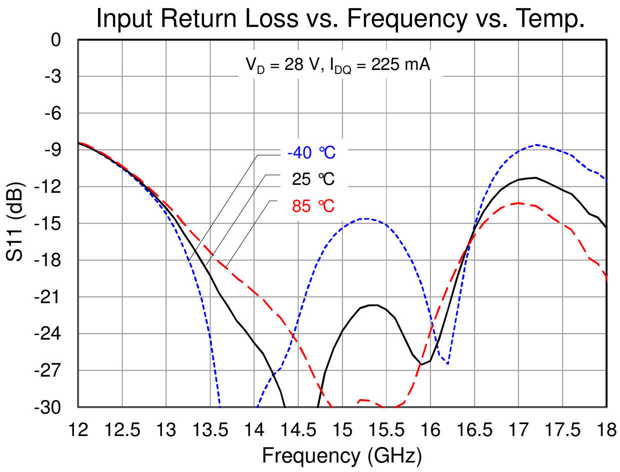


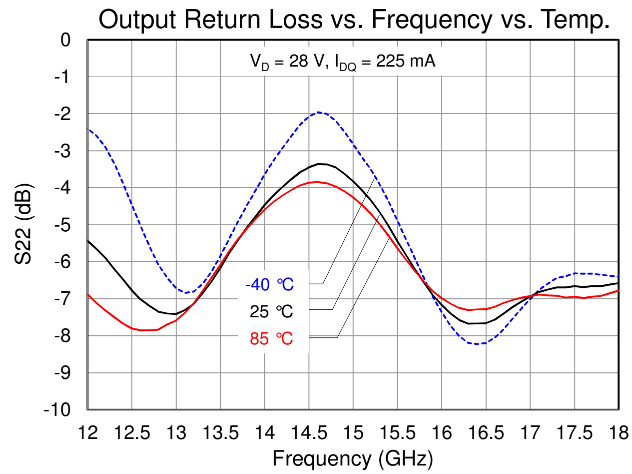
Typical Performance (Small Signal)



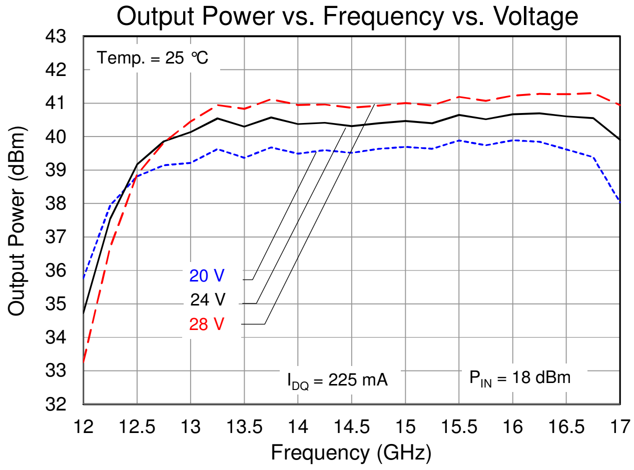


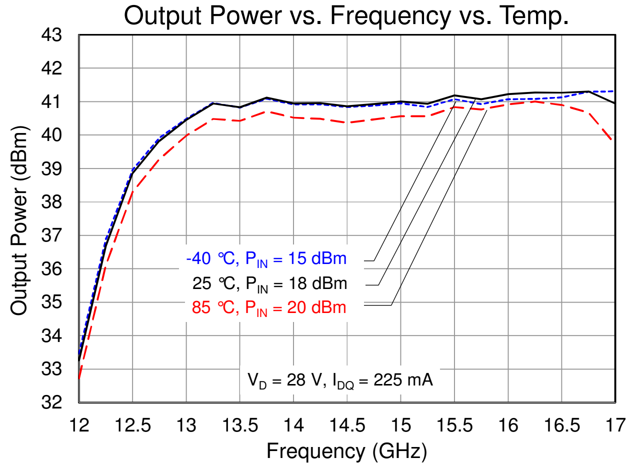


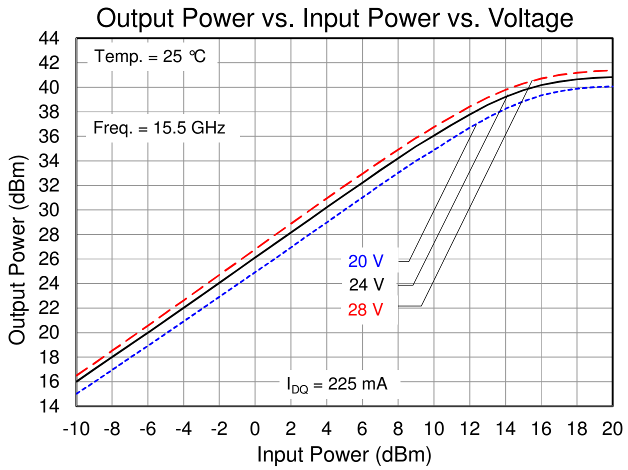


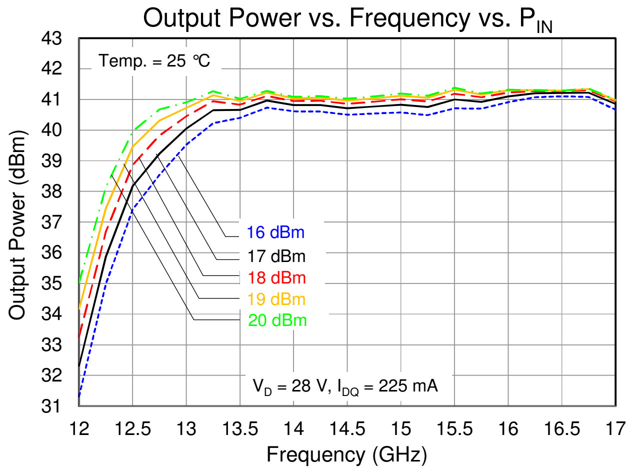


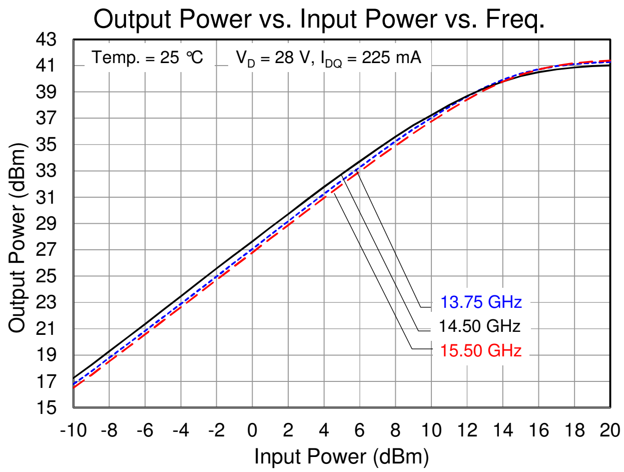
Typical Performance (CW Operation)











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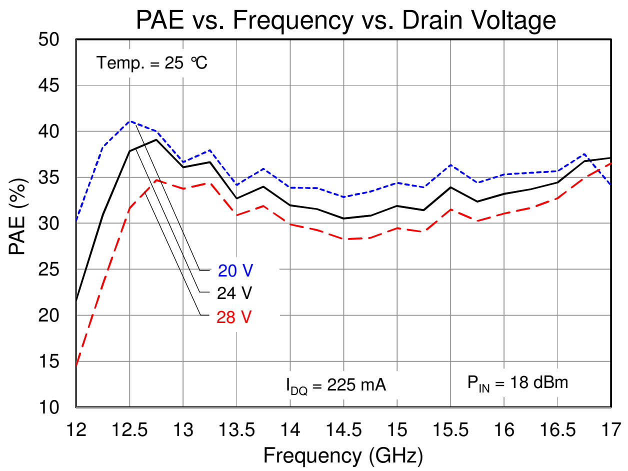

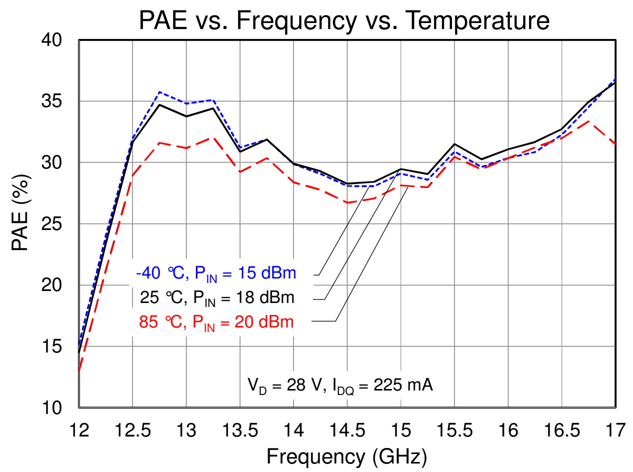

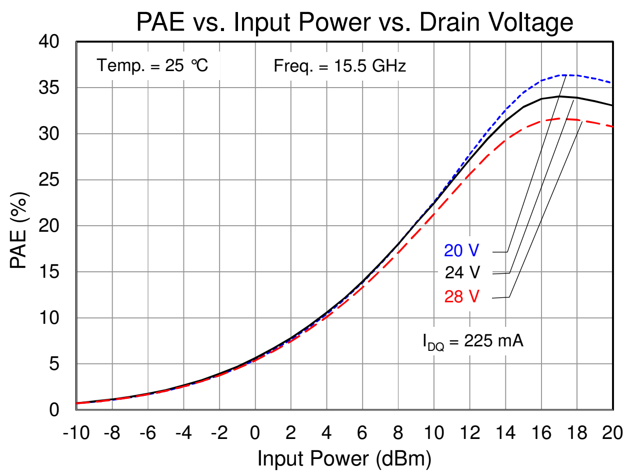

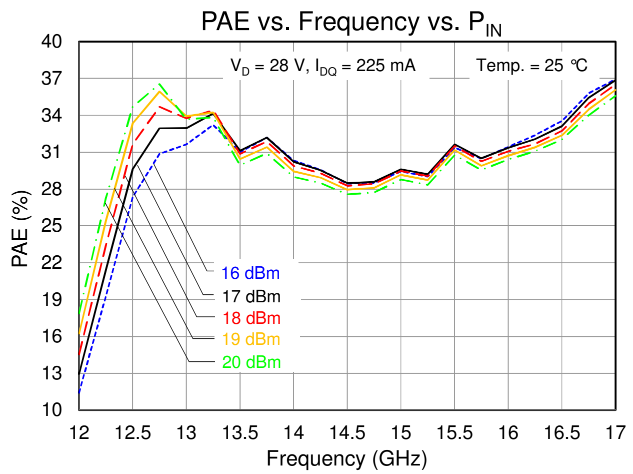

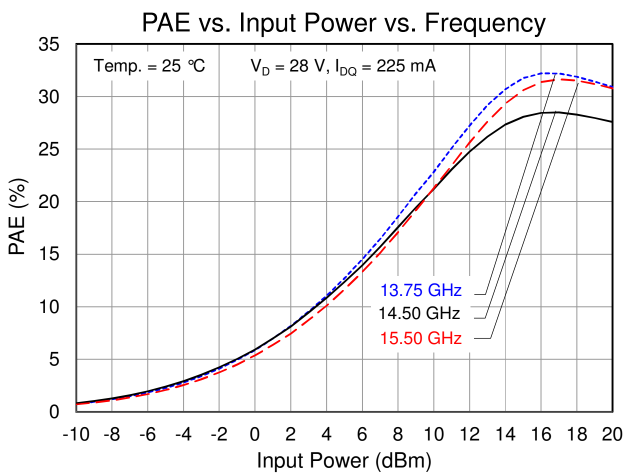

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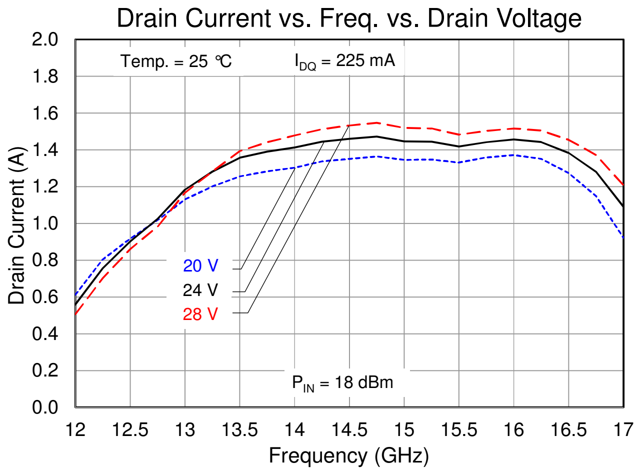

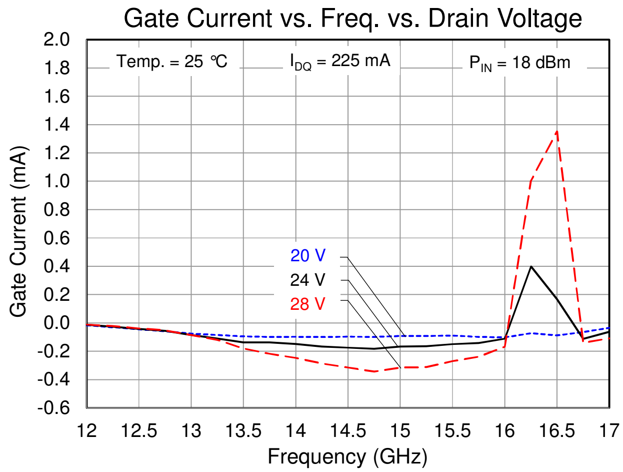

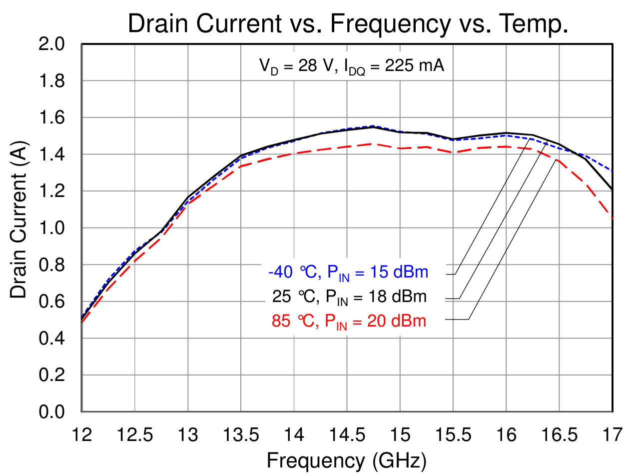

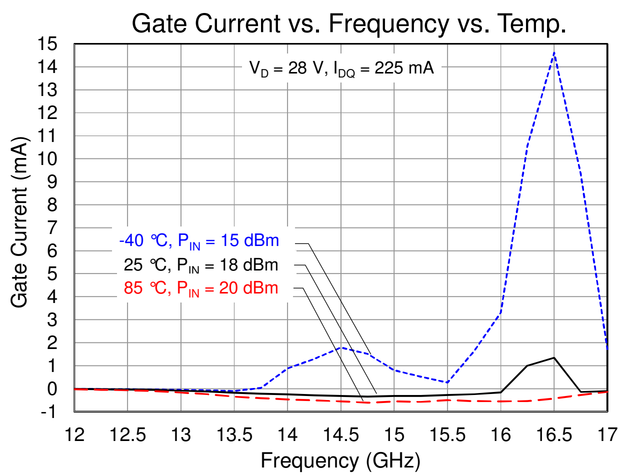

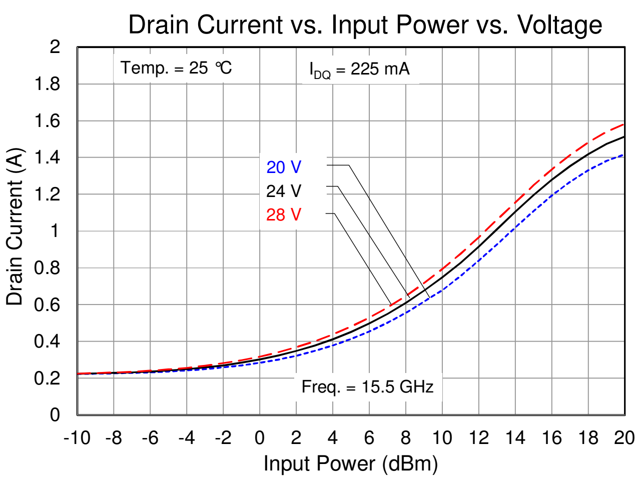

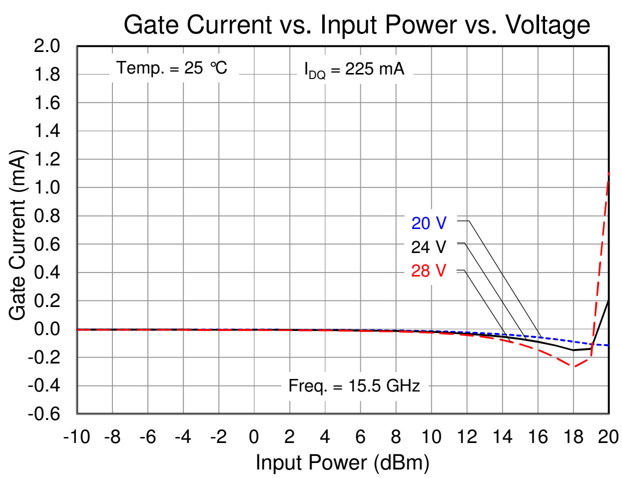

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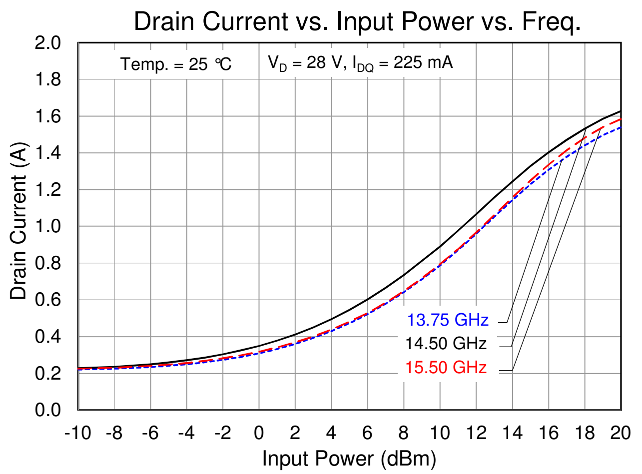
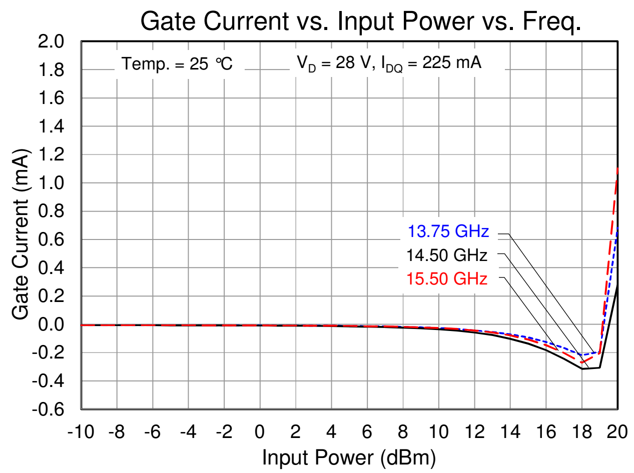
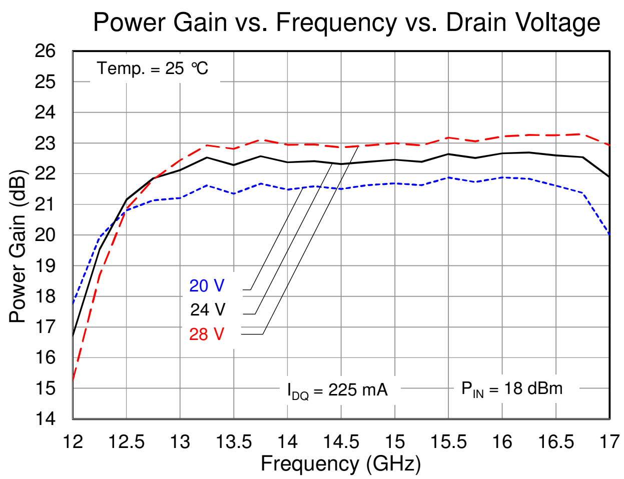
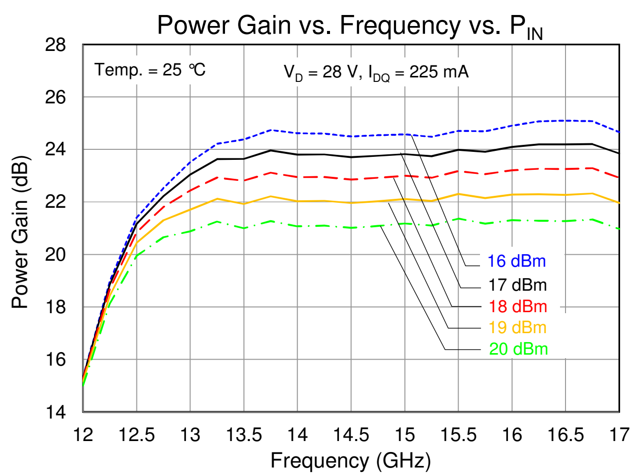
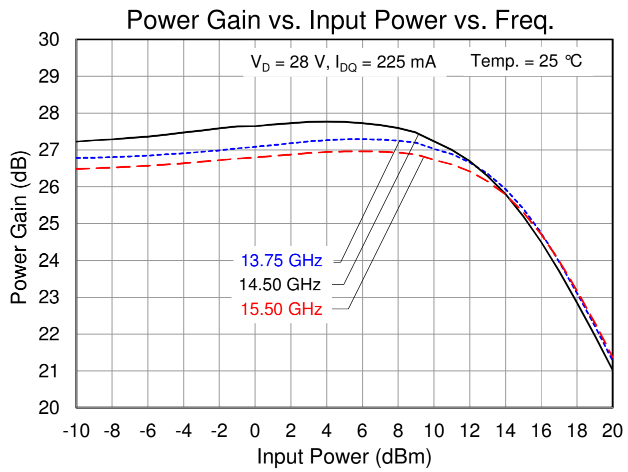
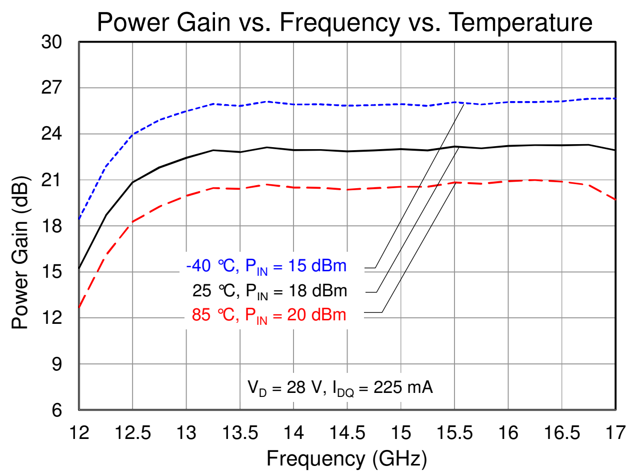




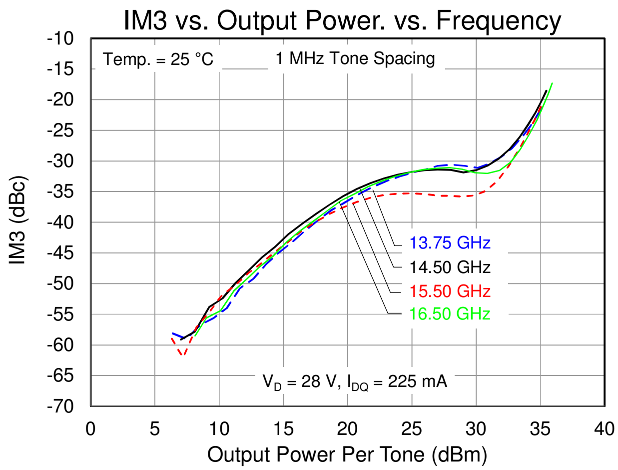


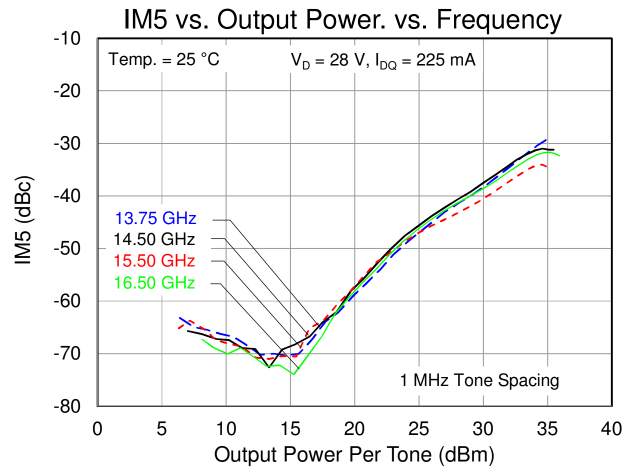


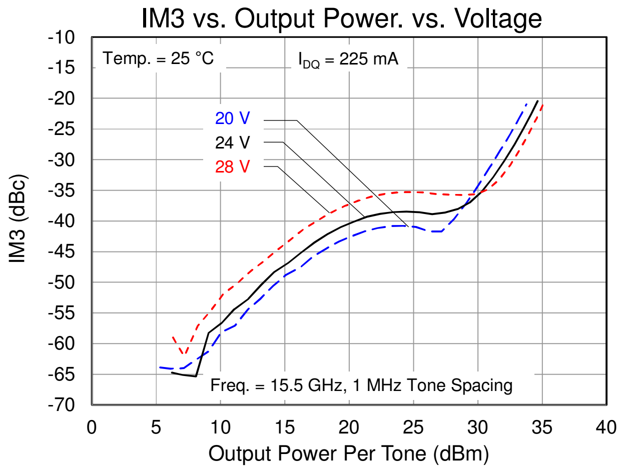


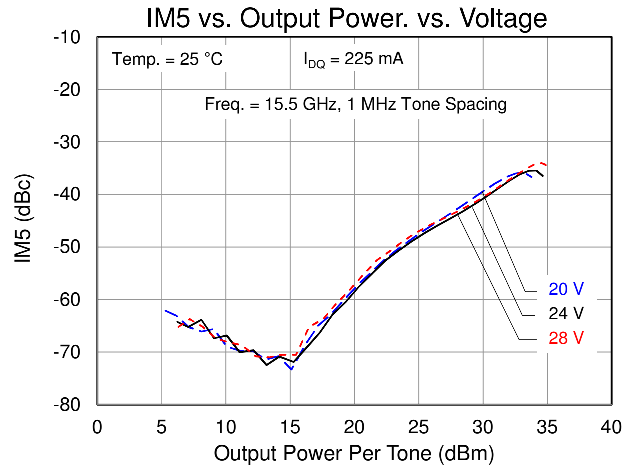


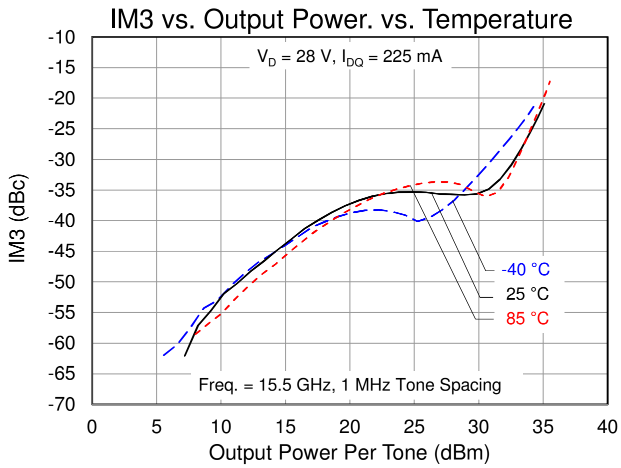
Typical Performance (Linearity)

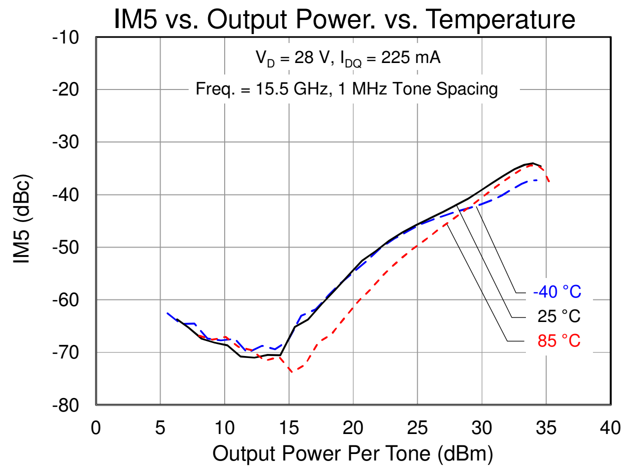




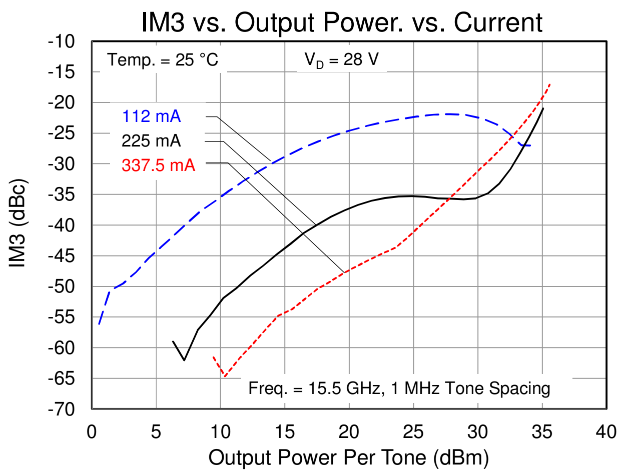


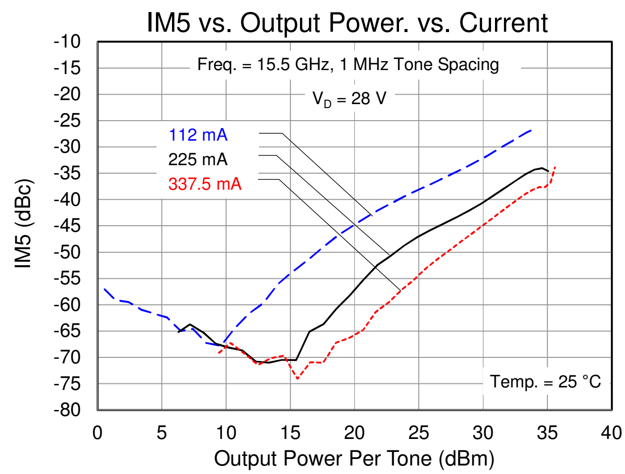


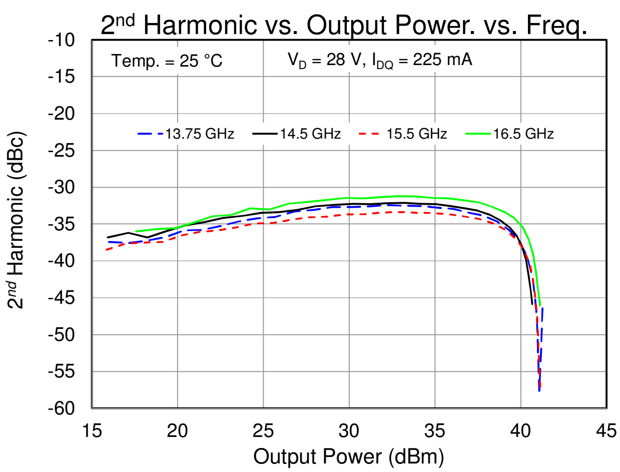


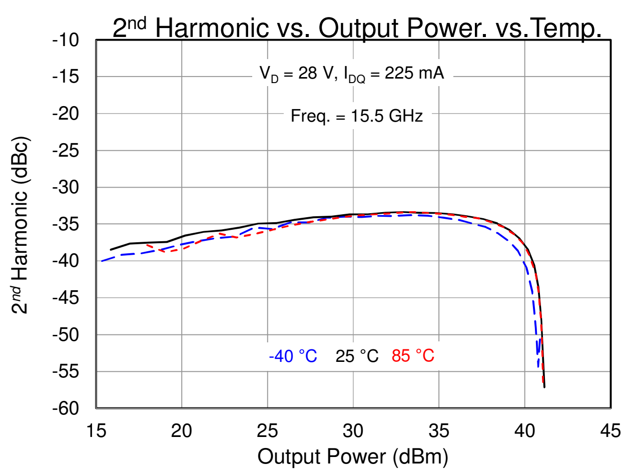


Typical Performance (Linearity)

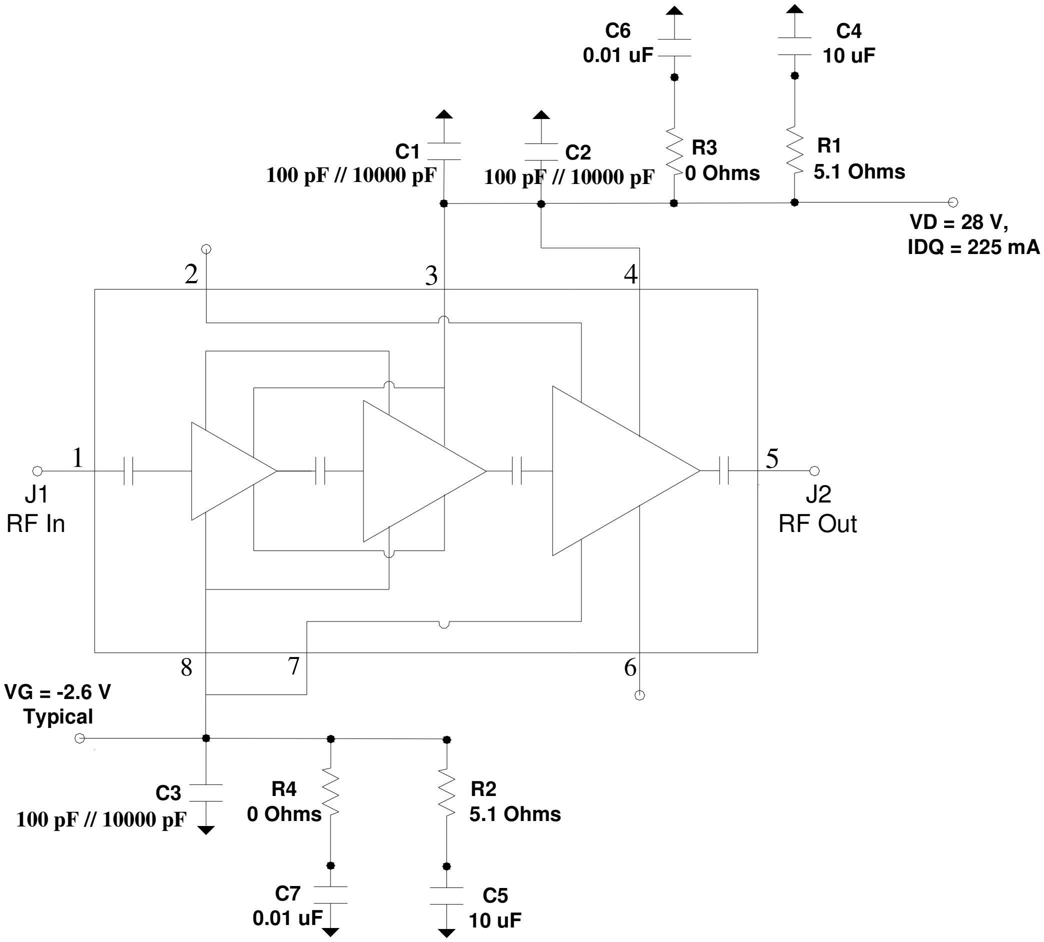








Application Circuit



Notes:

V_{G3} & V_{D3} can be biased from either side of top or bottom.

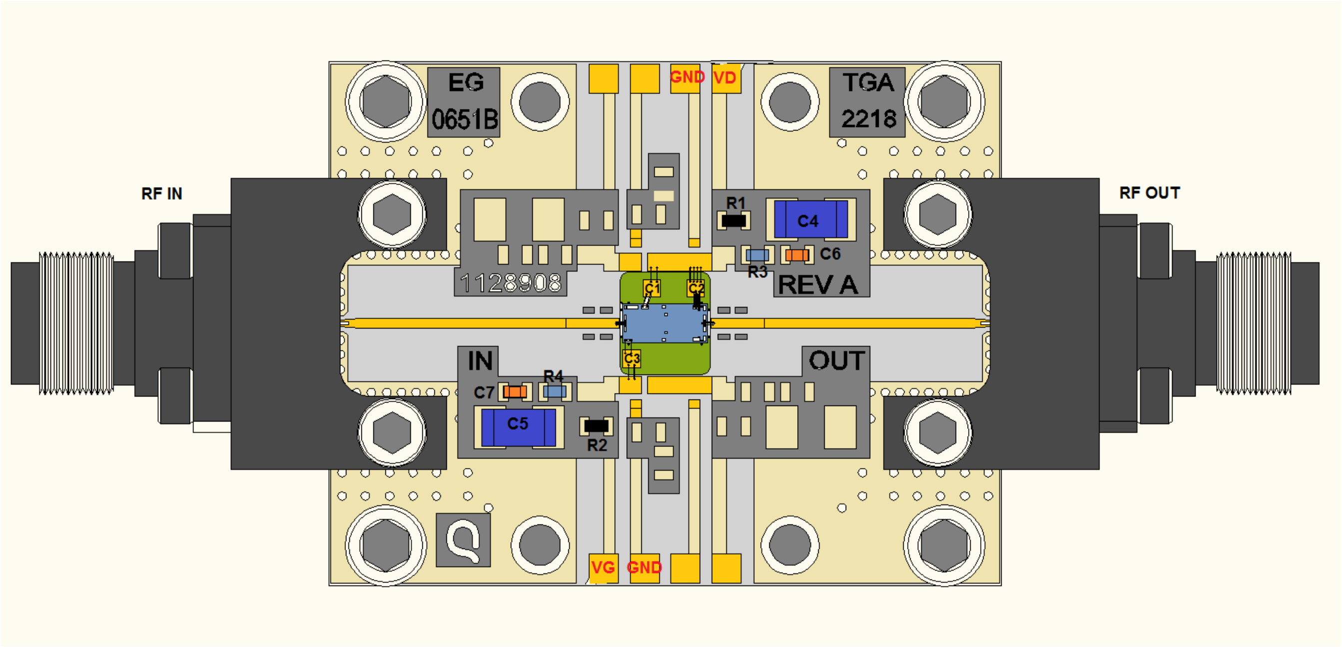
Bias-up Procedure

1. Set I_D limit to 1.8 A, I_G limit to 20 mA
2. Set V_G to -5.0 V
3. Set V_D +28 V
4. Adjust V_G more positive until I_{DQ} = 225 mA (V_G ~ -2.6V Typical)
5. Apply RF signal

Bias-down Procedure

1. Turn off RF signal
2. Reduce V_G to -5.0 V. Ensure I_{DQ} ~ 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Evaluation Board (EVB) Layout Assembly

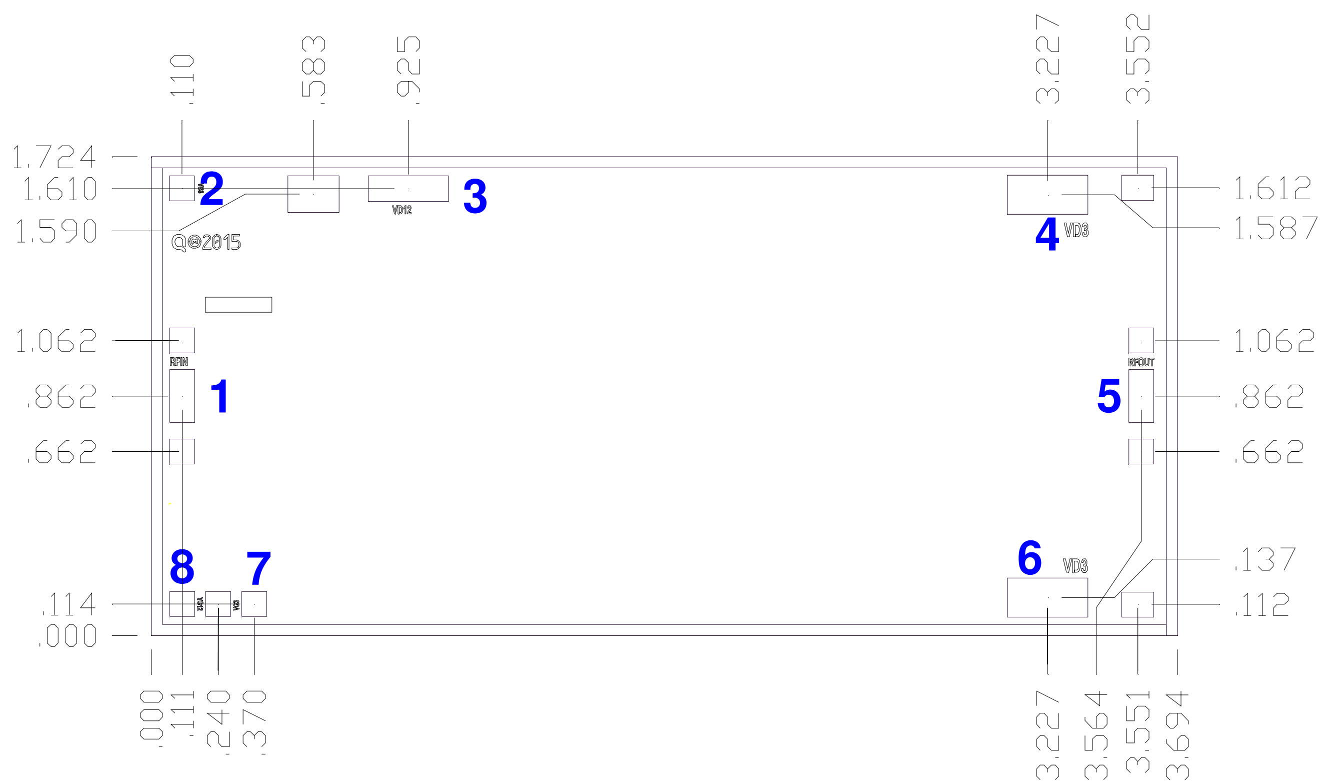


Notes: V_{G3} & V_{D3} can be biased from either side of top or bottom.

Bill of Materials

Reference Design	Value	Description	Manufacturer	Part Number
C1 – C3	100 pF || 10000 pF	SLC, 50V	Various	
C4, C5	10 uF	Cap, 1206, 50V, 20%, X5R	Various	
C6, C7	0.01uF	Cap, 0402, 50V, 10%, X7R	Various	
R1, R2	5.1 Ω	Res, 0402, 5%, SMT	Various	
R3, R4	0 Ω	Res, 0402, 5%, SMD	Various	

Mechanical Drawing & Bond Pad Description



Unit: millimeters
Thickness: 0.10
Die x, y size tolerance: +/- 0.050
Chip edge to bond pad dimensions are shown to center of pad
Ground is backside of die

Bond Pad	Symbol	Pad Size	Description
1	RF In	0.090 x 0.190	RF Input; matched to 50Ω; DC Blocked
2, 7	V_{G3}	0.090 x 0.090	Gate voltage 3, bias network is required; see Application Circuit on page 11 as an example.
3	V_{D12}	0.290 x 0.092	Drain voltage 1-2, bias network is required; see Application Circuit on page 11 as an example.
4, 6	V_{D3}	0.290 x 0.140	Drain voltage 3, bias network is required; see Application Circuit on page 11 as an example.
5	RF Out	0.090 x 0.190	RF Input; matched to 50Ω; DC Blocked
8	V_{G12}	0.090 x 0.090	Gate voltage 1-2, bias network is required; see Application Circuit on page 11 as an example.

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment (i.e. epoxy) can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300°C to 3-4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.