TGA2239

13 – 15.5 GHz 35 W GaN Power Amplifier

Product Description

Qorvo's TGA2239 is a Ku-band, high power MMIC amplifier fabricated on Qorvo's production 0.15 um GaN on SiC process. The TGA2239 operates from 13 – 15.5 GHz and provides a superior combination of power, gain and efficiency by achieving greater than 35 W of saturated output power with 24.5 dB of large signal gain and greater than 32 % power-added efficiency.

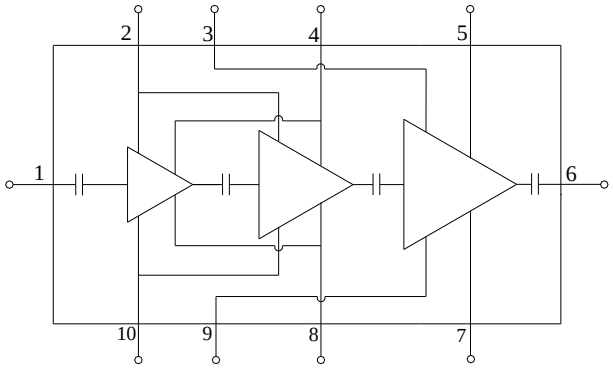
This superior performance provides system designers the flexibility to improve system performance while reducing size and cost.

The TGA2239 is fully matched to 50 Ω with integrated DC blocking capacitors on RF ports simplifying system integration. It is ideally suited for military and commercial Ku-band radar and satellite communication systems.

Lead-free and RoHS compliant.

Evaluation boards are available upon request.

Functional Block Diagram



Product Features

- Frequency Range: 13 – 15.5 GHz
- P_{SAT} : >45.5 dBm @ P_{IN} = 21 dBm
- PAE: >32 % @ P_{IN} = 21 dBm
- Large Signal Gain: >24.5 dB
- Small Signal Gain: 29.5 dB
- Bias: V_D = +22 V, I_{DQ} = 900 mA, V_G = −2.7 V Typical
- Process Technology QGaN15
- Chip Dimensions: 5.00 x 6.65 x 0.10 mm
- Performance Under CW Operation

Applications

- Satellite Communications
- Data Link
- Radar

Ordering Information

Part No.	ECCN	Description
TGA2239	3A001.b.2.b	13 – 15.5 GHz 35 W GaN Power Amplifier

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	29.5 V
Gate Voltage Range (V_G)	−5 to 0 V
Drain Current (I_{D1-2})	2.8 A
Drain Current (I_{D3})	4.3 A
Gate Current (I_{G1-2}) @ T_{CH} = 200 °C	−5 to 14.5 mA
Gate Current (I_{G3}) @ T_{CH} = 200 °C	−12.5 to 38 mA
Power Dissipation (P_{DISS}), 85°C, CW	117 W
Input Power (P_{IN}), CW, 50 Ω, V_D = +22 V, I_{DQ} = 900 mA, 85 °C	33 dBm
Input Power (P_{IN}), CW, VSWR 3:1, V_D = +22 V, I_{DQ} = 900 mA, 85 °C	30 dBm
Channel Temperature (T_{CH})	275 °C
Mounting Temperature (30 seconds)	320 °C
Storage Temperature	−55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

P_{IN}

Recommended Operating

Parameter	Value / Range
Drain Voltage (V_D)	+22 V
Drain Current (I_{DQ})	900 mA (Total)
Gate Voltage (V_G)	−2.7 V (Typ.)

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Min	Typ	Max	Units
Operational Frequency Range	13	–	15.5	GHz
Small Signal Gain	–	29.5	–	dB
Input Return Loss	–	>13	–	dB
Output Return Loss	–	>7.5	–	dB
Power Gain (P_{IN} = 21 dBm)	–	>24.5	–	dB
Output Power (P_{IN} = 21 dBm)	–	>45.5	–	dBm
Power Added Efficiency (P_{IN} = 21 dBm)	–	>32	–	%
Small Signal Gain Temperature Coefficient	–	−0.09	–	dB/°C
Output Power Temperature Coefficient	–	−0.028	–	dB/°C

Test conditions unless otherwise noted: 25 °C , V_D = +22 V, I_{DQ} = 900 mA, V_G = −2.7 V Typical, CW

Thermal and Reliability Information

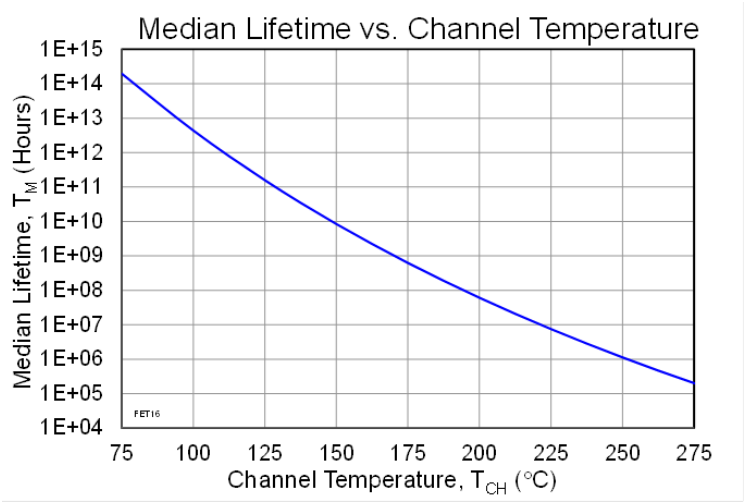
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C V_D = +22 V, I_{DQ} = 900 mA P_{DISS} = 19.8 W	1.26	ºC/W
Channel Temperature (T_{CH}) (No RF drive)		110	°C
Median Lifetime (T_M)		4.0 x 10^14	Hrs

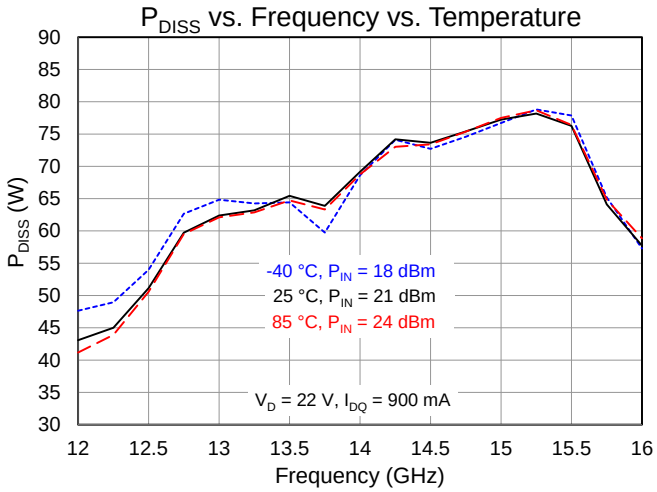
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, CW , V_D = +22 V, I_{DQ} = 900 mA Freq = 15.25 GHz, V_D = +22 V, I_{D_Drive} = 5 A, P_{OUT} = 24 dBm, P_{OUT} = 45.2 dBm, P_{DISS} = 79 W	1.13	ºC/W
Channel Temperature (T_{CH}) (Under RF drive)		174	°C
Median Lifetime (T_M)		3.46 x 10^10	Hrs

Notes:
1. Thermal resistance measured to back of carrier plate. MMIC mounted on 40 mils CuMo (80/20) carrier using 1.5 mil AuSn.

Median Lifetime

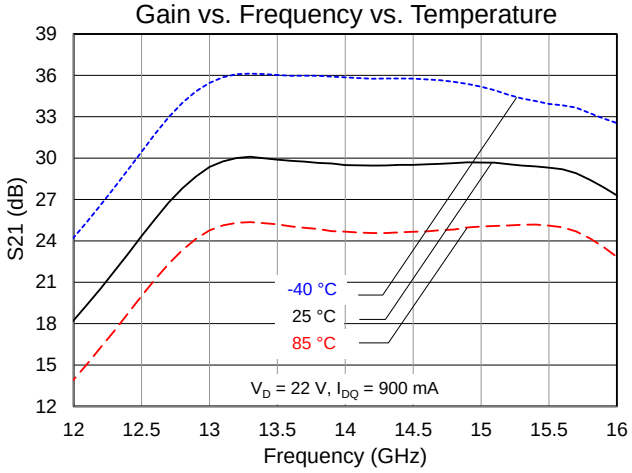
Test Conditions: V_D = +28 V; Failure Criteria = 10 % reduction in ID_MAX



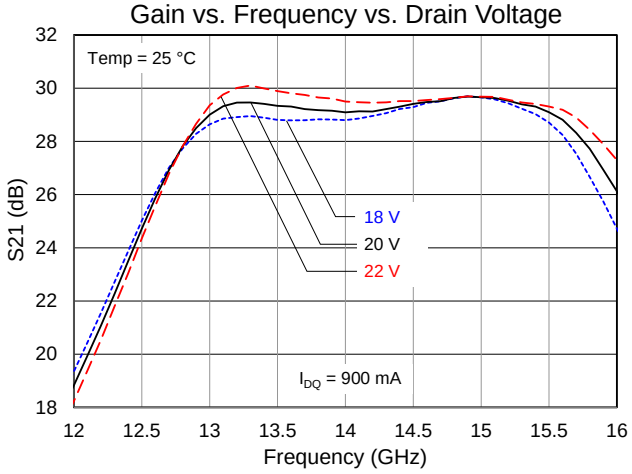


Typical Performance – Small Signal

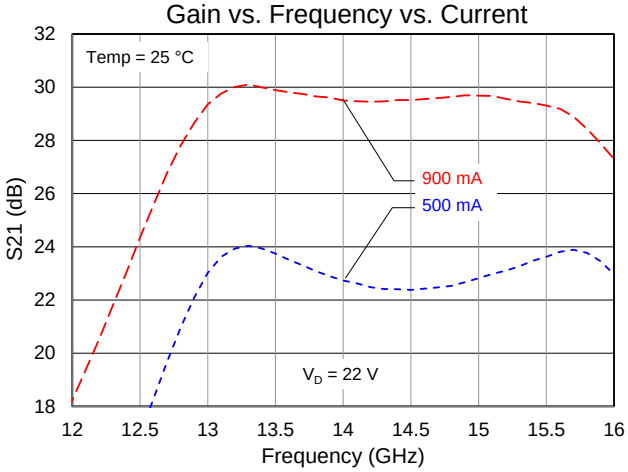
Gain vs. Frequency vs. Temperature



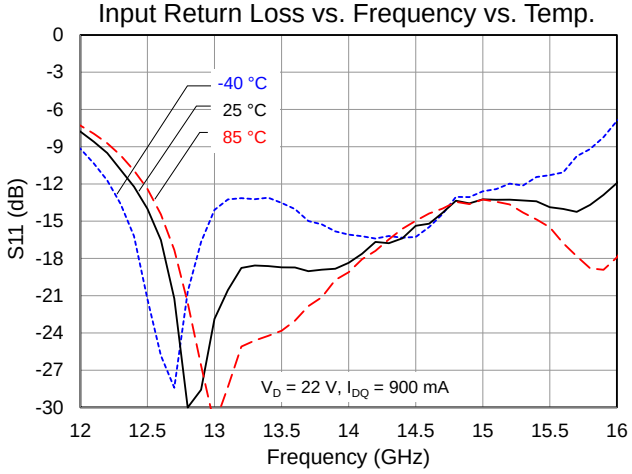
Gain vs. Frequency vs. Drain Voltage



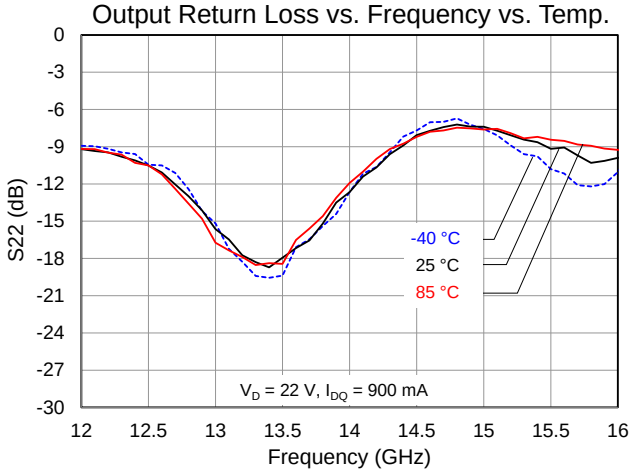
Gain vs. Frequency vs. Current



Input Return Loss vs. Frequency vs. Temp.

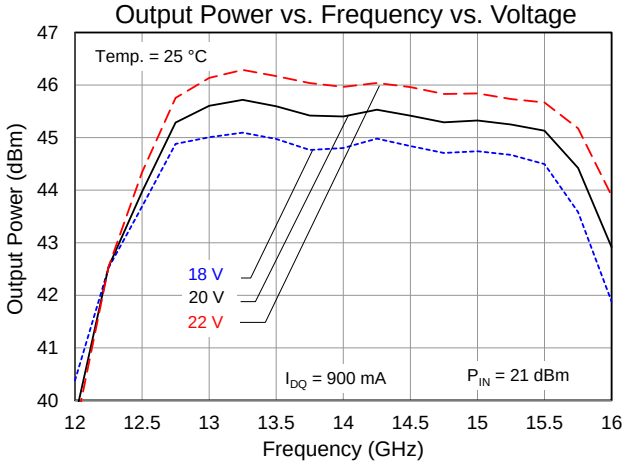


Output Return Loss vs. Frequency vs. Temp.

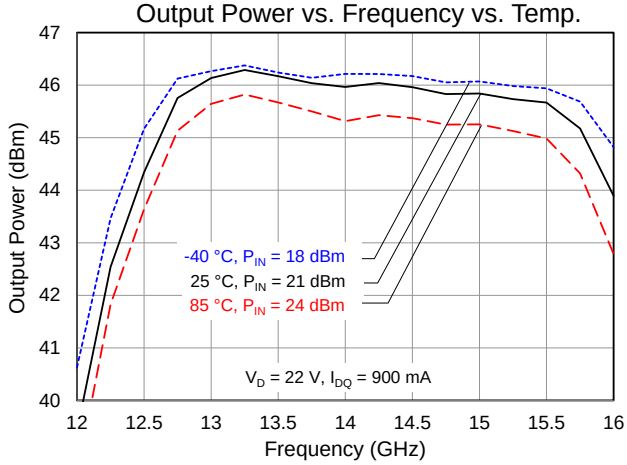


Typical Performance – (CW Operation)

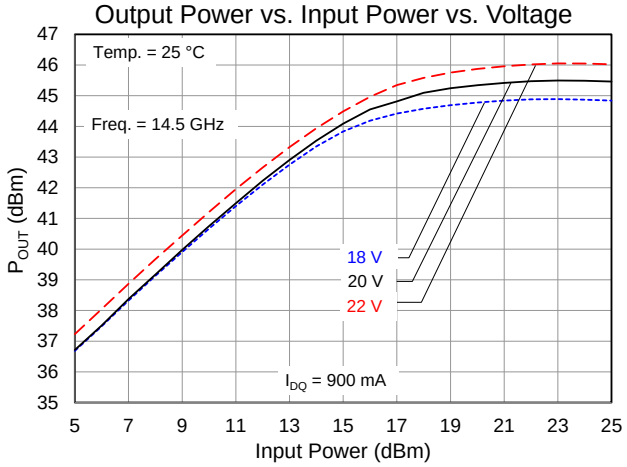
Output Power vs. Frequency vs. Voltage



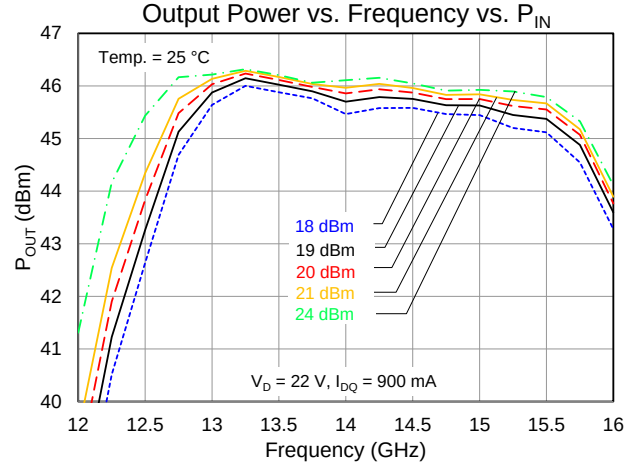
Output Power vs. Frequency vs. Temp.



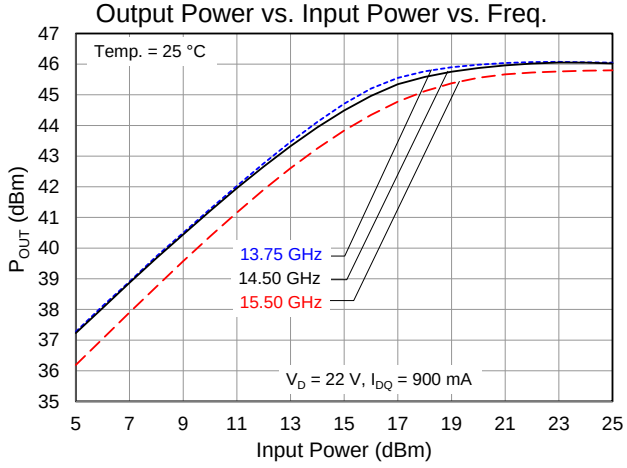
Output Power vs. Input Power vs. Voltage



Output Power vs. Frequency vs. P_{IN}

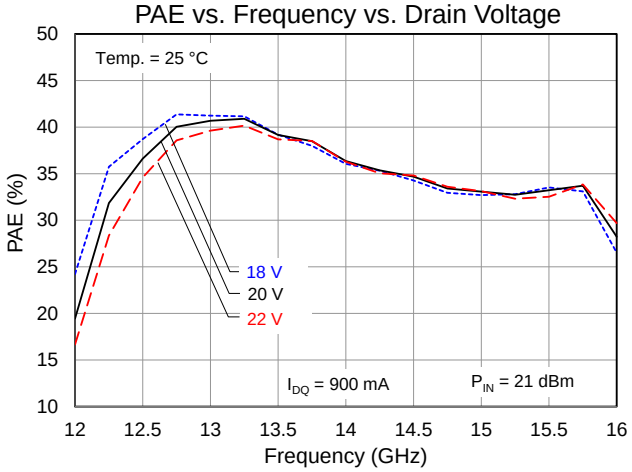


Output Power vs. Input Power vs. Freq.

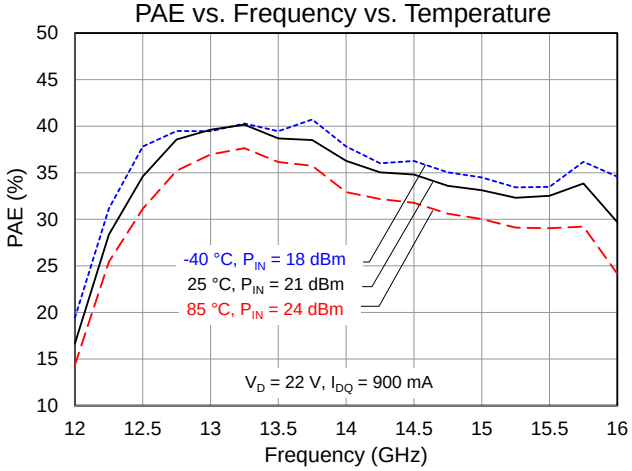


Typical Performance – (CW Operation)

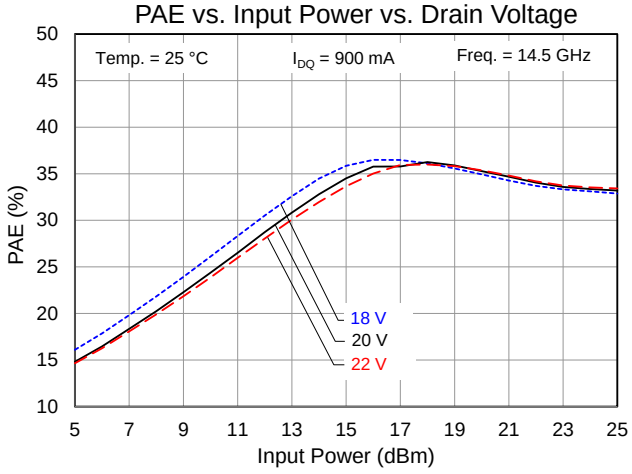
PAE vs. Frequency vs. Drain Voltage



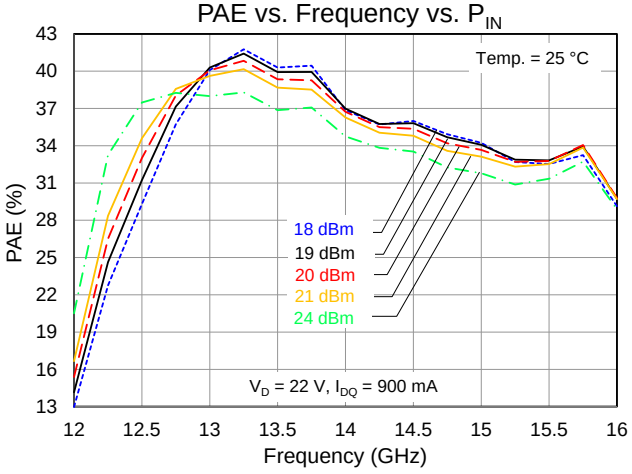
PAE vs. Frequency vs. Temperature



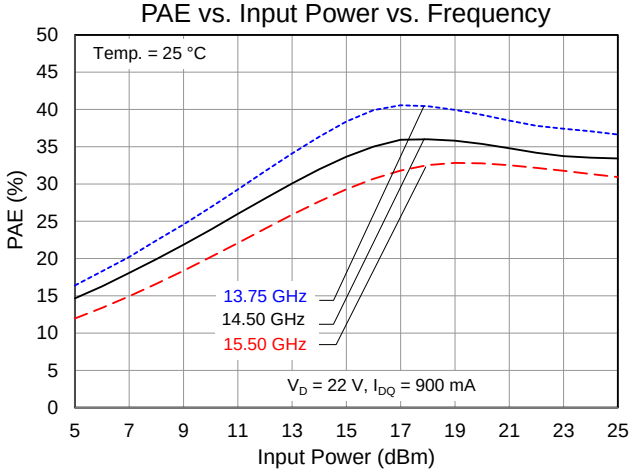
PAE vs. Input Power vs. Drain Voltage



PAE vs. Frequency vs. P_{IN}

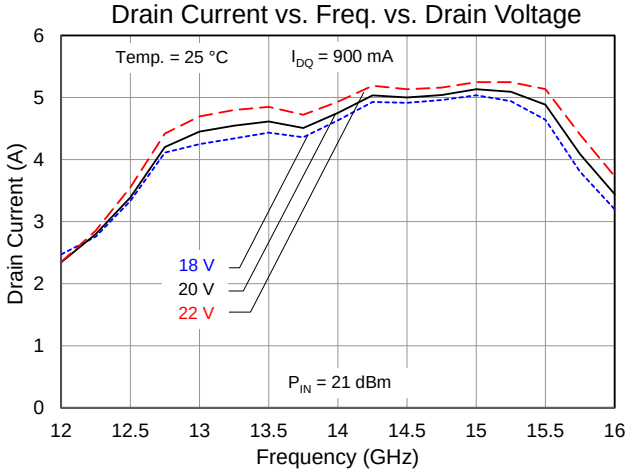


PAE vs. Input Power vs. Frequency

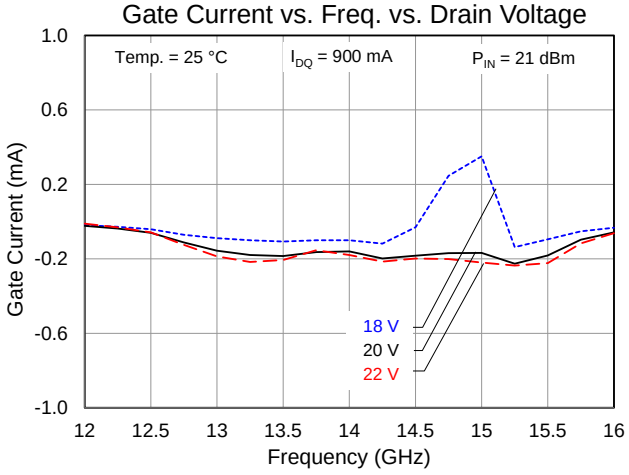


Typical Performance – (CW Operation)

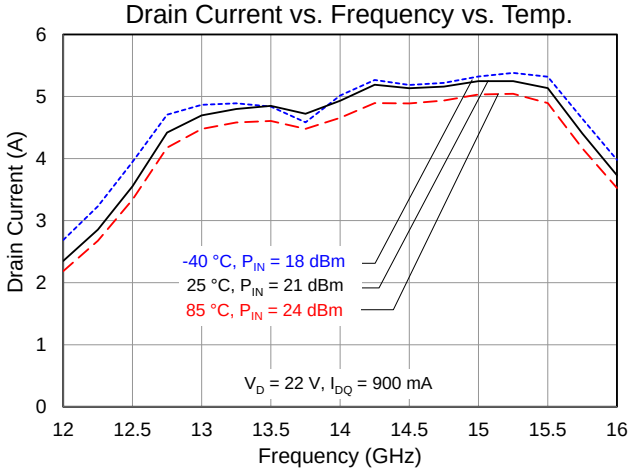
Drain Current vs. Freq. vs. Drain Voltage



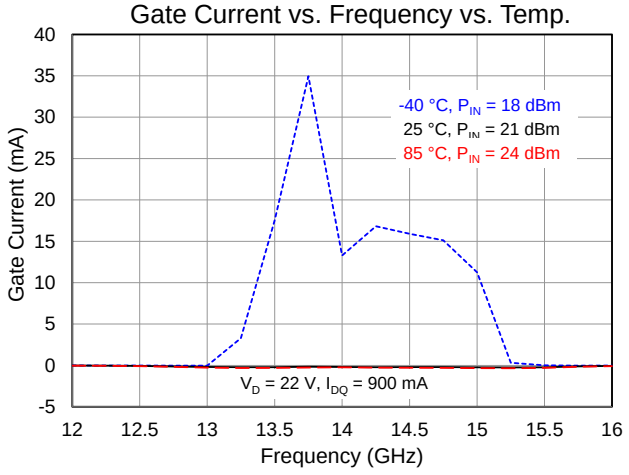
Gate Current vs. Freq. vs. Drain Voltage



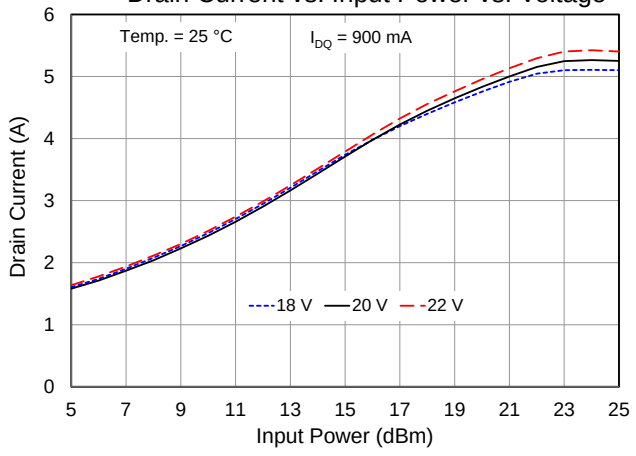
Drain Current vs. Frequency vs. Temp.



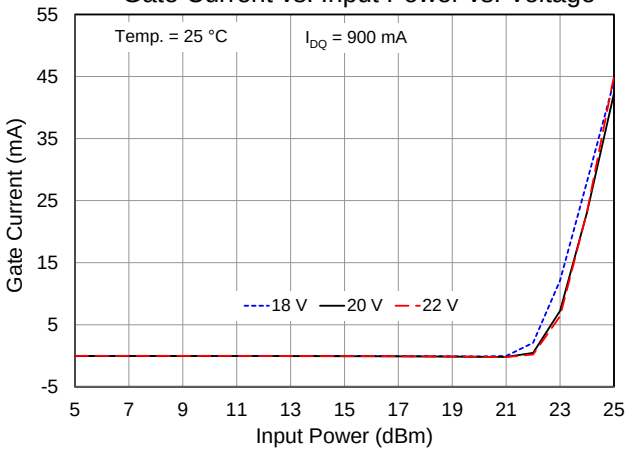
Gate Current vs. Frequency vs. Temp.



Drain Current vs. Input Power vs. Voltage

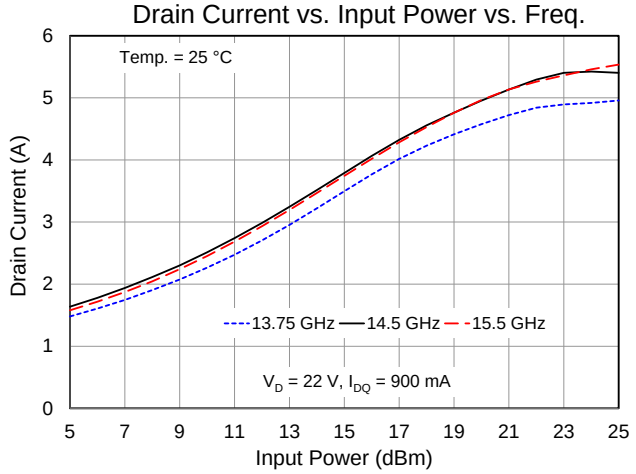


Gate Current vs. Input Power vs. Voltage

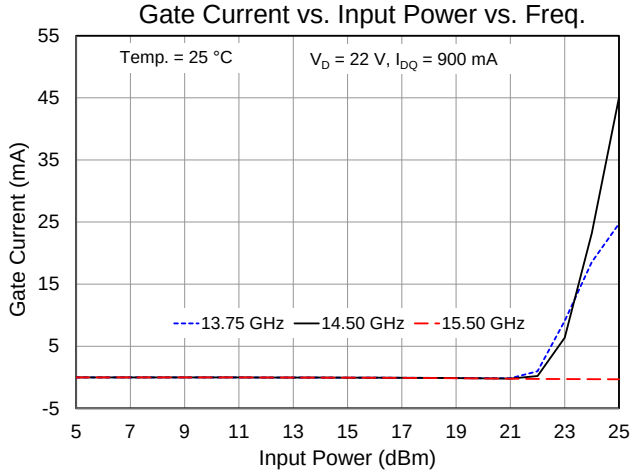


Typical Performance – (CW Operation)

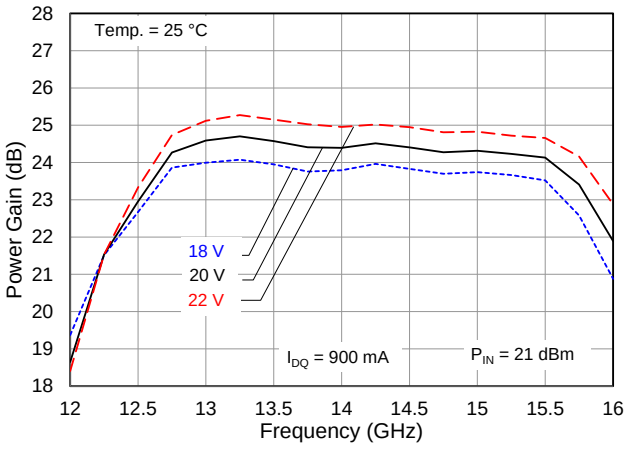
Drain Current vs. Input Power vs. Freq.



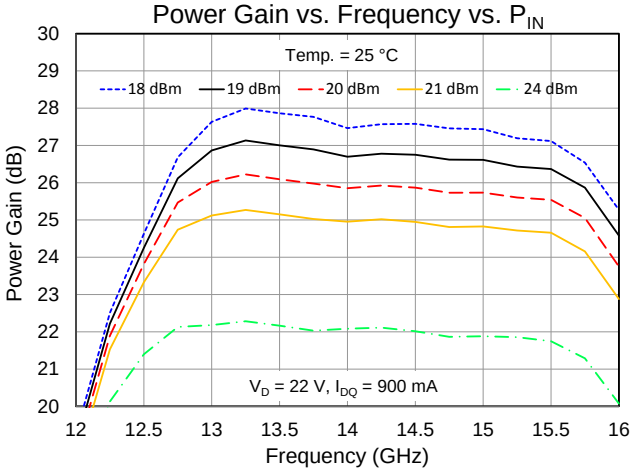
Gate Current vs. Input Power vs. Freq.



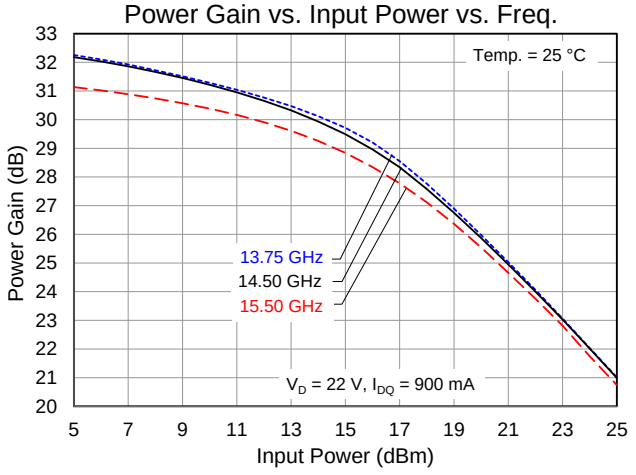
Power Gain vs. Frequency vs. Drain Voltage



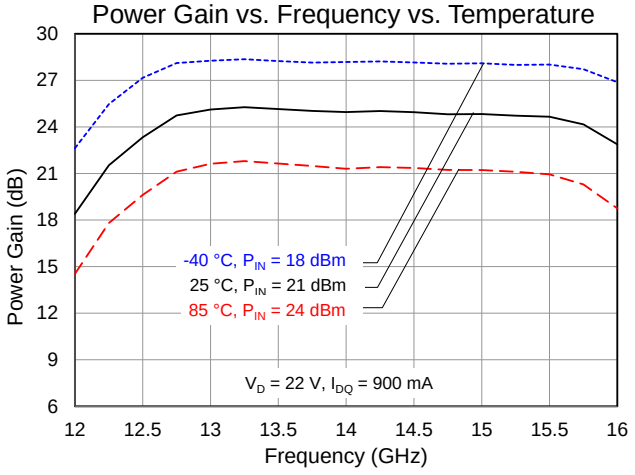
Power Gain vs. Frequency vs. P_{IN}



Power Gain vs. Input Power vs. Freq.

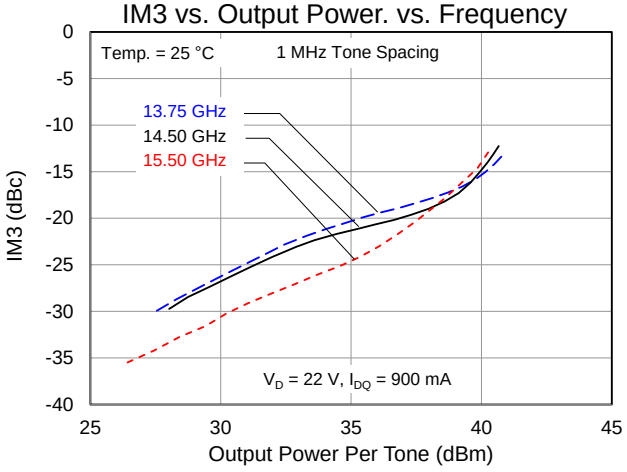


Power Gain vs. Frequency vs. Temperature

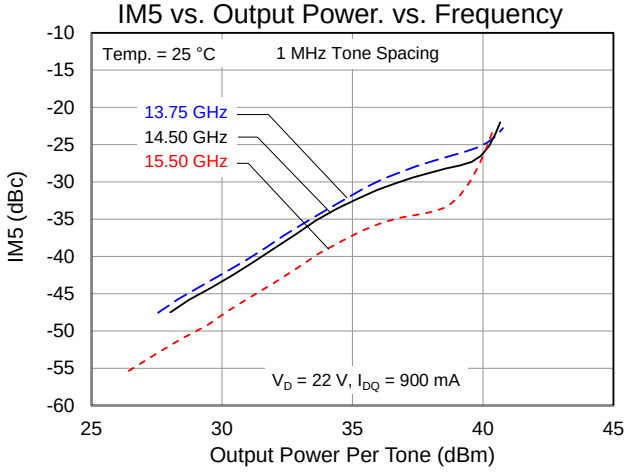


Typical Performance – Linearity

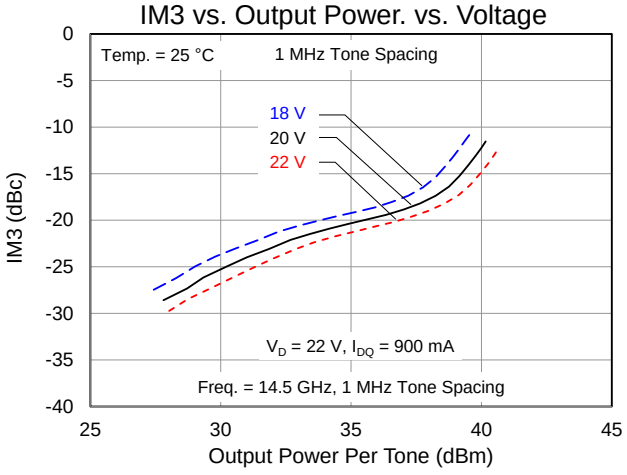
IM3 vs. Output Power. vs. Frequency



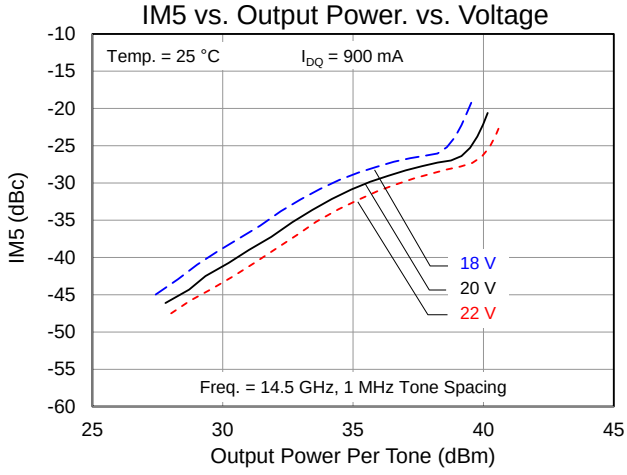
IM5 vs. Output Power. vs. Frequency



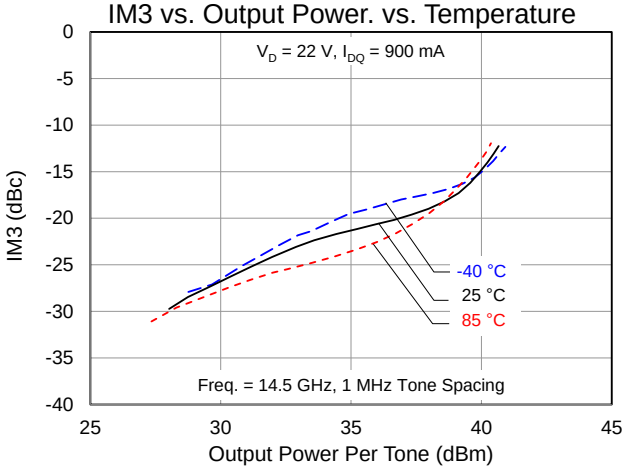
IM3 vs. Output Power. vs. Voltage



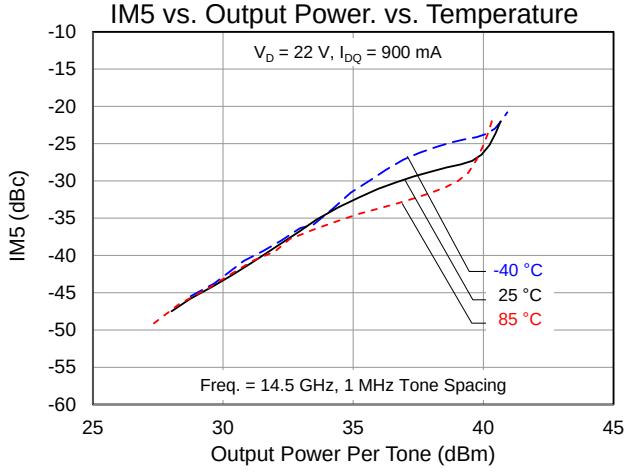
IM5 vs. Output Power. vs. Voltage



IM3 vs. Output Power. vs. Temperature

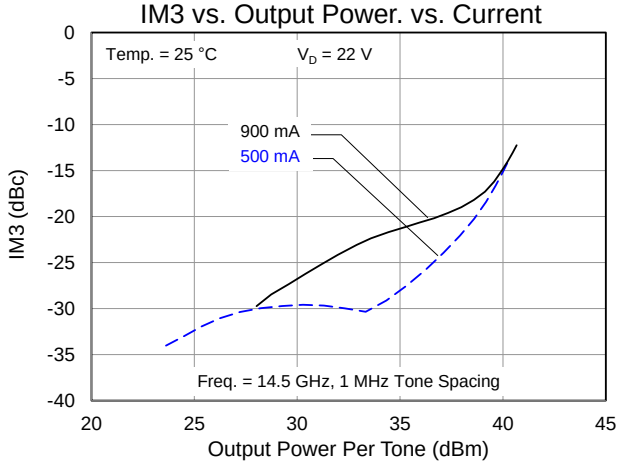


IM5 vs. Output Power. vs. Temperature

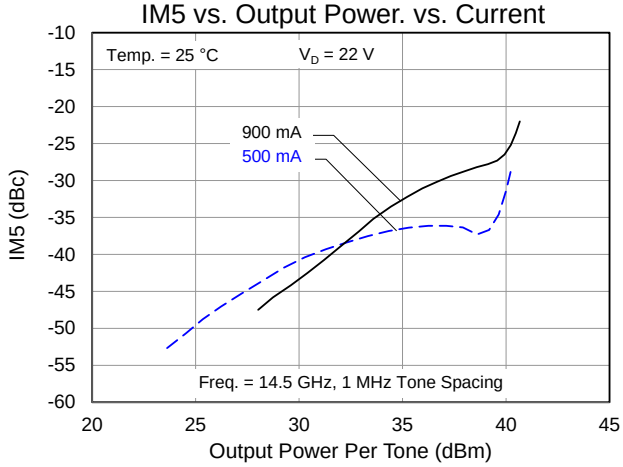


Typical Performance – Linearity

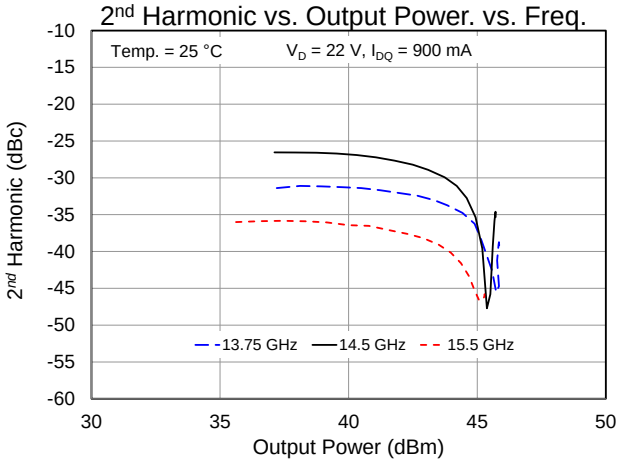
IM3 vs. Output Power. vs. Current



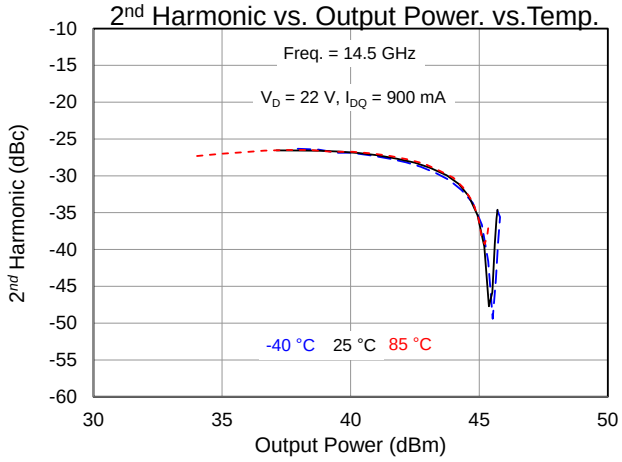
IM5 vs. Output Power. vs. Current



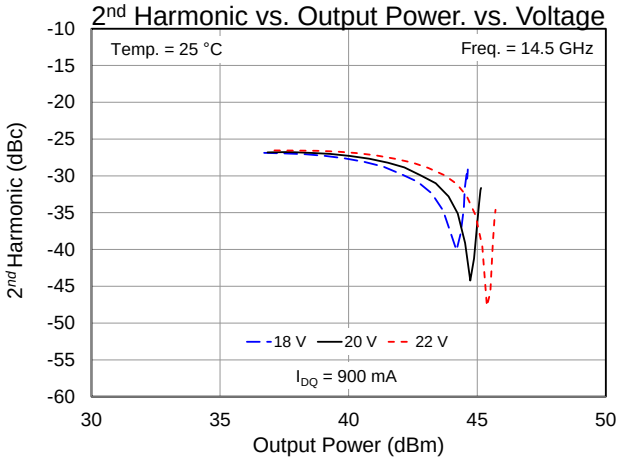
2nd Harmonic vs. Output Power. vs. Freq.



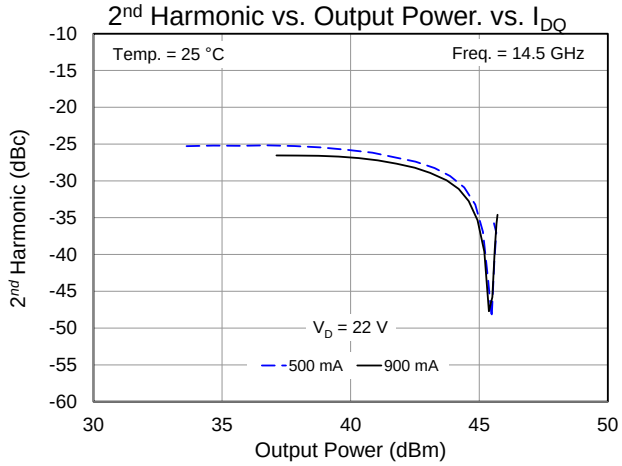
2nd Harmonic vs. Output Power. vs.Temp.



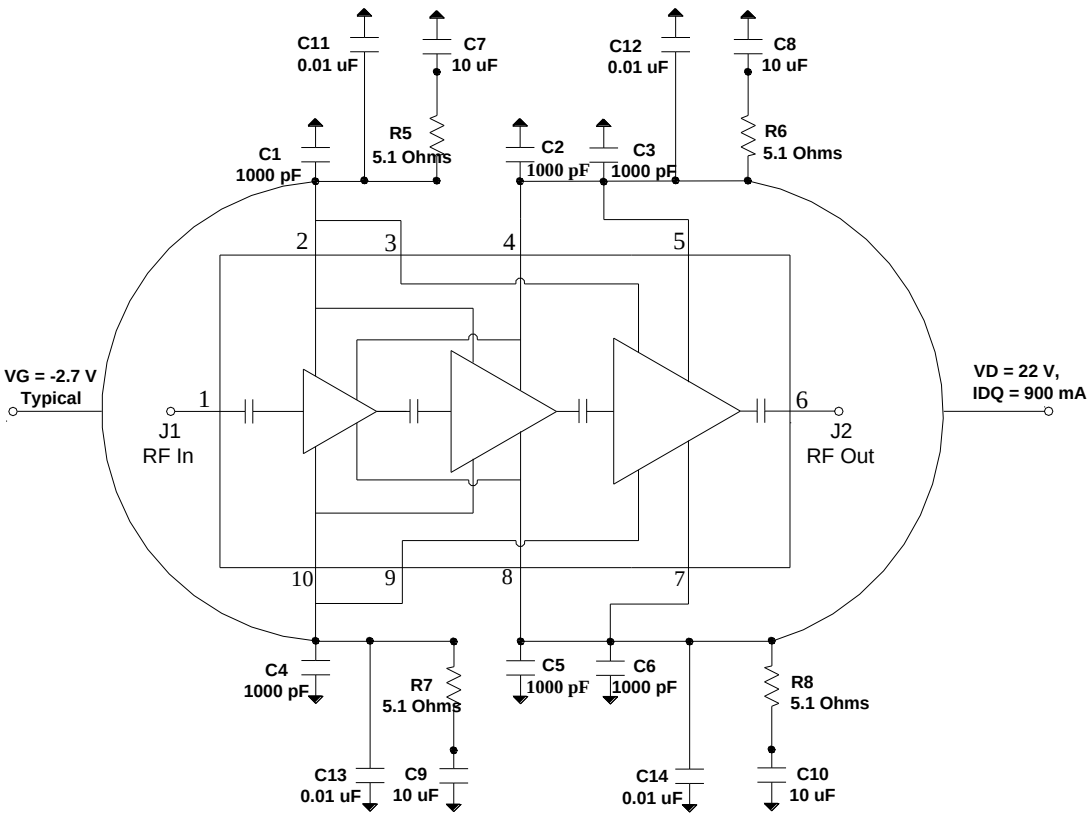
2nd Harmonic vs. Output Power. vs. Voltage



2nd Harmonic vs. Output Power. vs. I_{DQ}



Application Circuit



Notes:

V_G & V_D must be biased from both sides top and bottom.

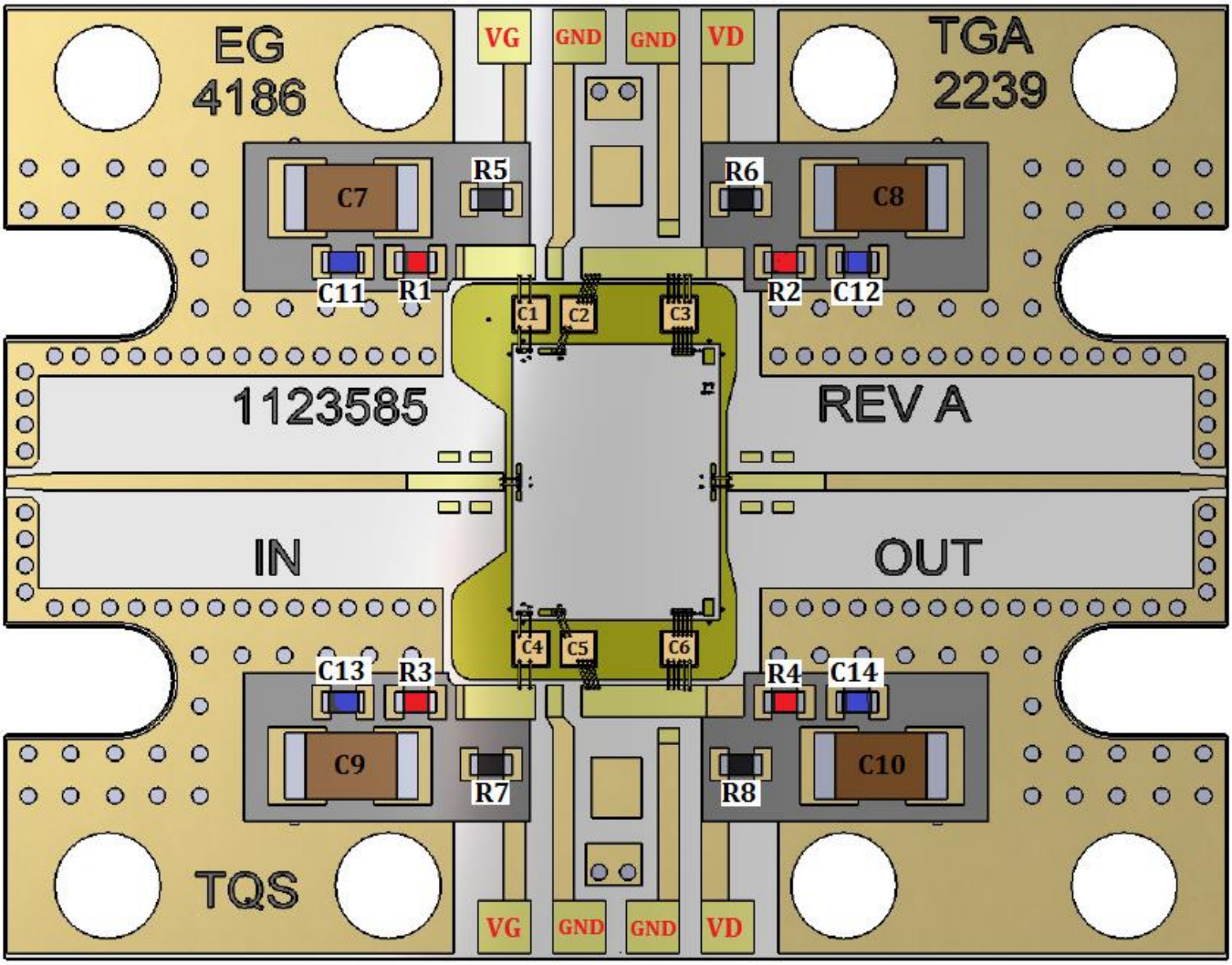
Bias Up Procedure

1. Set I_D limit to 6 A, I_G limit to 50 mA
2. Set V_G to −5 V
3. Set V_D +22 V
4. Adjust V_G until I_{DQ} = 900 mA (V_G ~ −2.7 V Typ.)
5. Apply RF signal

Bias Down Procedure

1. Turn off RF supply
2. Reduce V_G to −5 V; ensure I_{DQ} is approx. 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Evaluation Board (EVB) Layout Assembly

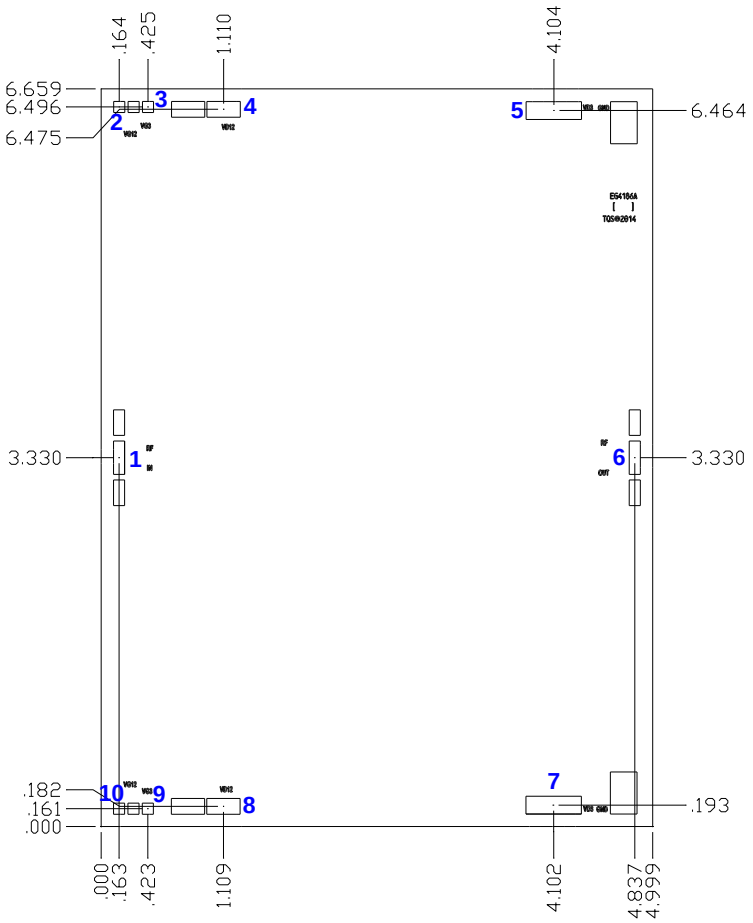


Notes:
1. VG & VD must be biased from both sides top and bottom.

Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1 – C6	1000 pF	SLC, +50 V	Various	–
C7 – C10	10 uF	Cap, 1206, +50 V, 20 %, X5R	Various	–
C11, C14	0.01uF	Cap, 0402, +50 V, 10 %, X7R	Various	–
R1 – R4	0 Ω	Res, 0402, 5 %, SMD	Various	–
R5 – R8	5.1 Ω	Res, 0402, 5 %, ROHS	Various	–

Mechanical Drawing



Unit: millimeters
Thickness: 0.10
Die x, y size tolerance: +/- 0.050
Chip edge to bond pad dimensions are shown to center of pad
Ground is backside of die

Bond Pad Description

Pad No.	Symbol	Pad Size	Description
1	RF In	0.101 x 0.302	RF Input; matched to 50 Ω, DC blocked
2, 10	VG1-2	0.101 x 0.101	Gate voltage 1, bias network is required; see Application Circuit on page 11 as an example.
3, 9	VG3	0.101 x 0.101	Gate voltage 3, bias network is required; see Application Circuit on page 11 as an example.
4, 8	VD1-2	0.302 x 0.143	Drain voltage 1, bias network is required; see Application Circuit on page 11 as an example.
5, 7	VD3	0.503 x 0.161	Drain voltage 3, bias network is required; see Application Circuit on page 11 as an example.
6	RF Out	0.101 x 0.302	RF Output; matched to 50 Ω, DC blocked

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment (i.e. epoxy) can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.