TGA2612-SM

6 – 12 GHz GaN LNA

Product Description

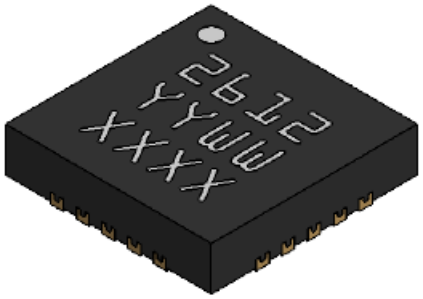
Qorvo's TGA2612-SM is a packaged broadband Low Noise Amplifier fabricated on Qorvo's QGaN25 0.25um GaN on SiC process. Covering 6–12 GHz, the TGA2612-SM typically provides >23 dM small signal gain, 19 dBm P1dB, and 27 dBm OTOI with <2 dB of Noise Figure. In addition to the high electrical performance, this GaN amplifier also provides a high level of input power robustness. Able to survive up to 2W of input power without performance degradation, Qorvo's TGA2612-SM provides flexibility regarding receive chain protection resulting in lower costs and reduced board space.

The TGA2612-SM is available in a surface mount 20-lead 4x4mm QFN. It is ideally suited for both radar and communications applications.

Fully matched to 50 ohms with integrated DC blocking caps on both I/O ports, the TGA2612-SM is ideally suited for both military and commercial radar and communications applications.

Lead–Free and RoHS compliant.

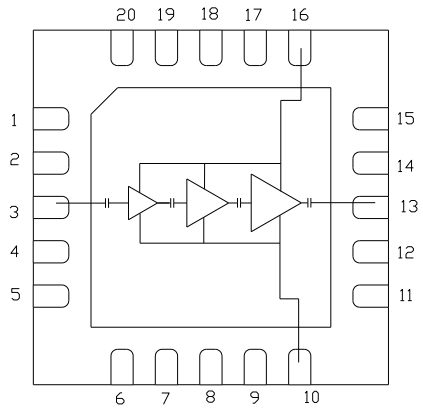
Evaluation boards are available upon request.



Product Features

- Frequency Range: 6 – 12 GHz
- NF: 2.0 dB
- P1dB: 19 dBm
- OTOI: 28 dBm
- Small Signal Gain: 22 dB
- Return Loss: > 7 dB
- Bias: V_D = 10 V, I_{DQ} = 100 mA; V_G = -2.3 V (Typical)
- Package Dimensions: 4.0 x 4.0 x 0.85 mm

Functional Block Diagram



Applications

- Commercial & Military Radar
- Communications

Ordering Information

Part No.	ECCN	Description
TGA2612-SM	EAR99	6 – 12 GHz GaN LNA

Absolute Maximum Ratings

Parameter	Range / Value	Units
Drain Voltage (V_D)	+40	V
Gate Voltage (V_G)	−5 to 0	V
Drain Current (I_D)	300	mA
Gate Current (I_G)	See graph on page 3	–
Power Dissipation, 85 °C (P_{DISS})	6	W
RF Input Power, CW, 50 Ω, (P_{IN})	33	dBm
Channel Temperature (T_{CH})	+275	°C
Mounting Temperature (30 seconds maximum)	+260	°C
Storage Temperature	−55 to +150	°C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	
Drain Voltage (V_D)	10 V
Gate Voltage (V_G)	-2.3 V Typical
Quiescent Drain Current (I_{DQ})	100 mA
Temperature (T_{BASE})	-40 to 85 °C

Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		6		12	GHz
Small Signal Gain			22		dB
Input Return Loss			> 7		dB
Noise Figure			2		dB
Output Power @ 1 dB Gain Compression (P_{1dB})			19		dBm
Output Power	@ P_{IN} = 10 dBm		25		
Output TOI			28		dBm
Small Signal Gain Temperature Coefficient			−0.05		dB / °C
Noise Figure Temperature Coefficient			0.01		dB / °C

Test conditions unless otherwise noted: T_{BASE} = +25 °C, V_D = 10V, I_{DQ} = 100mA, V_G = -2.3V Typical, CW

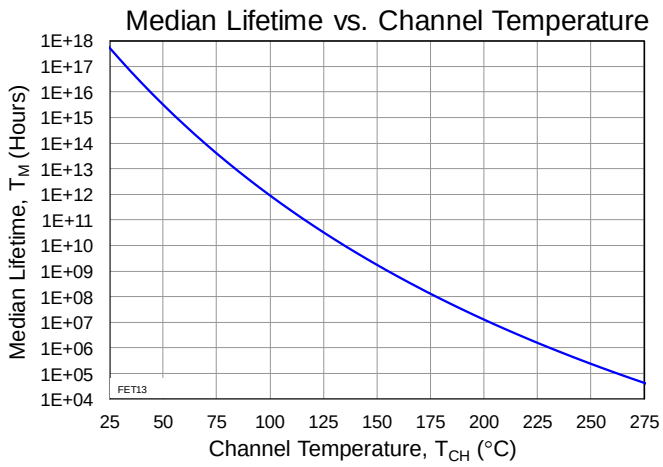
Thermal and Reliability Information

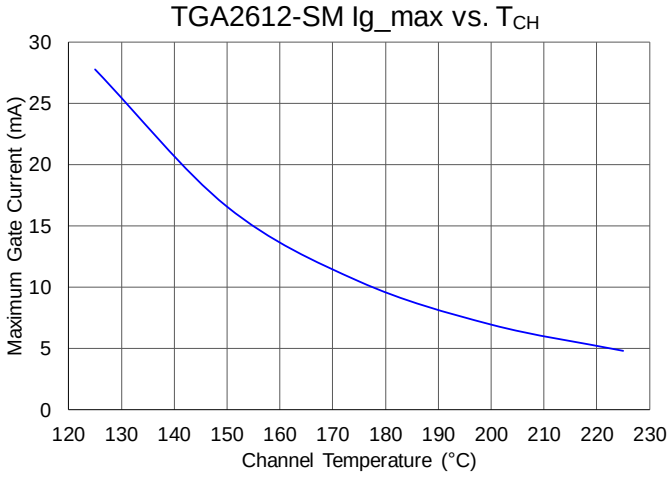
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = +85 °C, V_D = 10 V, I_{DQ} = 100 mA, I_{D_DRIVE} = 180 mA, P_{IN} = 10 dBm, P_{OUT} = 25 dBm, Freq. = 11 GHz, P_{DISS} = 1.6 W, CW	17	°C/W
Channel Temperature (T_{CH}) (1)		112	°C
Median Lifetime (T_M)		1.8E+11	Hrs.

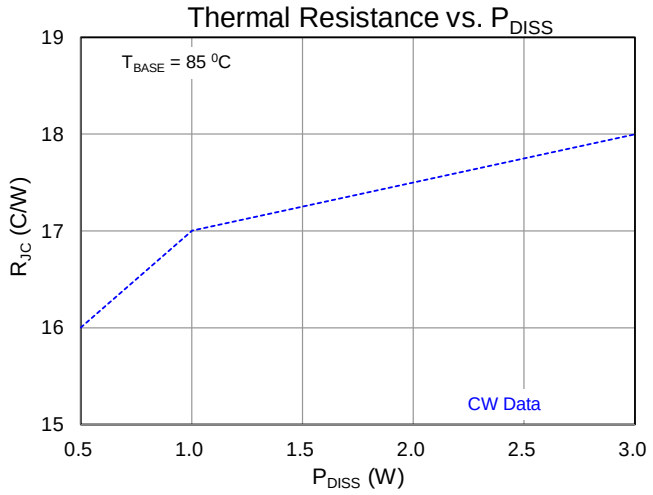
Notes:
1. Package backside temperature fixed at 85 °C.

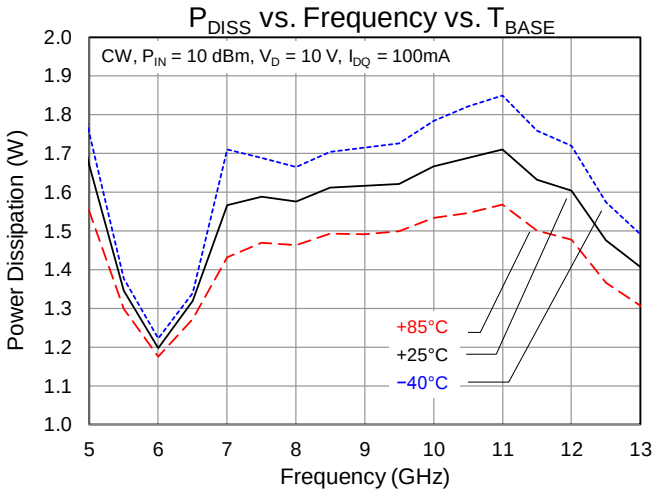
Median Lifetime

Test Conditions: V_D = 40 V; Failure Criterion = 10% reduction in $I_{D\ MAX}$



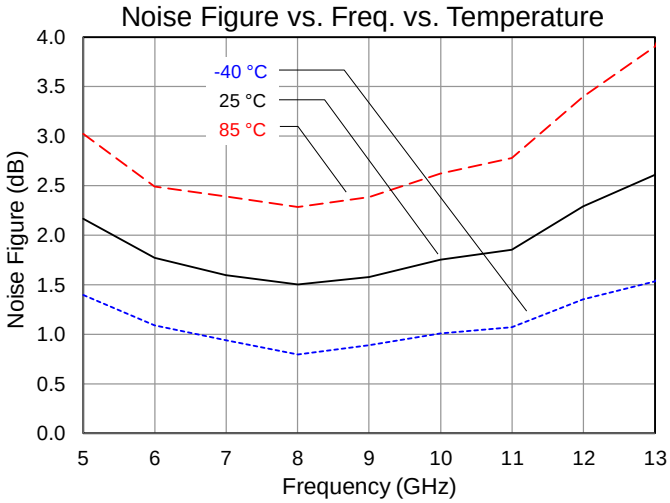


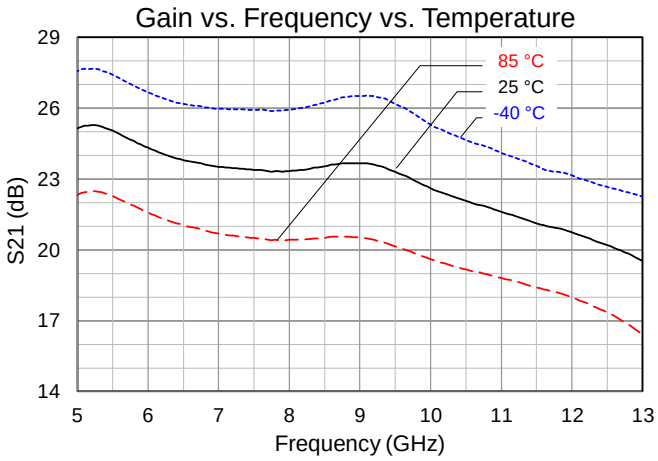


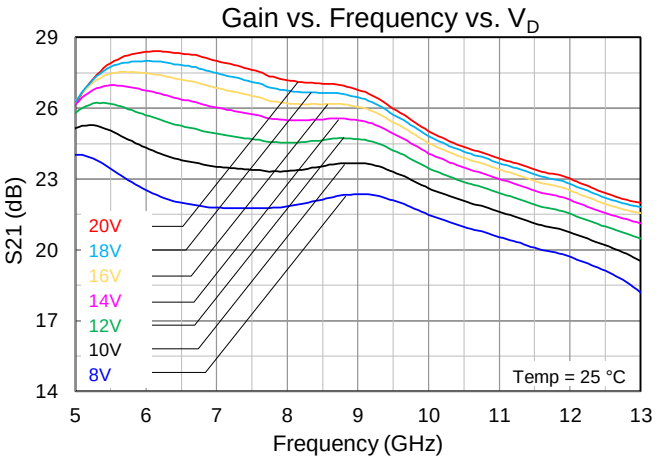


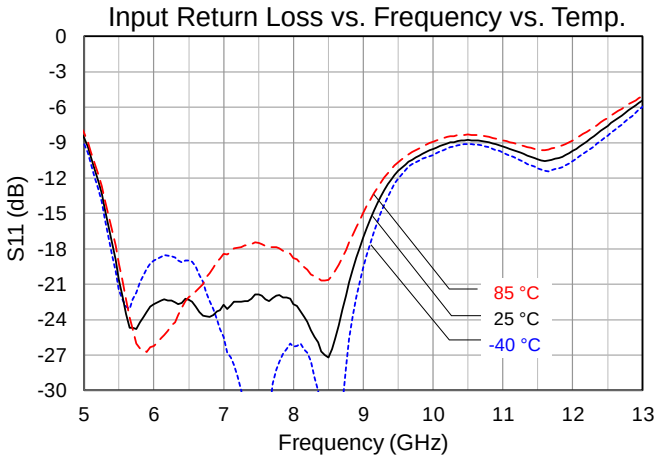
Performance Plots – Small Signal

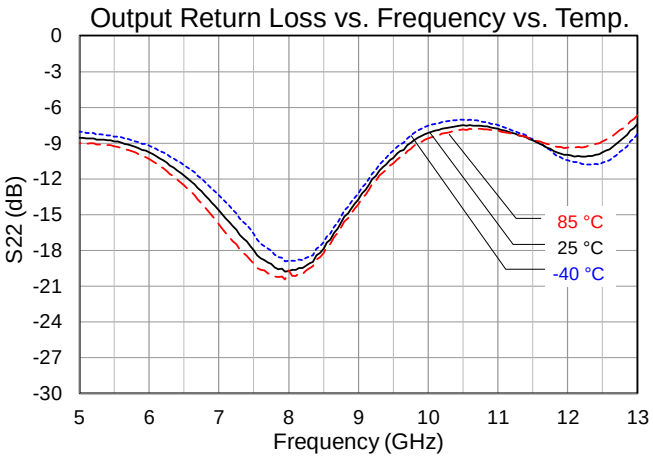
Conditions unless otherwise specified: V_D = 10 V, I_{DQ} = 100 mA, V_G = -2.3 V Typical, CW





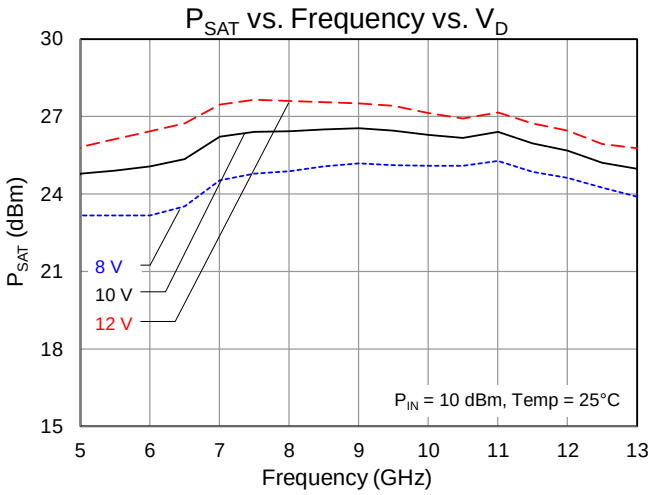


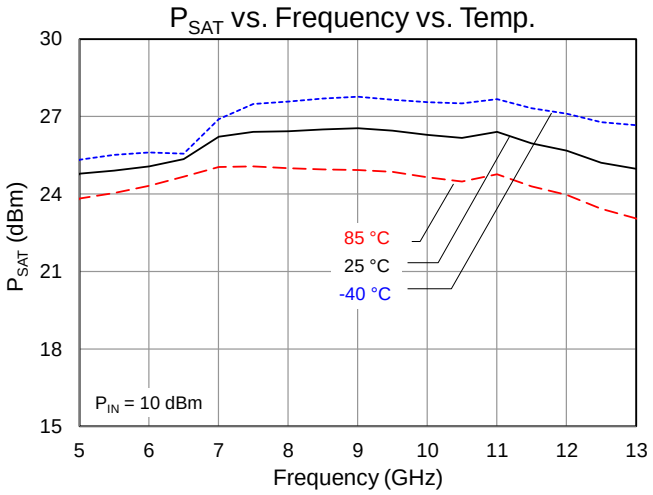


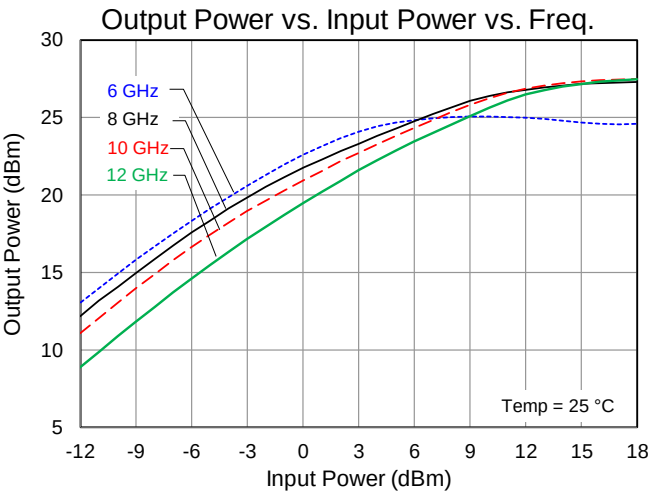


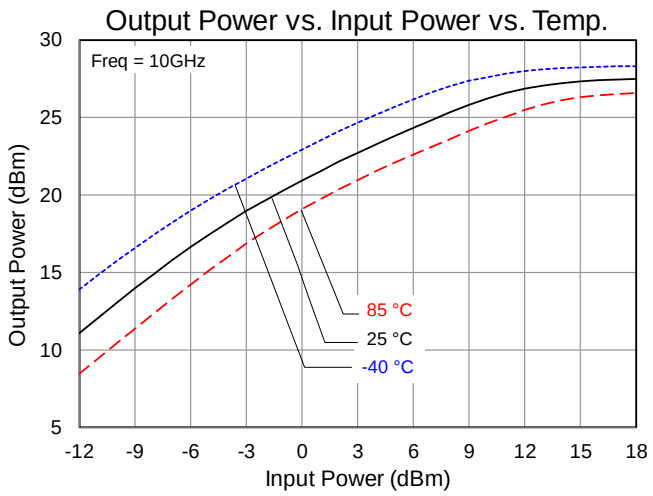
Performance Plots – Large Signal

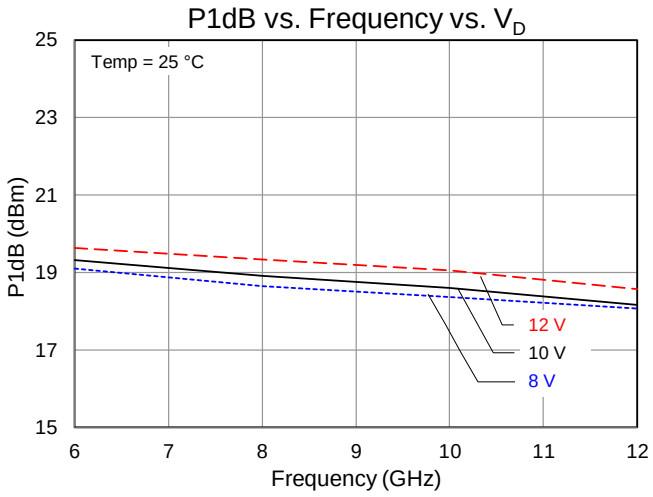
Conditions unless otherwise specified: V_D = 10 V, I_{DQ} = 100 mA, V_G = -2.3 V Typical, CW

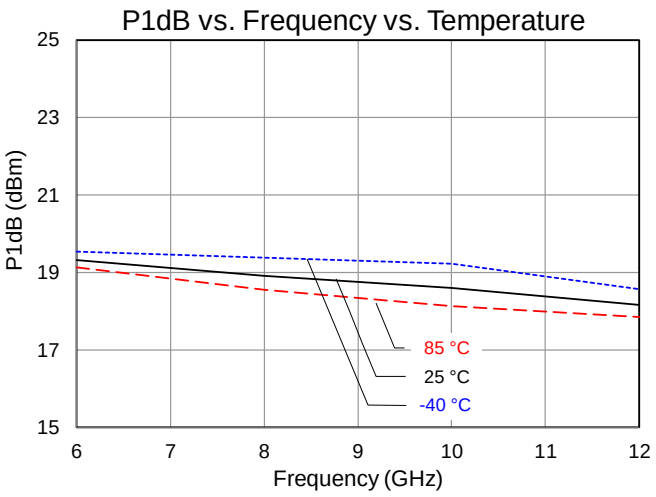








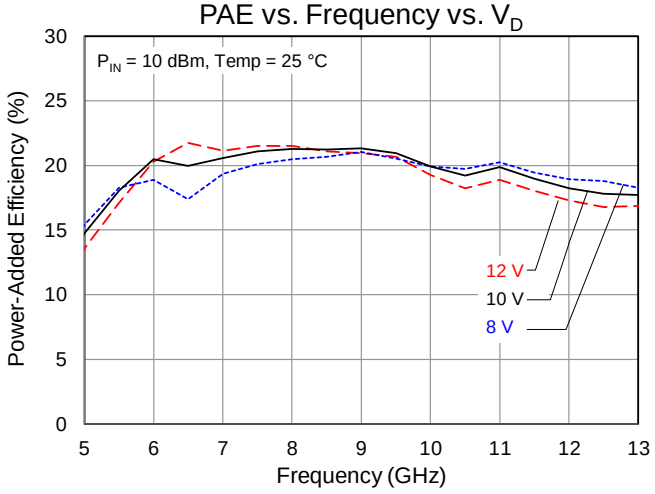




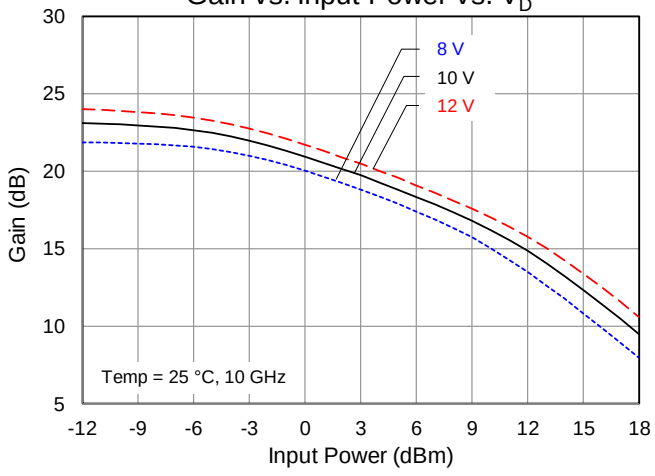
Performance Plots – Large Signal

Conditions unless otherwise specified: V_D = 10 V, I_{DQ} = 100 mA, V_G = -2.3 V Typical, CW

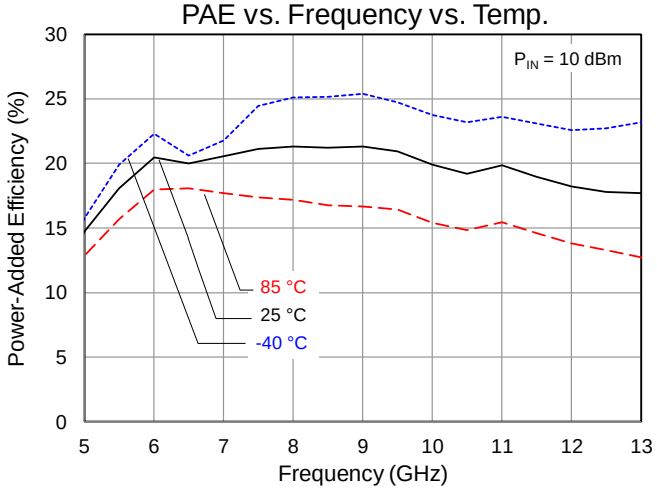
PAE vs. Frequency vs. V_D



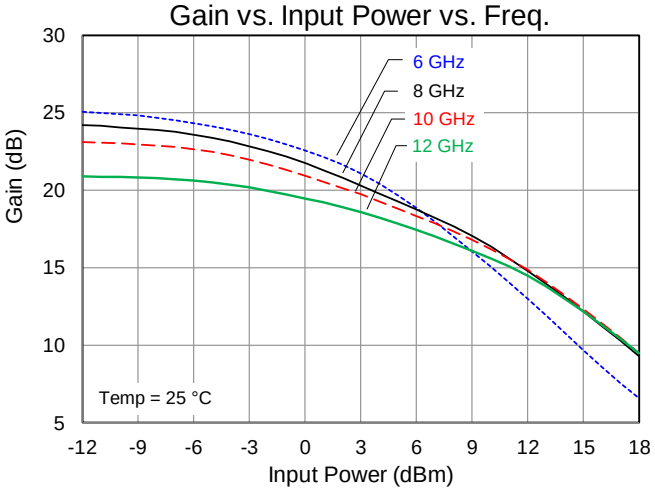
Gain vs. Input Power vs. V_D



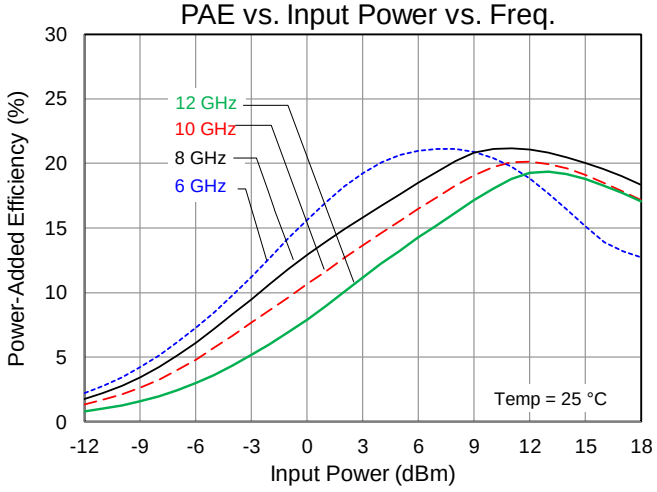
PAE vs. Frequency vs. Temp.



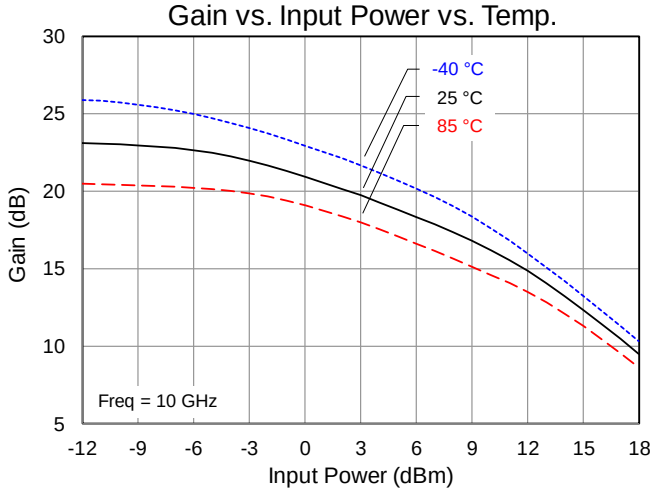
Gain vs. Input Power vs. Freq.



PAE vs. Input Power vs. Freq.



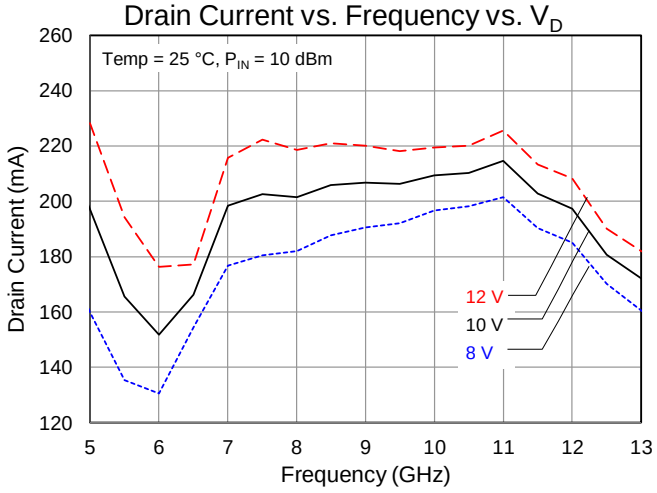
Gain vs. Input Power vs. Temp.



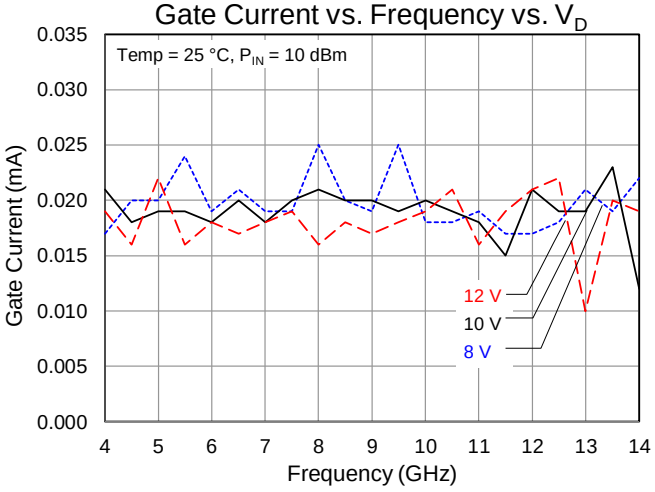
Performance Plots – Large Signal

Conditions unless otherwise specified: V_D = 10 V, I_{DQ} = 100 mA, V_G = -2.3 V Typical, CW

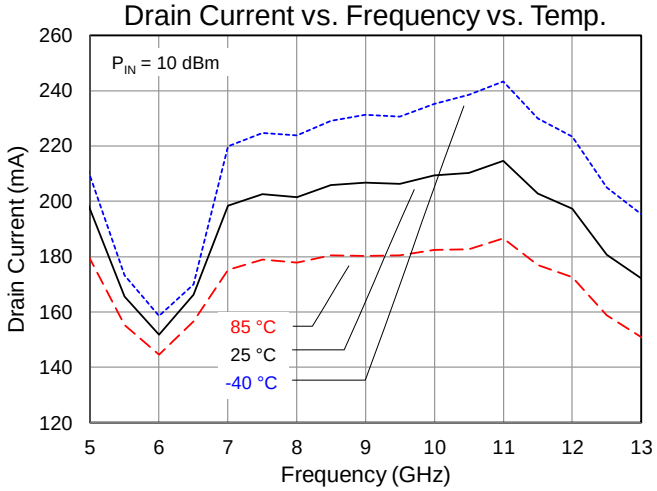
Drain Current vs. Frequency vs. V_D



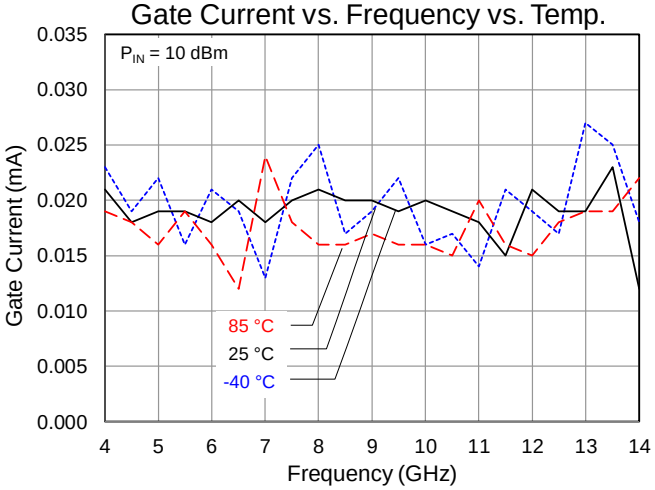
Gate Current vs. Frequency vs. V_D



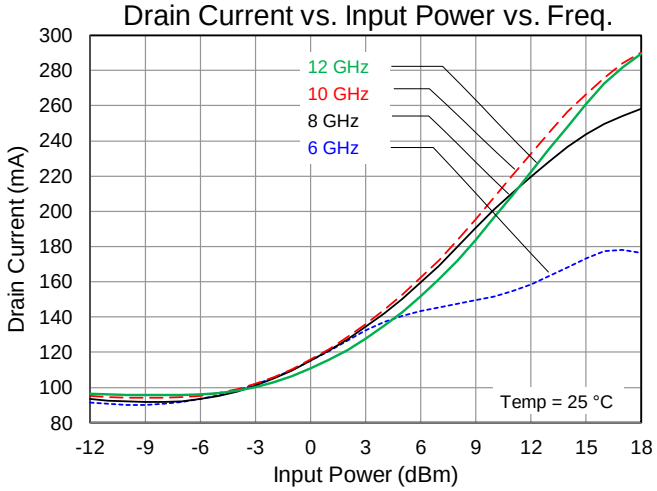
Drain Current vs. Frequency vs. Temp.



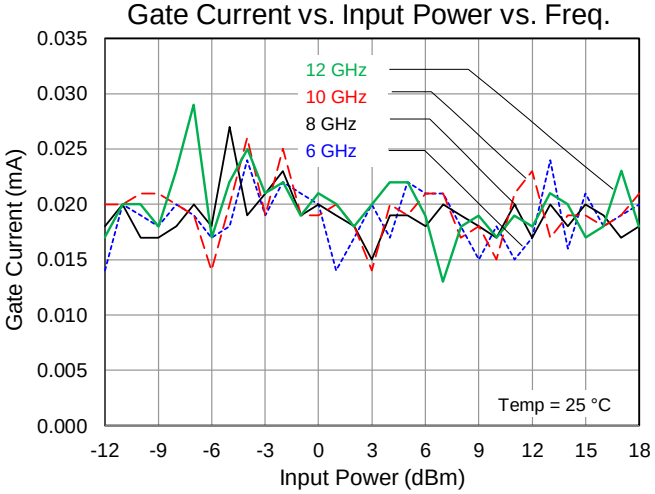
Gate Current vs. Frequency vs. Temp.



Drain Current vs. Input Power vs. Freq.



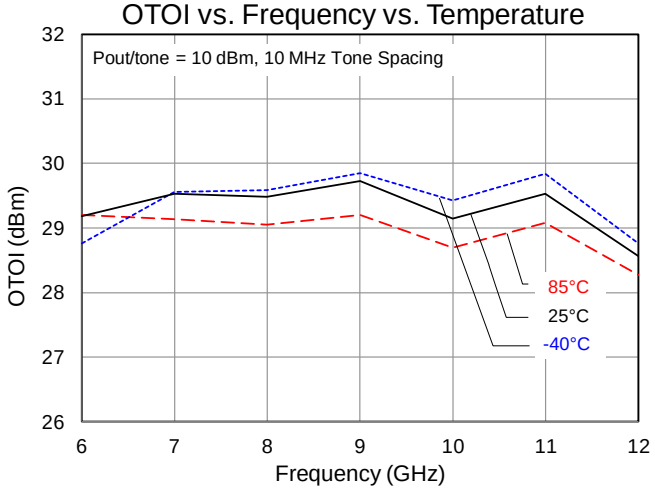
Gate Current vs. Input Power vs. Freq.



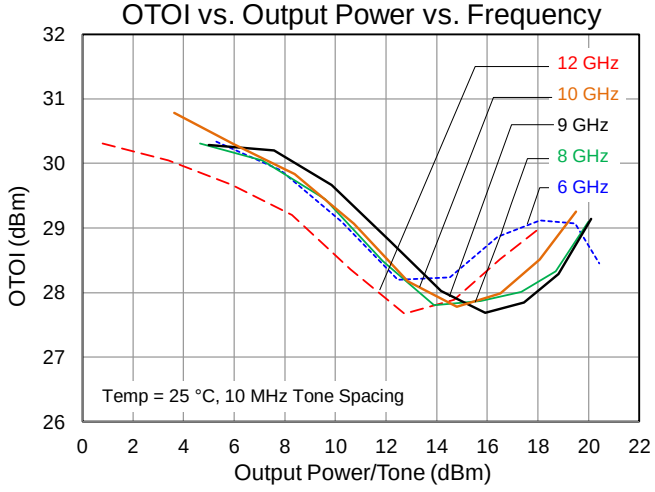
Performance Plots – Linearity

Conditions unless otherwise specified: V_D = 10 V, I_{DQ} = 100 mA, V_G = -2.3 V Typical, CW

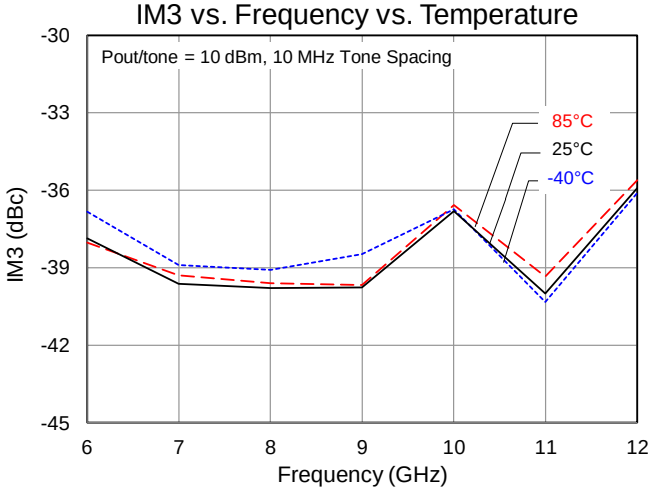
OTOI vs. Frequency vs. Temperature



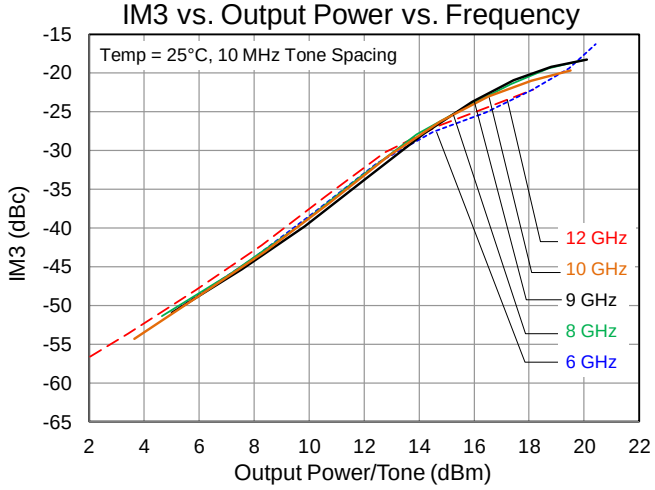
OTOI vs. Output Power vs. Frequency



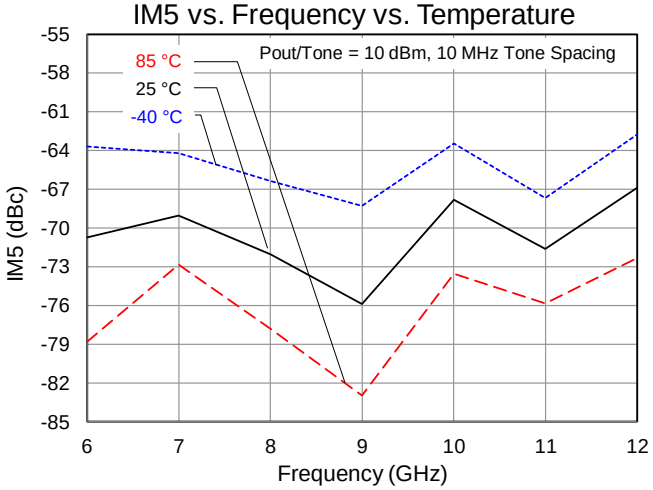
IM3 vs. Frequency vs. Temperature



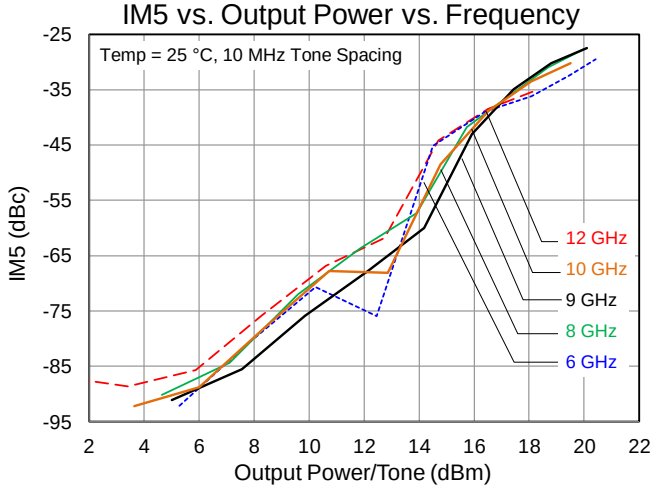
IM3 vs. Output Power vs. Frequency



IM5 vs. Frequency vs. Temperature



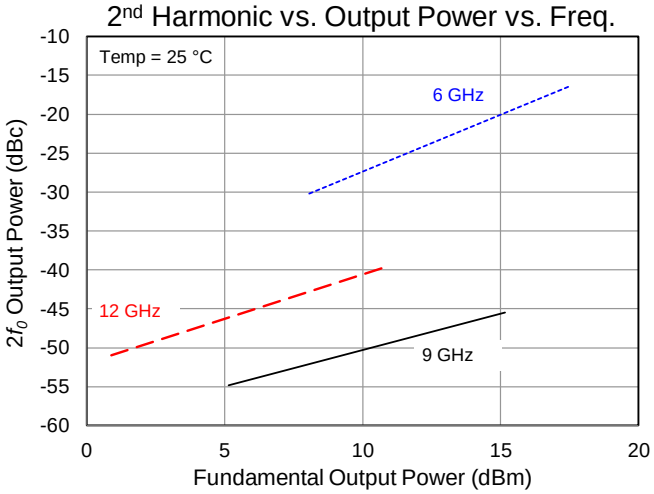
IM5 vs. Output Power vs. Frequency



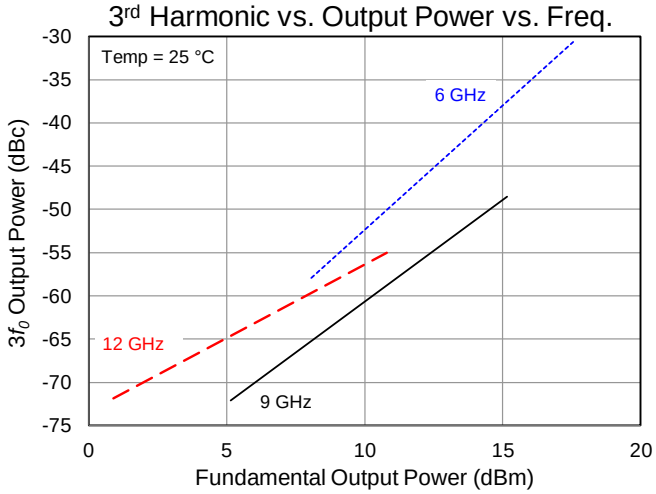
Performance Plots – Harmonic

Conditions unless otherwise specified: V_D = 10 V, I_{DQ} = 100 mA, V_G = -2.3 V Typical, CW

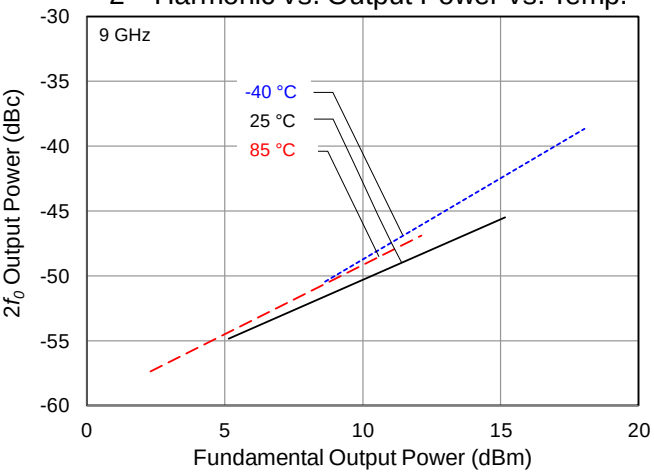
2nd Harmonic vs. Output Power vs. Freq.



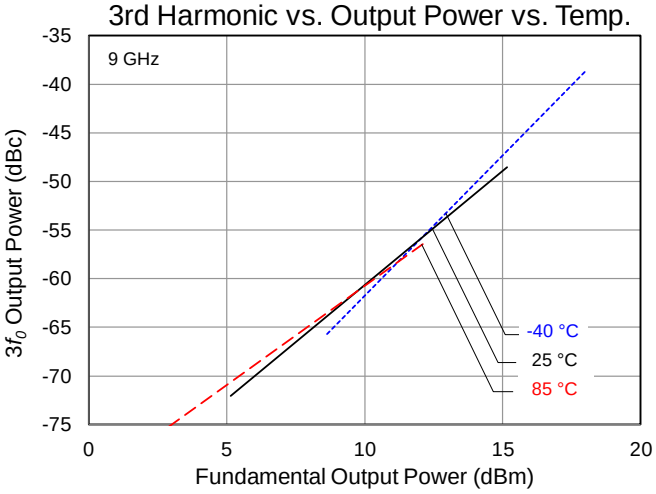
3rd Harmonic vs. Output Power vs. Freq.



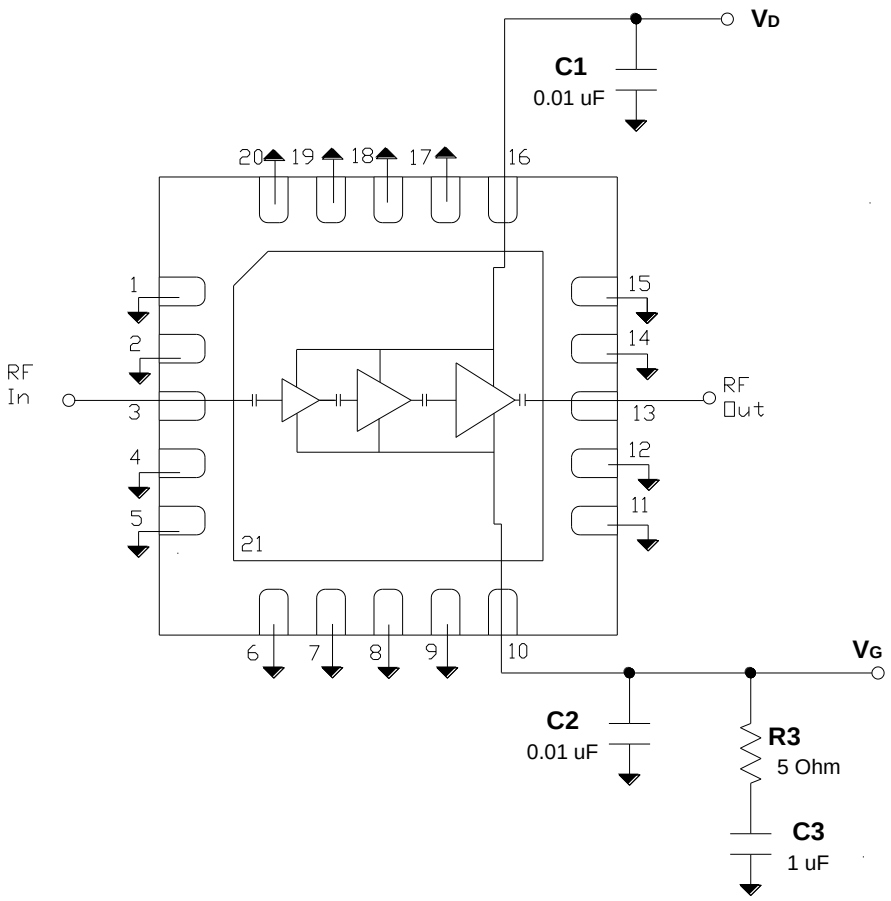
2nd Harmonic vs. Output Power vs. Temp.



3rd Harmonic vs. Output Power vs. Temp.



Application Circuit



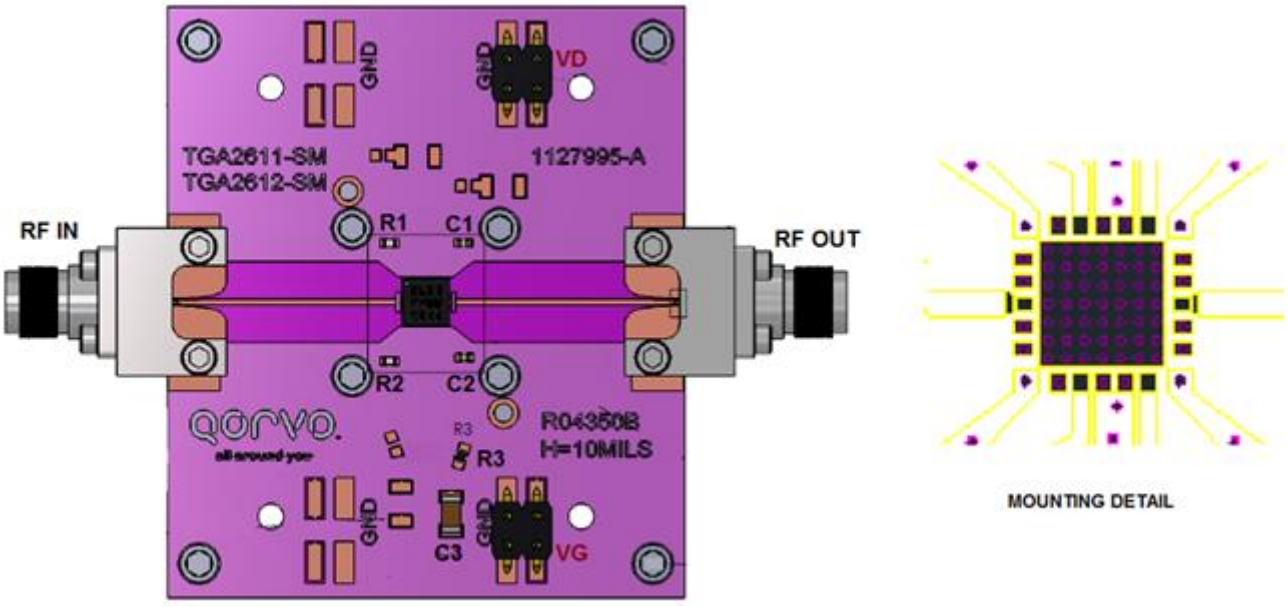
Bias Up Procedure

1. Set I_D limit to 300 mA, I_G limit to 1 mA
2. Set V_G to -5.0V
3. Set +10V to V_D
4. Adjust V_G more positive until I_{DQ} = 100 mA. (V_G ~ -2.3 V Typical)
5. Apply RF signal

Bias Down Procedure

1. Turn off RF signal
2. Set V_G to -5.0V. Ensure I_{DQ} ~ 0mA
3. Set V_D to 0V
4. Turn off V_D supply
5. Turn off V_G supply

Evaluation Board Layout



The microstrip line at the connector interface is optimized for the Southwest Microwave end launch connector 1092-01A-5.

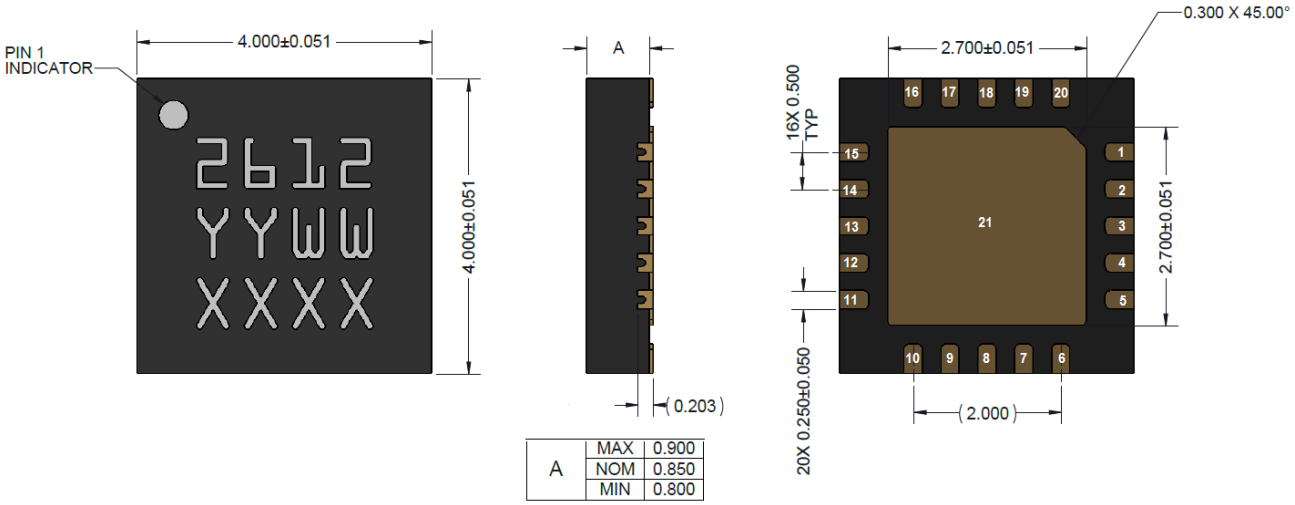
The pad pattern shown has been developed and tested for optimized assembly at Qorvo. The PCB land pattern has been developed to accommodate lead tolerances. Since processes vary from company to company, careful process development is recommended

Multiple vias should be employed under the package center paddle to minimize inductance resistance.

Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1, C2	0.01 µF	Cap, 0402, 50 V, 10%, X7R	Various	–
C3	1 µF	Cap, 1206, 50 V, 10%, X7R	Various	–
R1, R2	0 Ω	Res, 0402, 5% (Required for above EVB design)	Various	–
R3	5 Ω	Res, 0603, 5%	Various	–

Mechanical Information, Pin Configuration and Description



A		
	MAX	0.900
	NOM	0.850
	MIN	0.800

NOTES: UNLESS OTHERWISE SPECIFIED;

1. PACKAGE LEADS ARE GOLD PLATED.
2. PART IS MOLD ENCAPSULATED.
3. PART MARKING:
   2612 : PART NUMBER
   YY : PART ASSEMBLY YEAR
   WW : PART ASSEMBLY WEEK
   XXXX : BATCH ID

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS

TOLERANCES
X.XX = ±.25
X.XXX = ±.127
X.XXXX = ±.0254
ANGLES = 0.5°

Pin No.	Label	Description
1-2, 4-9, 11, 12, 14, 15, 17-20	N/C	Recommend grounding on PCB for improved package isolation. Connected to ground paddle (21)
3	RF Input	RF input, matched to 50 Ω, DC blocked
10	V_G	Gate voltage. Bias network required
13	RF Output	RF output, matched to 50 Ω, DC blocked
16	V_D	Drain voltage. Bias network required.
21	GND	Ground Paddle. Multiple vias should be employed to minimize inductance and thermal resistance.

Recommended Soldering Temperature Profile