TQP369185

DC – 6 GHz Gain Block

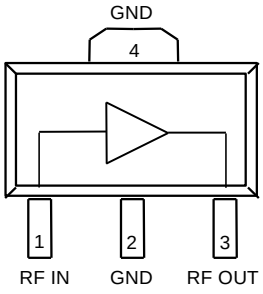
SOT-89 Package

General Description

The TQP369185 is a general-purpose buffer amplifier that offers high dynamic range in a low-cost surface-mount package. At 1.9 GHz, the amplifier typically provides 19 dB gain, +31.7 dBm OIP3, and 4.6 dB Noise Figure while drawing 75 mA current. The device combines dependable performance with consistent quality to maintain MTTF values exceeding 100 years at mounting temperatures of +85°C. The device is housed in a lead-free/green/RoHS-compliant industry-standard SOT-89 package.

The TQP369185 consists of a Darlington-pair amplifier using Qorvo's high reliability InGaP/GaAs HBT process technology. Internal active bias enables operation with only DC-blocking capacitors and an RF choke on the DC bias feed. This broadband MMIC amplifier can be directly applied to various current and next generation wireless technologies such as CDMA, W-CDMA, and LTE. In addition, the TQP369185 will work for other various applications within the DC to 6 GHz frequency range.

Functional Block Diagram



Product Features

- DC-6000 MHz
- 19 dB Gain at 1.9 GHz
- 4.7 dB Noise Figure at 1.9 GHz
- +31.7 dBm Output IP3 at 1.9 GHz
- +19.6 dBm P1dB at 1.9 GHz
- 50 Ohm Cascadable Gain Block
- Internal active bias
- SOT-89 Package

Applications

- Mobile Infrastructure
- LTE / WCDMA / CDMA
- CATV
- Point to Point
- General Purpose Wireless

Ordering Information

Part No.	Description
TQP369185	InGaP/GaAs HBT Gain Block
TQP369185-PCB	0.5-4 GHz Evaluation Board

Standard T/R size = 2500 pieces on a 13" reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−55 to 150°C
RF Input Power, CW, 50Ω, T=25°C	+25 dBm
Device Voltage (V_{CC})	+7.0 V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
T_{CASE}	−40		+85	°C
Tj (for >10^6 hours MTTF)			+170	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{CC} =5 V, T_{CASE}= +25°C, 50Ω system

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		DC		6000	MHz
Test Frequency			1900		MHz
Gain		17.5	19	20.5	dB
Input Return Loss			-13.5		dB
Output Return Loss			-9.6		dB
Output P1dB			+19.6		dBm
Output IP3	Pout=0 dBm/tone, Δf= 1 MHz	+28	+31.7		dBm
Noise Figure			4.6		dB
Device Voltage (V_{CC})		3.0	5		V
Device Current (I_{CC})		55	75	92	mA
Thermal Resistance (θ_{jc})	Junction to base(1)			82	°C/W

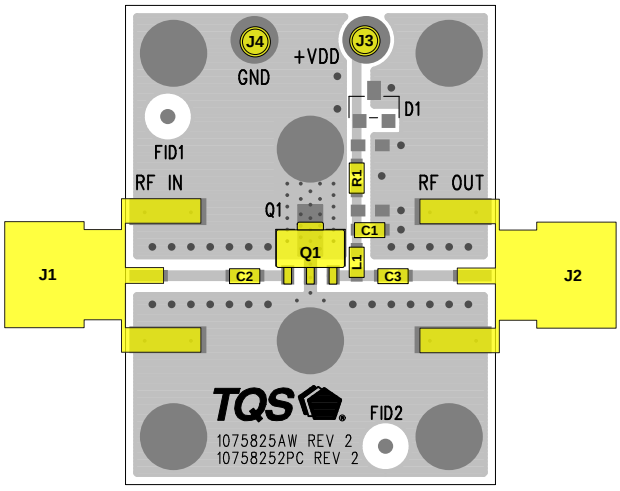
Notes:
1. Thermal path is from device junction through package ground tab (pins 2,4) to mounting surface.

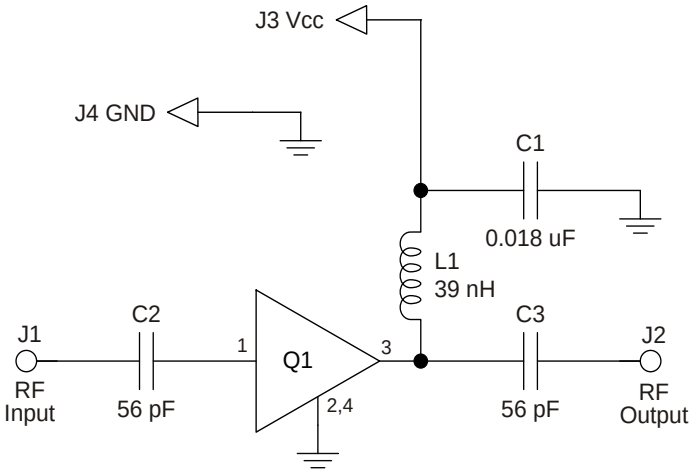
S-Parameters

Test Conditions: V_{CC}=+5.0 V (typ.), I_{CC}=72 mA (typ.), TCASE=+25°C, unmatched 50Ω system, calibrated to device leads

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
10	-19.3	-178.5	21.3	179.4	-26.2	0.5	-14.3	3.2
20	-19.0	-177.3	21.4	178.6	-26.1	0.5	-14.0	1.0
50	-18.6	-175.6	21.4	177.6	-26.0	-0.4	-14.3	-2.7
100	-18.4	-176.9	21.3	174.5	-26.1	-0.3	-14.4	-8.5
200	-17.9	-170.6	21.3	169.7	-26.1	-0.6	-14.0	-16.2
500	-16.9	-169.8	21.0	155.4	-26.0	-2.7	-13.4	-43.7
1000	-14.3	-173.6	20.5	132.9	-25.6	-6.1	-12.0	-83.8
1500	-12.3	178.7	20.0	110.6	-25.1	-10.7	-10.4	-119.2
2000	-10.7	163.5	19.3	89.1	-24.5	-18.4	-8.9	-149.9
2500	-9.1	148.7	18.5	68.1	-24.2	-26.3	-7.9	-177.8
3000	-7.8	136.2	17.7	49.2	-23.8	-34.8	-7.0	160.8
3500	-6.9	125.7	16.8	30.8	-23.5	-44.4	-6.3	141.0
4000	-6.5	115.7	15.8	12.5	-23.5	-53.7	-5.3	122.0
4500	-6.7	101.4	14.7	-4.6	-23.7	-62.5	-5.0	104.1
5000	-5.8	89.6	13.7	-19.6	-23.5	-69.4	-4.7	90.3
5500	-4.8	80.2	13.1	-36.1	-23.5	-79.2	-4.1	78.6
6000	-4.3	69.8	12.1	-52.3	-23.7	-89.4	-4.0	66.0

TQP369185-PCB Evaluation Board





Notes:

1. See Evaluation Board PCB Information section for material and stack-up.
2. All components are of 0603 size unless otherwise stated.
3. Zero Ohm resistor R1 is used to bridge a trace gap on PCB 1075825 and is not required in end user applications.

Bill of Material − TQP369185-PCB

Reference Des.	Value	Description	Manuf.	Part Number
Q1	n/a	High Linearity LNA Gain Block	Qorvo	TQP369185
C1	0.018 uF	Cap, Chip, 0603, 16V, X7R, 10%	various	
C2, C3	56 pF	Cap, Chip, 0603, 50V, NPO, 5%	various	
L1	39 nH	Inductor, 0603, 5%, CS Series	Coilcraft	
R1	0 Ω	Res, Chip, 603, 1/10W, 5%	various	

Component Values for Specific Frequencies

Use the component values in this table for optimal operation at specific frequencies.

Reference Designator	Frequency (MHz)						
	50	500	900	1900	2200	2500	3500
L1	820 nH	220 nH	68 nH	27 nH	22 nH	18 nH	15 nH
C2, C3	.018 uF	1000 pF	100 pF	68 pF	68 pF	56 pF	39 pF

Typical Performance – TQP369185-PCB

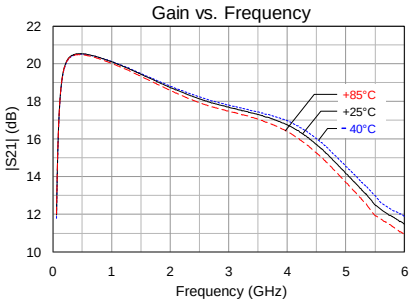
Test conditions unless otherwise noted: V_{SUPPLY} =+5 V, I_{CC} = 75 mA, T_{CASE} = +25˚C

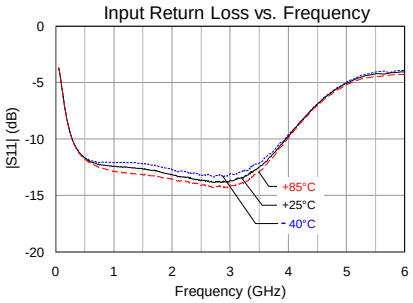
Parameter	Typical Value									Units
Frequency	500	900	1900	2100	2600	3500	4000	5000	6000	MHz
Gain	20.5	20.4	19.0	18.6	18.0	16.8	15.8	13.7	12.1	dB
Input Return Loss	11.7	12.4	12.3	13.3	13.7	-6.9	-6.5	-5.8	-4.3	dB
Output Return Loss	17.8	15.9	10	9.3	8.7	-6.3	-5.3	-4.7	-4	dB
Output P1dB	20.9	+19.8	+19.6	+19.5	+19	+17.5	+15.8	+13.9	+12.3	dBm
OIP3	+33.3	+32.3	+31.7	+31.7	+30.6	+28.6	+27.1	+24.4	+23.4	dBm
Noise Figure	4.5	4.7	4.6	4.7	4.8	4.9	5.1	5.6	6.3	dB

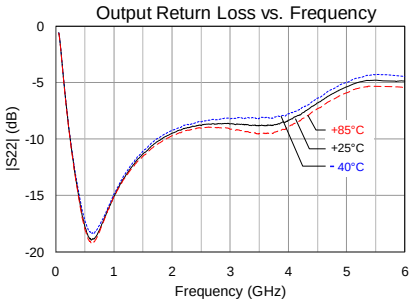
Notes:
1. OIP3 measured with two tones at an output power of 0 dBm / tone separated by 1 MHz.

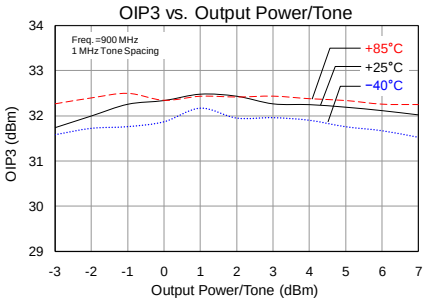
Performance Plots – TQP369185-PCB

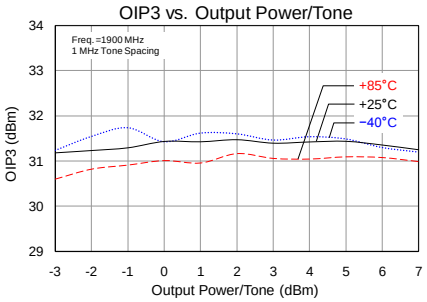
Test conditions unless otherwise noted: V_{SUPPLY} =+5 V, I_{CC} = 75 mA, T_{CASE} = +25˚C

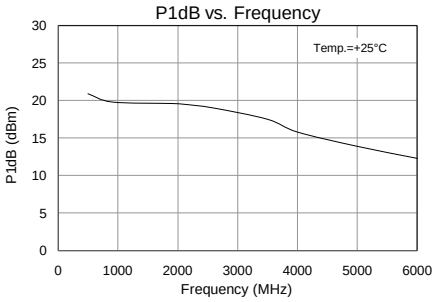


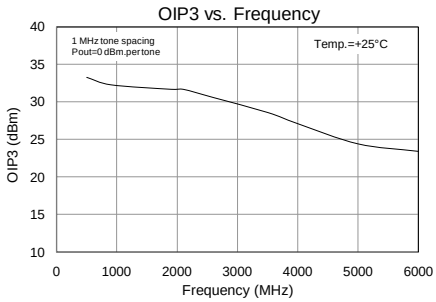


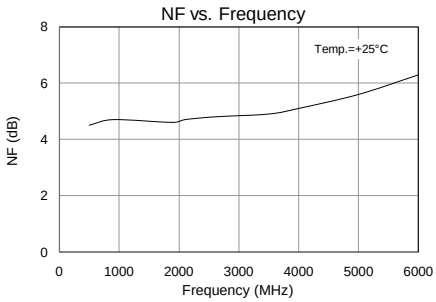




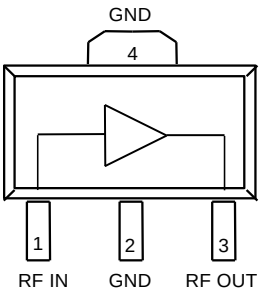








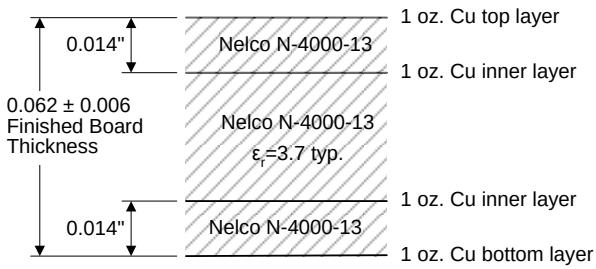
Pin Configuration and Description



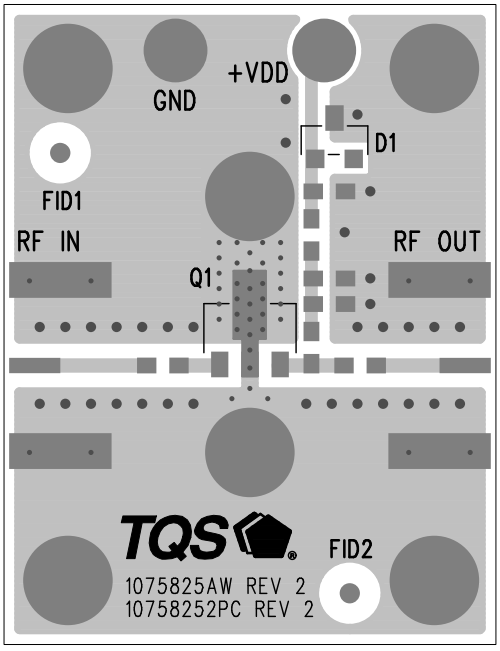
Pin No.	Label	Description
1	RF IN	RF input, matched to 50 ohms. External DC Block is required.
3	RF OUT	RF output / DC supply, matched to 50 ohms. External DC Block and bias choke, are required.
2, 4, Backside Paddle	GND Paddle	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.

Evaluation Board PCB Information

Qorvo PCB 1075825 Material and Stack-up

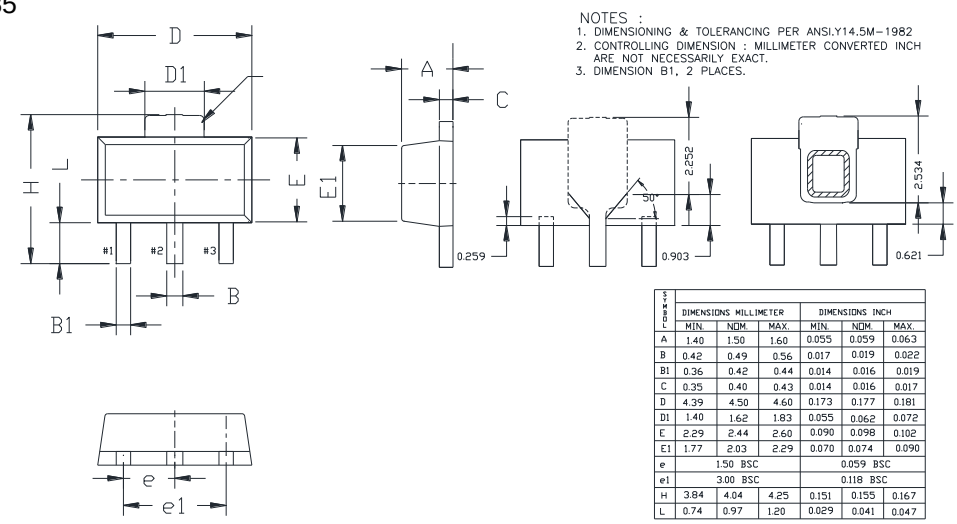


50 Ohm Line Dimensions: width=0.028"
spacing=0.028"



Package Marking and Dimensions

Marking: Part number – 369185
Lot code – XXXX

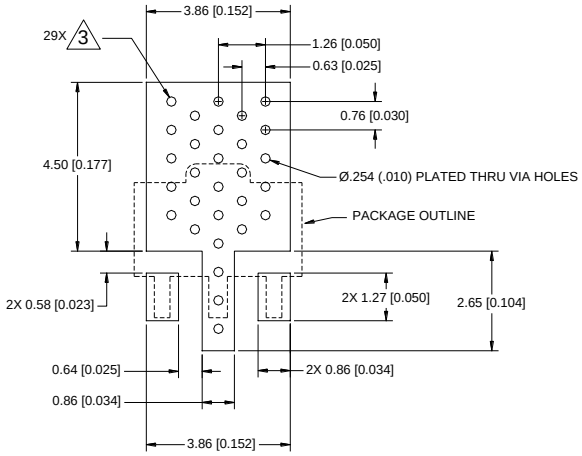


SYMBOL	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.40	1.50	1.60	0.055	0.059	0.063
B	0.42	0.49	0.56	0.017	0.019	0.022
B1	0.36	0.42	0.44	0.014	0.016	0.019
C	0.35	0.40	0.43	0.014	0.016	0.017
D	4.39	4.50	4.60	0.173	0.177	0.181
D1	1.40	1.62	1.83	0.055	0.062	0.072
E	2.29	2.44	2.60	0.090	0.098	0.102
E1	1.77	2.03	2.29	0.070	0.074	0.090
e	1.50 BSC			0.059 BSC		
e1	3.00 BSC			0.118 BSC		
H	3.84	4.04	4.25	0.151	0.155	0.167
L	0.74	0.97	1.20	0.029	0.041	0.047

Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
4. Contact plating: NiPdAu or Matte Tin

PCB Mounting Pattern



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation.
4. Do not remove or minimize via hole structure in the PCB. Thermal and RF grounding is critical.
5. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10").
6. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.