

P-Channel 80-V (D-S) MOSFET

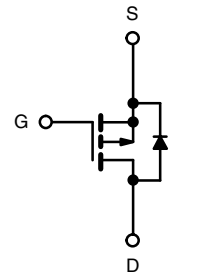
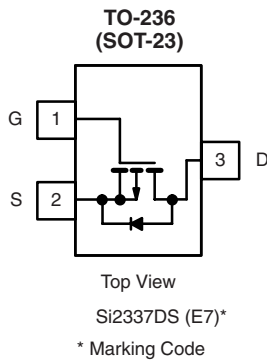
PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
- 80	0.270 at $V_{GS} = - 10$ V	- 2.2	7
	0.303 at $V_{GS} = - 6$ V	- 2.1	

FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET[®] Power MOSFET



RoHS
COMPLIANT
HALOGEN
FREE
Available



P-Channel MOSFET

Ordering Information: Si2337DS-T1-E3 (Lead (Pb)-free)
Si2337DS-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 80	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C)	$T_C = 25$ °C	- 2.2	A
	$T_C = 70$ °C	- 1.75	
	$T_A = 25$ °C	- 1.2 ^{b, c}	
	$T_A = 70$ °C	- 0.96 ^{b, c}	
Pulsed Drain Current	I_{DM}	- 7	
Continuous Source-Drain Diode Current	$T_C = 25$ °C	- 2.1	
	$T_A = 25$ °C	- 0.63 ^{b, c}	
Avalanche Current	I_{AS}	11	
Single-Pulse Avalanche Energy	E_{AS}	6.0	mJ
Maximum Power Dissipation	$T_C = 25$ °C	2.5	W
	$T_C = 70$ °C	1.6	
	$T_A = 25$ °C	0.76 ^{b, c}	
	$T_A = 70$ °C	0.48 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 50 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	R_{thJA}	120	166	°C/W
Maximum Junction-to-Foot (Drain)	R_{thJF}	40	50	

Notes:

- Package limited.
- Surface Mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- Maximum under Steady State conditions is 166 °C/W.

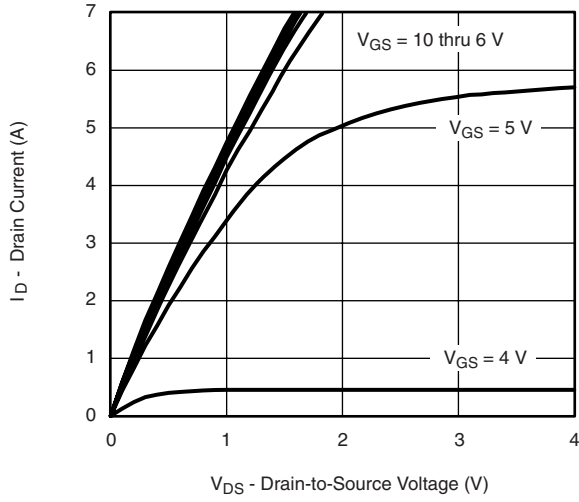
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	- 80			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		- 35.8		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			5.45		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	- 2		- 4	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -80\text{ V}, V_{GS} = 0\text{ V}$			- 1	μA
		$V_{DS} = -80\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			- 10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = -10\text{ V}$	- 7			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -1.2\text{ A}$		0.216	0.270	Ω
		$V_{GS} = -6\text{ V}, I_D = -1.1\text{ A}$		0.242	0.303	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\text{ V}, I_D = -1.2\text{ A}$		4.3		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		500		pF
Output Capacitance	C_{oss}			40		
Reverse Transfer Capacitance	C_{rss}			25		
Total Gate Charge	Q_g	$V_{DS} = -40\text{ V}, V_{GS} = -10\text{ V}, I_D = -1.2\text{ A}$		11	17.0	nC
				7	11.0	
Gate-Source Charge	Q_{gs}	$V_{DS} = -40\text{ V}, V_{GS} = -6\text{ V}, I_D = -1.2\text{ A}$		2.1		
Gate-Drain Charge	Q_{gd}			3.2		
Gate Resistance	R_g	$f = 1\text{ MHz}$		4.8		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -40\text{ V}, R_L = 42\text{ }\Omega$ $I_D \cong -0.96\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		10	15	ns
Rise Time	t_r			15	23	
Turn-Off Delay Time	$t_{d(off)}$			20	30	
Fall Time	t_f			15	23	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -40\text{ V}, R_L = 42\text{ }\Omega$ $I_D \cong -0.96\text{ A}, V_{GEN} = -6\text{ V}, R_g = 1\text{ }\Omega$		15	23	
Rise Time	t_r			18	27	
Turn-Off Delay Time	$t_{d(off)}$			20	30	
Fall Time	t_f			12	18	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			- 2.1	A
Pulse Diode Forward Current ^a	I_{SM}				- 7	
Body Diode Voltage	V_{SD}	$I_S = 0.63\text{ A}$		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 0.63\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		30	45	ns
Body Diode Reverse Recovery Charge	Q_{rr}			45	70	nC
Reverse Recovery Fall Time	t_a			25		ns
Reverse Recovery Rise Time	t_b			5		

Notes:

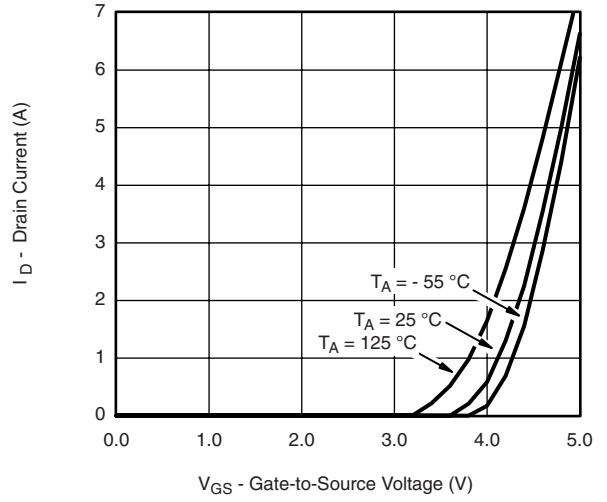
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

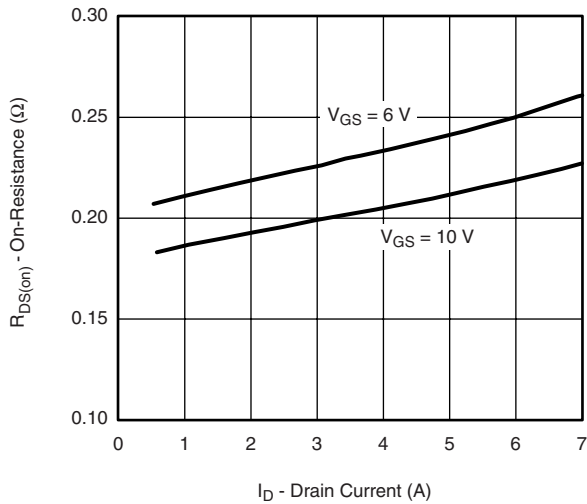
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



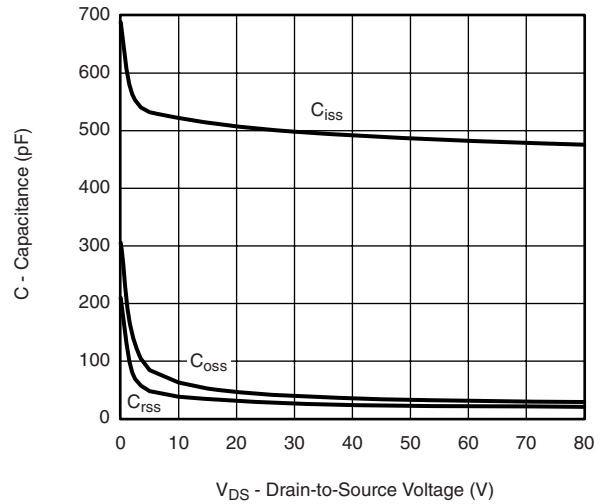
Output Characteristics



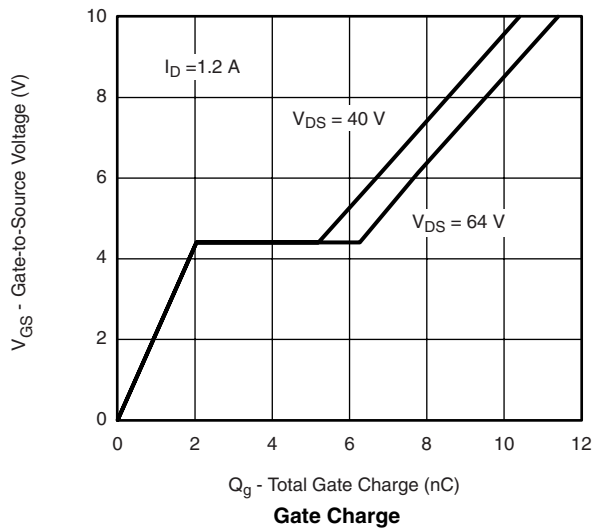
Transfer Characteristics



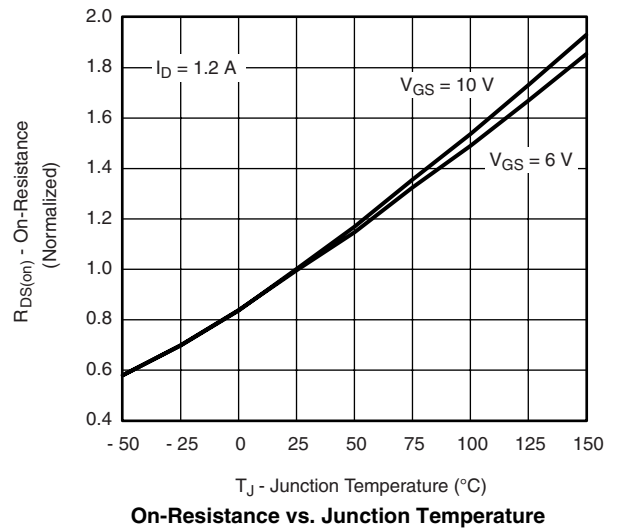
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

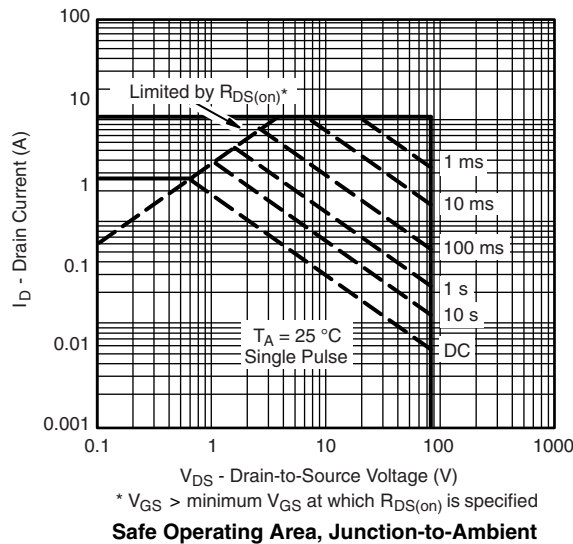
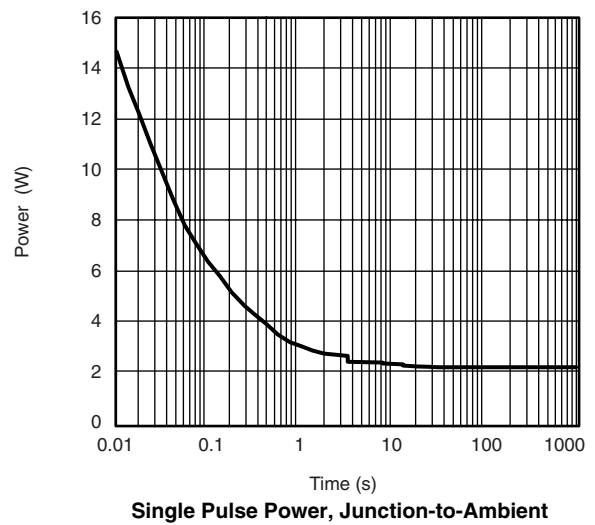
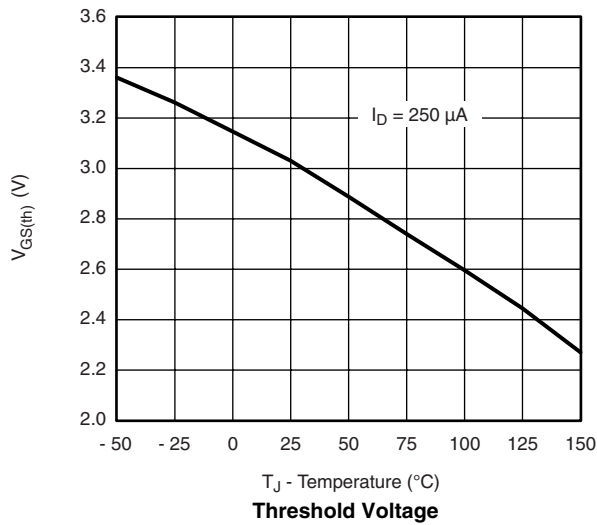
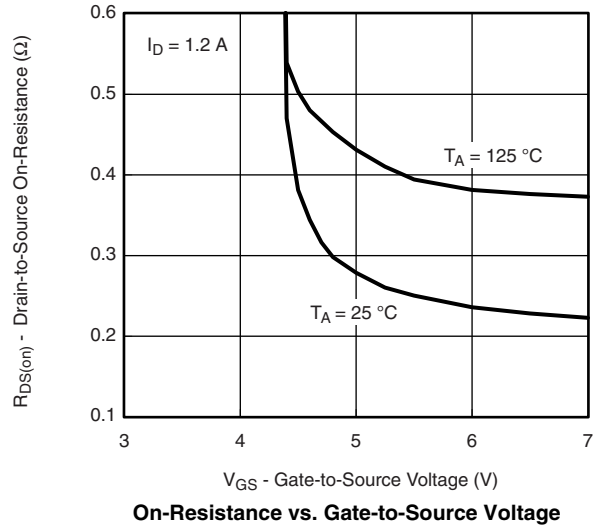
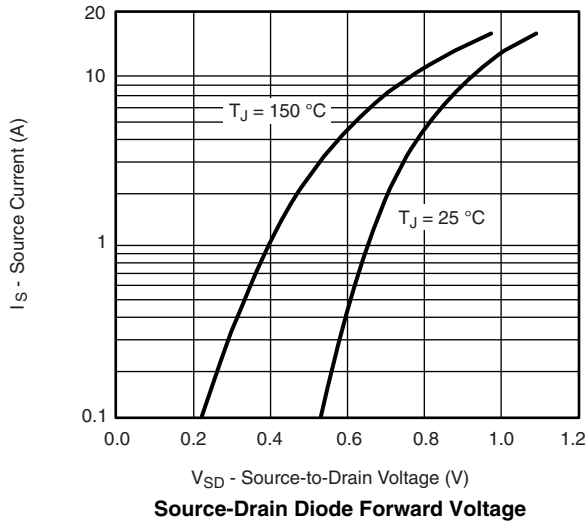


Gate Charge

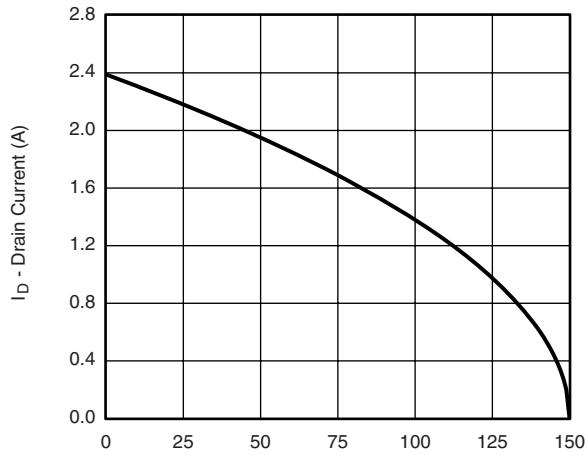


On-Resistance vs. Junction Temperature

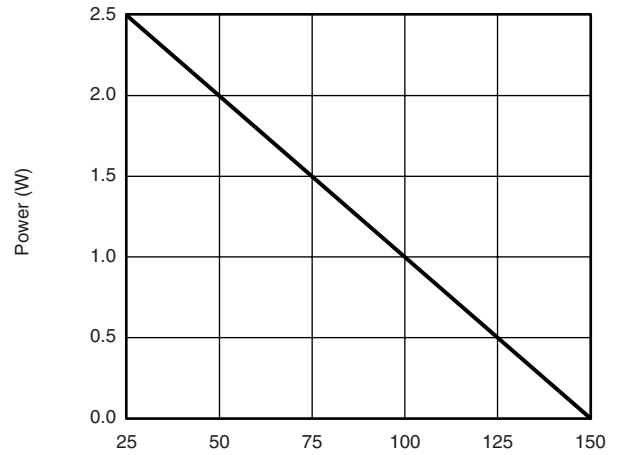
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



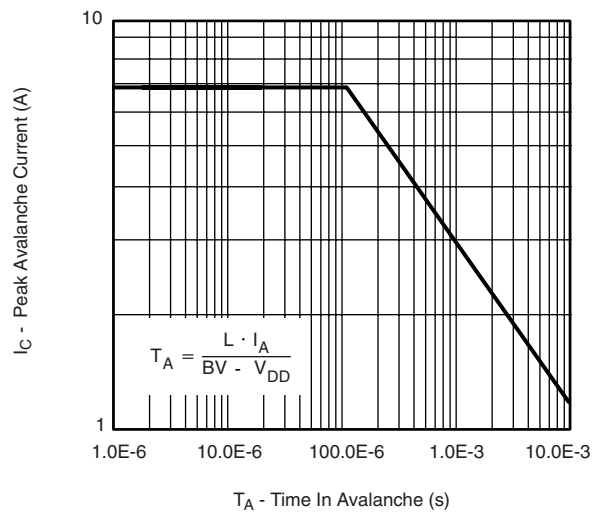
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



T_C - Case Temperature (°C)
Current Derating*



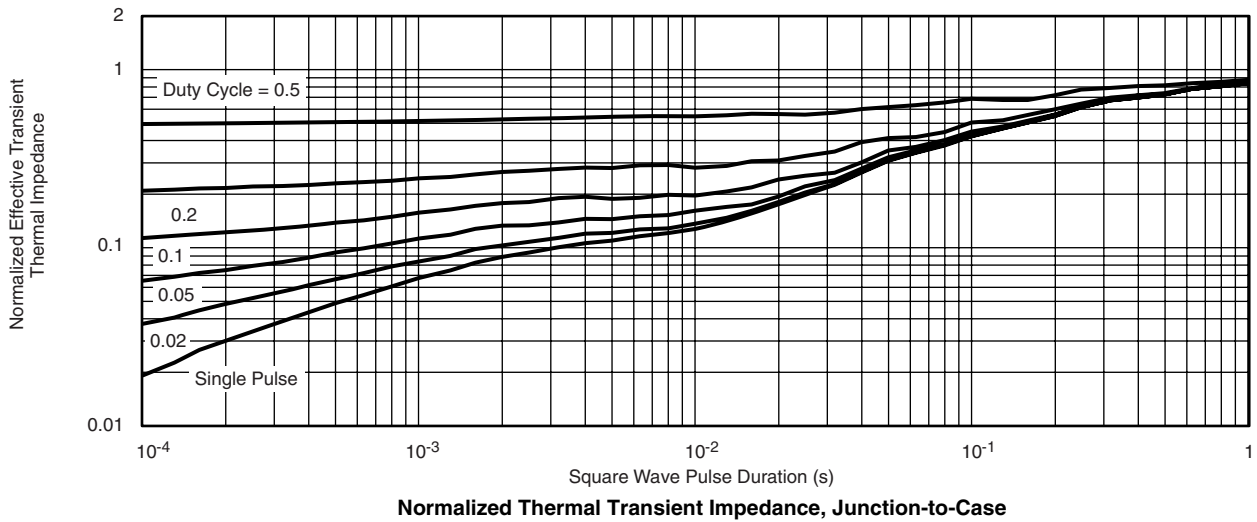
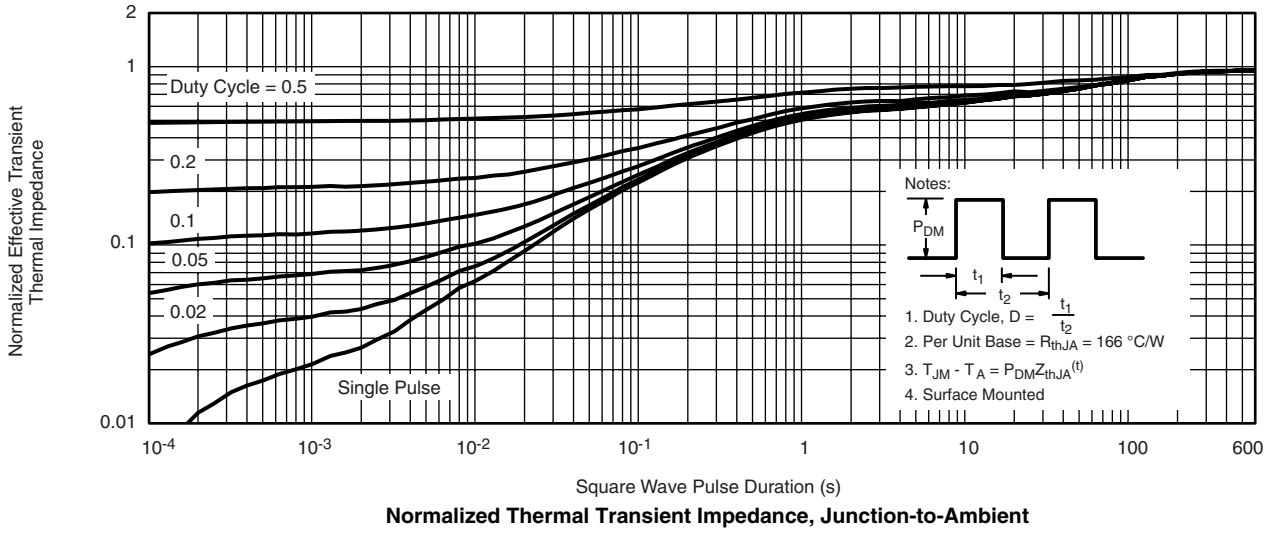
T_C - Case Temperature (°C)
Power Derating



Single Pulse Avalanche Capability

* The power dissipation P_D is based on T_{J(max)} = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73533.

SOT-23 (TO-236): 3-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	0.89	1.12	0.035	0.044
A ₁	0.01	0.10	0.0004	0.004
A ₂	0.88	1.02	0.0346	0.040
b	0.35	0.50	0.014	0.020
c	0.085	0.18	0.003	0.007
D	2.80	3.04	0.110	0.120
E	2.10	2.64	0.083	0.104
E ₁	1.20	1.40	0.047	0.055
e	0.95 BSC		0.0374 Ref	
e ₁	1.90 BSC		0.0748 Ref	
L	0.40	0.60	0.016	0.024
L ₁	0.64 Ref		0.025 Ref	
S	0.50 Ref		0.020 Ref	
q	3°	8°	3°	8°

ECN: S-03946-Rev. K, 09-Jul-01
 DWG: 5479

Mounting LITTLE FOOT[®] SOT-23 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (<http://www.vishay.com/doc?72286>), for the basis of the pad design for a LITTLE FOOT SOT-23 power MOSFET footprint. In converting this footprint to the pad set for a power device, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

The electrical connections for the SOT-23 are very simple. Pin 1 is the gate, pin 2 is the source, and pin 3 is the drain. As in the other LITTLE FOOT packages, the drain pin serves the additional function of providing the thermal connection from the package to the PC board. The total cross section of a copper trace connected to the drain may be adequate to carry the current required for the application, but it may be inadequate thermally. Also, heat spreads in a circular fashion from the heat source. In this case the drain pin is the heat source when looking at heat spread on the PC board.

Figure 1 shows the footprint with copper spreading for the SOT-23 package. This pattern shows the starting point for utilizing the board area available for the heat spreading copper. To create this pattern, a plane of copper overlies the drain pin and provides planar copper to draw heat from the drain lead and start the process of spreading the heat so it can be dissipated into the

ambient air. This pattern uses all the available area underneath the body for this purpose.



FIGURE 1. Footprint With Copper Spreading

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, “thermal” connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low-impedance path for heat to move away from the device.

RECOMMENDED MINIMUM PADS FOR SOT-23



Recommended Minimum Pads
Dimensions in Inches/(mm)

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