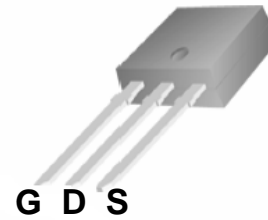




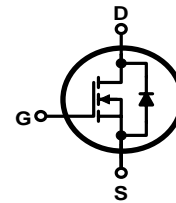
PIN Connection TO-251(I-PAK)

Features:

- Low Intrinsic Capacitances.
- Excellent Switching Characteristics.
- Extended Safe Operating Area.
- Unrivalled Gate Charge :Qg=29nC (Typ.).
- BVDSS=650V, I_D=7A
- R_{DS(on)} : 1.2Ω (Max) @V_G=10V
- 100% Avalanche Tested



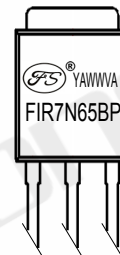
Schematic diagram



Order Information

Part No.	MOQ		
	Tube	Box	Carton
FIR7N65FG-ITH	50	1000	5000

Marking Diagram



- Y = Year
- A = Assembly Location
- WW = Work Week
- VA = Version & Assembly plant
- FIR7N65BP = Specific Device Code

Absolute Maximum Ratings (Ta=25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V _{DSS}	Drain-Source Voltage	650	V
I _D	Drain Current	T _j =25°C	7.0
		T _j =100°C	4.7
V _{GS(TH)}	Gate Threshold Voltage	±30	V
E _{AS}	Single Pulse Avalanche Energy (note1)	420	mJ
I _{AR}	Avalanche Current (note2)	7.0	A
P _D	Power Dissipation (T _j =25°C)	90	W
T _j	Junction Temperature(Max)	150	°C
T _{stg}	Storage Temperature	-55~+150	°C
TL	Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds	300	°C

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
R _{θJC}	Thermal Resistance, Junction to Case	-	1.39	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient	-	110	°C/W



Electrical Characteristics (Ta=25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0	650	-	-	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D =250μA, Reference to 25°C	-	0.67	-	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =650V, V _{GS} =0V	-	-	10	μA
		V _{DS} =520V, T _j =125°C	-	-	100	
I _{GSSF}	Gate-body leakage Current, Forward	V _{GS} =+30V, V _{DS} =0V	-	-	100	nA
I _{GSSR}	Gate-body leakage Current, Reverse	V _{GS} =-30V, V _{DS} =0V	-	-	-100	
On Characteristics						
V _{GS(TH)}	Gate Threshold Voltage	I _D =250μA, V _{DS} =V _{GS}	2	-	4	V
R _{DS(ON)}	Static Drain-Source On-Resistance	I _D =3.5A, V _{GS} =10V	-	-	1.2	Ω
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0, f=1.0MHz	-	1100	1430	pF
C _{oss}	Output Capacitance		-	135	175	
C _{rss}	Reverse Transfer Capacitance		-	16	21	
Switching Characteristics						
T _{d(on)}	Turn-On Delay Time	V _{DD} =325V, I _D =7A R _G =25Ω (Note 3,4)	-	30	70	ns
T _r	Turn-On Rise Time		-	80	170	
T _{d(off)}	Turn-Off Delay Time		-	65	140	
T _f	Turn-Off Rise Time		-	60	130	
Q _g	Total Gate Charge	V _{DS} =520V, V _{GS} =10V, I _D =7A (Note 3,4)	-	29	38	nC
Q _{gs}	Gate-Source Charge		-	7	-	
Q _{gd}	Gate-Drain Charge		-	14.5	-	
Drain-Source Diode Characteristics and Maximum Ratings						
I _s	Max. Diode Forward Current	-	-	-	7	A
I _{SM}	Max. Pulsed Forward Current	-	-	-	28	
V _{SD}	Diode Forward Voltage	I _D =7A	-	-	1.4	V
T _{rr}	Reverse Recovery Time	I _S =7A, V _{GS} =0V diF/dt=100A/μs	-	320	-	μs
Q _{rr}	Reverse Recovery Charge	(Note3)	-	2.4	-	μC

- Notes : 1, L=17.1mH, I_{AS}=7A, V_{DD}=50V, R_G=25Ω, Starting T_J =25°C
 2, Repetitive Rating : Pulse width limited by maximum junction temperature
 3, Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%
 4, Essentially Independent of Operating Temperature



Typical Characteristics

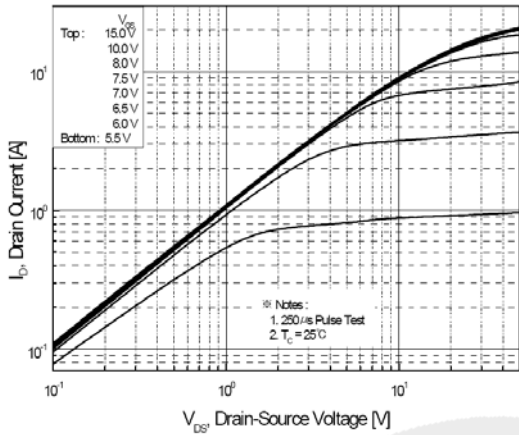


Figure 1. On-Region Characteristics

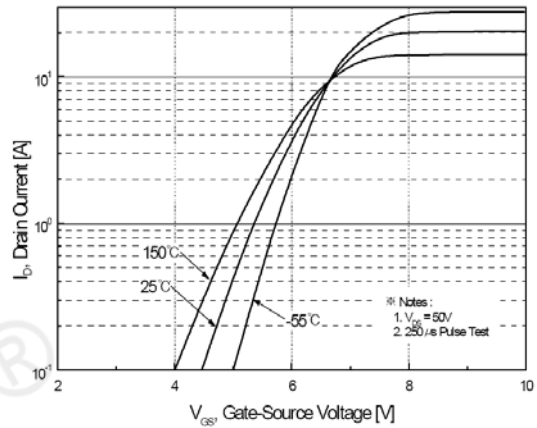


Figure 2. Transfer Characteristics

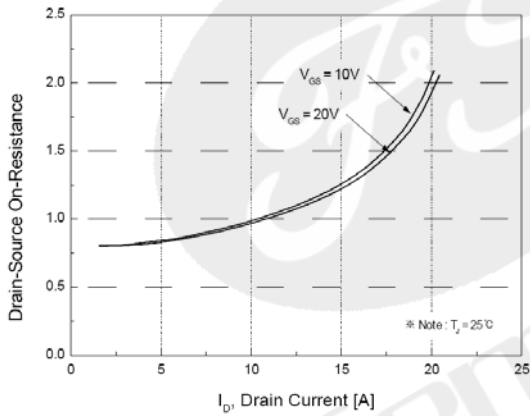


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

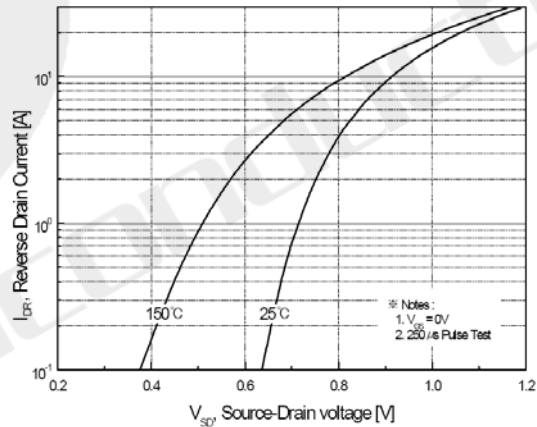


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

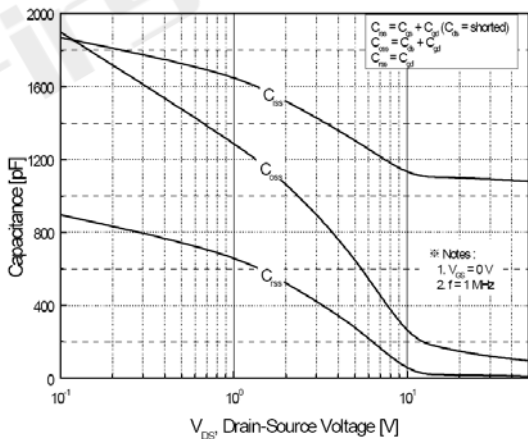


Figure 5. Capacitance Characteristics

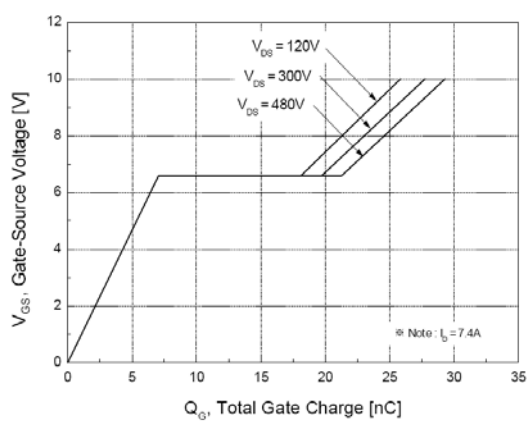


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

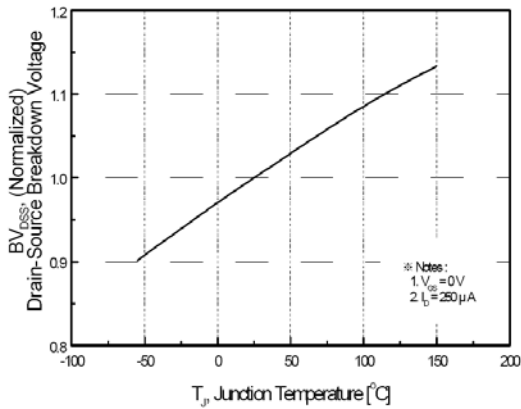


Figure 7. Breakdown Voltage Variation vs Temperature

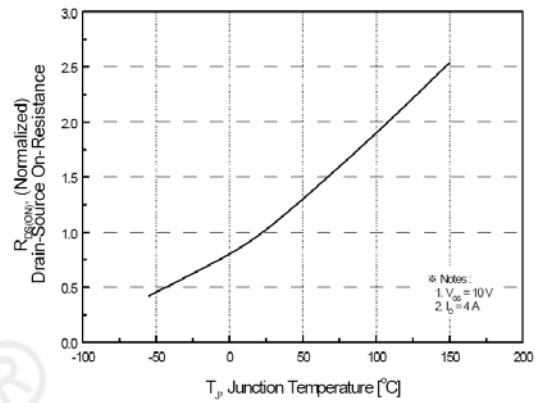


Figure 8. On-Resistance Variation vs Temperature

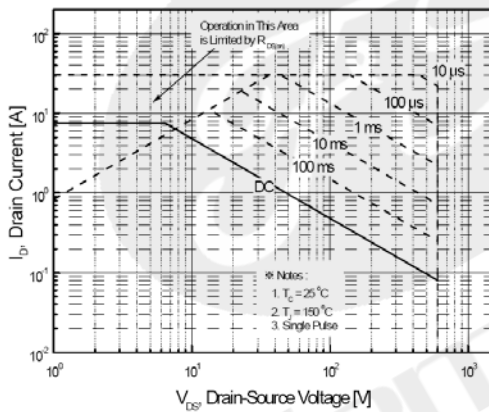


Figure 9-2. Maximum Safe Operating Area

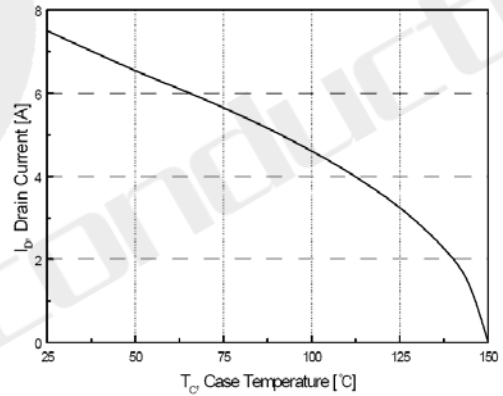


Figure 10. Maximum Drain Current vs Case Temperature

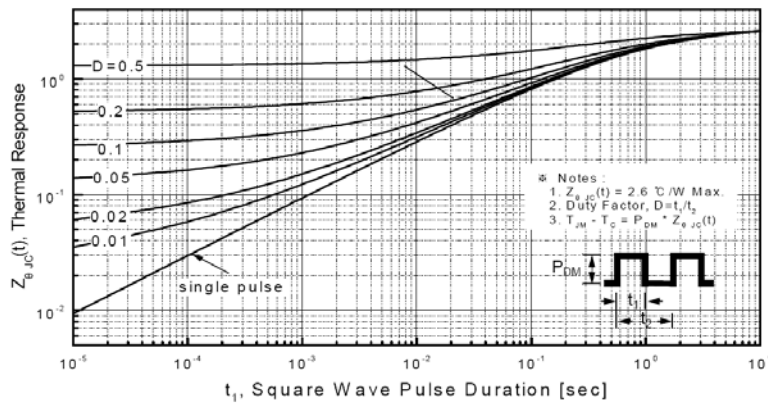
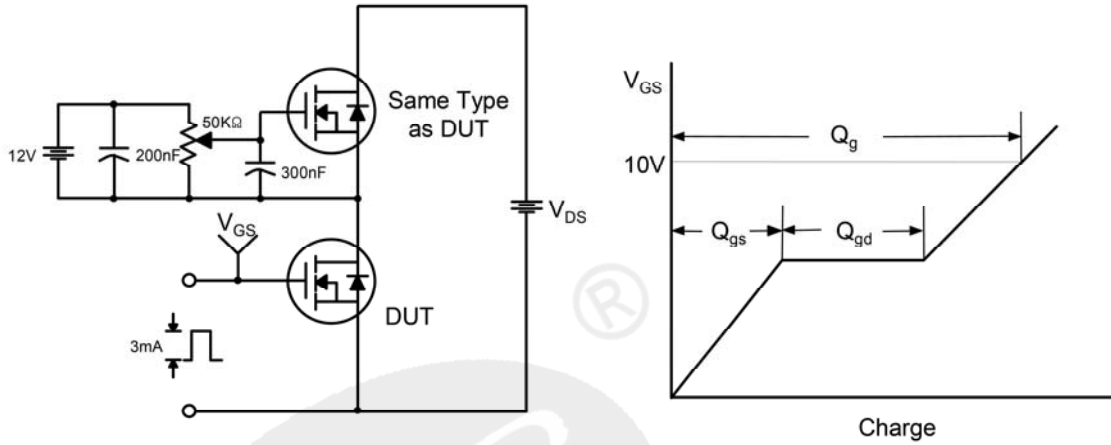
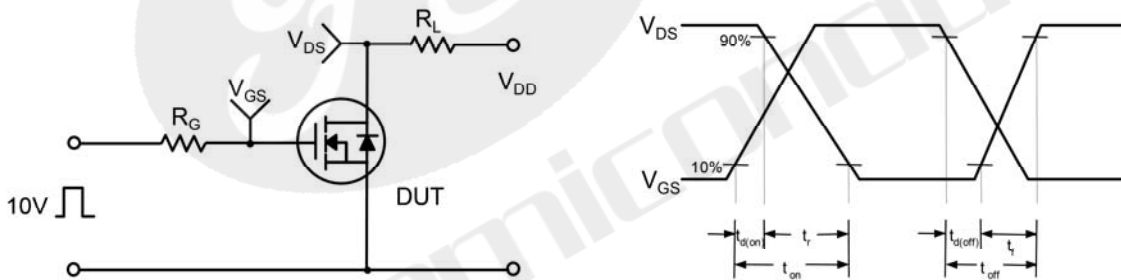


Figure 11-2. Transient Thermal Response Curve

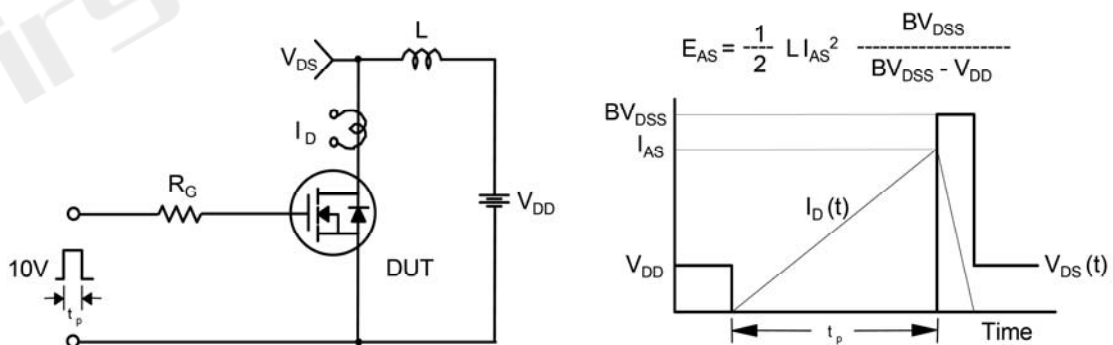
Gate Charge Test Circuit & Waveform



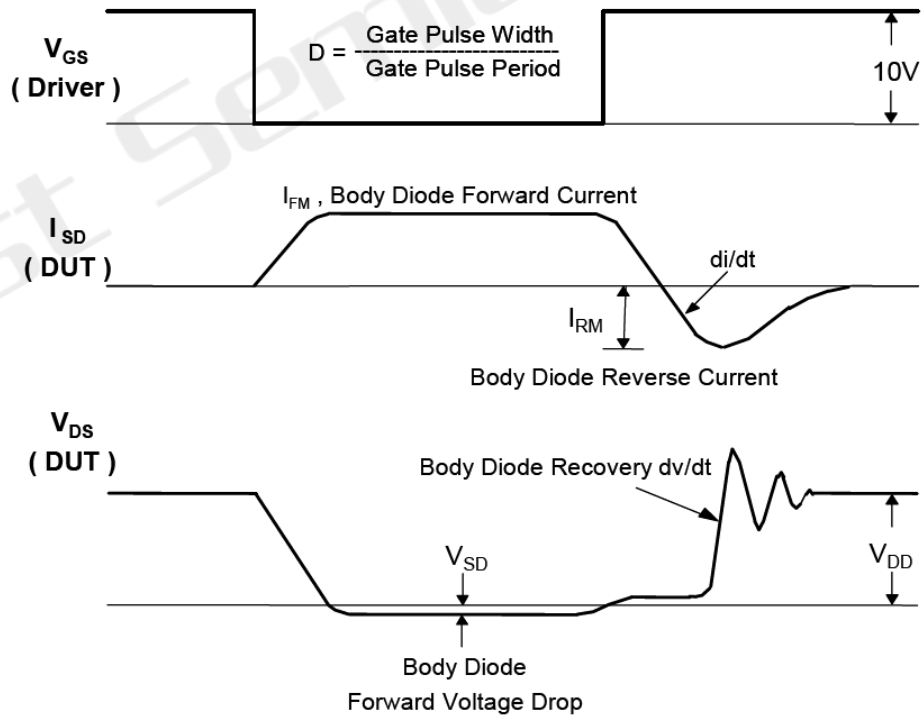
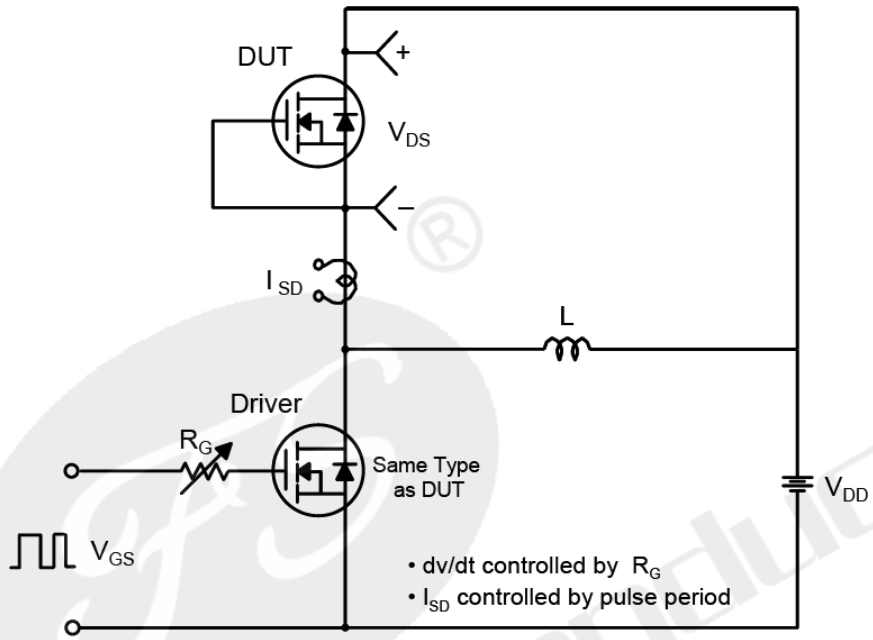
Resistive Switching Test Circuit & Waveforms



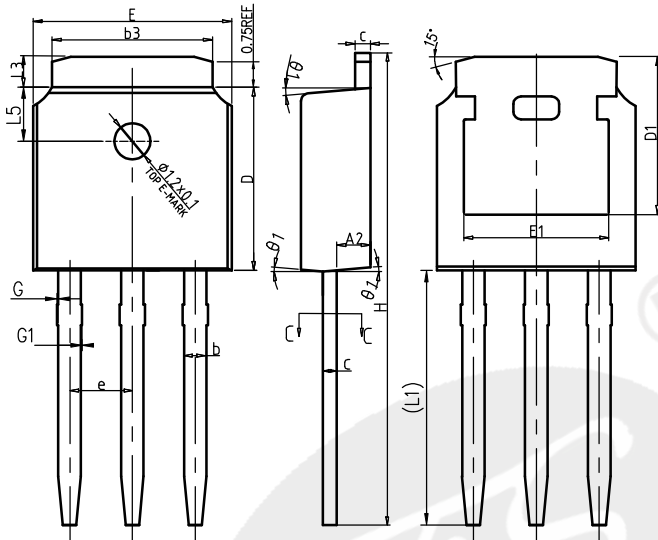
Unclamped Inductive Switching Test Circuit & Waveforms



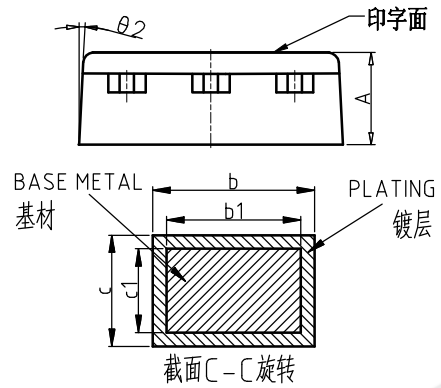
Peak Diode Recovery dv/dt Test Circuit & Waveform



TO-251(I-PAK)



Units: mm



COMMON DIMENSIONS

SYMBOL	MM		
	MIN	NOM	MAX
A	2.20	2.30	2.38
A2	0.97	1.07	1.17
b	0.72	0.78	0.85
b1	0.71	0.76	0.81
b3	5.23	5.33	5.46
c	0.47	0.53	0.58
c1	0.46	0.51	0.56
D	6.00	6.10	6.20
D1	5.30REF		
E	6.50	6.60	6.70
E1	4.70	4.83	4.92
e	2.286BSC		
H	16.10	16.40	16.60
L1	9.20	9.40	9.60
L3	0.90	1.02	1.25
L5	1.70	1.80	1.90
1	5°	7°	9°
2	5°	7°	9°

NOTES

1.ALL DIMENSIONS REFER TO JEDEC STANDARD TO-251 AA, DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.



Declaration

- FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.
- Any semiconductor product under certain conditions has the possibility of failure or failure, The buyer has the responsibility to comply with safety standards and take safety measures when using FIRST products for system design and manufacturing, To avoid To avoid potential failure risks, which may cause personal injury or property damage!
- Product promotion endless, our company will wholeheartedly provide customers with better products!

ATTACHMENT

Revision History

Date	REV	Description	Page
2018.01.01	1.0	Initial release	