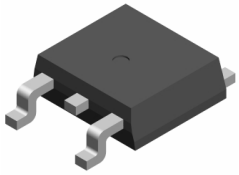
First Semiconductor

FIR60N075LG

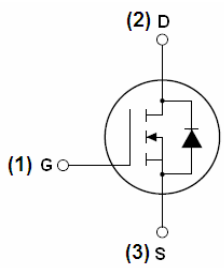
N-Channel Enhancement Mode Power Mosfet

PIN Connection TO-252



Description

The FIR60N075LG uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

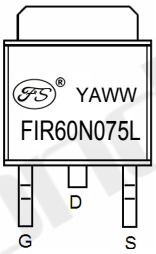


Features

- V_{DS}=75V；I_D=60A@ V_{GS}=10V；
  $R_{DS(ON)}$<8.5mΩ @ V_{GS}=10V
- Special process technology for high ESD capability
- Special designed for Convertors and power controls
- High density cell design for ultra low Rdson
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



Marking Diagram

Y	= Year
A	= Assembly Location
WW	= Work Week
FIR60N075L	= Specific Device Code

Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
FIR60N075L	FIR60N075LG	TO-252	-	-	-

Absolute Maximum Ratings (TA=25℃)

Parameter	Symbol	Value	Unit
Drain-Source Voltage (V_{GS}=0V)	V_{DS}	75	V
Gate-Source Voltage (V_{DS}=0V)	V_{GS}	±20	V
Drain Current (DC) at Tc=25℃	$I_{D\ (DC)}$	60	A
Drain Current (DC) at Tc=100℃	$I_{D\ (DC)}$	48	A
Drain Current-Continuous@ Current-Pulsed (Note 1)	$I_{DM\ (pluse)}$	310	A
Peak diode recovery voltage	dv/dt	30	V/ns
Maximum Power Dissipation(Tc=25℃)	P_D	140	W
Derating factor		0.95	W/℃
Single pulse avalanche energy (Note 2)	E_{AS}	300	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2.EAS condition：Tj=25℃,VDD=50V,VG=10V,L=0.5mH

Thermal Characteristic

Parameter	Symbol	Value	Unit
Thermal Resistance，Junction-to-Case（Maximum）	R_{thJC}	1.05	℃/W
Thermal Resistance，Junction-to-Ambient （Maximum）	R_{thJA}	50	℃/W

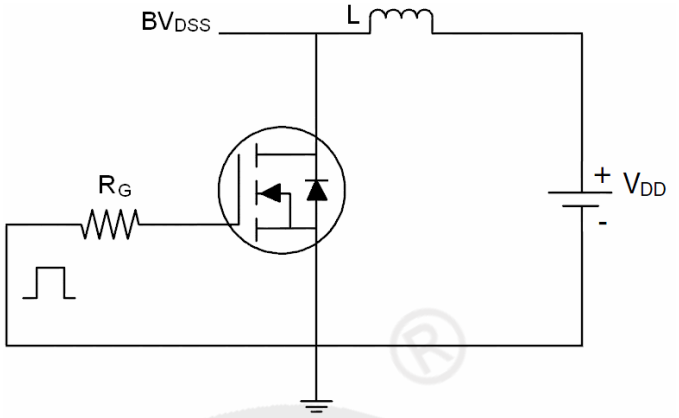
Electrical Characteristics (TA=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
On/off states						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	75	84	-	V
Zero Gate Voltage Drain Current(Tc=25℃)	I_{DSS}	V_{DS}=75V,V_{GS}=0V	-	-	1	μA
Zero Gate Voltage Drain Current(Tc=125℃)	I_{DSS}	V_{DS}=75V,V_{GS}=0V	-	-	10	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=30A	-	6.8	8.5	mΩ
Dynamic Characteristics						
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=30A	-	60	-	S
Input Capacitance	C_{lss}	V_{DS}=25V,V_{GS}=0V, F=1.0MHz	-	3100	-	PF
Output Capacitance	C_{oss}		-	310	-	PF
Reverse Transfer Capacitance	C_{rss}		-	260	-	PF
Total Gate Charge	Q_g	V_{DS}=30V,I_D=30A, V_{GS}=10V	-	100	-	nC
Gate-Source Charge	Q_{gs}		-	18	-	nC
Gate-Drain Charge	Q_{gd}		-	27	-	nC
Switching times						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=30V,I_D=2A,R_L=15Ω V_{GS}=10V,R_G=2.5Ω	-	18.2	-	nS
Turn-on Rise Time	t_r		-	15.6	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	70.5	-	nS
Turn-Off Fall Time	t_f		-	13.8	-	nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I_{SD}		-	-	80	A
Pulsed Source-drain current(Body Diode)	I_{SDM}		-	-	320	A
Forward on voltage(Note 1)	V_{SD}	Tj=25℃,I_{SD}=30A,V_{GS}=0V	-	-	1.2	V
Reverse Recovery Time(Note 1)	t_{rr}	Tj=25℃,I_F=75A,di/dt=100A/μs	-	-	53	nS
Reverse Recovery Charge(Note 1)	Q_{rr}		-	-	105	nC
Forward Turn-on Time	t_{on}	Intrinsic turn-on time is negligible(turn-on is dominated by L_S+L_D)				

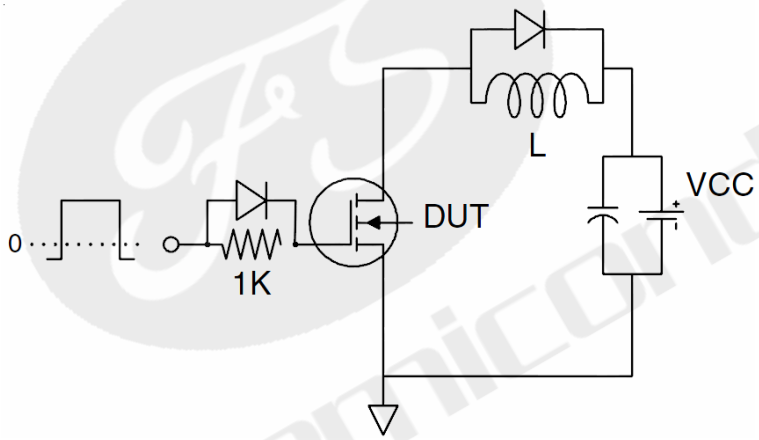
Notes 1.Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 1.5%, R_G=25Ω, Starting Tj=25℃

Test circuit

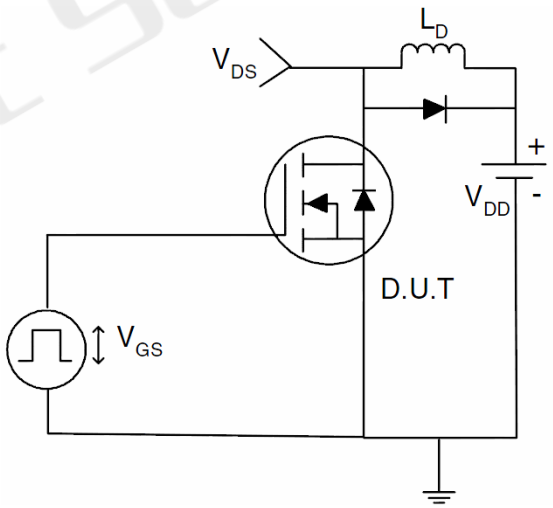
1）E_{AS} test circuits



2）Gate charge test circuit:



3）Switch Time Test Circuit ：



Typical Electrical And Thermal Characteristics(Curves)

Figure1. Safe operating area

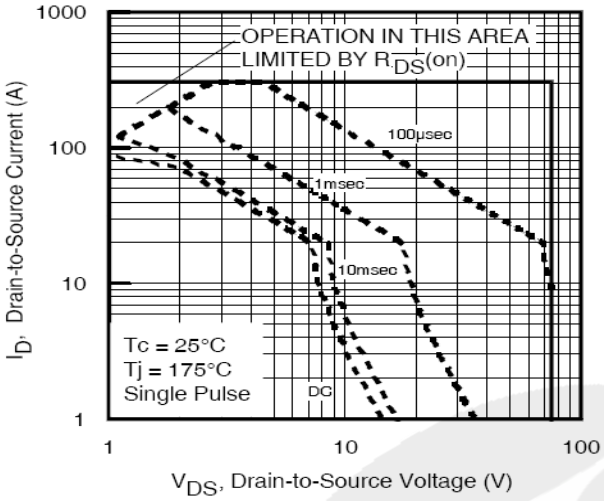


Figure2. Source-Drain Diode Forward Voltage

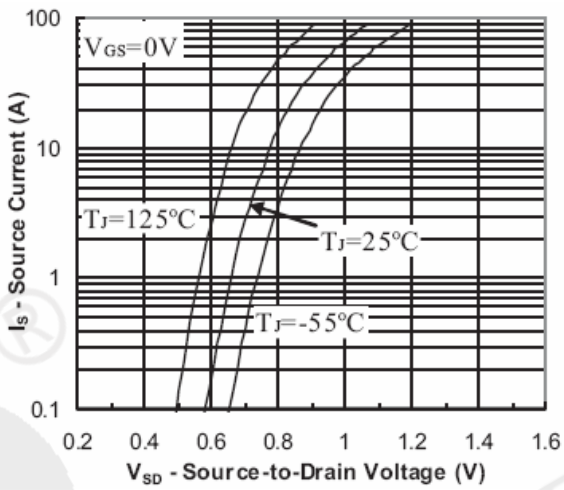


Figure3. Output characteristics

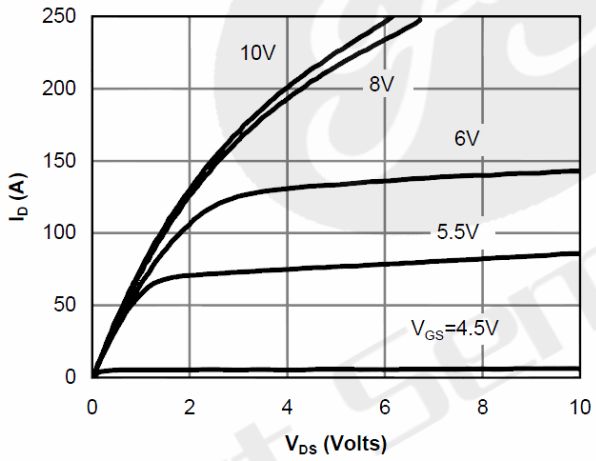


Figure4. Transfer characteristics

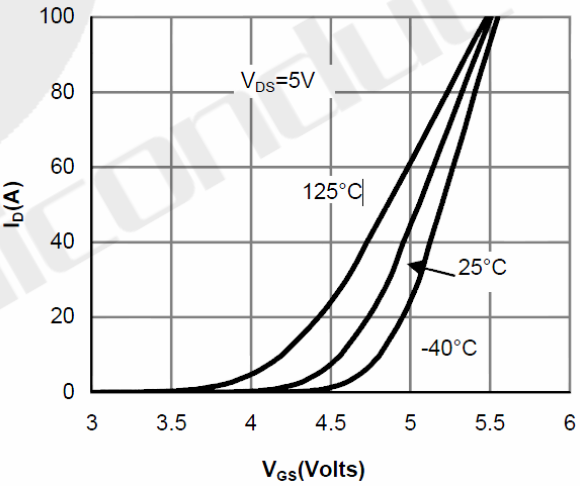


Figure5. Static drain-source on resistance

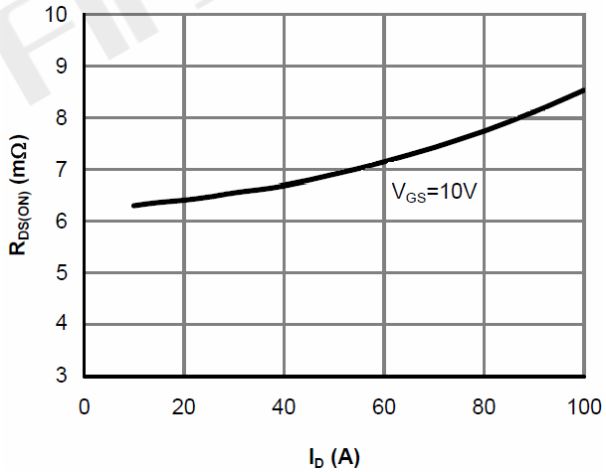


Figure6. $R_{DS(ON)}$ vs Junction Temperature

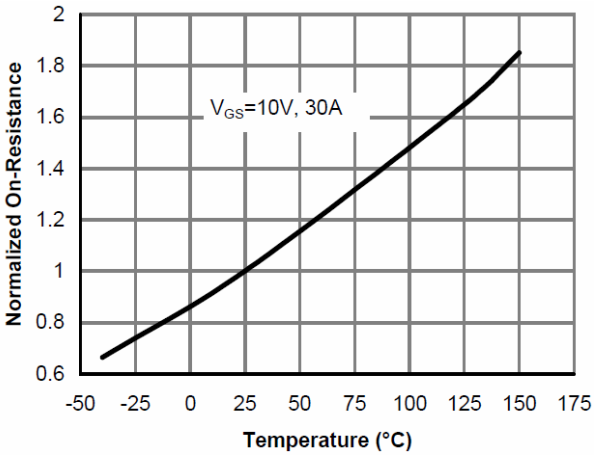


Figure7. BV_{DSS} vs Junction Temperature

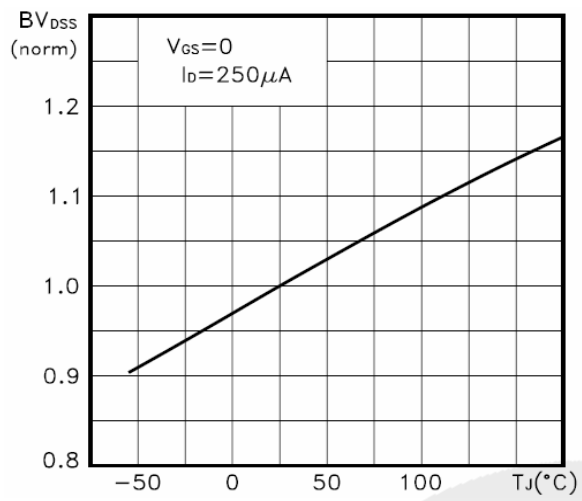


Figure8. $V_{GS(th)}$ vs Junction Temperature

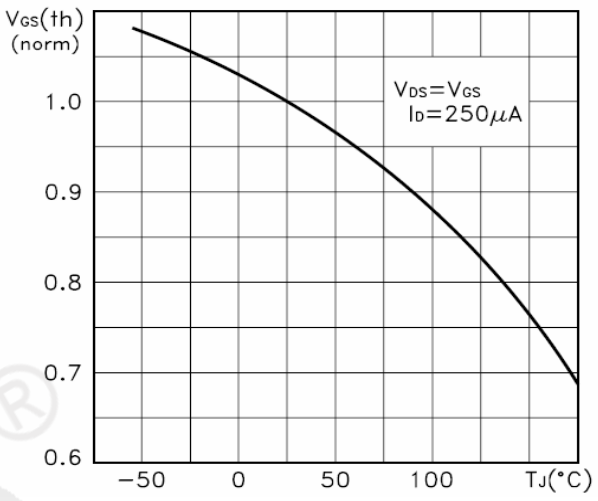


Figure9. Gate charge waveforms

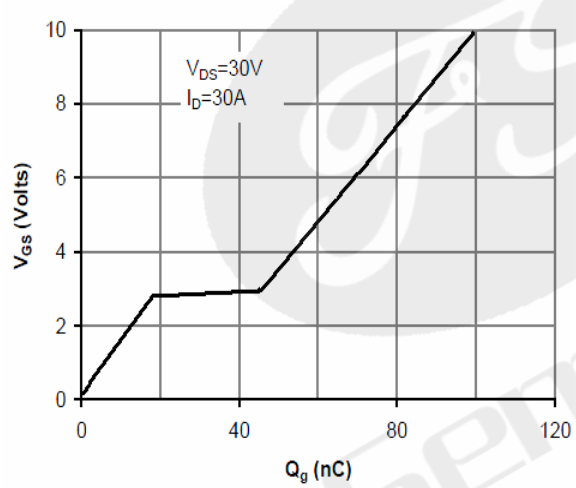


Figure10. Capacitance

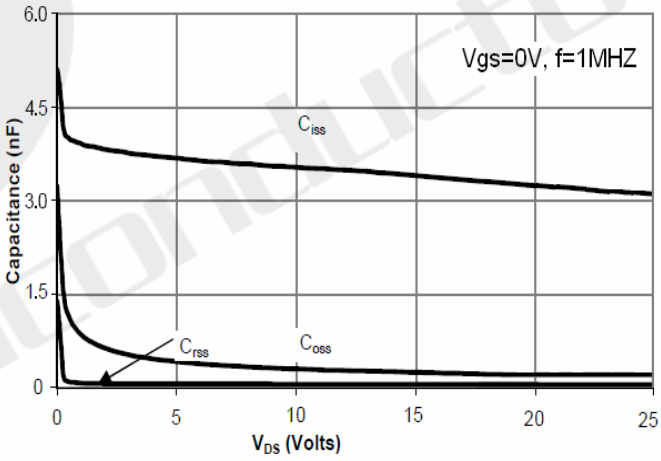
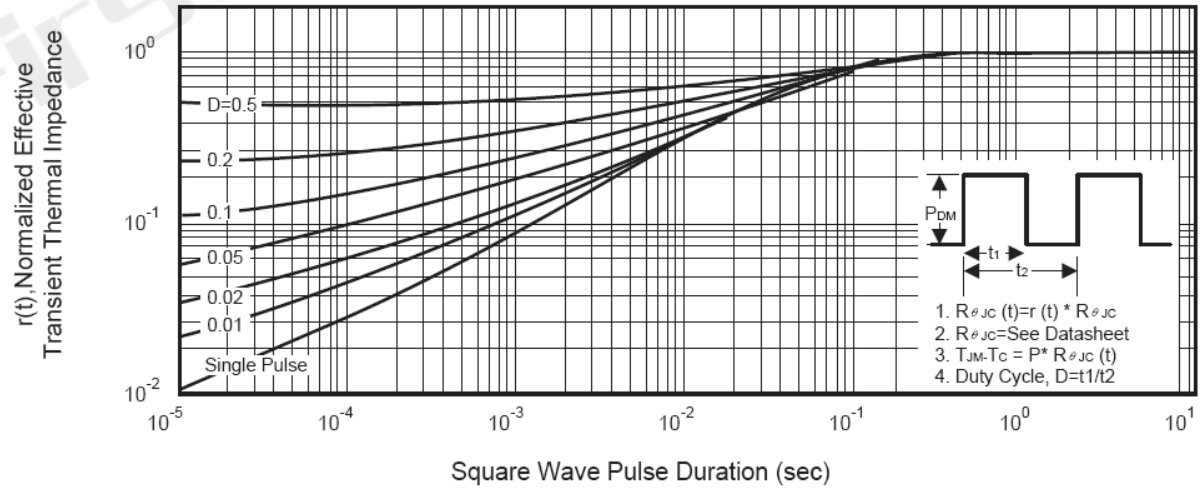
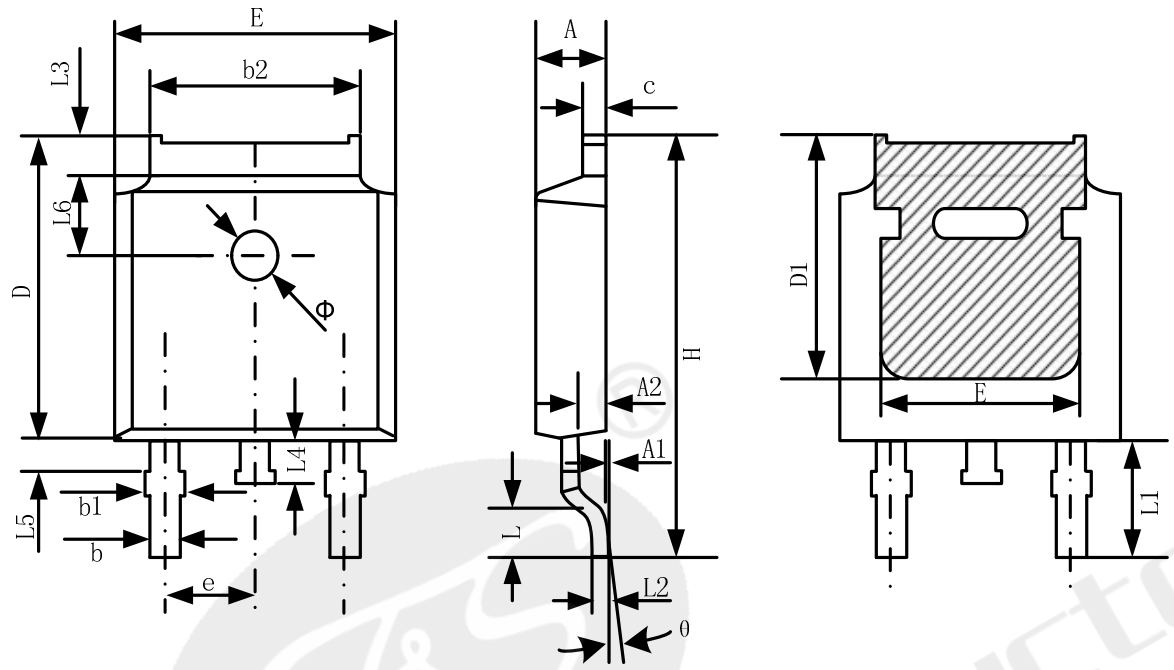


Figure11. Normalized Maximum Transient Thermal Impedance



Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.20	2.38	0.087	0.094
A1	0.00	0.10	0.000	0.004
A2	0.90	1.10	0.035	0.043
b	0.72	0.85	0.028	0.033
b1	0.72	0.90	0.028	0.035
b2	5.13	5.46	0.202	0.215
c	0.47	0.60	0.019	0.024
D	6.00	6.20	0.236	0.244
D1	5.25	--	0.207	--
E	6.50	6.70	0.256	0.264
E1	4.70	--	0.185	--
e	2.19	2.39	0.086	0.094
H	9.80	10.40	0.386	0.409
L	1.40	1.70	0.055	0.067
L1	2.90 REF		0.114 REF	
L2	0.508 BSC		0.020 BSC	
L3	0.90	1.25	0.035	0.049
L4	0.60	1.00	0.024	0.039
L5	0.15	0.75	0.006	0.030
L6	1.80 REF		0.071 REF	
Φ	1.20	1.40	0.047	0.055
θ	0°	8°	0°	8°

Declaration

- FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.
- Any semiconductor product under certain conditions has the possibility of failure or failure,The buyer has the responsibility to comply with safety standards and take safety measures when using FIRST products for system design and manufacturing,To avoid To avoid potential failure risks, which may cause personal injury or property damage!
- Product promotion endless, our company will wholeheartedly provide customers with better products!

ATTACHMENT

Revision History

Date	REV	Description	Page
2018.01.01	1.0	Initial release	