



# SGM48751

## 8:1 CMOS Analog Signal Multiplexer

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### GENERAL DESCRIPTION

The SGM48751 is a CMOS analog IC configured as an 8-channel multiplexer. This CMOS device can operate from 2.5V to 5.5V single supplies. Each switch can handle rail-to-rail analog signals. The off-leakage current is only 1nA (TYP) at +25°C.

All digital inputs can support 1.8V logic control I/O.

The SGM48751 is available in Green SOIC-16, SSOP-16, TSSOP-16 and TQFN-3x3-16L packages. It operates over an ambient temperature range of -40°C to +85°C.

### APPLICATIONS

Battery-Operated Equipment  
Audio and Video Signal Routing  
Low-Voltage Data-Acquisition Systems  
Communications Circuits  
Automotive

### FEATURES

- **Guaranteed On-Resistance**  
**48Ω (TYP) with +5V Supply**
- **Guaranteed On-Resistance Match Between Channels**
- **Low Off-Leakage Current 1nA (TYP) at +25°C**
- **Low On-Leakage Current 1nA (TYP) at +25°C**
- **Optimized Rise Time and Fall Time of A, B, C Control Pins to Reduce Clock Feedthrough Effect**
- **2.5V to 5.5V Single-Supply Operation**
- **1.8V Logic Compatible**
- **High Off-Isolation: -83dB ( $R_L = 50\Omega$ ,  $f = 1\text{MHz}$ )**
- **-40°C to +85°C Operating Temperature Range**
- **Available in Green SOIC-16, SSOP-16, TSSOP-16 and TQFN-3x3-16L Packages**

**PACKAGE/ORDERING INFORMATION**

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM48751	SOIC-16	-40°C to +85°C	SGM48751YS16G/TR	SGM48751YS16 XXXXX	Tape and Reel, 2500
	SSOP-16	-40°C to +85°C	SGM48751YQS16G/TR	SGM48751 YQS16 XXXXX	Tape and Reel, 3000
	TSSOP-16	-40°C to +85°C	SGM48751YTS16G/TR	SGM48751 YTS16 XXXXX	Tape and Reel, 4000
	TQFN-3x3-16L	-40°C to +85°C	SGM48751YTQ16G/TR	48751TQ XXXXX	Tape and Reel, 4000

NOTE: XXXXX = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

**ABSOLUTE MAXIMUM RATINGS**

V<sub>CC</sub> to GND ..... -0.3V to 6V  
 Voltage into Any Terminal <sup>(1)</sup> ..... -0.3V to (V<sub>CC</sub> + 0.3V)  
 Continuous Current into Any Terminal ..... ±20mA  
 Peak Current, X<sub>L</sub>  
 (Pulsed at 1ms, 10% duty cycle) ..... ±40mA  
 Junction Temperature ..... +150°C  
 Storage Temperature Range ..... -65°C to +150°C  
 Lead Temperature (Soldering, 10s) ..... +260°C  
 ESD Susceptibility  
 HBM ..... 4000V  
 MM ..... 300V

NOTE:

1. Voltages exceeding V<sub>CC</sub> or GND on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

**RECOMMENDED OPERATING CONDITIONS**

Supply Voltage Range ..... 2.5V to 5.5V  
 Operating Temperature Range ..... -40°C to +85°C

**OVERSTRESS CAUTION**

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

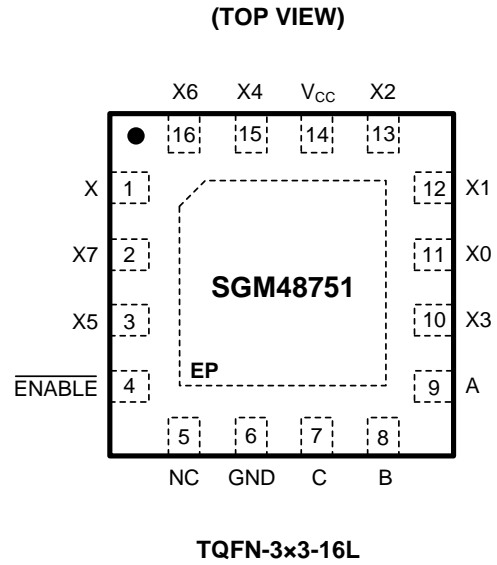
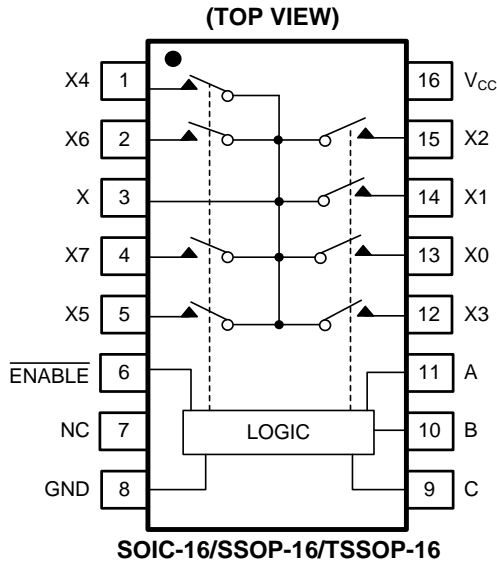
**ESD SENSITIVITY CAUTION**

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**DISCLAIMER**

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN		NAME	FUNCTION
SOIC-16/SSOP-16/TSSOP-16	TQFN-3x3-16L		
13, 14, 15, 12, 1, 5, 2, 4	11, 12, 13, 10, 15, 3, 16, 2	X0-X7	Analog Switch Inputs X0-X7.
3	1	X	Analog Switch "X" Output.
16	14	V <sub>CC</sub>	Positive Analog and Digital Supply Voltage Input.
11	9	A	Digital Address "A" Input.
10	8	B	Digital Address "B" Input.
9	7	C	Digital Address "C" Input.
8	6	GND	Ground. Connect to digital ground.
7	5	NC	No Connect.
6	4	ENABLE	Digital Enable Input. Normally connected to GND.
—	Exposed Pad	EP	Exposed Pad. Connect EP to GND.

FUNCTION TABLE

ENABLE INPUT	SELECT INPUTS			ON SWITCHES
	C	B	A	
H	X	X	X	All Switches Open
L	L	L	L	X-X0
L	L	L	H	X-X1
L	L	H	L	X-X2
L	L	H	H	X-X3
L	H	L	L	X-X4
L	H	L	H	X-X5
L	H	H	L	X-X6
L	H	H	H	X-X7

X = Don't care

NOTE: Input and output pins are identical and interchangeable. Either may be considered an input or output; signals pass equally well in either direction.

## ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = 5.0V, Full = -40°C to +85°C, typical values are at T<sub>A</sub> = +25°C, unless otherwise noted.)

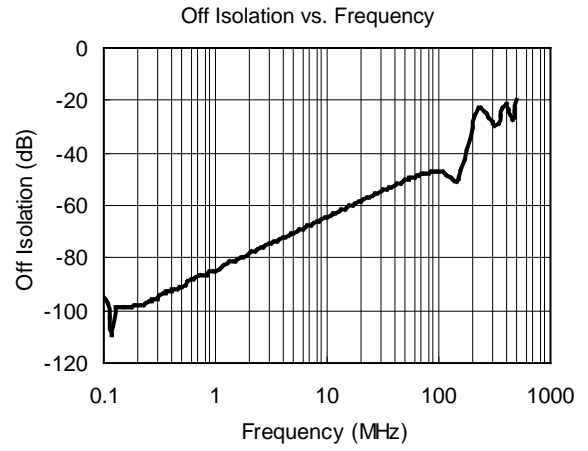
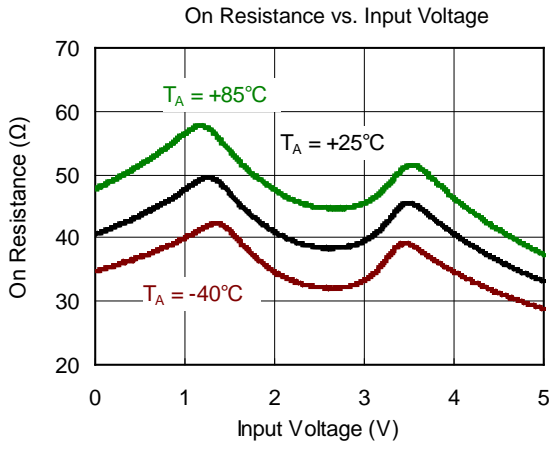
PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
<b>ANALOG SWITCH</b>							
Analog Signal Range	V <sub>X-</sub> , V <sub>X</sub>		Full	GND		V <sub>CC</sub>	V
On-Resistance	R <sub>ON</sub>	V <sub>CC</sub> = 5.0V, I <sub>X</sub> = 1mA	+25°C		48	58	Ω
			Full			67	
On-Resistance Match Between Channels	ΔR <sub>ON</sub>	V <sub>CC</sub> = 5.0V, I <sub>X</sub> = 1mA	+25°C		1.5	5	Ω
			Full			5.3	
On-Resistance Flatness	R <sub>FLAT(ON)</sub>	V <sub>CC</sub> = 5.0V, I <sub>X</sub> = 1mA	+25°C		17	25	Ω
			Full			28	
X <sub>-</sub> Off Leakage Current	I <sub>X-(OFF)</sub>	V <sub>CC</sub> = 5.0V, V <sub>X-</sub> = 4.5V or 0V, V <sub>X</sub> = 4.5V or 0V	+25°C		1	1000	nA
X Off Leakage Current	I <sub>X(OFF)</sub>	V <sub>CC</sub> = 5.0V, V <sub>X-</sub> = 4.5V or 0V, V <sub>X</sub> = 4.5V or 0V	+25°C		1	1000	nA
X On Leakage Current	I <sub>X(ON)</sub>	V <sub>CC</sub> = 5.0V, V <sub>X</sub> = 4.5V or 0V	+25°C		1	1000	nA
<b>DIGITAL I/O</b>							
Logic Input Logic Threshold High	V <sub>AH</sub> , V <sub>BH</sub> , V <sub>CH</sub> , V <sub>ENABLE</sub>		+25°C	1.7			V
Logic Input Logic Threshold Low	V <sub>AL</sub> , V <sub>BL</sub> , V <sub>CL</sub> , V <sub>ENABLE</sub>		+25°C			0.5	V
Input-Current High	I <sub>AH</sub> , I <sub>BH</sub> , I <sub>CH</sub> , I <sub>ENABLE</sub>	V <sub>A</sub> , V <sub>B</sub> , V <sub>C</sub> , V <sub>ENABLE</sub> = V <sub>CC</sub>	+25°C		1	1000	nA
Input-Current Low	I <sub>AL</sub> , I <sub>BL</sub> , I <sub>CL</sub> , I <sub>ENABLE</sub>	V <sub>A</sub> , V <sub>B</sub> , V <sub>C</sub> , V <sub>ENABLE</sub> = 0V	+25°C		1	1000	nA
<b>DYNAMIC CHARACTERISTICS</b>							
Address Transition Time	t <sub>TRANS</sub>	V <sub>X-</sub> = ±3V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Test Circuit 1	+25°C		85		ns
ENABLE Turn-On Time	t <sub>ON</sub>	V <sub>X-</sub> = 3V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Test Circuit 2	+25°C		60		ns
ENABLE Turn-Off Time	t <sub>OFF</sub>	V <sub>X-</sub> = 3V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Test Circuit 2	+25°C		70		ns
Internal A, B, C Rise Time	t <sub>R</sub>		+25°C		45		ns
Internal A, B, C Fall Time	t <sub>F</sub>		+25°C		50		ns
Break-Before-Make Time Delay	t <sub>D</sub>	V <sub>X-</sub> = 3V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Test Circuit 3	+25°C		50		ns
Charge Injection	Q	R <sub>S</sub> = 0Ω, C <sub>L</sub> = 1nF, Test Circuit 4	+25°C		6		pC
Off Isolation	O <sub>ISO</sub>	R <sub>L</sub> = 50Ω, f = 1MHz, Test Circuit 5	+25°C		-83		dB
Input Off-Capacitance	C <sub>X-(OFF)</sub>	V <sub>X-</sub> = 0V, f = 1MHz, Test Circuit 6	+25°C		4.7		pF
Output Off-Capacitance	C <sub>X(OFF)</sub>	V <sub>X-</sub> = 0V, f = 1MHz, Test Circuit 6	+25°C		12.7		pF
Output On-Capacitance	C <sub>X(ON)</sub>	V <sub>X-</sub> = 0V, f = 1MHz, Test Circuit 6	+25°C		16		pF
-3dB Bandwidth	BW	R <sub>L</sub> = 50Ω	+25°C		180		MHz
Total Harmonic Distortion	THD	R <sub>L</sub> = 600Ω, 5V <sub>P-P</sub> , f = 20Hz to 20kHz	+25°C		0.7		%
<b>POWER SUPPLY</b>							
Power Supply Range	V <sub>CC</sub>		Full	2.5		5.5	V
Power Supply Current	I <sub>CC</sub>	V <sub>CC</sub> = 5.0V, V <sub>A</sub> , V <sub>B</sub> , V <sub>C</sub> , V <sub>ENABLE</sub> = V <sub>CC</sub> or 0	+25°C		0.001	6	μA

**ELECTRICAL CHARACTERISTICS (continued)**(V<sub>CC</sub> = 3.3V, Full = -40°C to +85°C, typical values are at T<sub>A</sub> = +25°C, unless otherwise noted.)

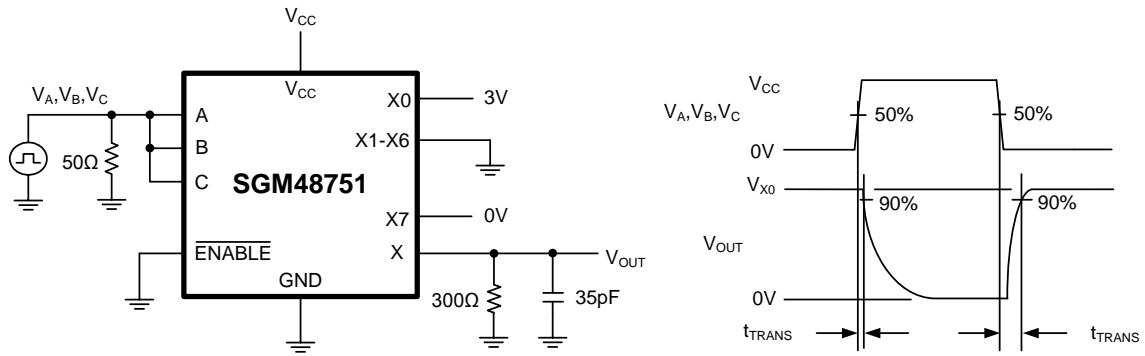
PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
<b>ANALOG SWITCH</b>							
Analog Signal Range	V <sub>X-</sub> , V <sub>X</sub>		Full	GND		V <sub>CC</sub>	V
On-Resistance	R <sub>ON</sub>	I <sub>X</sub> = 1mA	+25°C		80	110	Ω
			Full			116	
X <sub>-</sub> Off Leakage Current	I <sub>X(OFF)</sub>	V <sub>X-</sub> = 1V, 3V, V <sub>X</sub> = 3V, 1V	+25°C		1	1000	nA
X Off Leakage Current	I <sub>X(OFF)</sub>	V <sub>X-</sub> = 1V, 3V, V <sub>X</sub> = 3V, 1V	+25°C		1	1000	nA
X On Leakage Current	I <sub>X(ON)</sub>	V <sub>X</sub> = 3V, 1V	+25°C		1	1000	nA
<b>DIGITAL I/O</b>							
Logic Input Logic Threshold High	V <sub>AH</sub> , V <sub>BH</sub> , V <sub>CH</sub> , V <sub>ENABLE</sub>		+25°C	1.7			V
Logic Input Logic Threshold Low	V <sub>AL</sub> , V <sub>BL</sub> , V <sub>CL</sub> , V <sub>ENABLE</sub>		+25°C			0.5	V
Input-Current High	I <sub>AH</sub> , I <sub>BH</sub> , I <sub>CH</sub> , I <sub>ENABLE</sub>	V <sub>A</sub> , V <sub>B</sub> , V <sub>C</sub> , V <sub>ENABLE</sub> = V <sub>CC</sub>	+25°C		1	1000	nA
Input-Current Low	I <sub>AL</sub> , I <sub>BL</sub> , I <sub>CL</sub> , I <sub>ENABLE</sub>	V <sub>A</sub> , V <sub>B</sub> , V <sub>C</sub> , V <sub>ENABLE</sub> = 0V	+25°C		1	1000	nA
<b>DYNAMIC CHARACTERISTICS</b>							
Address Transition Time	t <sub>TRANS</sub>	V <sub>X-</sub> = 3V/0V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Test Circuit 1	+25°C		150		ns
ENABLE Turn-On Time	t <sub>ON</sub>	V <sub>X-</sub> = 3V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Test Circuit 2	+25°C		110		ns
ENABLE Turn-Off Time	t <sub>OFF</sub>	V <sub>X-</sub> = 3V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Test Circuit 2	+25°C		100		ns
Internal A, B, C Rise Time	t <sub>R</sub>		+25°C		80		ns
Internal A, B, C Fall Time	t <sub>F</sub>		+25°C		85		ns
Break-Before-Make Time Delay	t <sub>D</sub>	V <sub>X-</sub> = 3V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Test Circuit 3	+25°C		80		ns
-3dB Bandwidth	BW	R <sub>L</sub> = 50Ω	+25°C		180		MHz
Charge Injection	Q	R <sub>S</sub> = 0Ω, C = 1nF, V <sub>S</sub> = 2.5V, Test Circuit 4	+25°C		4		pC
<b>POWER SUPPLY</b>							
Power Supply Current	I <sub>CC</sub>	V <sub>A</sub> , V <sub>B</sub> , V <sub>C</sub> , V <sub>ENABLE</sub> = V <sub>CC</sub> or 0	+25°C		0.001	3	μA

TYPICAL PERFORMANCE CHARACTERISTICS

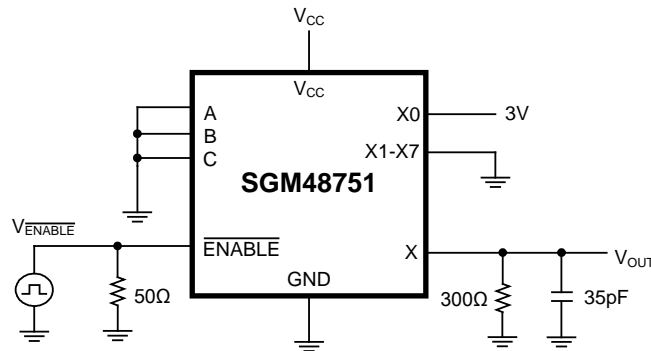
V<sub>CC</sub> = 5.0V, unless otherwise noted.



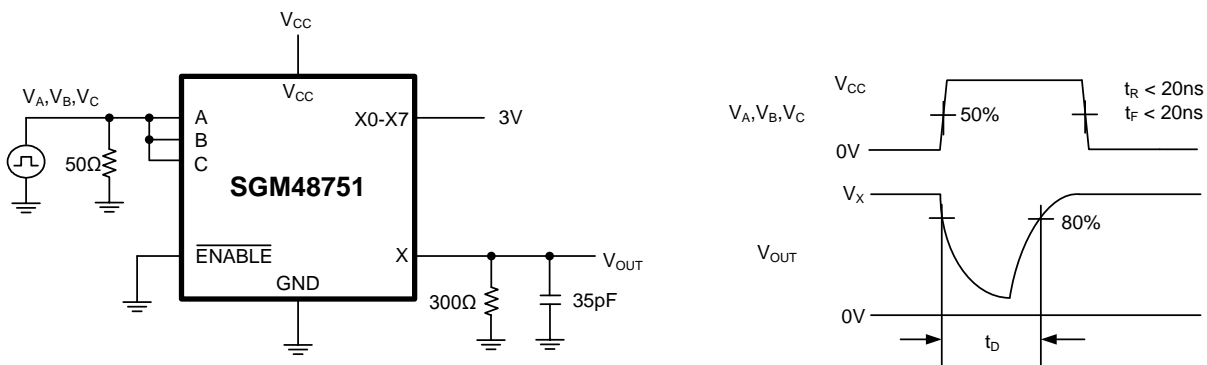
TEST CIRCUITS



Test Circuit 1. Address Transition Times ( $t_{TRANS}$ )

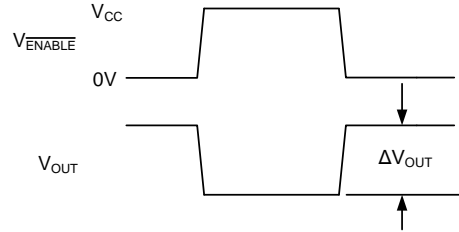
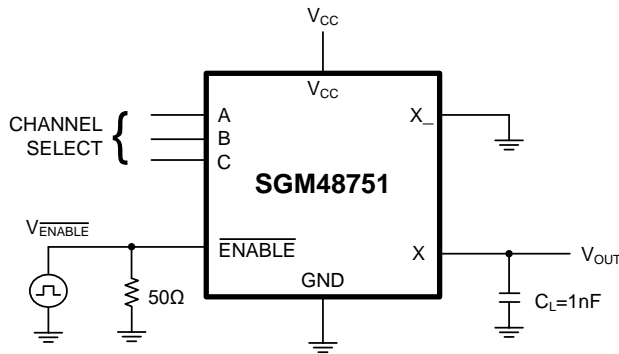


Test Circuit 2. Switching Times ( $t_{ON}$ ,  $t_{OFF}$ )



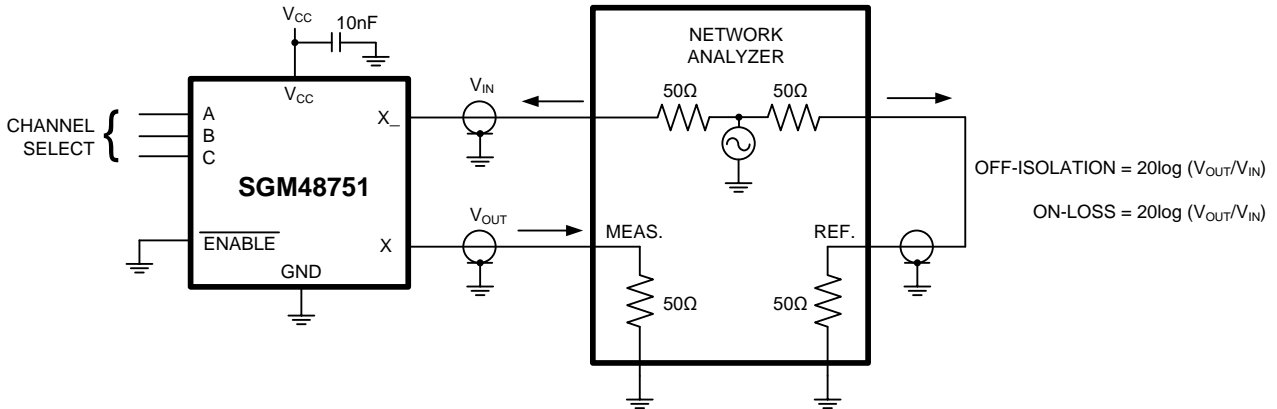
Test Circuit 3. Break-Before-Make Time Delay ( $t_D$ )

TEST CIRCUITS (continued)



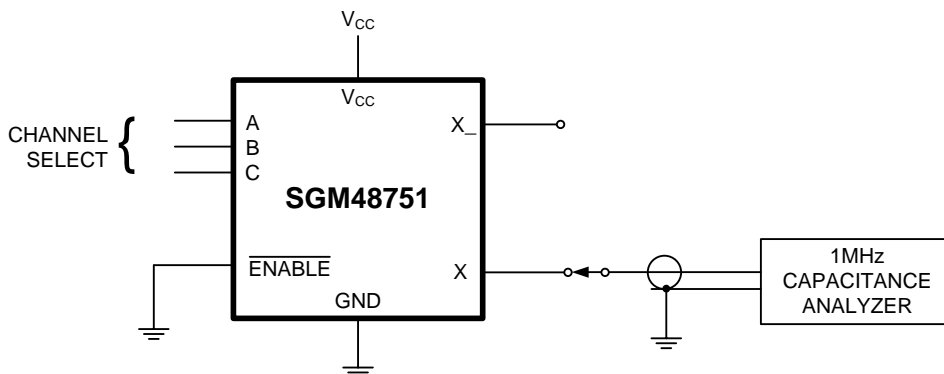
$\Delta V_{OUT}$  IS THE MEASURED VOLTAGE DUE TO CHARGE TRANSFER ERROR Q WHEN THE CHANNEL TURNS OFF.  
 $Q = \Delta V_{OUT} \times C_L$

Test Circuit 4. Charge Injection (Q)



MEASUREMENTS ARE STANDARDIZED AGAINST SHORT AT SOCKET TERMINALS.  
 OFF-ISOLATION IS MEASURED BETWEEN COM AND "OFF" NO TERMINAL ON EACH SWITCH.  
 ON-LOSS IS MEASURED BETWEEN COM AND "ON" NO TERMINAL ON EACH SWITCH.  
 SIGNAL DIRECTION THROUGH SWITCH IS REVERSED; WORST VALUES ARE RECORDED.

Test Circuit 5. Off Isolation, On Loss



Test Circuit 6. Capacitance



## APPLICATION INFORMATION

### Power-Supply Considerations

#### Overview

The SGM48751 construction is typical of most CMOS analog switch. It supports single power supply.  $V_{CC}$  and GND are used to drive the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD protection diodes are internally connected between each analog-signal pin and both  $V_{CC}$  and GND. If any analog signal exceeds  $V_{CC}$  or GND, one of these diodes will conduct. During normal operation, these and other reverse-biased ESD diodes leak, forming the only current drawn from  $V_{CC}$  or GND.

Virtually all the analog leakage current comes from the ESD diodes. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either  $V_{CC}$  or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the  $V_{CC}$  and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of either the same or opposite polarity.

#### Over-Voltage Protection

Proper power-supply sequencing is recommended for the CMOS device. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence  $V_{CC}$  on first, followed by the logic inputs and analog signals. If power-supply sequencing is not possible, add one 100 $\Omega$  resistor in series with the supply  $V_{CC}$  pin for over-voltage protection (Figure 1).

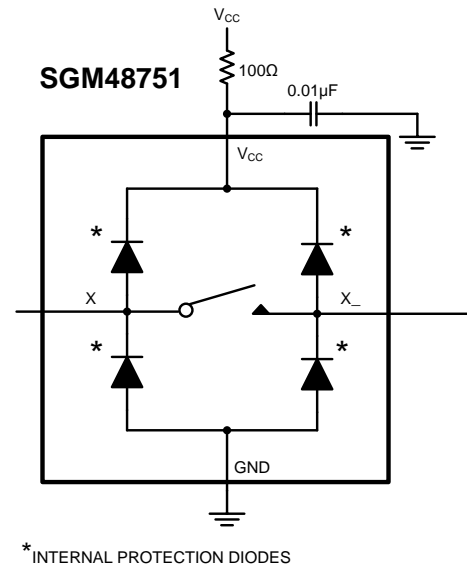
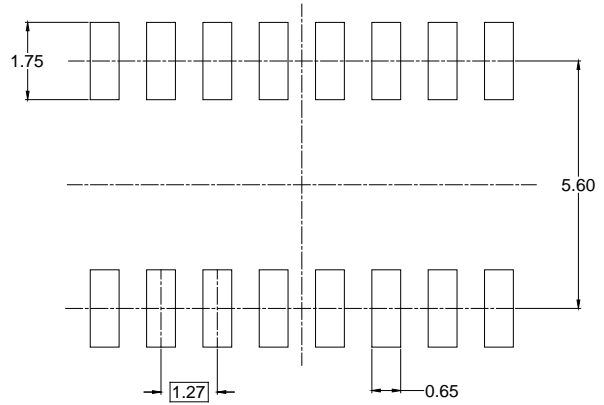
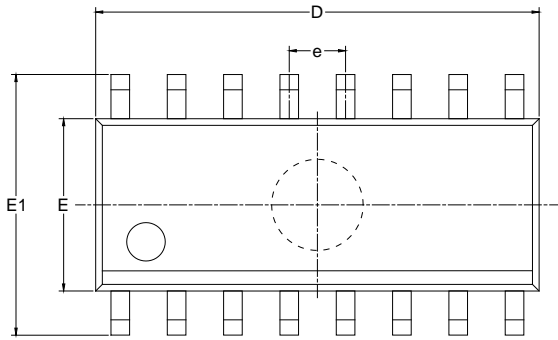


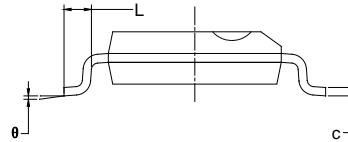
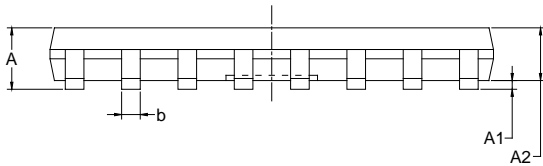
Figure 1. Over-Voltage Protection Using External Resistor

PACKAGE OUTLINE DIMENSIONS

SOIC-16



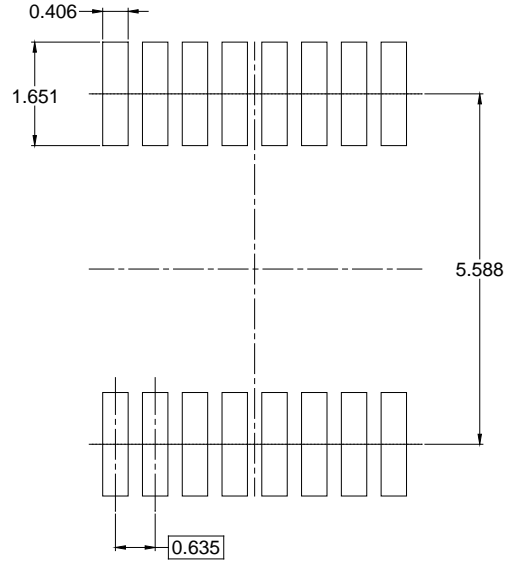
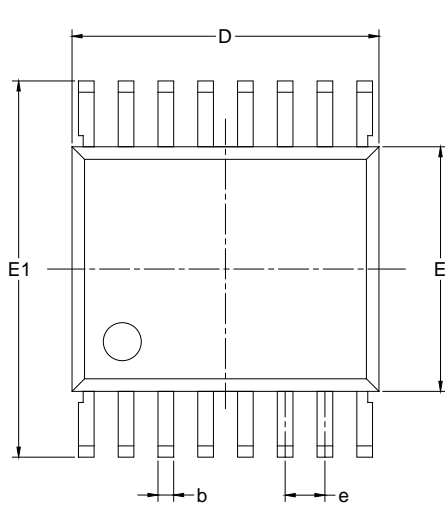
RECOMMENDED LAND PATTERN (Unit: mm)



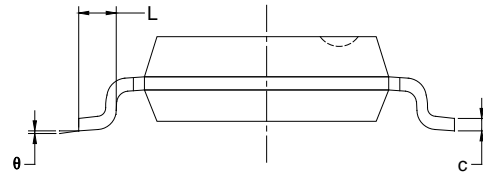
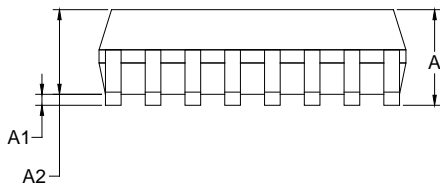
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

PACKAGE OUTLINE DIMENSIONS

SSOP-16



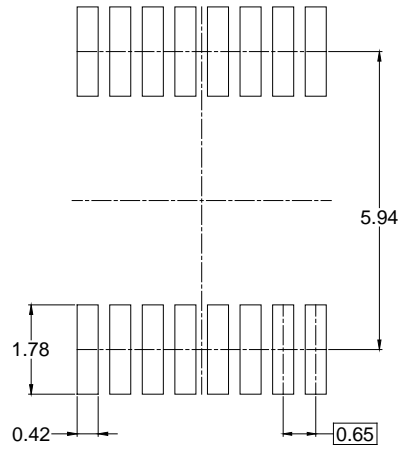
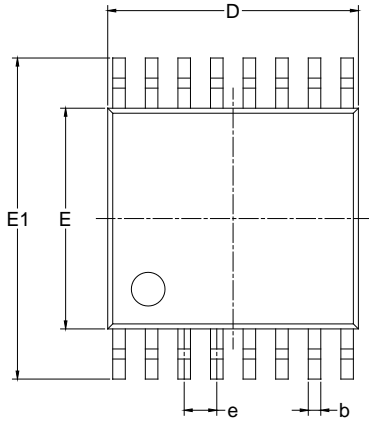
RECOMMENDED LAND PATTERN (Unit: mm)



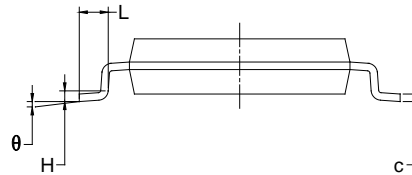
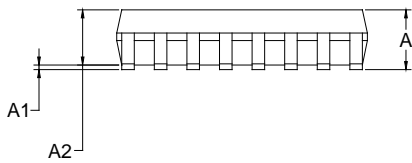
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.200	0.300	0.008	0.012
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	0.635 BSC		0.025 BSC	
L	0.400	1.270	0.016	0.050
$\theta$	0°	8°	0°	8°

PACKAGE OUTLINE DIMENSIONS

TSSOP-16



RECOMMENDED LAND PATTERN (Unit: mm)

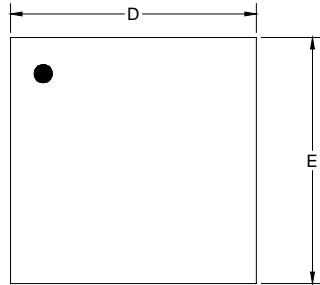


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.860	5.100	0.191	0.201
E	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.244	0.260
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°

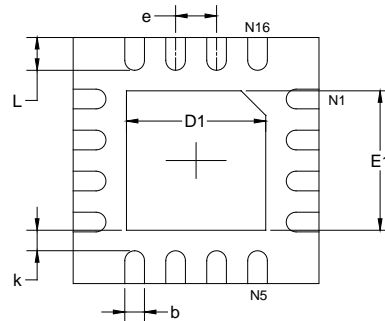
# PACKAGE INFORMATION

## PACKAGE OUTLINE DIMENSIONS

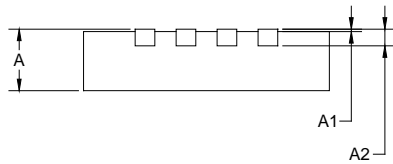
### TQFN-3x3-16L



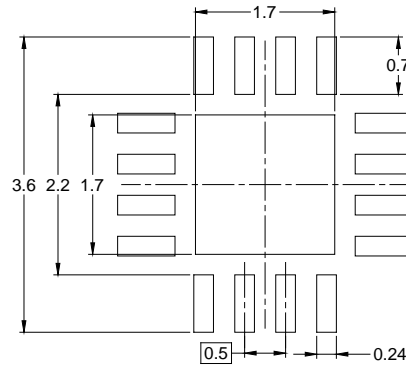
TOP VIEW



BOTTOM VIEW



SIDE VIEW



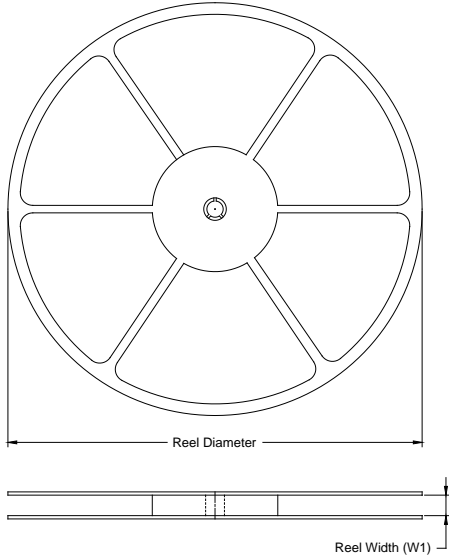
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E	2.900	3.100	0.114	0.122
E1	1.600	1.800	0.063	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

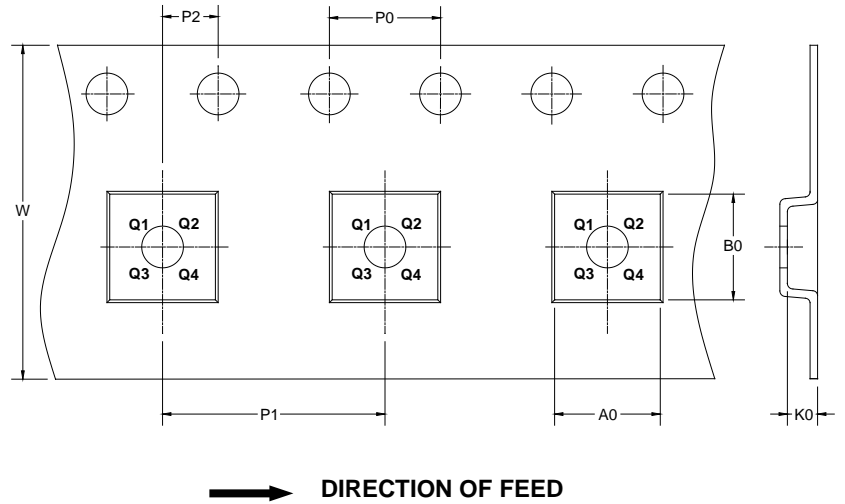
# PACKAGE INFORMATION

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS



### TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

### KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-16	13"	16.4	6.50	10.30	2.10	4.0	8.0	2.0	16.0	Q1
SSOP-16	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
TSSOP-16	13"	12.4	6.90	5.60	1.20	4.0	8.0	2.0	12.0	Q1
TQFN-3x3-16L	13"	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1

D00001

## CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DD0002