

**DESCRIPTION**

The AA88347L is a CMOS processed digital to analog converter (DAC) with 8-bit resolution, low leakage and operating current. The AA88347L has 8 channels with built in operational amplifier output buffers which could operate in the full-swing voltage range from VCC to GND and enhance the Drive/Sink ability up to max. 1mA. Digital data (DI) input serially in a max. 2.5 MHz clock (CLK) rate. The latched 12-bit digital data is converted into an analog DC voltage in the range from VSS to VDD with 8-bit resolution in one of the 8 channels by the D/A converter in a max. 200 μ s settling time. AA88347L is a single 3V power DAC. Analog DC output could be full voltage swing as the analog power is equal to the system power. In addition to normal D/A converter applications, AA88347L is also available for electronic volume and instead of potentiometers for adjustment due to its high stability on the capacitive load. 16 pins TSSOP package type are available for AA88347L. Its operational temperature range is specified over -20°C to 85°C .

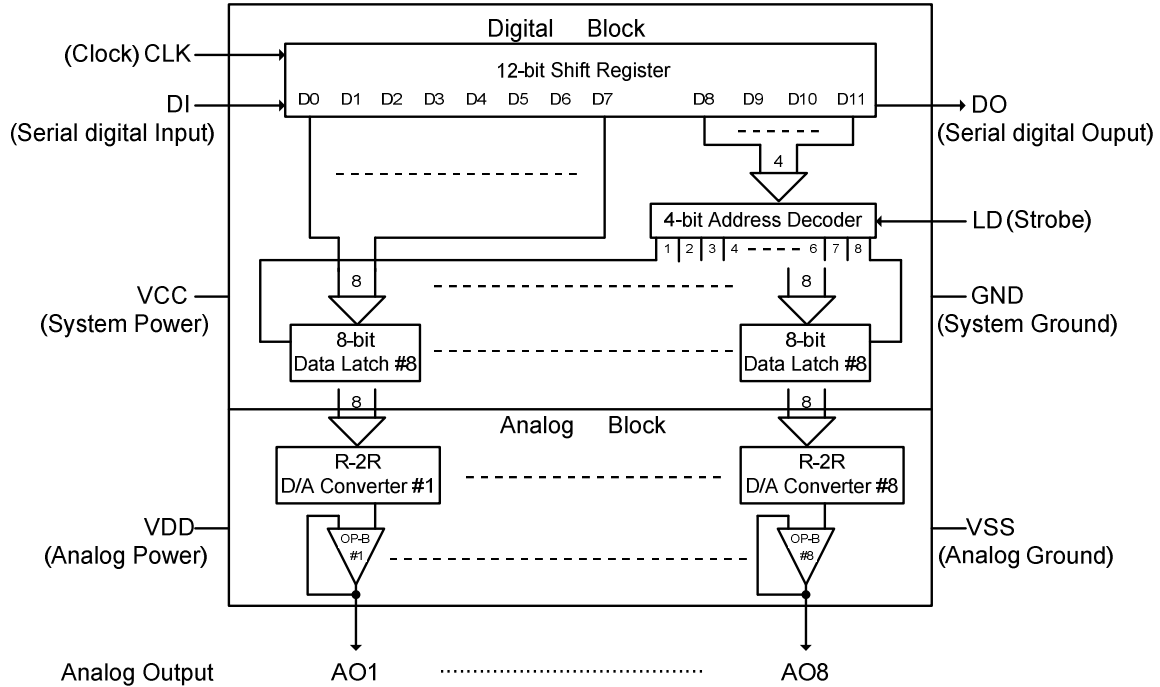
FEATURES

- 12 bits serial data input (3 wire serial data transfer method, DI, CLK, LD)
- R-2R resistor ladder used for D/A conversion
- 8 channels with 8-bit resolution monotonic D/A converter
- 8 channels buffer operational amplifiers operating in the full voltage range from VCC to GND only if VDD=VCC and VSS=GND
- Max. 2.5 MHz serial digital data input
- Serial I/O for cascade application
- Max. 1.0 mA output drive/sink current
- Two separate power supply/ground lines for system and analog power supply
- Single +3 V system power supply

APPLICATION

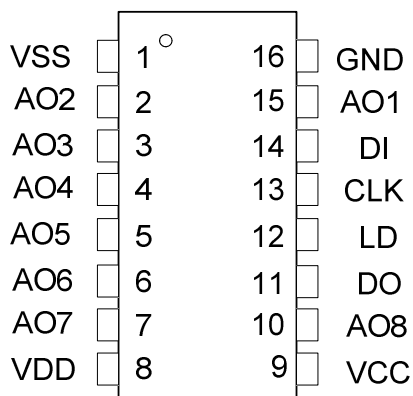
DVD, CD-R, CD-RW, DVC, digital camera, and other industrial equipments

■ BLOCK DIAGRAM



- * VCC and GND are for digital block and operational amplifier buffer block
- * VDD, VSS are only for Analog block except operational amplifier buffer block
- * $VSS + 2V \leq VDD \leq VCC$
- * $GND \leq VSS \leq VDD - 2V$

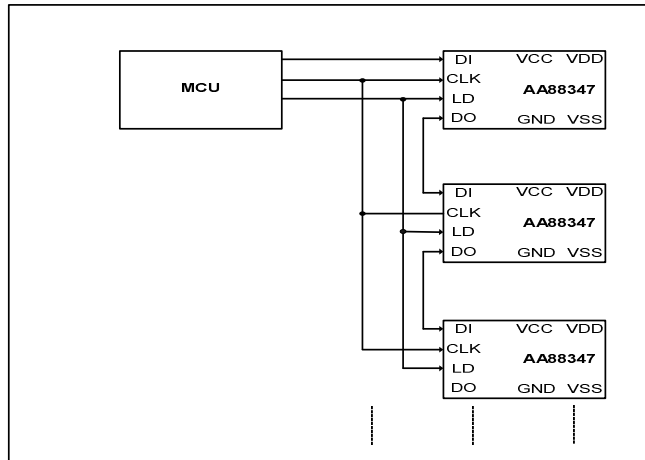
■ PIN DESCRIPTIONS



TOP VIEW

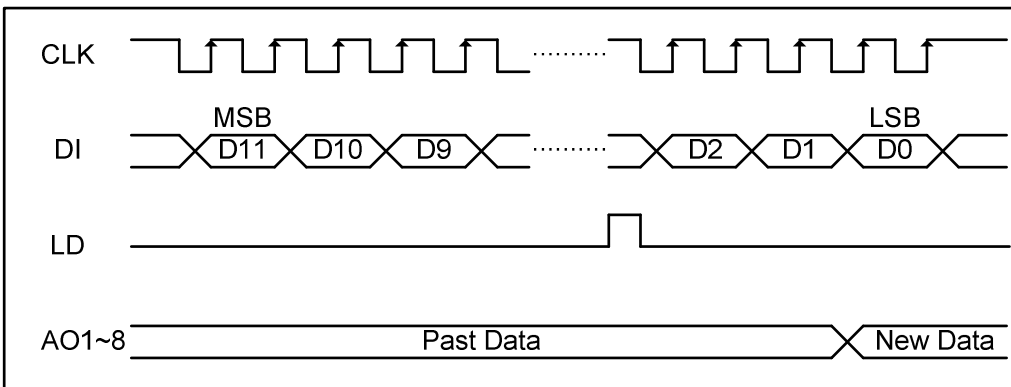
| PIN NO. | PIN NAME | PIN FUNCTION |
|-------------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9 | VCC | +3V system power supply pin |
| 16 | GND | System ground pin |
| 8 | VDD | Analog power supply pin |
| 1 | VSS | Analog ground pin |
| 13 | CLK | Serial clock input pin. At its rising edge, DI data shift into the Shift-Register. |
| 12 | LD | Data Strobe pin. When it's on high, upper 4-bit and lower 8-bit of the 12-bit in the Shift-Register be latched into the Address Decoder and the Data-Latch, respectively |
| Data Input/Output | | |
| 14 | D1 | Serial Digital Data input pin |
| 11 | DO | Serial Digital Data output pin. Output from the 12th data in the Shift-Register |
| DAC Output | | |
| 15 | AO1 | 8-bit D/A converter outputs Output range is from VSS to VDD |
| 2 | AO2 | |
| 3 | AO3 | |
| 4 | AO4 | |
| 5 | AO5 | |
| 6 | AO6 | |
| 7 | AO7 | |
| 10 | AO8 | |

■ CASCADE CONNECTION

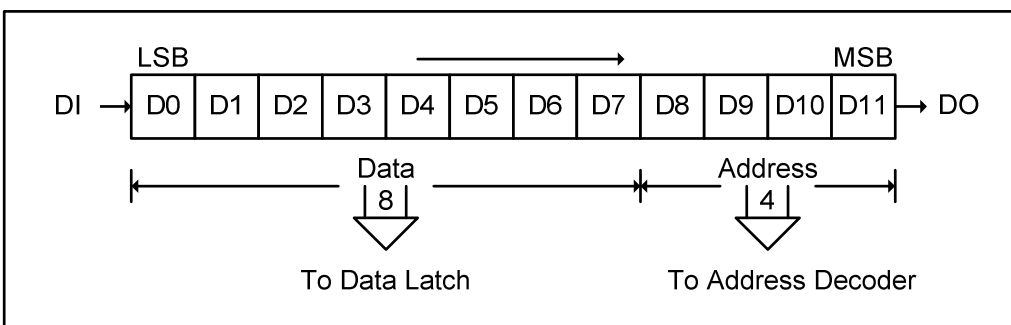


- VDD and VSS of each AA88347L could be different depend on the application consideration

■ DATA INPUT FORMAT



■ DATA FORMAT IN SHIFT REGISTER



■ DATA CONVERSION



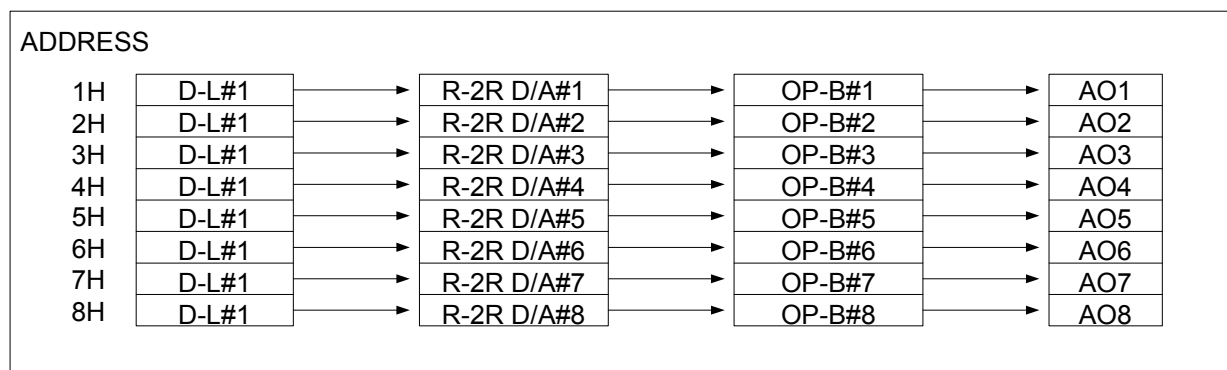
PRELIMINARY

8-BIT DAC

| Data | | | | | | | | DAC Output Level |
|------|----|----|----|----|----|----|----|------------------|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | AOX |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VSS |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | VSS + LSB* |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | VSS + 2 * LSB |
| { | { | { | { | { | { | { | { | { |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | VDD - LSB |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | VDD |

* LSB = (VDD-VSS)/255

■ CHANNEL MAP



■ ADDRESS DECODING

| ADDRESS | | | | DATA LATCH SELECTED |
|---------|----|-----|-----|---------------------|
| D8 | D9 | D10 | D11 | |
| 0 | 0 | 0 | 0 | NA |
| 0 | 0 | 0 | 1 | Data Latch #1 |
| 0 | 0 | 1 | 0 | Data Latch #2 |
| 0 | 0 | 1 | 1 | Data Latch #3 |
| 0 | 1 | 0 | 0 | Data Latch #4 |
| 0 | 1 | 0 | 1 | Data Latch #5 |
| 0 | 1 | 1 | 0 | Data Latch #6 |
| 0 | 1 | 1 | 1 | Data Latch #7 |
| 1 | 0 | 0 | 0 | Data Latch #8 |



PRELIMINARY

8-BIT DAC

| | | | | |
|---|---|---|---|----|
| 1 | 0 | 0 | 1 | NA |
| 1 | 0 | 1 | 0 | NA |
| 1 | 0 | 1 | 1 | NA |
| 1 | 1 | 0 | 0 | NA |
| 1 | 1 | 0 | 1 | NA |
| 1 | 1 | 1 | 0 | NA |
| 1 | 1 | 1 | 1 | NA |

■ **ABSOLUTE MAXIMUM RATINGS**

TA=25°C, unless otherwise noted

| PARAMETER | SYMBOL | RATING | | | UNIT |
|-------------------------------|--------|--------|-----|-----------|------|
| | | MIN | TYP | MAX | |
| System Voltage | VCC | -0.3 | — | +7.0 | V |
| Analog Voltage | VDD | -0.3 | — | +7.0 | V |
| Input Voltage | VIN | -0.3 | — | VCC + 0.3 | V |
| Output Voltage | VOOUT | -0.3 | — | VCC + 0.3 | V |
| Power Dissipation | PD | — | — | 250 | mW |
| Operating Ambient Temperature | TA | -20 | — | +85 | °C |
| Storage Temperature | TS | -55 | — | +150 | °C |

NOTE: Stress above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for the extended periods of time may affect device reliability.

■ **ELECTRICAL CHARACTERISTICS**

◆ **RECOMMENDED OPERATING CONDITIONS**

| SYMBOL | PARAMETER | CONDITIONS | LIMITS | | | UNIT |
|--------|-----------|------------|--------|-----|-----|------|
| | | | MIN | TYP | MAX | |



PRELIMINARY

8-BIT DAC

| | | | | | | | |
|-----|------------------------------------------------------|------------------------------------------------------------|-----------------------|------|-----------|------|-------------|
| VCC | System Voltage | $VCC \geq VDD,$ $VDD - VSS \geq 2.0V$ $VSS \geq GND$ | 2.7 | 3.0 | 3.6 | V | |
| GND | | | — | 0 | — | V | |
| VDD | Analog Voltage | | 2.0 | — | VCC | V | |
| VSS | | | GND | — | VCC - 2.0 | V | |
| IAO | Analog Output Current | | VAO shift $\leq 0.3V$ | -1.0 | — | +1.0 | mA |
| COL | Analog Output Load Capacitance for Oscillation limit | | | — | — | +1.0 | μF |
| TA | Operating Ambient Temperature | | | -20 | — | +85 | $^{\circ}C$ |

◆ DC CHARACTERISTICS

Digital Block

TA = 25 $^{\circ}C$

| PARAMETER | SYMBOL | VALUE | | | UNIT | CONDITIONS |
|----------------------------|--------|-----------|-----|---------|---------|-----------------------|
| | | MIN | TYP | MAX | | |
| System Voltage | VCC | 2.7 | 3.0 | 3.6 | V | |
| System Current | ICC | — | 1.0 | 3.0 | mA | CLK = 1 MHz, No load; |
| Input Leakage Current | IILK | -5 | — | +5 | μA | VIN = 0V / 3V |
| Digital Input Low Voltage | VIL | — | — | 0.2-VCC | V | |
| Digital Input High Voltage | VIH | 0.8-VCC | — | — | V | |
| Digital Output Low | VOL | — | — | 0.4 | V | IOL = +2.5 mA |
| Digital Output High | VOH | VCC - 0.4 | — | — | V | IOH = -400 μA |

Analog Block

TA = 25 $^{\circ}C$

| PARAMETER | SYMBOL | VALUE | | | UNIT | CONDITIONS |
|----------------------------------------|--------|-----------|-----|-----------|------|---------------------|
| | | MIN | TYP | MAX | | |
| Analog Current | IDD | — | 0.5 | 0.8 | mA | No load |
| Analog Voltage | VDD | 2.0 | — | VCC | V | VDD - VSS \geq 2V |
| | VSS | GND | — | VCC - 2.0 | V | |
| Analog Output Drive Range (VCC=VDD=3V, | VAOH | VDD - 0.1 | VDD | VDD + 0.1 | V | IAOH = 0 μA |
| | VAOH | VDD - 0.2 | VDD | VDD + 0.2 | V | IAOH = -500 μ |



PRELIMINARY

8-BIT DAC

| | | | | | | |
|----------------------------------------------------------------------|------|-----------|-----|-----------|-----|-------------------------------------------------|
| VSS=GND=0V, Data=#FF) | VAOH | VDD - 0.3 | VDD | VDD + 0.3 | V | IAOH = -1mA |
| Analog Output Sink Range (VCC=VDD=5V, VSS=GND=0V, Data=#00) | VAOL | VSS - 0.1 | VSS | VSS + 0.1 | V | IAOL = 0 μA |
| | VAOL | VSS - 0.2 | VSS | VSS + 0.2 | V | IAOL = 500 μA |
| | VAOL | VSS - 0.3 | VSS | VSS + 0.3 | V | IAOL = 1mA |
| Resolution (AOx) | RES | — | 8 | — | bit | VCC = 3.6V, GND=0V |
| Integral Non-Linearity | INL | -3.0 | — | +3.0 | LSB | VDD=3.36V, VSS=0.3 LSB = 12mv, no load |
| Differential Non-Linearity | DNL | -1.0 | 0 | +2.0 | LSB | |

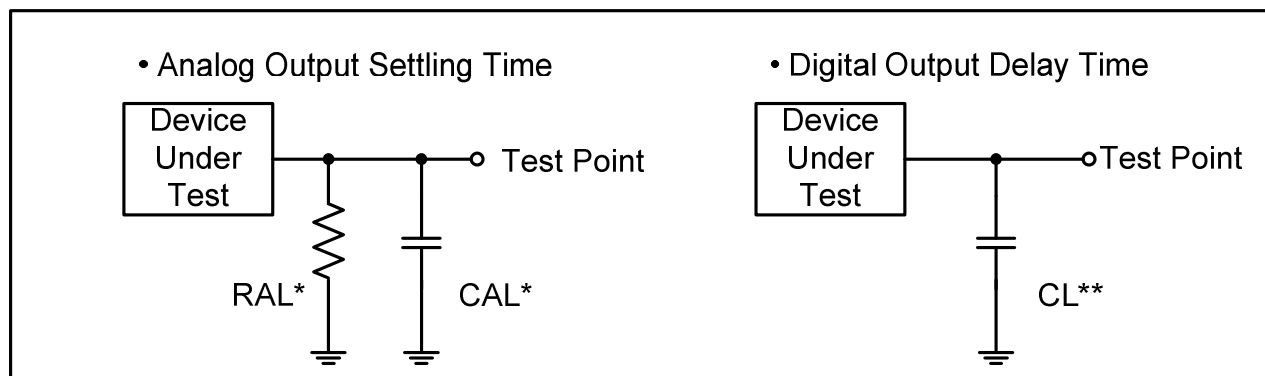
NOTES: Integral Non-Linearity: The difference between the digital data converted DC analog values and a reference straight line drawn through the first and the last output values
 Differential Non-Linearity: The difference between the ideal and real increment value of DC analog voltage when the digital data increase 1 bit.

◆ **AC CHARACTERISTICS**

TA = 25°C

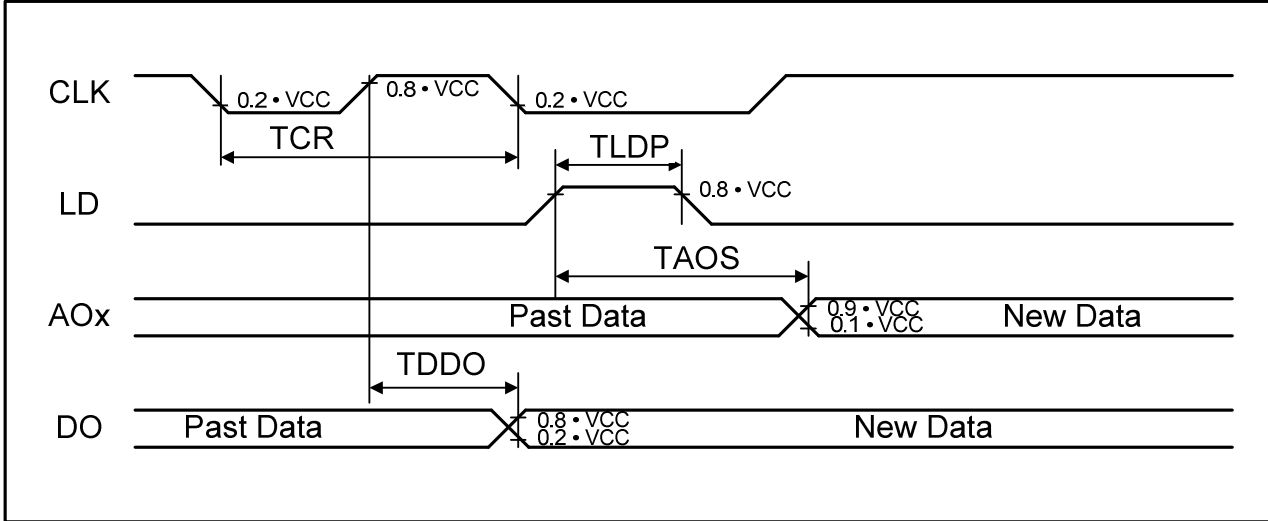
| PARAMETER | SYMBOL | VALUE | | | UNIT | CONDITIONS |
|-----------------------------|--------|-------|------|-----|------|---------------------------------------|
| | | MIN | TYP | MAX | | |
| Clock Rate | TCR | 400 | 1000 | — | ns | |
| Load Strobe Pulse Width | TLDP | — | 200 | — | ns | |
| Analog Output Settling Time | TAOS | — | — | 200 | μs | *RAL = 10 kΩ, CAL = 50pF (#00--> #FF) |
| Digital Output Delay | TDDO | — | — | 170 | ns | **CL = 100 pF (Max.) |

AC TEST CONDITION





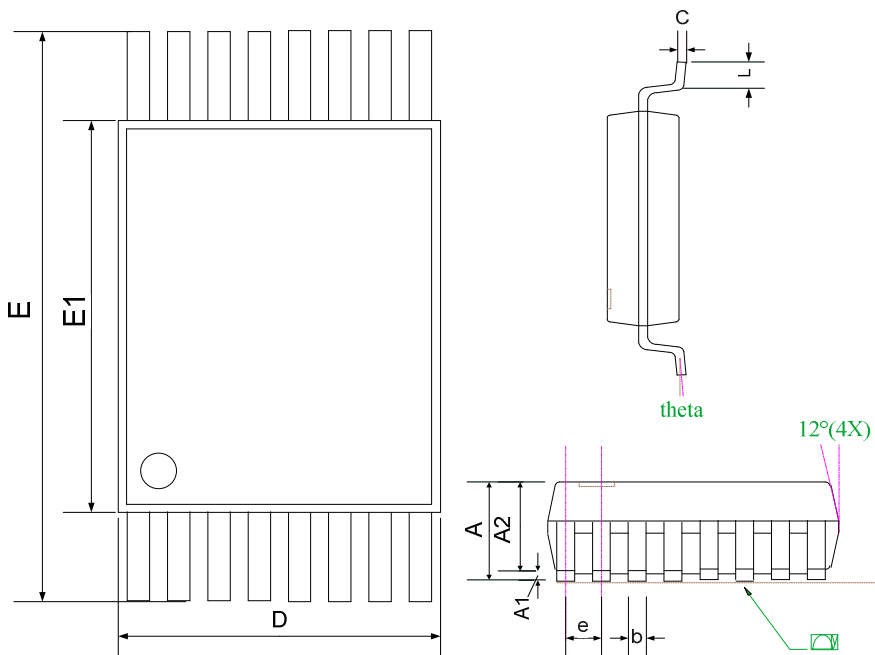
TIMING CHART



■ ORDERING INFORMATION

| ORDER NO. | PACKAGE | PACKING | ONE REEL Q'TY | MARK CHART |
|-----------|----------|-------------|---------------|---------------------------------------------------------------------------------------------------------------------------------------|
| AA88347L | TSSOP16L | Tape & Reel | 2,500ea | <div style="border: 1px solid black; padding: 5px; width: fit-content;"> AA88347 XXXX L </div> |

■ PACKAGE DIMENSIONS



| SYMBOLS | DIMENSIONS IN MILLIMETERS | | | DIMENSIONS IN INCHES | | |
|---------|---------------------------|------|------|----------------------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | --- | --- | 1.20 | --- | --- | 0.048 |
| A1 | 0.05 | --- | 0.15 | 0.002 | --- | 0.006 |
| A2 | 0.80 | 1.00 | 1.05 | 0.031 | 0.039 | 0.041 |
| b | 0.19 | --- | 0.30 | 0.007 | --- | 0.012 |
| C | 0.09 | --- | 0.20 | 0.004 | --- | 0.008 |
| D | 4.90 | 5.00 | 5.10 | 0.193 | 0.197 | 0.201 |
| E | 6.20 | 6.40 | 6.60 | 0.244 | 0.252 | 0.260 |
| E1 | 4.30 | 4.40 | 4.50 | 0.169 | 0.173 | 0.177 |
| e | --- | 0.65 | --- | --- | 0.026 | --- |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| y | --- | --- | 0.10 | --- | --- | 0.004 |
| theta | 0° | --- | 8° | 0° | --- | 8° |

NOTE

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS
2. TOLERANCE +/- 0.1 mm UNLESS OTHERWISE SPECIFIED
3. COPLANARITY : 0.1 mm
4. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
5. FOLLOWED FROM JEDEC MO-153