TEXAS INSTRUMENTS

TPS3705-30, TPS3705-33, TPS3705-50, TPS3707-30, TPS3707-50

SLVS184E – NOVEMBER 1998 – REVISED JULY 2017

TPS370x-xx Processor Supervisory Circuits With Power-Fail

1 Features

- Power-On Reset Generator With Fixed Delay Time of 200 ms (No External Capacitor Needed)
- Precision Supply Voltage Monitor: 2.5 V, 3 V, 3.3 V, and 5 V
- Pin-for-Pin Compatible With the MAX705 Through MAX708 Series
- Integrated Watchdog Time (TPS3705-xx Only)
- Voltage Monitor for Power-Fail or Low-Battery Warning
- Maximum Supply Current of 50 µA
- 8-Pin MSOP and 8-Pin SOIC Packages
- Temperature Range: –40°C to 85°C

2 Applications

- Designs Using DSPs, Microcontrollers, or Microprocessors
- Industrial Equipment
- Programmable Controls
- Automotive Systems
- Portable or Battery Powered Equipment
- Intelligent Instruments
- Wireless Communication Systems
- Notebook or Desktop Computers

3 Description

The TPS370x-xx family of microprocessor supply-voltage supervisors provide circuit initialization and timing supervision, primarily for DSP and processor-based systems.

During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage V_{DD} becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors V_{DD} and keeps $\overline{\text{RESET}}$ active as long as V_{DD} remains below the threshold voltage V_{IT+}. When the supply voltage drops below the threshold voltage V_{IT-}, the output becomes active (low) again. No external components are required. All the devices of this family have a fixed-sense threshold voltage V_{IT-} set by an internal voltage divider.

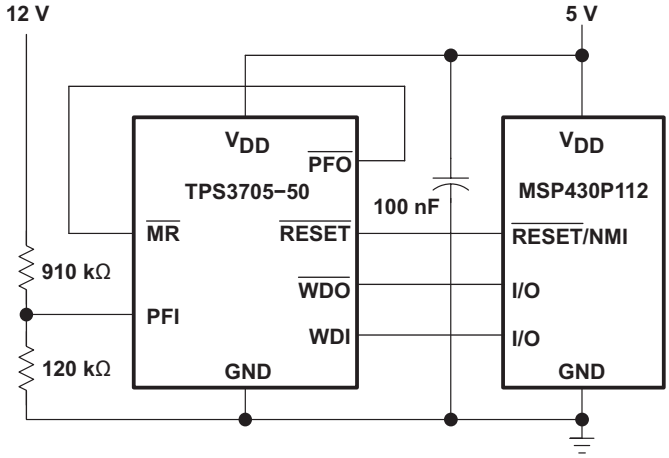
The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in either 8-pin MSOP or standard SOIC packages. The TPS370x-xx devices are characterized for operation over a temperature range of −40°C to 85°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS3705-xx, TPS3707-xx	MSOP-PowerPAD™ (8)	3.00 mm × 3.00 mm
	SOIC (8)	3.90 mm × 4.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical MSP430 Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (May 2016) to Revision E — **Page**

- Updated package body sizes in the *Device Information* table ... 1
- Added *Receiving Notification of Documentation Updates* section ... 15

Changes from Revision C (December 2005) to Revision D — **Page**

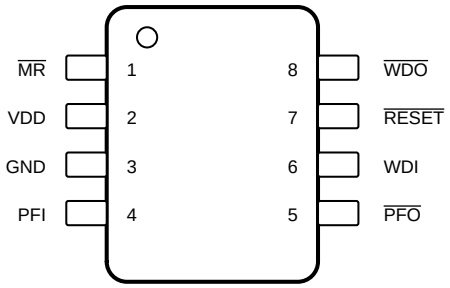
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Device Comparison Table

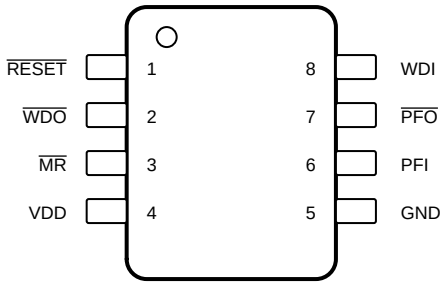
T_A	THRESHOLD VOLTAGE	PACKAGED DEVICES		MARKING DGN PACKAGE	CHIP FORM (Y)
		SMALL OUTLINE (D)	POWER-PAD µ-SMALL OUTLINE (DGN)		
–40°C to 85°C	2.63 V	TPS3705−30D	TPS3705−30DGN	TIAAT	TPS3705-30Y
	2.93 V	TPS3705−33D	TPS3705−33DGN	TIAAU	TPS3705−33Y
	4.55 V	TPS3705−50D	TPS3705−50DGN	TIAAV	TPS3705−50Y
	2.25 V	TPS3707−25D	TPS3707−25DGN	TIAAW	TPS3707−25Y
	2.63 V	TPS3707−30D	TPS3707−30DGN	TIAAX	TPS3707−30Y
	2.93 V	TPS3707−33D	TPS3707−33DGN	TIAAY	TPS3707−33Y
	4.55 V	TPS3707−50D	TPS3707−50DGN	TIAAZ	TPS3707−50Y

6 Pin Configuration and Functions

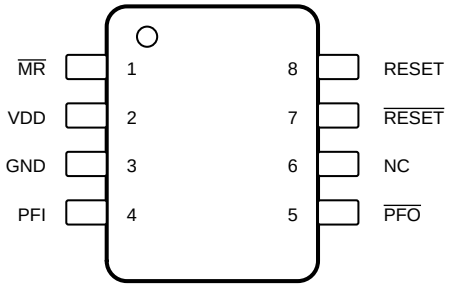
TPS3705-xx D Package
8-Pin SOIC
Top View



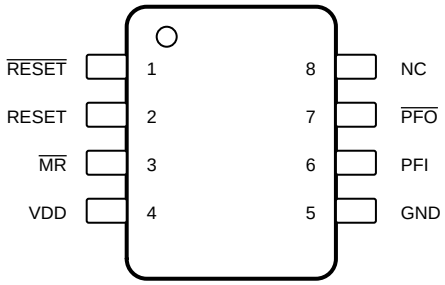
TPS3705-xx DGN Package
8-Pin MSOP-PowerPAD
Top View



TPS3707-xx D Package
8-Pin SOIC
Top View



TPS3707-xx DGN Package
8-Pin MSOP-PowerPAD
Top View



Pin Functions

PIN					I/O	DESCRIPTION
NAME	TPS3705-xx		TPS3707-xx			
	SOIC	MSOP-PowerPAD	SOIC	MSOP-PowerPAD		
GND	3	5	3	5	—	Ground
$\overline{MR}$	1	3	1	3	I	Manual reset
NC	—	—	6	8	—	No internal connection
PFI	4	6	4	6	I	Power-fail comparator input
$\overline{PFO}$	5	7	5	7	O	Power-fail comparator output
$\overline{RESET}$	7	1	7	1	O	Active-low reset output
RESET	—	—	8	2	O	Active-high reset output
V_{DD}	2	4	2	4	—	Supply voltage
WDI	6	8	—	—	I	Watchdog timer input
$\overline{WDO}$	8	2	—	—	O	Watchdog timer output

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V_{DD}(2)		7	V
PFI voltage range, V_{PFI}	–0.3	V_{DD} + 0.3	V
All other pins(2)	–0.3	7	V
Maximum low output current, I_{OL}		5	mA
Maximum high output current, I_{OH}		–5	mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD})		±20	mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD})		±20	mA
Continuous total power dissipation	See *Dissipation Ratings*		
Soldering temperature		260	°C
Operating temperature, T_A	–40	85	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than t = 1000h continuously.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	2		6	V
V_I	Input voltage	0		V_{DD} + 0.3	V
V_{IH}	High-level input voltage	0.7 × V_{DD}			V
V_{IL}	Low-level input voltage			0.3 × V_{DD}	V
Δt/ΔV	Input transition rise and fall rate at $\overline{MR}$ or WDI			100	ns/V
T_A	Operating free-air temperature	–40		85	°C

7.4 Thermal Information

THERMAL METRIC[1]		TPS3705-xx D (SOIC) 8 PINS	TPS3707-xx DGN (MSOP-PowerPAD) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	118.2	66.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.4	62.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.5	45.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.8	7.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	57.9	44.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	18.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	TPS370x-xx, V_{DD} = 1.1 V, I_{OH} = –4 µA	0.8			V
		TPS3707-25, TPS370x-30, TPS370x-33, $V_{DD} = V_{IT+} + 0.2$ V, I_{OH} = –500 µA	0.7 × V_{DD}			
		TPS370x-50, $V_{DD} = V_{IT+} + 0.2$ V, I_{OH} = –800 µA	V_{DD} – 1.5			
		TPS370x-xx, V_{DD} = 6 V, I_{OH} = –800 µA	V_{DD} – 1.5			
V_{OL}	Low-level output voltage	TPS3707-25, TPS370x-30, TPS370x-33, $V_{DD} = V_{IT+} + 0.2$ V, I_{OL} = 1 mA			0.3	V
		TPS370x-50, $V_{DD} = V_{IT+} + 0.2$ V, I_{OL} = 2.5 mA			0.4	
		TPS370x-xx, V_{DD} = 6 V, I_{OL} = 3 mA			0.4	
	Power-up reset voltage[1]	$V_{DD} \geq 1.1$ V, I_{OL} = 50 µA			0.3	V
$V_{IT–}$	Negative-going input threshold voltage[2]	TPS3707-25, T_A = 0°C to 85°C	2.2	2.25	2.3	V
		TPS370x-30, T_A = 0°C to 85°C	2.57	2.63	2.68	
		TPS370x-33, T_A = 0°C to 85°C	2.87	2.93	2.98	
		TPS370x-50, T_A = 0°C to 85°C	4.45	4.55	4.63	
		TPS3707-25, T_A = –40°C to 85°C	2.2	2.25	2.32	
		TPS370x-30, T_A = –40°C to 85°C	2.57	2.63	2.7	
		TPS370x-33, T_A = –40°C to 85°C	2.87	2.93	3	
		TPS370x-50, T_A = –40°C to 85°C	4.45	4.55	4.65	
	Negative-going input threshold voltage, PFI[2]	TPS370x-xx, $V_{DD} \geq 2$ V, T_A = –40°C to 85°C	1.2	1.25	1.3	
V_{hys}	Hysteresis, V_{DD}	TPS3707-25		40		mV
		TPS370x-30		50		
		TPS370x-33		50		
		TPS370x-50		70		
	Hysteresis, PFI	TPS370x-xx		10		
$I_{IH(AV)}$	Average high-level input current, WDI	WDI = V_{DD} = 6 V, time average (dc = 88%)		100	150	µA
$I_{IL(AV)}$	Average low-level input current, WDI	WDI = 0 V, V_{DD} = 6 V, time average (dc = 12%)		–15	–20	µA
I_{IH}	High-level input current, WDI	WDI = V_{DD} = 6 V		120	170	µA
	High-level input current, $\overline{MR}$	$\overline{MR}$ = 0.7 × V_{DD}, V_{DD} = 6 V		–130	–180	
I_{IL}	Low-level input current, WDI	WDI = 0 V, V_{DD} = 6 V		–120	–170	µA
	Low-level input current, $\overline{MR}$	$\overline{MR}$ = 0 V, V_{DD} = 6 V		–430	–600	
I_I	Input current, PFI	V_{DD} = 6 V, 0 V ≤ V_I ≤ V_{DD}	–1	0	1	µA

(1) The lowest supply voltage at which $\overline{RESET}$ becomes active, $t_{r,VDD} \geq 15$ µs/V
(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near to the supply terminals

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	TPS3705-xx, V_{DD} = 2 V to 6 V, $\overline{MR}$ = V_{DD}, $\overline{MR}$, WDI and outputs unconnected		30	50	µA
		TPS3707-xx, V_{DD} = 2 V to 6 V, $\overline{MR}$ = V_{DD}, $\overline{MR}$, WDI and outputs unconnected		20	50	
C_i	Input capacitance	V_I = 0 V to V_{DD}		5		pF

7.6 Timing Requirements

at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_w	Pulse width	At V_{DD}, V_{DD} = V_{IT+} + 0.2 V, V_{DD} = V_{IT-} – 0.2 V	6			µs
		At $\overline{MR}$ and WDI, V_{DD} ≥ V_{IT+} + 0.2 V, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.7 × V_{DD}	100			ns

7.7 Switching Characteristics

at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{t(out)}$	Watchdog time out	V_{DD} ≥ V_{IT+} + 0.2 V, see Figure 1	1.1	1.6	2.3	s
t_d	Delay time	V_{DD} ≥ V_{IT+} + 0.2 V, see Figure 1	140	200	280	ms
t_{PHL}	Propagation (delay) time, high-to-low-level output	$\overline{MR}$ to $\overline{RESET}$ delay, V_{DD} ≥ V_{IT+} + 0.2 V, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.7 × V_{DD}		50	250	ns
t_{PLH}	Propagation (delay) time, low-to-high-level output	$\overline{MR}$ to RESET delay (TPS3707-xx only) V_{DD} ≥ V_{IT+} + 0.2 V, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.7 × V_{DD}		50	250	ns
t_{PHL}	Propagation (delay) time, high-to-low-level output	V_{DD} to $\overline{RESET}$ delay		3	5	µs
t_{PLH}	Propagation (delay) time, low-to-high-level output	V_{DD} to RESET delay (TPS3707-xx only)		3	5	µs
t_{PHL}	Propagation (delay) time, high-to-low-level output	PFI to $\overline{PFO}$ delay, V_{DD} = 2 V to 6 V		0.5	1	µs
t_{PLH}	Propagation (delay) time, low-to-high-level output	PFI to $\overline{PFO}$ delay, V_{DD} = 2 V to 6 V		0.5	1	µs

7.8 Dissipation Ratings

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DGN	2.14 W	17.1 mW/°C	1.37 W	1.11 W
D	725 mW	5.8 mW/°C	464 mW	377 mW

7.9 Timing Diagram

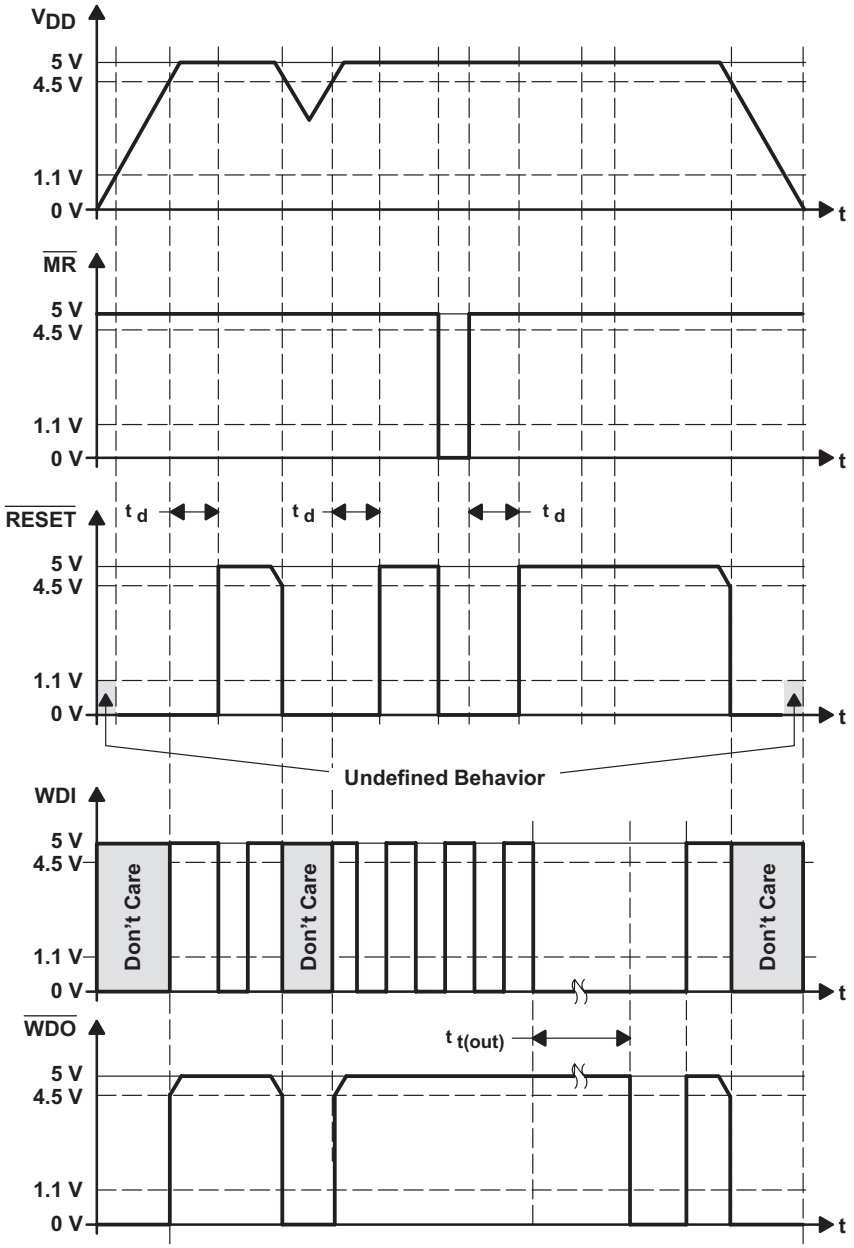


Figure 1. Timing Diagrams

7.10 Typical Characteristics

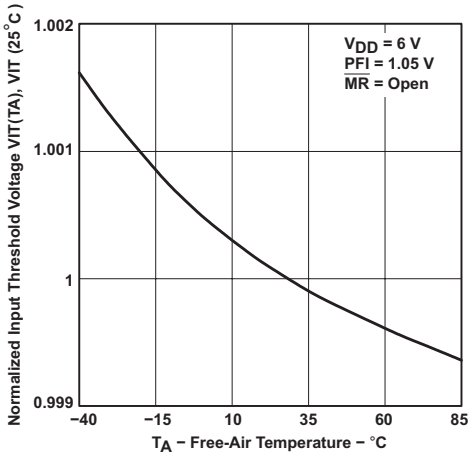


Figure 2. Normalized Input Threshold Voltage vs Free-Air Temperature at V_{DD}

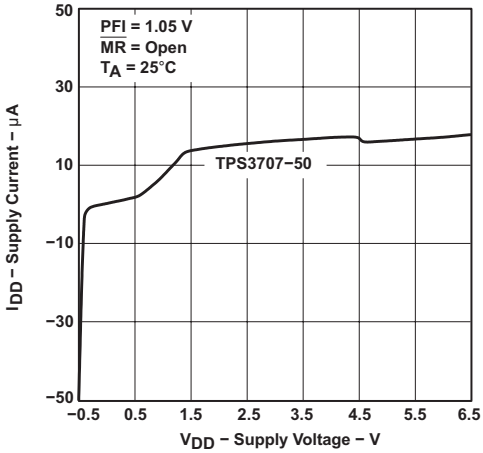


Figure 3. Supply Current vs Supply Voltage

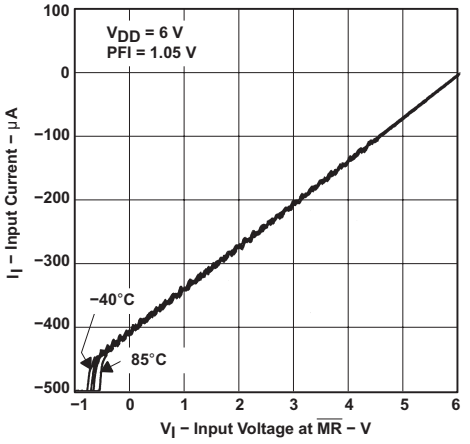


Figure 4. Input Current vs Input Voltage at $\overline{MR}$

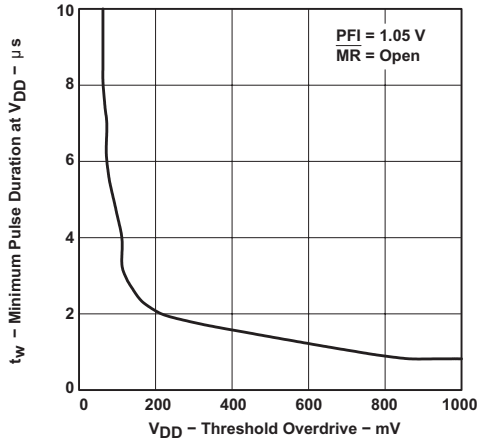


Figure 5. Minimum Pulse Duration at V_{DD} vs V_{DD} Threshold Overdrive

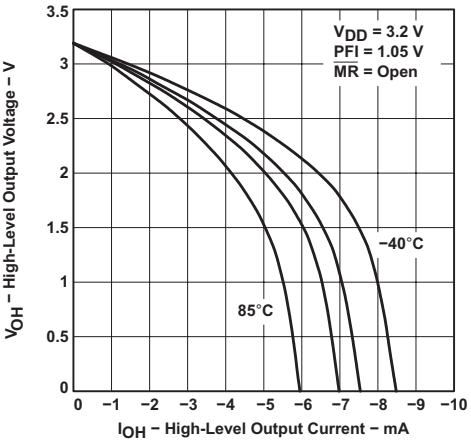


Figure 6. High-Level Output Voltage vs High-Level Output Current

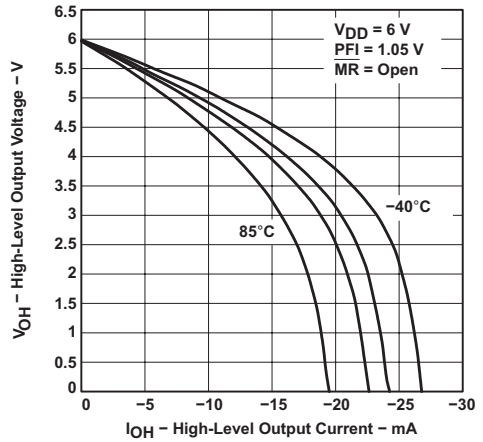


Figure 7. High-Level Output Voltage vs High-Level Output Current

Typical Characteristics (continued)

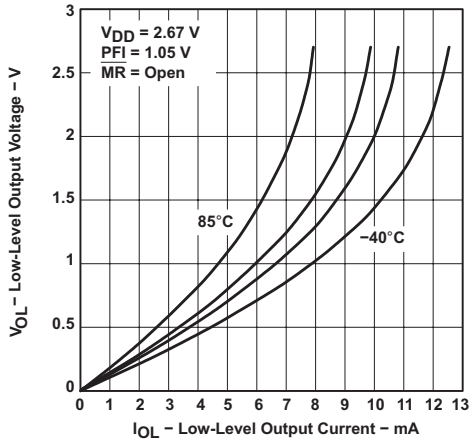


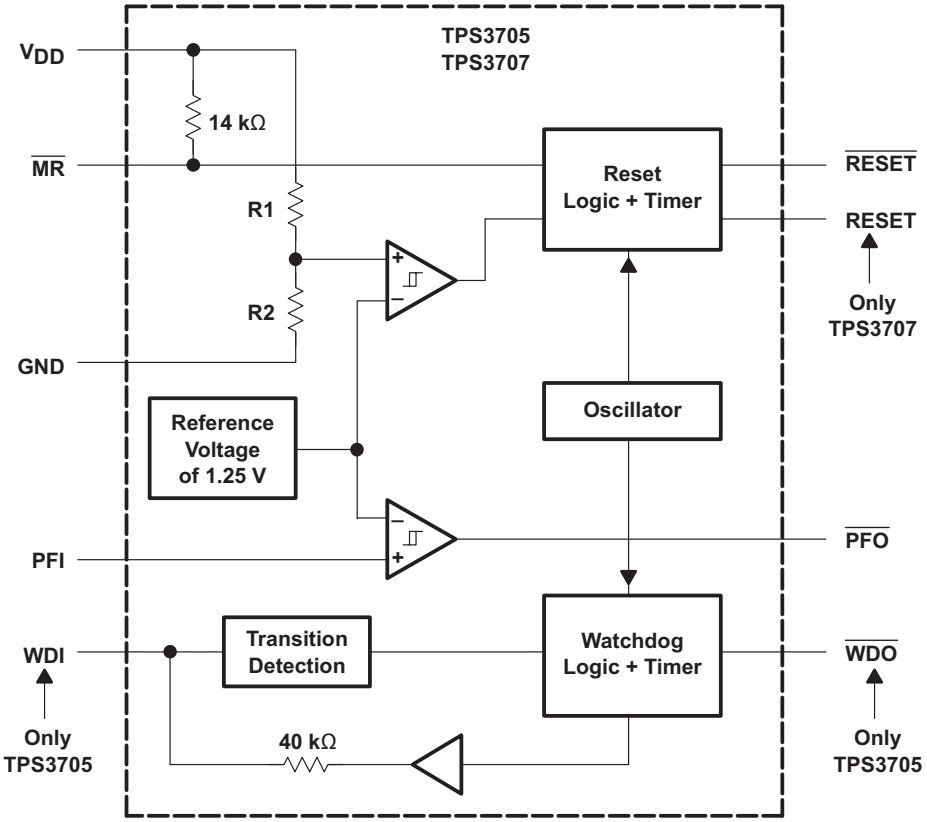
Figure 8. Low-Level Output Voltage vs Low-Level Output Current

8 Detailed Description

8.1 Overview

The TPS370x-xx family of supervisors feature an integrated reference and comparator for V_{DD} supervision, an additional power-fail supervisor, and a manual reset input. The TPS3705-xx devices feature a watchdog timer, where the TPS3707-xx devices feature a complimentary RESET output.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Manual Reset Input

The TPS370x-xx devices incorporate a manual reset input, $\overline{MR}$. A low level at $\overline{MR}$ causes $\overline{RESET}$ to become active.

8.3.2 Power-Fail Comparator

The TPS370x-xx family integrates a power-fail comparator which can be used for low-battery detection, power-fail warning, or for monitoring a power supply other than the main supply.

8.3.3 Watchdog Timer

The TPS3705-xx devices have a watchdog timer that is periodically triggered by a positive or negative transition at WDI. When the supervising system fails to retrigger the watchdog circuit within the timeout interval, $t_{t(out)}$ = 1.6 s, $\overline{WDO}$ becomes active. This event also reinitializes the watchdog timer. Leaving WDI unconnected disables the watchdog.

The TPS3707-xx devices do not have the watchdog function, but include a high-level output RESET.

8.4 Device Functional Modes

8.4.1 V_{DD} < 1.1 V

When V_{DD} is less than 1.1 V, the status of the outputs cannot be determined.

8.4.2 1.1 V < V_{DD} ≤ 2 V

When V_{DD} is greater than 1.1 V but less than 2 V, the output states are valid. However, the specifications in *Electrical Characteristics* do not apply.

8.4.3 2 V < V_{DD} < 6 V

When V_{DD} is greater than 2 V but less than 6 V, the device is within the recommended operating conditions (see *Recommended Operating Conditions*). See Table 1, Table 2, and Table 3 for corresponding truth tables.

Table 1. TPS3705 Truth Table

$\overline{MR}$	$V_{DD} > V_{IT}$	$\overline{RESET}$	TYPICAL DELAY
H → L	1	H → L	30 ns
L → H	1	L → H	200 ms
H	1 → 0	H → L	3 µs
H	0 → 1	L → H	200 ms

Table 2. TPS3707 Truth Table

$\overline{MR}$	$V_{DD} > V_{IT}$	$\overline{RESET}$	RESET	TYPICAL DELAY
H → L	1	H → L	L → H	30 ns
L → H	1	L → H	H → L	200 ms
H	1 → 0	H → L	L → H	3 µs
H	0 → 1	L → H	H → L	200 ms

Table 3. TPS370x Truth Table

PFI > V_{IT}	$\overline{PFO}$	TYPICAL DELAY
0 → 1	L → H	0.5 µs
1 → 0	H → L	0.5 µs

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS370x-xx family of devices offers several options for power monitoring. The TPS3705-xx offers a watchdog supervisor, V_{DD} rail monitoring, and a power-fail interrupt monitor. The TPS3707-xx offers V_{DD} rail monitoring with complimentary outputs and a power-fail interrupt monitor.

9.2 Typical Application

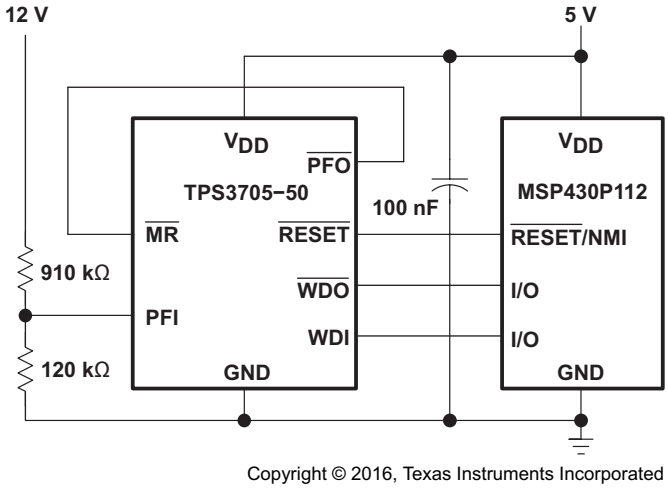


Figure 9. Typical MSP430 Application

9.2.1 Design Requirements

Table 4 lists the required design parameters for Figure 9.

Table 4. Application Parameters

DESIGN PARAMETER	VALUE
Monitored voltage 1	5 V
Monitored voltage 2	12 V

9.2.2 Detailed Design Procedure

To create two voltage monitoring rails, the PFI input can be used along with the MR pin to create a single output. The 5-V monitor is created by selecting a 5-V device option, giving threshold of 4.55 V. The PFI input is configured to any adjustable rail with a voltage divider. Use Equation 1 to select resistors.

$$V_{TH} = \frac{R_1 + R_2}{R_2} \times V_{IT-} = \frac{910\,k + 120\,k}{120\,k} \times 1.25 = 10.73\ V \quad (1)$$

9.2.3 Application Curves

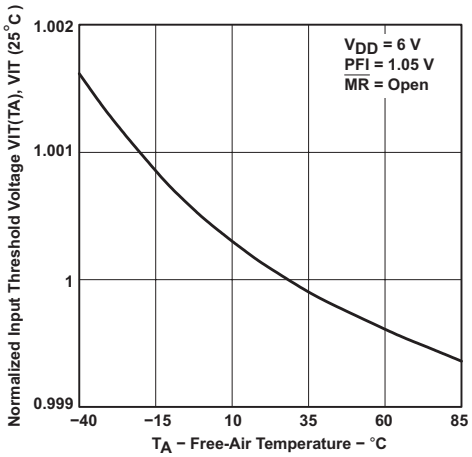


Figure 10. Normalized Input Threshold Voltage vs Free-Air Temperature at V_{DD}

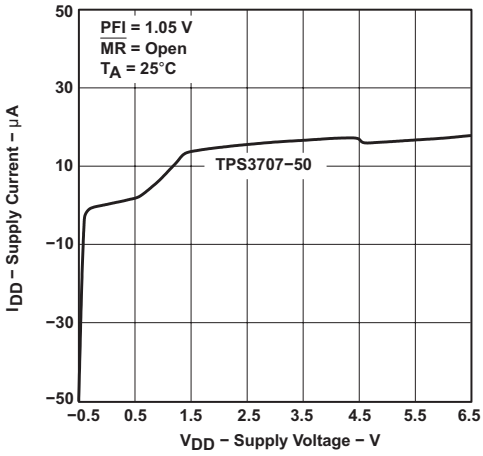


Figure 11. Supply Current vs Supply Voltage

10 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range from 2 V to 6 V.

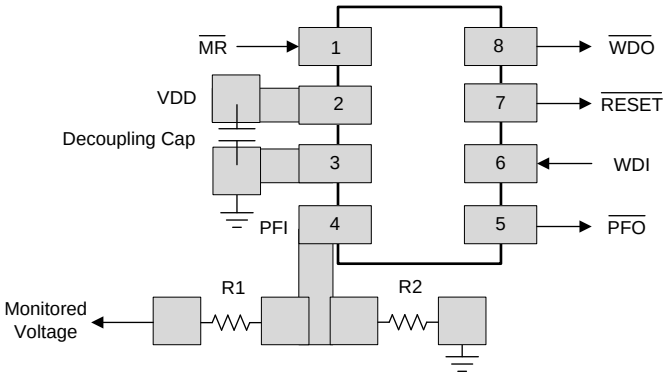
11 Layout

11.1 Layout Guidelines

Place a 0.1-µF decoupling capacitor as close to the device as possible.

If a resistor divider is used, place the resistors as close to the device as possible to minimize noise coupling.

11.2 Layout Example



TPS3705 D Package

Figure 12. TPS3705 Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3705-30D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70530	Samples
TPS3705-30DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAT	Samples
TPS3705-30DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70530	Samples
TPS3705-30DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70530	Samples
TPS3705-33D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70533	Samples
TPS3705-33DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70533	Samples
TPS3705-33DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAU	Samples
TPS3705-33DGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAU	Samples
TPS3705-33DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAU	Samples
TPS3705-33DGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAU	Samples
TPS3705-33DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70533	Samples
TPS3705-33DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70533	Samples
TPS3705-50D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70550	Samples
TPS3705-50DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70550	Samples
TPS3705-50DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAV	Samples
TPS3705-50DGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAV	Samples
TPS3705-50DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAV	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3705-50DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70550	Samples
TPS3705-50DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70550	Samples
TPS3707-25D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70725	Samples
TPS3707-25DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70725	Samples
TPS3707-25DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAW	Samples
TPS3707-25DGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAW	Samples
TPS3707-25DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAW	Samples
TPS3707-25DGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAW	Samples
TPS3707-25DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70725	Samples
TPS3707-30D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70730	Samples
TPS3707-30DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70730	Samples
TPS3707-30DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAX	Samples
TPS3707-30DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAX	Samples
TPS3707-30DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70730	Samples
TPS3707-33D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70733	Samples
TPS3707-33DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70733	Samples
TPS3707-33DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAY	Samples
TPS3707-33DGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAY	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3707-33DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAY	Samples
TPS3707-33DGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAY	Samples
TPS3707-33DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70733	Samples
TPS3707-33DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70733	Samples
TPS3707-50D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70750	Samples
TPS3707-50DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70750	Samples
TPS3707-50DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAZ	Samples
TPS3707-50DGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAZ	Samples
TPS3707-50DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAZ	Samples
TPS3707-50DGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAZ	Samples
TPS3707-50DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70750	Samples
TPS3707-50DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	70750	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

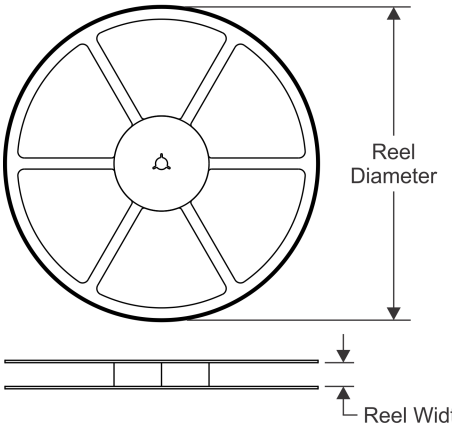
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

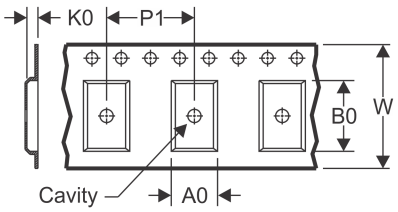
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

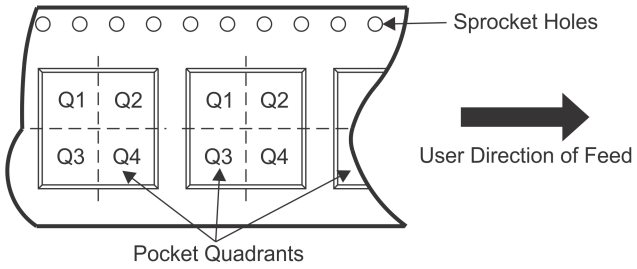


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

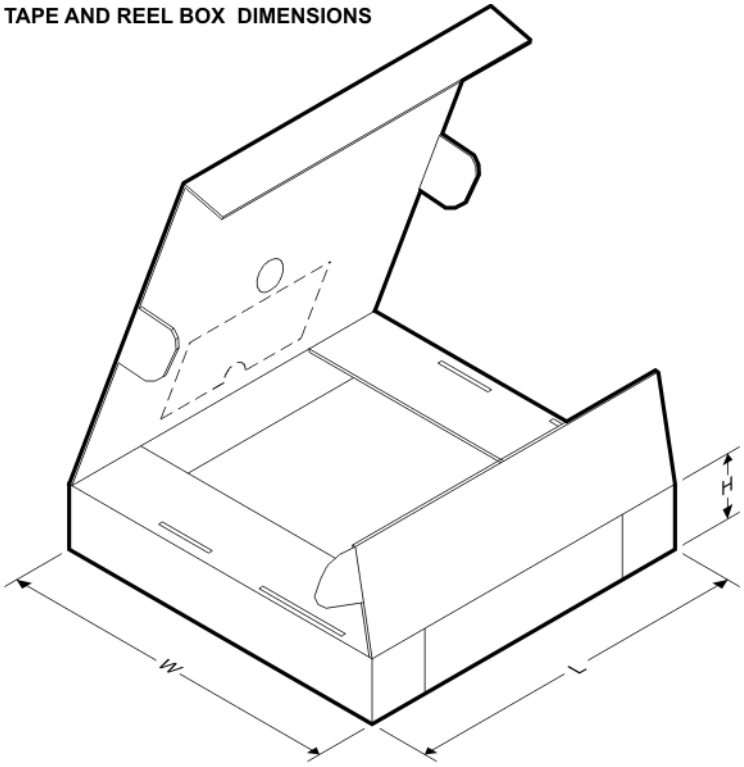


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3705-30DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3705-33DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3705-33DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3705-50DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3705-50DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3707-25DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3707-25DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3707-30DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3707-30DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3707-30DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3707-33DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3707-33DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3707-50DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3707-50DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

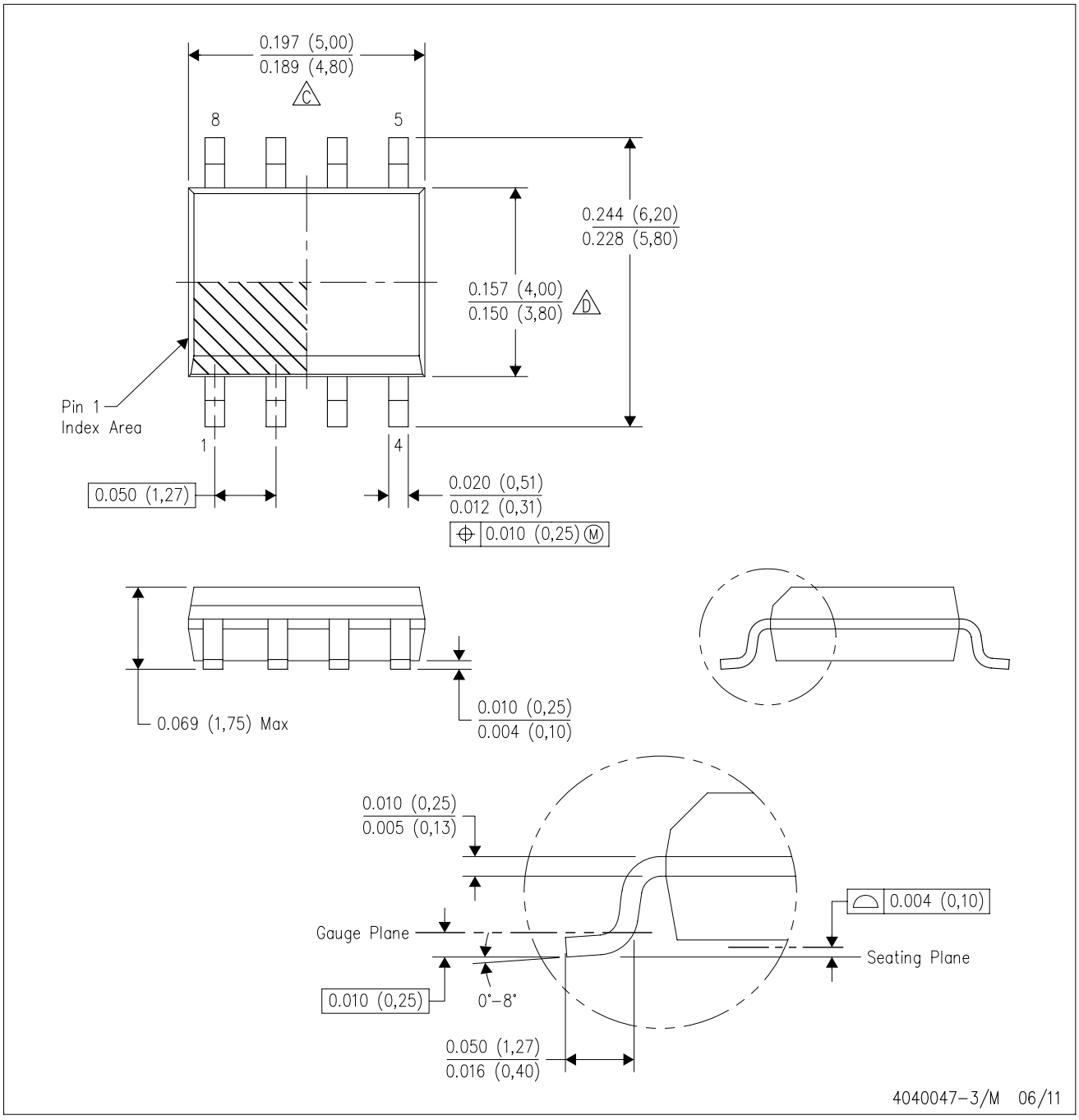


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3705-30DR	SOIC	D	8	2500	367.0	367.0	38.0
TPS3705-33DGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
TPS3705-33DR	SOIC	D	8	2500	367.0	367.0	38.0
TPS3705-50DGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
TPS3705-50DR	SOIC	D	8	2500	367.0	367.0	38.0
TPS3707-25DGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
TPS3707-25DR	SOIC	D	8	2500	367.0	367.0	38.0
TPS3707-30DGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
TPS3707-30DR	SOIC	D	8	2500	367.0	367.0	35.0
TPS3707-30DR	SOIC	D	8	2500	367.0	367.0	38.0
TPS3707-33DGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
TPS3707-33DR	SOIC	D	8	2500	367.0	367.0	38.0

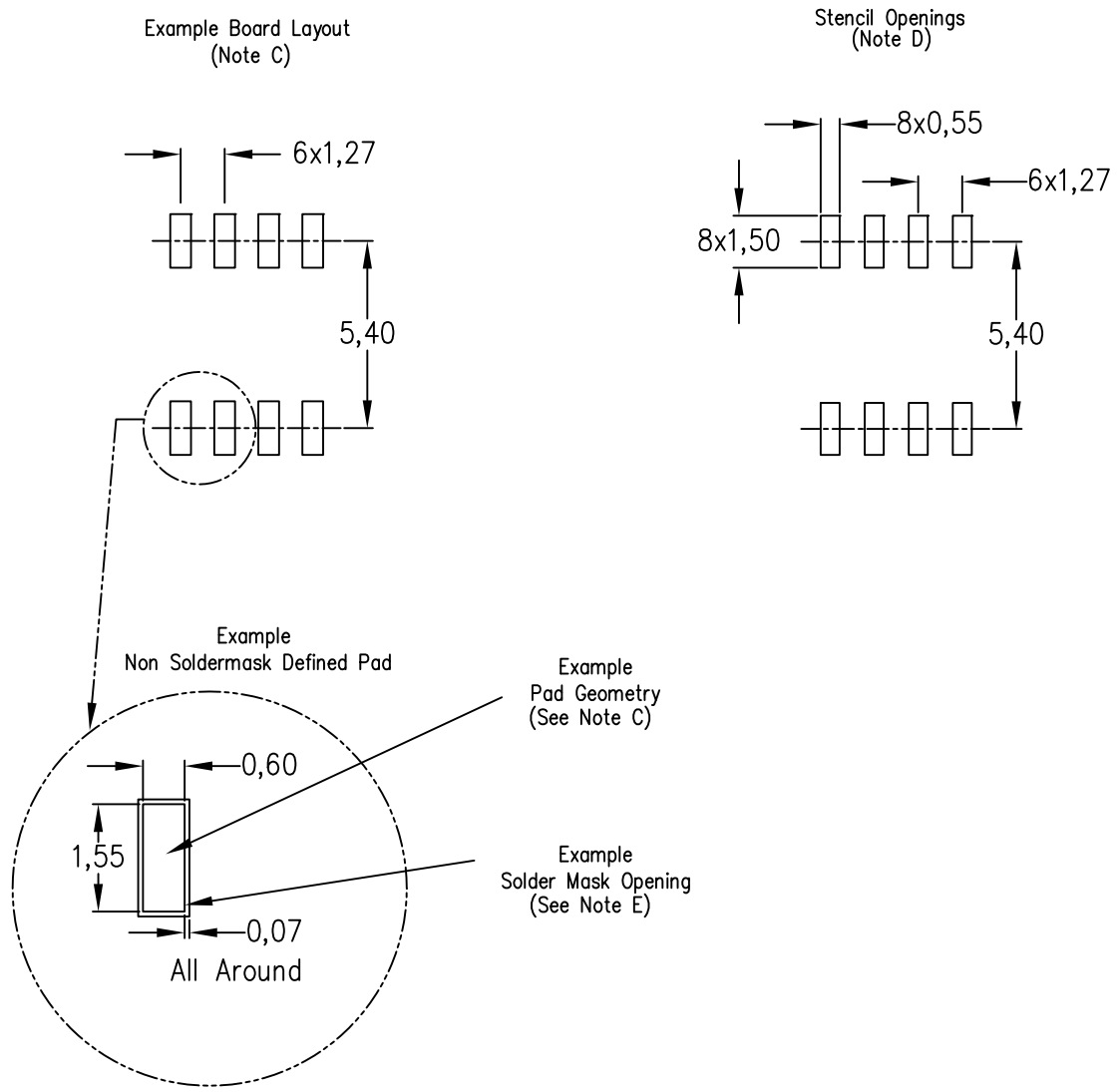
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3707-50DGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
TPS3707-50DR	SOIC	D	8	2500	367.0	367.0	38.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



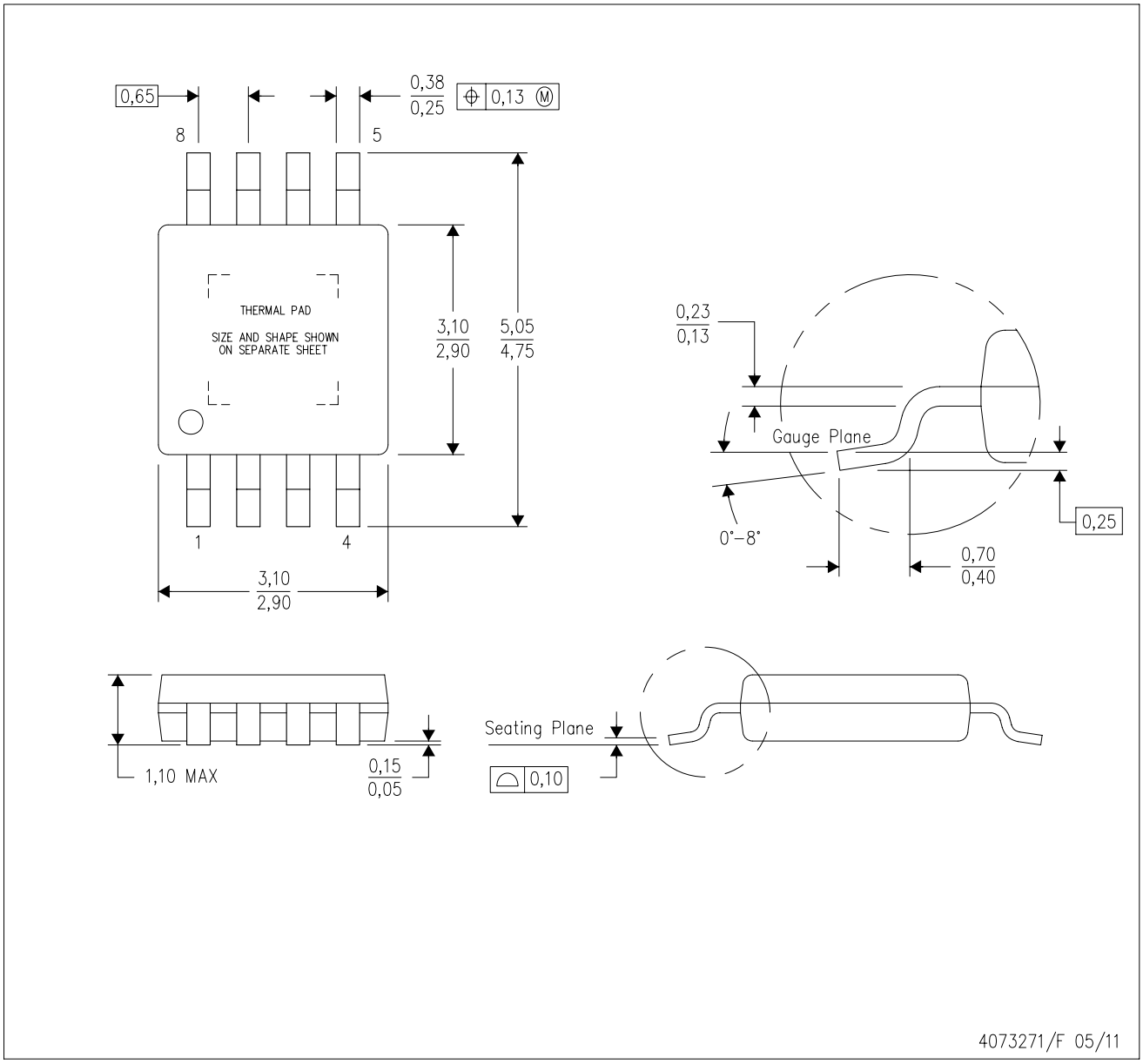
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

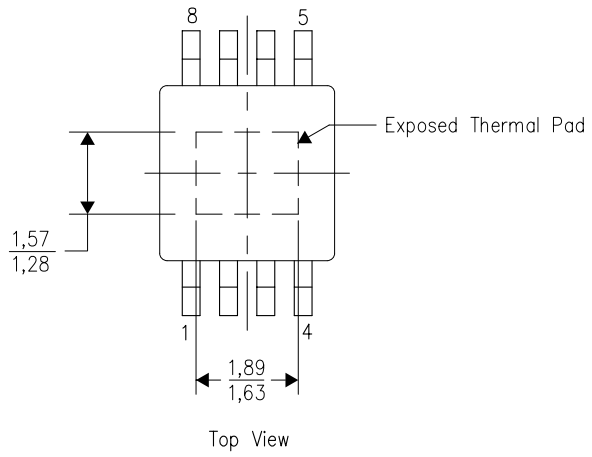
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

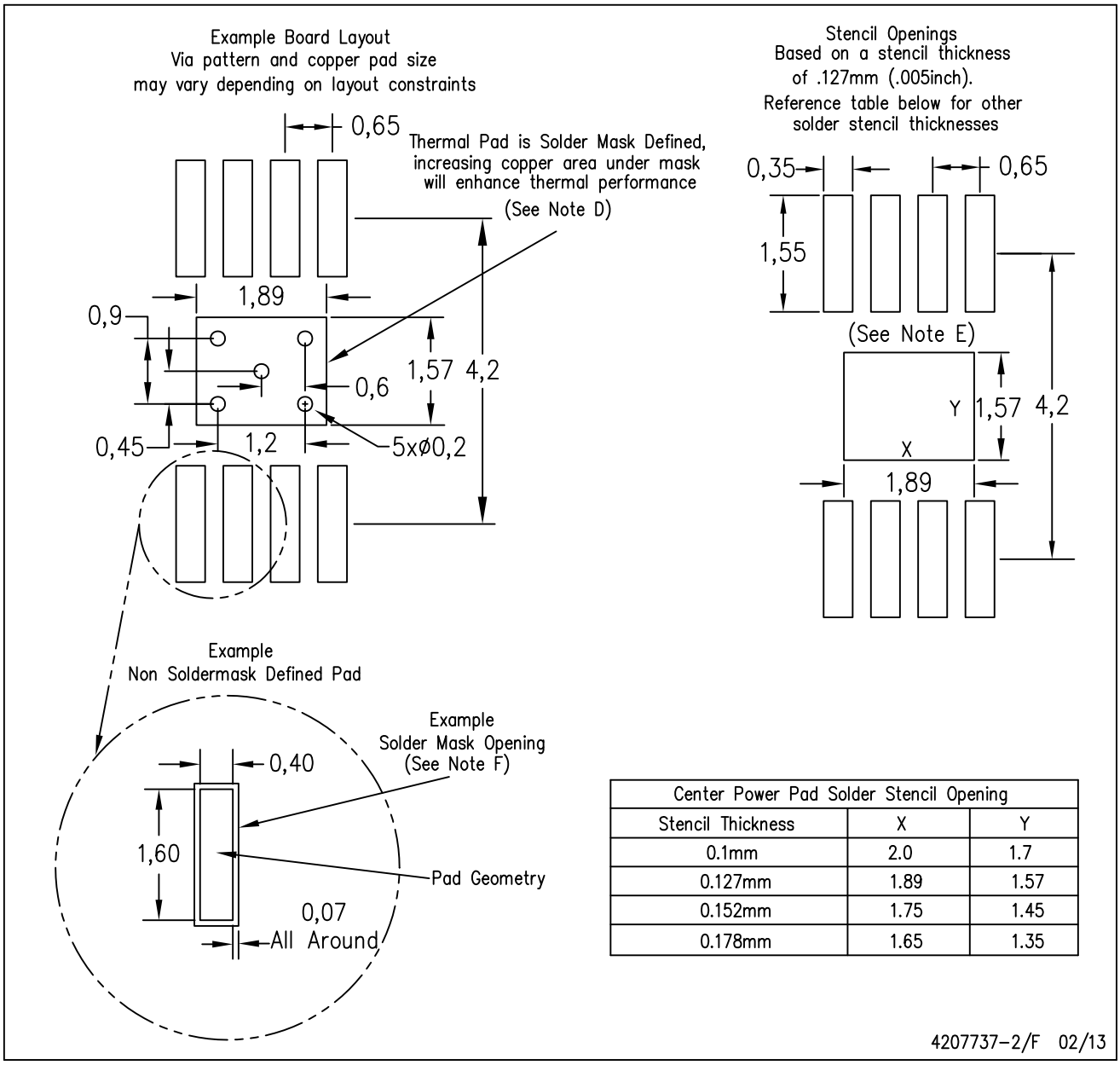
Exposed Thermal Pad Dimensions

4206323–2/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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