SILICON LABS

BGM13S Blue Gecko *Bluetooth* ® SiP Module Data Sheet

The BGM13S is Silicon Labs' first SiP module solution for *Bluetooth* 5.0 LE connectivity. It supports 2 Mbps, 1 Mbps and coded LE Bluetooth PHYs. Also, with 512 kB of flash and 64 kB of RAM, the BGM13S is suited to meet Bluetooth Mesh networking memory requirements effectively.

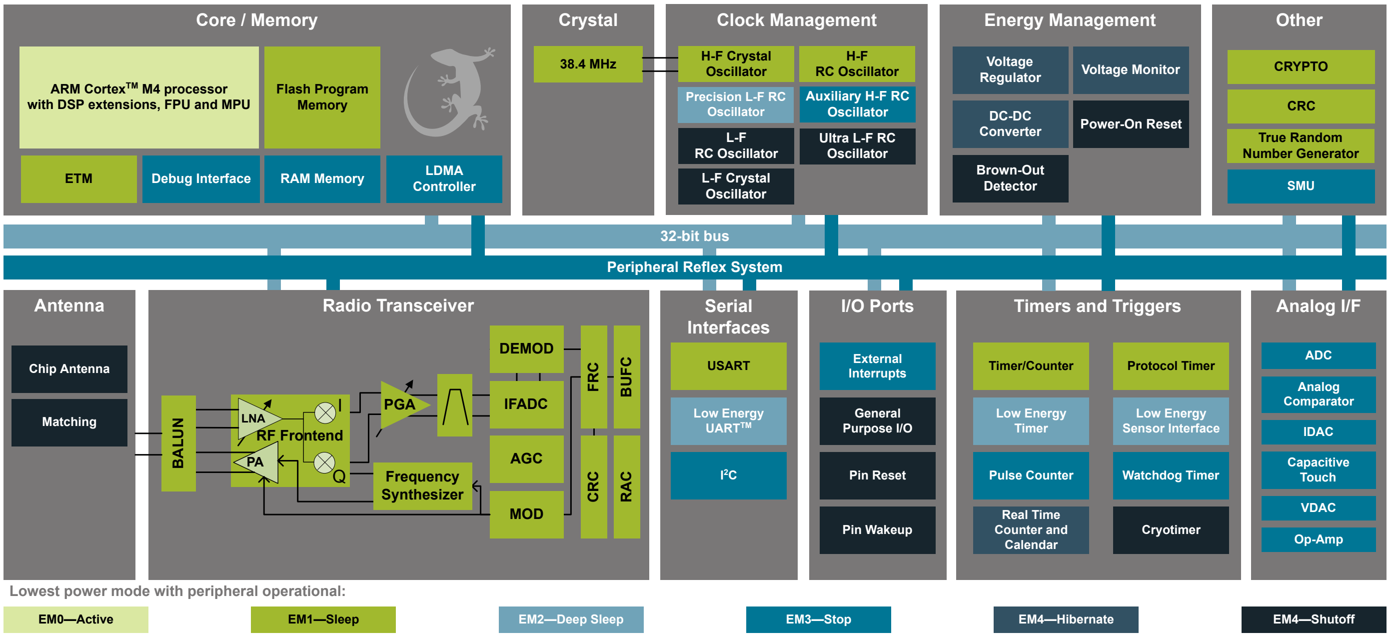
Based on the EFR32BG13 Blue Gecko SoC, the BGM13S delivers robust RF performance, low energy consumption, a wide selection of MCU peripherals, regulatory test certificates for various regions and countries, and a simplified development experience, all in a 6.5 × 6.5 mm package. Together with the certified software stacks and powerful tools also offered by Silicon Labs, the BGM13S minimizes the area requirements, engineering efforts and development costs associated with adding Bluetooth 5.0 or Bluetooth Mesh connectivity to any product, accelerating its time-to-market.

The BGM13S is intended for a broad range of applications, including:

- Wearables
- IoT end-node devices and gateways
- Health, sports, and wellness
- Industrial, home, and building automation
- Beacons
- Smart phone, tablet, and PC accessories

KEY FEATURES

- Bluetooth 5.0 LE compliant
- Fit for Bluetooth Mesh
- Antenna or RF Pin variants
- Up to +18 dBm TX power
- -94.1 dBm RX sensitivity at 1 Mbps
- 32-bit ARM® Cortex®-M4 core at 38.4 MHz
- 512/64 kB of flash/RAM memory
- Autonomous Hardware Crypto Accelerators
- Integrated DC-DC converter
- 32 GPIO pins
- 6.5 mm × 6.5 mm × 1.4 mm



1. Feature List

- **Supported Protocols**
  - Bluetooth 5.0 LE
  - Bluetooth Mesh
- **Wireless System-on-Chip**
  - 2.4 GHz radio
  - TX power up to +18 dBm
  - High Performance 32-bit 38.4 MHz ARM Cortex®-M4 with DSP instruction and floating-point unit for efficient signal processing
  - 512 kB flash program memory
  - 64 kB RAM data memory
  - Embedded Trace Macrocell (ETM) for advanced debugging
  - Integrated DC-DC converter
- **High Receiver Performance**
  - -102.1 dBm sensitivity at 125 kbit/s GFSK
  - -97.9 dBm sensitivity at 500 kbit/s GFSK
  - -94.1 dBm sensitivity at 1 Mbit/s GFSK
  - -90.2 dBm sensitivity at 2 Mbit/s GFSK
- **Low Energy Consumption**
  - 9.7 mA RX current at 1 Mbps, GFSK
  - 8.9 mA TX current at 0 dBm output power
  - 87 μA/MHz in Active Mode (EM0)
  - 1.4 μA EM2 DeepSleep current (full RAM retention and RTCC running from LFXO)
  - 1.14 μA EM3 Stop current (State/RAM retention)
  - Wake on Radio with signal strength detection, preamble pattern detection, frame detection and timeout
- **Regulatory Certifications**
  - FCC
  - CE
  - IC / ISEDC
  - MIC / Telec
- **Wide Operating Range**
  - 1.8 V to 3.8 V single power supply
  - -40 °C to +85 °C
- **Dimensions**
  - 6.5 mm × 6.5 mm × 1.4 mm
- **Support for Internet Security**
  - General Purpose CRC
  - True Random Number Generator (TRNG)
  - 2 × Hardware Cryptographic Accelerators (CRYPTO) for AES 128/256, SHA-1, SHA-2 (SHA-224 and SHA-256) and ECC
- **Wide Selection of MCU Peripherals**
  - 12-bit 1 Msps SAR Analog to Digital Converter (ADC)
  - 2 × Analog Comparator (ACMP)
  - 2 × Digital to Analog Converter (VDAC)
  - 3 × Operational Amplifier (Opamp)
  - Digital to Analog Current Converter (IDAC)
  - Low-Energy Sensor Interface (LESENSE)
  - Multi-channel Capacitive Sense Interface (CSEN)
  - 32 pins connected to analog channels (APORT) shared between analog peripherals
  - 32 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - 2 ×16-bit Timer/Counter
    - 3 or 4 Compare/Capture/PWM channels
  - 1 × 32-bit Timer/Counter
    - 3 Compare/Capture/PWM channels
  - 32-bit Real Time Counter and Calendar
  - 16-bit Low Energy Timer for waveform generation
  - 32-bit Ultra Low Energy Timer/Counter for periodic wake-up from any Energy Mode
  - 16-bit Pulse Counter with asynchronous operation
  - 2 × Watchdog Timer
  - 3 × Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/I^{2}S)
  - Low Energy UART (LEUART™)
  - 2 × I^{2}C interface with SMBus support and address recognition in EM3 Stop

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Protocol Stack	Max TX Power	Antenna	Flash (kB)	RAM (kB)	GPIO	Packaging
BGM13S32F512GA-V2	Bluetooth LE	18 dBm	Built-in	512	64	32	Cut Tape
BGM13S32F512GA-V2R	Bluetooth LE	18 dBm	Built-in	512	64	32	Reel
BGM13S32F512GN-V2	Bluetooth LE	18 dBm	RF pin	512	64	32	Cut Tape
BGM13S32F512GN-V2R	Bluetooth LE	18 dBm	RF pin	512	64	32	Reel
BGM13S22F512GA-V2	Bluetooth LE	8 dBm	Built-in	512	64	32	Cut Tape
BGM13S22F512GA-V2R	Bluetooth LE	8 dBm	Built-in	512	64	32	Reel
BGM13S22F512GN-V2	Bluetooth LE	8 dBm	RF pin	512	64	32	Cut Tape
BGM13S22F512GN-V2R	Bluetooth LE	8 dBm	RF pin	512	64	32	Reel

End-product manufacturers must verify that the module is configured to meet regulatory limits for each region in accordance with the formal certification test reports.

Devices ship with the Gecko UART DFU bootloader 1.4.1 + NCP application from Bluetooth SDK 2.8.1.0. The firmware settings conform to the diagram shown in Figure 5.1 Typical Connections for BGM13S with UART Network Co-Processor on page 66.

Table of Contents

3. System Overview

3.1 Introduction

The BGM13S product family combines an energy-friendly MCU with a highly integrated radio transceiver and a high performance, ultra robust antenna. The devices are well suited for any battery operated application, as well as other system where ultra-small size, reliable high performance RF, low-power consumption and easy application development are key requirements. This section gives a short introduction to the full radio and MCU system.

A detailed block diagram of the BGM13S module is shown in the figure below.

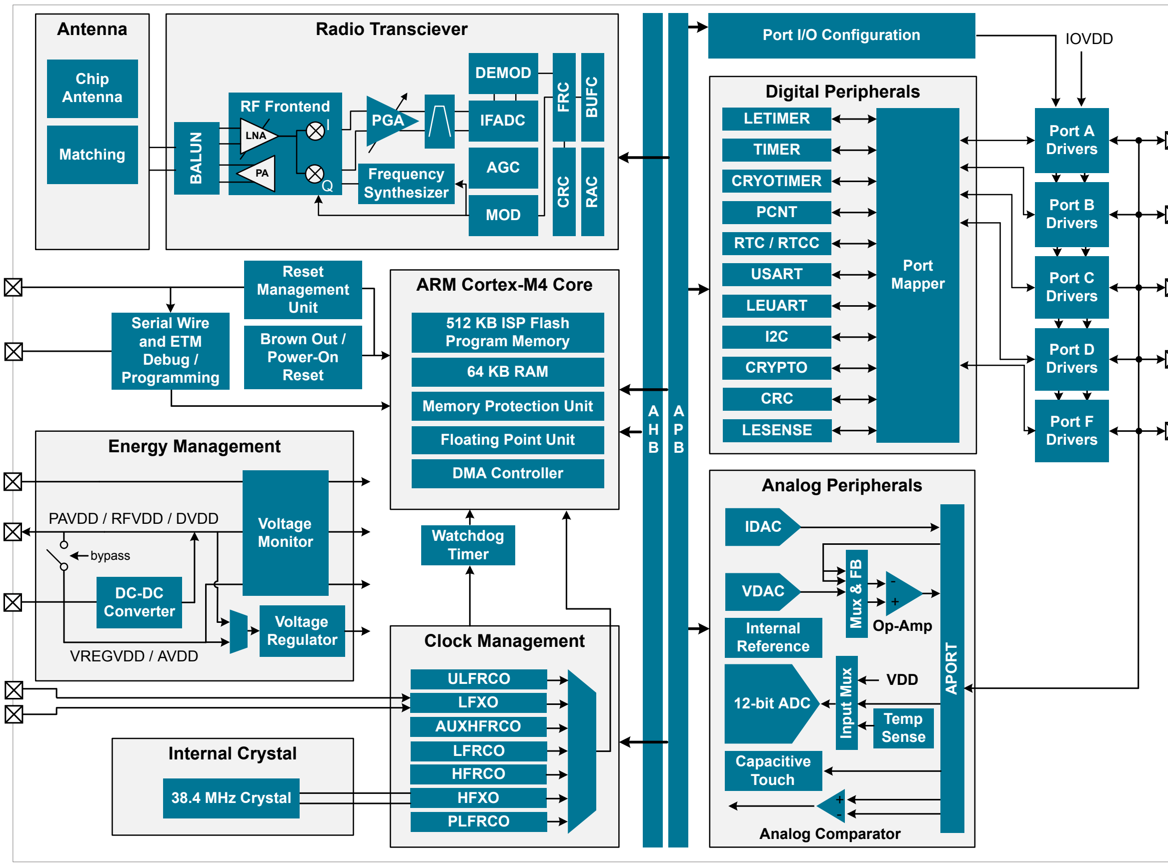


Figure 3.1. BGM13S Block Diagram

3.2 Radio

The BGM13S features a radio transceiver supporting Bluetooth® low energy protocol.

3.2.1 Antenna Interface

The BGM13S has two antenna solution variants. One of them is a high-performance integrated chip antenna (BGM13SxxFxxxxA) and the other is a 50 Ohm matched RF pin to attach an external antenna to the module (BGM13SxxFxxxxN).

Table 3.1. Antenna Efficiency and Peak Gain

Parameter	With optimal layout	Note
Efficiency	-1 to -2 dB	Antenna efficiency, gain and radiation pattern are highly dependent on the application PCB layout and mechanical design. Refer to for PCB layout and antenna integration guidelines for optimal performance.
Peak gain	1 dBi	

3.2.2 RFSENSE

The RFSENSE block generates a system wakeup interrupt upon detection of wideband RF energy at the antenna interface, providing true RF wakeup capabilities from low energy modes including EM2, EM3 and EM4.

RFSENSE triggers on a relatively strong RF signal and is available in the lowest energy modes, allowing exceptionally low energy consumption. RFSENSE does not demodulate or otherwise qualify the received signal, but software may respond to the wakeup event by enabling normal RF reception.

Various strategies for optimizing power consumption and system response time in presence of false alarms may be employed using available timer peripherals.

3.2.3 Packet and State Trace

The BGM13S Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data and state information
- Data observability on a single-pin UART data output, or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data and state / meta information in a single serial data stream

3.2.4 Random Number Generator

The Frame Controller (FRC) implements a random number generator that uses entropy gathered from noise in the RF receive chain. The data is suitable for use in cryptographic applications.

Output from the random number generator can be used either directly or as a seed or entropy source for software-based random number generator algorithms such as Fortuna.

3.3 Power

The BGM13S has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An integrated DC-DC buck regulator is utilized to further reduce the current consumption. Figure 3.2 Power Supply Configuration for BGM13S22xxx Devices on page 9 and Figure 3.3 Power Supply Configuration for BGM13S32xxx Devices on page 9 show how the external and internal supplies of the module are connected for different part numbers.

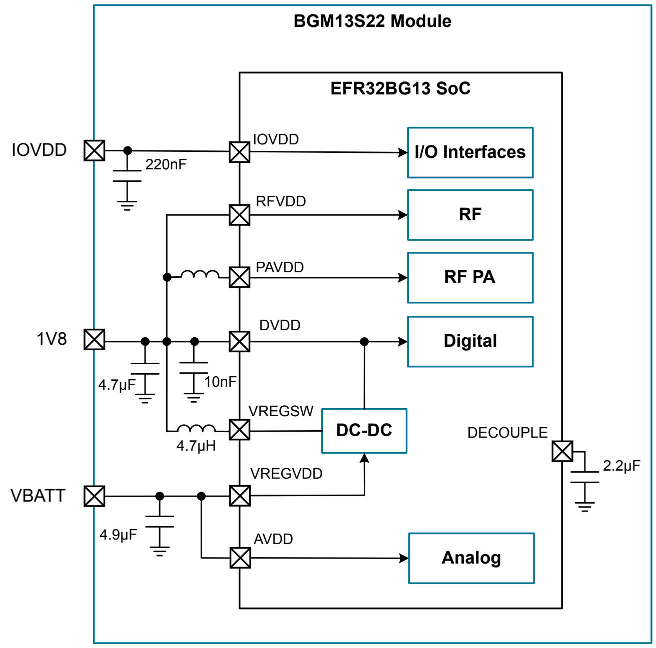


Figure 3.2. Power Supply Configuration for BGM13S22xxx Devices

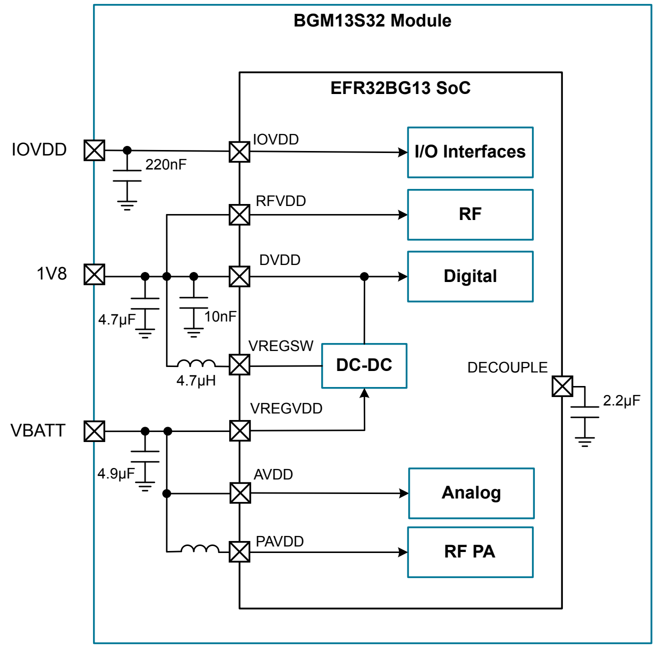


Figure 3.3. Power Supply Configuration for BGM13S32xxx Devices

3.3.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the dc-dc regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.3.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3. Patented RF noise mitigation allows operation of the DC-DC converter without degrading sensitivity of radio components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.3.3 Power Domains

The BGM13S has two peripheral power domains for operation in EM2 and EM3. If all of the peripherals in a peripheral power domain are configured as unused, the power domain for that group will be powered off in the low-power mode, reducing the overall current consumption of the device.

Table 3.2. Peripheral Power Subdomains

Peripheral Power Domain 1	Peripheral Power Domain 2
ACMP0	ACMP1
PCNT0	CSEN
ADC0	VDAC0
LETIMER0	LEUART0
LESENSE	I2C0
APORT	I2C1
-	IDAC

3.4 General Purpose Input/Output (GPIO)

BGM13S has up to 32 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.5 Clocking

3.5.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the BGM13S. Individual enabling and disabling of clocks to all peripherals is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.5.2 Internal Oscillators and Crystal

The BGM13S fully integrates two crystal oscillators, five RC oscillators, and a 38.4 MHz crystal.

- The high-frequency crystal oscillator (HFXO) and integrated 38.4 MHz crystal provide a precise timing reference for the MCU and radio.
- The low-frequency crystal oscillator (LFXO) provides an accurate timing reference for low energy modes and the real-time-clock circuits.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range.
- An integrated auxilliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire Viewer port with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) for low power operation where high accuracy is not required.
- An integrated low frequency precision 32.768 kHz RC oscillator (PLFRCO) can be used as a timing reference in low energy modes, with 500 ppm accuracy.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.6 Counters/Timers and PWM

3.6.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.6.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit WTIMER_0 only.

3.6.3 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. When receiving frames, the RTCC value can be used for timestamping. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes down to EM4H.

A secondary RTC is used by the RF protocol stack for event scheduling, leaving the primary RTCC block available exclusively for application software.

3.6.4 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.6.5 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

3.6.6 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The module may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

3.6.7 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

3.7 Communications and Other Digital Peripherals

3.7.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O interface. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I^2S

3.7.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™ provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.7.3 Inter-Integrated Circuit Interface (I^2C)

The I^2C interface enables communication between the MCU and a serial I^2C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.7.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripherals without software involvement. Peripherals producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals, which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.7.5 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface LESENSE™ is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators, ADC, and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable finite state machine which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

3.8 Security Features

3.8.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC block implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.8.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. EFR32 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2^m), SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO1 block is tightly linked to the Radio Buffer Controller (BUFC) enabling fast and efficient autonomous cipher operations on data buffer content. It allows fast processing of GCM (AES), ECC and SHA with little CPU intervention.

CRYPTO also provides trigger signals for DMA read and write operations.

3.8.3 True Random Number Generator (TRNG)

The TRNG is a non-deterministic random number generator based on a full hardware solution. The TRNG is validated with NIST800-22 and AIS-31 test suites as well as being suitable for FIPS 140-2 certification (for the purposes of cryptographic key generation).

3.8.4 Security Management Unit (SMU)

The Security Management Unit (SMU) allows software to set up fine-grained security for peripheral access, which is not possible in the Memory Protection Unit (MPU). Peripherals may be secured by hardware on an individual basis, such that only priveleged accesses to the peripheral's register interface will be allowed. When an access fault occurs, the SMU reports the specific peripheral involved and can optionally generate an interrupt.

3.9 Analog

3.9.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog peripherals on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.9.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.9.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.9.4 Capacitive Sense (CSEN)

The CSEN module is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such a switches and sliders. The CSEN module uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The module can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

3.9.5 Digital to Analog Current Converter (IDAC)

The IDAC can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The full-scale current is programmable between 0.05 µA and 64 µA with several ranges consisting of various step sizes.

3.9.6 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksps, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per single-ended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.9.7 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas, and are available down to EM3. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC module or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

3.10 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the BGM13S. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.11 Core and Memory

3.11.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4 RISC processor achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Up to 512 kB flash program memory
- Up to 64 kB RAM data memory
- Configuration and event handling of all peripherals
- 2-pin Serial-Wire debug interface

3.11.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.11.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.12 Memory Map

The BGM13S memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

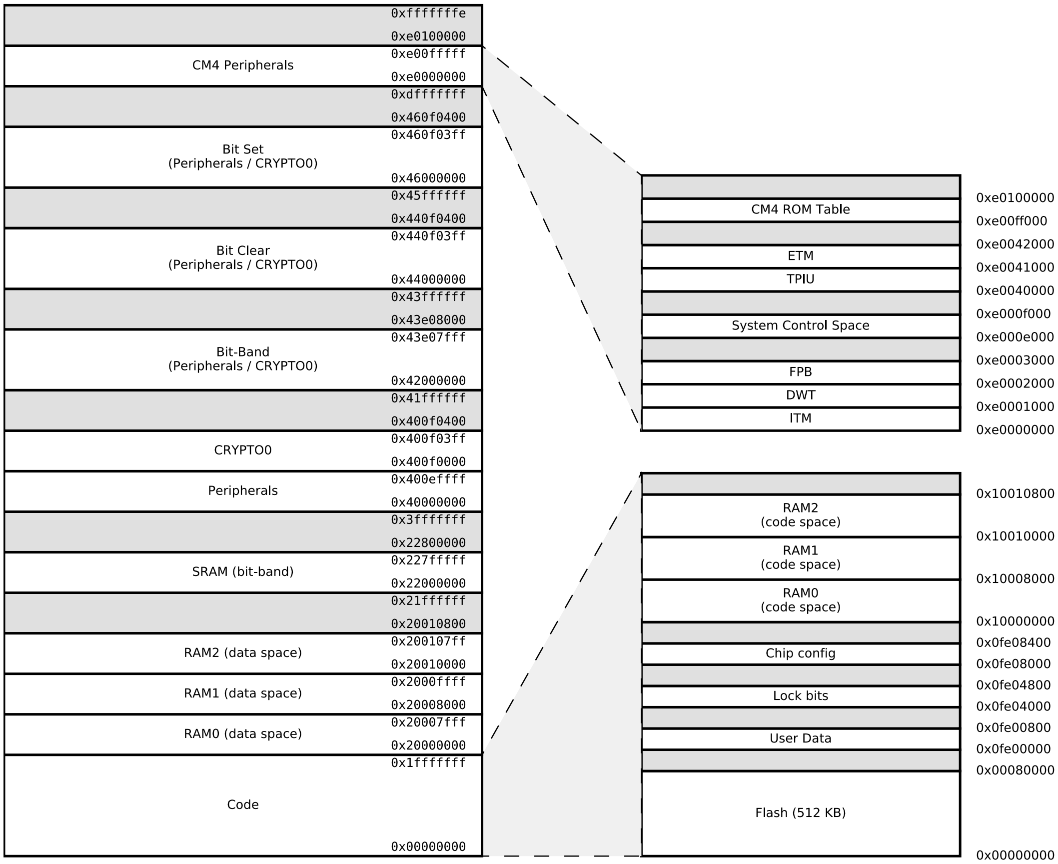


Figure 3.4. BGM13S Memory Map — Core Peripherals and Code Space

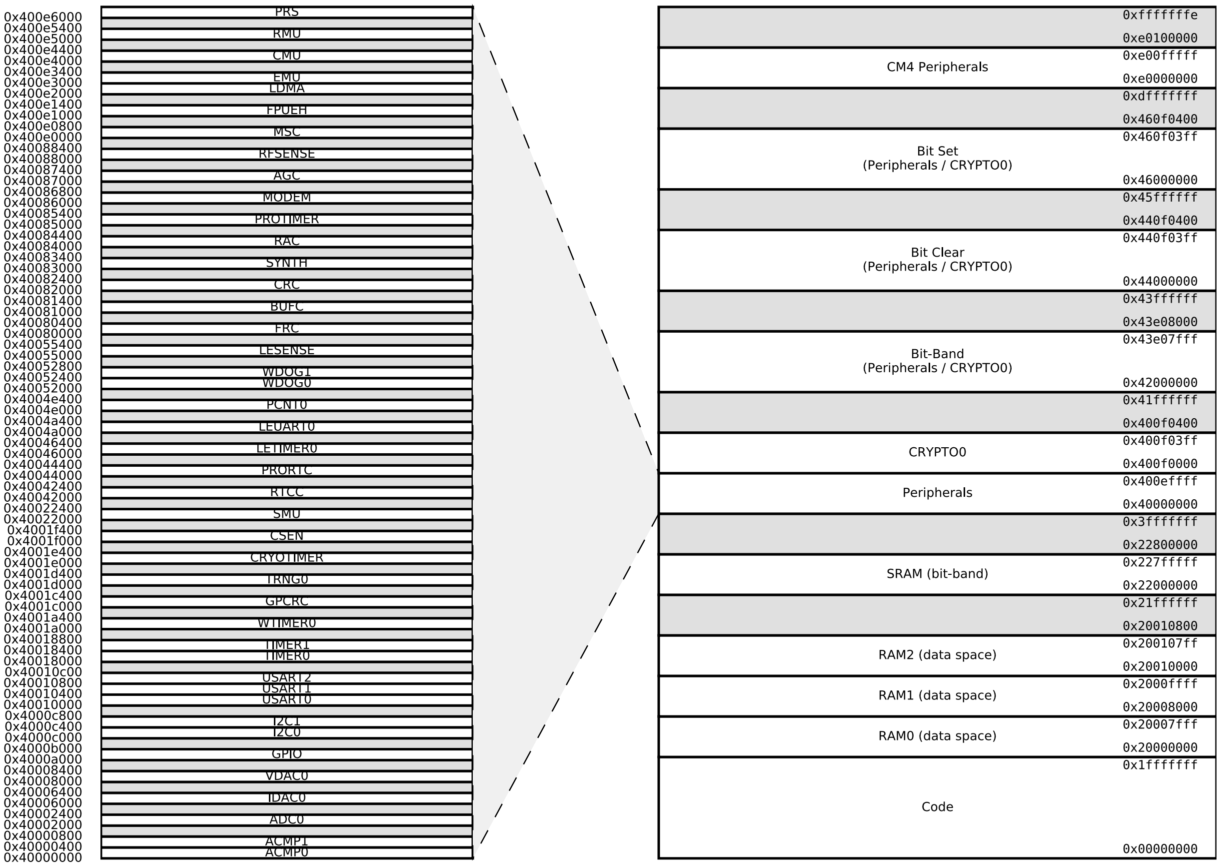


Figure 3.5. BGM13S Memory Map — Peripherals

3.13 Configuration Summary

Many peripherals on the BGM13S are available in multiple instances. However, certain USART, TIMER and WTIMER instances implement only a subset of the full features for that peripheral type. The table below describes the specific features available on these peripheral instances. All remaining peripherals support full configuration.

Table 3.3. Configuration Summary

Peripheral	Configuration	Pin Connections
USART0	IrDA SmartCard	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	IrDA I^2S SmartCard	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	IrDA SmartCard	US2_TX, US2_RX, US2_CLK, US2_CS
TIMER0	with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	-	TIM1_CC[3:0]
WTIMER0	with DTI	WTIM0_CC[2:0], WTIM0_CDTI[2:0]

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_{AMB}=25 °C and V_{DD}= 3.3 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

The BGM13S module is powered primarily from the VBATT supply pin. GPIO are powered from the IOVDD supply pin. There are also several internal supply rails mentioned in the electrical specifications, whose connections vary based on transmit power configuration. Refer to 3.3 Power for the relationship between the module's external supply pins and the internal voltage supply rails.

Refer to Table 4.2 General Operating Conditions on page 19 for more details about operational supply and temperature limits.

4.1.1 Absolute Maximum Ratings

Stress levels beyond those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions beyond those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-40	—	85	°C
Voltage on any supply pin	V_{DDMAX}		-0.3	—	3.8	V
Voltage ramp rate on any supply pin	$V_{DDRAMPMAX}$		—	—	1	V / µs
DC voltage on any GPIO pin	V_{DIGPIN}	5V tolerant GPIO pins[1 2 3]	-0.3	—	Min of 5.25 and IOVDD +2	V
		Standard GPIO pins	-0.3	—	IOVDD+0.3	V
Maximum RF level at input	$P_{RFMAX2G4}$		—	—	10	dBm
Total current into supply pins	I_{VDDMAX}	Source	—	—	200	mA
Total current into VSS ground lines	I_{VSSMAX}	Sink	—	—	200	mA
Current per I/O pin	I_{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	$I_{IOALLMAX}$	Sink	—	—	200	mA
		Source	—	—	200	mA
Junction temperature	T_J		-40	—	105	°C

Note:
1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage = IOVDD.
2. Valid for IOVDD in valid operating range or when IOVDD is undriven (high-Z). If IOVDD is connected to a low-impedance source below the valid operating range (e.g. IOVDD shorted to VSS), the pin voltage maximum is IOVDD + 0.3 V, to avoid exceeding the maximum IO current specifications.
3. To operate above the IOVDD supply rail, over-voltage tolerance must be enabled according to the GPIO_Px_OVTDIS register. Pins with over-voltage tolerance disabled have the same limits as Standard GPIO.

4.1.2 Operating Conditions

The following subsections define the operating conditions for the module.

4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range	T_A	-G temperature grade	-40	25	85	°C
VBATT operating supply voltage[1]	V_{VBATT}	DCDC in regulation	2.4	3.3	3.8	V
		DCDC in bypass 50mA load	1.8	3.3	3.8	V
VBATT current	I_{VBATT}	DCDC in bypass, T ≤ 85 °C	—	—	200	mA
HFCORECLK frequency	f_{CORE}	VSCALE2, MODE = WS1	—	—	40	MHz
		VSCALE0, MODE = WS0	—	—	20	MHz
HFCLK frequency	f_{HFCLK}	VSCALE2	—	—	40	MHz
		VSCALE0	—	—	20	MHz

Note:

1. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as $V_{VBATT\_min}+I_{LOAD} * R_{BYP\_max}$.

4.1.3 DC-DC Converter

Test conditions: V_DCDC_I=3.3 V, V_DCDC_O=1.8 V, I_DCDC_LOAD=50 mA, Heavy Drive configuration, F_DCDC_LN=7 MHz, unless otherwise indicated.

Table 4.3. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{DCDC_I}	Bypass mode, I_{DCDC_LOAD} = 50 mA	1.8	—	$V_{VREGVDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 100 mA, or Low power (LP) mode, 1.8 V output, I_{DCDC_LOAD} = 10 mA	2.4	—	$V_{VREGVDD\_MAX}$	V
Output voltage programmable range[1]	V_{DCDC_O}		1.8	—	$V_{VREGVDD}$	V
Regulation DC accuracy	ACC_{DC}	Low Noise (LN) mode, 1.8 V target output	1.7	—	1.9	V
Regulation window[2]	WIN_{REG}	Low Power (LP) mode, LPCMPBIASEMxx[3] = 0, 1.8 V target output, $I_{DCDC\_LOAD} \leq 75$ μA	1.63	—	2.2	V
		Low Power (LP) mode, LPCMPBIASEMxx[3] = 3, 1.8 V target output, $I_{DCDC\_LOAD} \leq 10$ mA	1.63	—	2.1	V
Steady-state output ripple	V_R	Radio disabled	—	3	—	mVpp
Output voltage under/overshoot	V_{OV}	CCM Mode (LNFORCECCM[3] = 1), Load changes between 0 mA and 100 mA	—	25	60	mV
		DCM Mode (LNFORCECCM[3] = 0), Load changes between 0 mA and 10 mA	—	45	90	mV
		Overshoot during LP to LN CCM/DCM mode transitions compared to DC level in LN mode	—	200	—	mV
		Undershoot during BYP/LP to LN CCM (LNFORCECCM[3] = 1) mode transitions compared to DC level in LN mode	—	40	—	mV
		Undershoot during BYP/LP to LN DCM (LNFORCECCM[3] = 0) mode transitions compared to DC level in LN mode	—	100	—	mV
DC line regulation	V_{REG}	Input changes between $V_{VREGVDD\_MAX}$ and 2.4 V	—	0.1	—	%
DC load regulation	I_{REG}	Load changes between 0 mA and 100 mA in CCM mode	—	0.1	—	%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max load current	I_{LOAD_MAX}	Low noise (LN) mode, Medium or Heavy Drive[4]	—	—	80	mA
		Low noise (LN) mode, Light Drive[4]	—	—	50	mA
		Low power (LP) mode, LPCMPBIASEMxx[3] = 0	—	—	75	µA
		Low power (LP) mode, LPCMPBIASEMxx[3] = 3	—	—	10	mA

Note:

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, $V_{VREGVDD}$.
2. LP mode controller is a hysteretic controller that maintains the output voltage within the specified limits.
3. LPCMPBIASEMxx refers to either LPCMPBIASEM234H in the EMU_DCDCMISCCTRL register or LPCMPBIASEM01 in the EMU_DCDCLOEM01CFG register, depending on the energy mode.
4. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.

4.1.4 Current Consumption

4.1.4.1 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VBATT = 3.3 V. T = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T = 25 °C.

Table 4.4. Current Consumption 3.3 V using DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise DCM mode[1]	I_{ACTIVE_DCM}	38.4 MHz crystal, CPU running while loop from flash[2]	—	87	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	69	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	70	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	82	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	76	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	615	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise CCM mode[3]	I_{ACTIVE_CCM}	38.4 MHz crystal, CPU running while loop from flash[2]	—	97	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	80	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	81	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	92	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	94	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1145	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise CCM mode[3]	$I_{ACTIVE\_CCM\_VS}$	19 MHz HFRCO, CPU running while loop from flash	—	101	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1124	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Noise DCM mode[1]	I_{EM1_DCM}	38.4 MHz crystal[2]	—	56	—	µA/MHz
		38 MHz HFRCO	—	39	—	µA/MHz
		26 MHz HFRCO	—	46	—	µA/MHz
		1 MHz HFRCO	—	588	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise DCM mode[1]	$I_{EM1\_DCM\_VS}$	19 MHz HFRCO	—	50	—	µA/MHz
		1 MHz HFRCO	—	572	—	µA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, with voltage scaling enabled, DCDC in LP mode[4]	I_{EM2_VS}	Full 64 kB RAM retention and RTCC running from LFXO	—	1.4	—	μA
		Full 64 kB RAM retention and RTCC running from LFRCO	—	1.5	—	μA
		1 bank RAM retention and RTCC running from LFRCO[5]	—	1.3	—	μA
Current consumption in EM3 mode, with voltage scaling enabled	I_{EM3_VS}	Full 64 kB RAM retention and CRYOTIMER running from ULFRCO	—	1.14	—	μA
Current consumption in EM4H mode, with voltage scaling enabled	I_{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	0.75	—	μA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.44	—	μA
		128 byte RAM retention, no RTCC	—	0.42	—	μA
Current consumption in EM4S mode	I_{EM4S}	No RAM retention, no RTCC	—	0.07	—	μA

Note:

1. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD.
2. CMU_HFXOCTRL_LOWPOWER=0.
3. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD.
4. DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPCMPBIASEM234H=0, LPCLIMILIMSEL=1, ANASW=DVDD.
5. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

4.1.4.2 Current Consumption 1.8 V (DC-DC Converter in Bypass Mode)

Unless otherwise indicated, typical conditions are: VBATT = 1.8 V. T = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T = 25 °C.

Table 4.5. Current Consumption 1.8 V (DC-DC Converter in Bypass Mode)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash[1]	—	128	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	97	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	98	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	119	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	100	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	243	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled	I_{ACTIVE_VS}	19 MHz HFRCO, CPU running while loop from flash	—	86	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	206	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	38.4 MHz crystal[1]	—	76	—	µA/MHz
		38 MHz HFRCO	—	47	—	µA/MHz
		26 MHz HFRCO	—	48	—	µA/MHz
		1 MHz HFRCO	—	191	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled	I_{EM1_VS}	19 MHz HFRCO	—	43	—	µA/MHz
		1 MHz HFRCO	—	163	—	µA/MHz
Current consumption in EM2 mode, with voltage scaling enabled	I_{EM2_VS}	Full 64 kB RAM retention and RTCC running from LFXO	—	1.8	—	µA
		Full 64 kB RAM retention and RTCC running from LFRCO	—	2.0	—	µA
		1 bank (16 kB) RAM retention and RTCC running from LFRCO[2]	—	1.6	—	µA
Current consumption in EM3 mode, with voltage scaling enabled	I_{EM3_VS}	Full 64 kB RAM retention and CRYOTIMER running from ULFRCO	—	1.43	—	µA
Current consumption in EM4H mode, with voltage scaling enabled	I_{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	0.83	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.37	—	µA
		128 byte RAM retention, no RTCC	—	0.36	—	µA
Current consumption in EM4S mode	I_{EM4S}	no RAM retention, no RTCC	—	0.05	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:
1. CMU_HFXOCTRL_LOWPOWER=0.
2. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

4.1.4.3 Current Consumption 3.3 V (DC-DC Converter in Bypass Mode)

Unless otherwise indicated, typical conditions are: VBATT = 3.3 V. T = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T = 25 °C.

Table 4.6. Current Consumption 3.3 V (DC-DC Converter in Bypass Mode)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash[1]	—	128	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	97	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	98	107	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	119	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	100	109	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	246	430	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled	I_{ACTIVE_VS}	19 MHz HFRCO, CPU running while loop from flash	—	86	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	209	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	38.4 MHz crystal[1]	—	76	—	µA/MHz
		38 MHz HFRCO	—	47	51	µA/MHz
		26 MHz HFRCO	—	49	55	µA/MHz
		1 MHz HFRCO	—	195	374	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled	I_{EM1_VS}	19 MHz HFRCO	—	43	—	µA/MHz
		1 MHz HFRCO	—	167	—	µA/MHz
Current consumption in EM2 mode, with voltage scaling enabled	I_{EM2_VS}	Full 64 kB RAM retention and RTCC running from LFXO	—	1.9	—	µA
		Full 64 kB RAM retention and RTCC running from LFRCO	—	2.2	—	µA
		1 bank (16 kB) RAM retention and RTCC running from LFRCO[2]	—	1.9	3.3	µA
Current consumption in EM3 mode, with voltage scaling enabled	I_{EM3_VS}	Full 64 kB RAM retention and CRYOTIMER running from ULFRCO	—	1.53	3.0	µA
Current consumption in EM4H mode, with voltage scaling enabled	I_{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	0.93	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.45	—	µA
		128 byte RAM retention, no RTCC	—	0.44	0.9	µA
Current consumption in EM4S mode	I_{EM4S}	No RAM retention, no RTCC	—	0.04	0.18	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: 1. CMU_HFXOCTRL_LOWPOWER=0. 2. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1						

4.1.4.4 Current Consumption Using Radio

Unless otherwise indicated, typical conditions are: VBATT = 3.3 V. T = 25 °C. DC-DC on. Minimum and maximum values in this table represent the worst conditions across process variation at T = 25 °C.

Table 4.7. Current Consumption Using Radio

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled), T ≤ 85 °C	I_{RX_ACTIVE}	125 kbit/s, 2GFSK, F = 2.4 GHz, Radio clock prescaled by 4	—	9.4	—	mA
		500 kbit/s, 2GFSK, F = 2.4 GHz, Radio clock prescaled by 4	—	9.4	—	mA
		1 Mbit/s, 2GFSK, F = 2.4 GHz, Radio clock prescaled by 4	—	9.7	—	mA
		2 Mbit/s, 2GFSK, F = 2.4 GHz, Radio clock prescaled by 4	—	10.5	—	mA
Current consumption in receive mode, listening for packet (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled), T ≤ 85 °C	I_{RX_LISTEN}	125 kbit/s, 2GFSK, F = 2.4 GHz, No radio clock prescaling	—	10.4	—	mA
		500 kbit/s, 2GFSK, F = 2.4 GHz, No radio clock prescaling	—	10.4	—	mA
		1 Mbit/s, 2GFSK, F = 2.4 GHz, No radio clock prescaling	—	10.7	—	mA
		2 Mbit/s, 2GFSK, F = 2.4 GHz, No radio clock prescaling	—	11.5	—	mA
Current consumption in transmit mode (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled), T ≤ 85 °C	I_{TX}	F = 2.4 GHz, CW, 0 dBm output power, Radio clock prescaled by 3	—	8.9	—	mA
		F = 2.4 GHz, CW, 0 dBm output power, Radio clock prescaled by 1	—	9.7	—	mA
		F = 2.4 GHz, CW, 8 dBm output power	—	27.4	—	mA
		F = 2.4 GHz, CW, 18 dBm output power, PAVDD connected directly to external 3.3V supply	—	122.7	—	mA

4.1.5 Wake Up Times

Table 4.8. Wake Up Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wake up time from EM1	t_{EM1_WU}		—	3	—	AHB Clocks
Wake up from EM2	t_{EM2_WU}	Code execution from flash	—	10.9	—	μs
		Code execution from RAM	—	3.8	—	μs
Wake up from EM3	t_{EM3_WU}	Code execution from flash	—	10.9	—	μs
		Code execution from RAM	—	3.8	—	μs
Wake up from EM4H[1]	t_{EM4H_WU}	Executing from flash	—	90	—	μs
Wake up from EM4S[1]	t_{EM4S_WU}	Executing from flash	—	300	—	μs
Time from release of reset source to first instruction execution	t_{RESET}	Soft Pin Reset released	—	51	—	μs
		Any other reset released	—	358	—	μs
Power mode scaling time	t_{SCALE}	VSCALE0 to VSCALE2, HFCLK = 19 MHz[2] [3]	—	31.8	—	μs
		VSCALE2 to VSCALE0, HFCLK = 19 MHz[4]	—	4.3	—	μs

Note:
1. Time from wake up request until first instruction is executed. Wakeup results in device reset.
2. Scaling up from VSCALE0 to VSCALE2 requires approximately 30.3 μs + 28 HFCLKs.
3. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV/μs for approximately 20 μs. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 μF capacitor) to 70 mA (with a 2.7 μF capacitor).
4. Scaling down from VSCALE2 to VSCALE0 requires approximately 2.8 μs + 29 HFCLKs.

4.1.6 Brown Out Detector (BOD)

Table 4.9. Brown Out Detector (BOD)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AVDD BOD threshold	$V_{AVDDBOD}$	AVDD rising	—	—	1.8	V
		AVDD falling (EM0/EM1)	1.62	—	—	V
		AVDD falling (EM2/EM3)	1.53	—	—	V
AVDD BOD hysteresis	$V_{AVDDBOD\_HYST}$		—	20	—	mV
AVDD BOD response time	$t_{AVDDBOD\_DELAY}$	Supply drops at 0.1V/μs rate	—	2.4	—	μs
EM4 BOD threshold	$V_{EM4DBOD}$	AVDD rising	—	—	1.7	V
		AVDD falling	1.45	—	—	V
EM4 BOD hysteresis	V_{EM4BOD_HYST}		—	25	—	mV
EM4 BOD response time	t_{EM4BOD_DELAY}	Supply drops at 0.1V/μs rate	—	300	—	μs

4.1.7 Frequency Synthesizer

Table 4.10. Frequency Synthesizer

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF synthesizer frequency range	f_{RANGE}	2400 - 2483.5 MHz	2400	—	2483.5	MHz
LO tuning frequency resolution with 38.4 MHz crystal	f_{RES}	2400 - 2483.5 MHz	—	—	73	Hz
Frequency deviation resolution with 38.4 MHz crystal	df_{RES}	2400 - 2483.5 MHz	—	—	73	Hz
Maximum frequency deviation with 38.4 MHz crystal	df_{MAX}	2400 - 2483.5 MHz	—	—	1677	kHz

4.1.8 2.4 GHz RF Transceiver Characteristics

4.1.8.1 RF Transmitter General Characteristics for 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VBATT = 3.3 V. DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

Table 4.11. RF Transmitter General Characteristics for 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum TX power[1]	$POUT_{MAX}$	18 dBm-rated part numbers.	—	17.9	—	dBm
		8 dBm-rated part numbers	—	7.8	—	dBm
Minimum active TX Power	$POUT_{MIN}$	CW		-30	—	dBm
Output power step size	$POUT_{STEP}$	-5 dBm< Output power < 0 dBm	—	1	—	dB
		0 dBm < output power < $POUT_{MAX}$	—	0.5	—	dB
Output power variation vs supply at $POUT_{MAX}$	$POUT_{VAR\_V}$	1.8 V < $V_{VREGVDD}$ < 3.3 V, PAVDD connected directly to external supply, for output power > 10 dBm.	—	4.5	—	dB
		1.8 V < $V_{VREGVDD}$ < 3.3 V using DC-DC converter	—	2.1	—	dB
Output power variation vs temperature at $POUT_{MAX}$	$POUT_{VAR\_T}$	From -40 to +85 °C, PAVDD connected to DC-DC output	—	1.7	—	dB
		From -40 to +85 °C, PAVDD connected to external supply	—	1.7	—	dB
Output power variation vs RF frequency at $POUT_{MAX}$	$POUT_{VAR\_F}$	Over RF tuning frequency range, PAVDD connected to external supply	—	0.3	—	dB
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.

4.1.8.2 RF Receiver General Characteristics for 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VBATT = 3.3 V. DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

Table 4.12. RF Receiver General Characteristics for 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz
Receive mode maximum spurious emission	$SPUR_{RX}$	30 MHz to 1 GHz	—	-57	—	dBm
		1 GHz to 12 GHz	—	-47	—	dBm
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	$SPUR_{RX\_FCC}$	216 MHz to 960 MHz, Conducted Measurement	—	-55.2	—	dBm
		Above 960 MHz, Conducted Measurement	—	-47.2	—	dBm
Level above which RFSENSE will trigger[1]	$RFSENSE_{TRIG}$	CW at 2.45 GHz	—	-24	—	dBm
Level below which RFSENSE will not trigger[1]	$RFSENSE_{THRES}$	CW at 2.45 GHz	—	-50	—	dBm

Note:

1. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range.

4.1.8.3 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 125 kbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VBATT = 3.3 V. DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

Table 4.13. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power spectral density limit	PSD_{LIMIT}	Per FCC part 15.247 at 10 dBm	—	—	8	dBm/3kHz
		Per FCC part 15.247 at 20 dBm[1]	—	—	8	dBm/3kHz
Spurious emissions out-of-band, excluding harmonics captured in $SPUR_{HARM,FCC}$. Emissions taken at $POUT_{MAX}$, PAVDD connected to external 3.3 V supply	$SPUR_{OOB\_FCC}$	Per FCC part 15.205/15.209, Above 2.483 GHz or below 2.4 GHz; continuous transmission of CW carrier, Restricted Bands[2 3]	—	-47	—	dBm

Note:

1. Output power limited to 14 dBm to ensure compliance with FCC specifications.
2. For 2476 MHz, 1.2 dB of power backoff is used to achieve this value.
3. For 2478 MHz, 5.8 dB of power backoff is used to achieve this value.

4.1.8.4 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 125 kbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VBATT = 3.3 V. DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

Table 4.14. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level, 0.1% BER	SAT	Signal is reference signal[1]. Packet length is 20 bytes.	—	10	—	dBm
Sensitivity, 0.1% BER	SENS	Signal is reference signal[1]. Using DC-DC converter.	—	-102.1	—	dBm
		With non-ideal signals as specified in RF-PHY.TS.4.2.2, section 4.6.1.	—	-101.8	—	dBm
N+1 adjacent channel selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -79 dBm	C/I_{1+}	Interferer is reference signal at +1 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	-14.0	—	dB
N-1 adjacent channel selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -79 dBm	C/I_{1-}	Interferer is reference signal at -1 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	-13.6	—	dB
Selectivity to image frequency, 0.1% BER. Desired is reference signal at -79 dBm	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision	—	-51.6	—	dB
Selectivity to image frequency ± 1 MHz, 0.1% BER. Desired is reference signal at -79 dBm	C/I_{IM+1}	Interferer is reference signal at image frequency ± 1 MHz with 1 MHz precision	—	-55.5	—	dB

Note:

1. Reference signal is defined 2GFSK at -79 dBm, Modulation index = 0.5, BT = 0.5, Bit rate = 125 kbps, desired data = PRBS9; interferer data = PRBS15; frequency accuracy better than 1 ppm.

4.1.8.5 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 500 kbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VBATT = 3.3 V. DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

Table 4.15. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power spectral density limit	PSD_{LIMIT}	Per FCC part 15.247 at 10 dBm	—	-9.8	—	dBm/ 3kHz
		Per FCC part 15.247 at 20 dBm[1]	—	—	8	dBm/ 3kHz
Spurious emissions out-of-band, excluding harmonics captured in $SPUR_{HARM,FCC}$. Emissions taken at $POUT_{MAX}$, PAVDD connected to external 3.3 V supply	$SPUR_{OOB\_FCC}$	Per FCC part 15.205/15.209, Above 2.483 GHz or below 2.4 GHz; continuous transmission of CW carrier, Restricted Bands[2] [3]	—	-47	—	dBm

Note:

1. Output power limited to 14 dBm to ensure compliance with FCC specifications.
2. For 2476 MHz, 1.2 dB of power backoff is used to achieve this value.
3. For 2478 MHz, 5.8 dB of power backoff is used to achieve this value.

4.1.8.6 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 500 kbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VBATT = 3.3 V. DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

Table 4.16. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level, 0.1% BER	SAT	Signal is reference signal[1]. Packet length is 20 bytes.	—	10	—	dBm
Sensitivity, 0.1% BER	SENS	Signal is reference signal[1]. Using DC-DC converter.	—	-97.9	—	dBm
		With non-ideal signals as specified in RF-PHY.TS.4.2.2, section 4.6.1.	—	-97.0	—	dBm
N+1 adjacent channel selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -72 dBm	C/I_{1+}	Interferer is reference signal at +1 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	-9.2	—	dB
N-1 adjacent channel selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -72 dBm	C/I_{1-}	Interferer is reference signal at -1 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	-9.0	—	dB
Alternate selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -72 dBm	C/I_2	Interferer is reference signal at ± 2 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	-46.5	—	dB
Selectivity to image frequency, 0.1% BER. Desired is reference signal at -72 dBm	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision	—	-46.5	—	dB
Selectivity to image frequency ± 1 MHz, 0.1% BER. Desired is reference signal at -72 dBm	C/I_{IM+1}	Interferer is reference signal at image frequency ± 1 MHz with 1 MHz precision	—	-50.7	—	dB

Note:

1. Reference signal is defined 2GFSK at -72 dBm, Modulation index = 0.5, BT = 0.5, Bit rate = 500 kbps, desired data = PRBS9; interferer data = PRBS15; frequency accuracy better than 1 ppm.

4.1.8.7 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VBATT = 3.3 V. DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

Table 4.17. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
In-band spurious emissions, with allowed exceptions[1]	$SPUR_{INB}$	At ± 2 MHz, 10 dBm	—	-39.7	—	dBm
		At ± 3 MHz, 10 dBm	—	-43.6	—	dBm
		At ± 2 MHz, 20 dBm	—	—	-20	dBm
		At ± 3 MHz, 20 dBm	—	—	-30	dBm
Spurious emissions out-of-band, excluding harmonics captured in $SPUR_{HARM,FCC}$. Emissions taken at $POUT_{MAX}$, PAVDD connected to external 3.3 V supply	$SPUR_{OOB\_FCC}$	Per FCC part 15.205/15.209, Above 2.483 GHz or below 2.4 GHz; continuous transmission of CW carrier, Restricted Bands[2] [3]	—	-47	—	dBm

Note:

1. Per Bluetooth Core_5.0, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.
2. For 2476 MHz, 1.5 dB of power backoff is used to achieve this value.
3. For 2478 MHz, 4.2 dB of power backoff is used to achieve this value.

4.1.8.8 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VBATT = 3.3 V. DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

Table 4.18. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level, 0.1% BER	SAT	Signal is reference signal[1]. Packet length is 20 bytes.	—	10	—	dBm
Sensitivity, 0.1% BER	SENS	Signal is reference signal[1]. Using DC-DC converter.	—	-94.1	—	dBm
		With non-ideal signals as specified in RF-PHY.TS.4.2.2, section 4.6.1.	—	-93.8	—	dBm
Signal to co-channel interferer, 0.1% BER	C/I_{CC}	Desired signal 3 dB above reference sensitivity.	—	9.0	—	dB
N+1 adjacent channel selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I_{1+}	Interferer is reference signal at +1 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	-3.3	—	dB
N-1 adjacent channel selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I_{1-}	Interferer is reference signal at -1 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	-1.6	—	dB
Alternate selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I_2	Interferer is reference signal at ± 2 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	-42.0	—	dB
Alternate selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I_3	Interferer is reference signal at ± 3 MHz offset. Desired frequency 2404 MHz ≤ Fc ≤ 2480 MHz	—	-46.4	—	dB
Selectivity to image frequency, 0.1% BER. Desired is reference signal at -67 dBm	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision	—	-42.0	—	dB
Selectivity to image frequency ± 1 MHz, 0.1% BER. Desired is reference signal at -67 dBm	C/I_{IM+1}	Interferer is reference signal at image frequency ± 1 MHz with 1 MHz precision	—	-47.1	—	dB
Intermodulation performance	IM	Per Core_4.1, Vol 6, Part A, Section 4.4 with n = 3	—	-18.4	—	dBm

Note:

1. Reference signal is defined 2GFSK at -67 dBm, Modulation index = 0.5, BT = 0.5, Bit rate = 1 Mbps, desired data = PRBS9; interferer data = PRBS15; frequency accuracy better than 1 ppm.

4.1.8.9 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VBATT = 3.3 V. DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

Table 4.19. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
In-band spurious emissions, with allowed exceptions[1]	$SPUR_{INB}$	At ± 4 MHz, 10 dBm	—	-38.2	—	dBm
		At ± 6 MHz, 10 dBm	—	-41.1	—	dBm
		At ± 4 MHz, 20 dBm	—	-30.1	—	dBm
		At ± 6 MHz, 20 dBm	—	-31.4	—	dBm
Spurious emissions out-of-band, excluding harmonics captured in $SPUR_{HARM,FCC}$. Emissions taken at $POUT_{MAX}$, PAVDD connected to external 3.3 V supply	$SPUR_{OOB\_FCC}$	Per FCC part 15.205/15.209, Above 2.483 GHz or below 2.4 GHz; continuous transmission of CW carrier, Restricted Bands[2 3 4 5]	—	-47	—	dBm

Note:

1. Per Bluetooth Core_5.0, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.
2. For 2472 MHz, 1.3 dB of power backoff is used to achieve this value.
3. For 2474 MHz, 3.8 dB of power backoff is used to achieve this value.
4. For 2476 MHz, 7 dB of power backoff is used to achieve this value.
5. For 2478 MHz, 11.2 dB of power backoff is used to achieve this value.

4.1.8.10 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VBATT = 3.3 V. DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

Table 4.20. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level, 0.1% BER	SAT	Signal is reference signal[1]. Packet length is 20 bytes.	—	10	—	dBm
Sensitivity, 0.1% BER	SENS	Signal is reference signal[1]. Using DC-DC converter.	—	-90.2	—	dBm
		With non-ideal signals as specified in RF-PHY.TS.4.2.2, section 4.6.1.	—	-89.9	—	dBm
Signal to co-channel interferer, 0.1% BER	C/I_{CC}	Desired signal 3 dB above reference sensitivity.	—	8.6	—	dB
N+1 adjacent channel selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I_{1+}	Interferer is reference signal at +2 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	-7.6	—	dB
N-1 adjacent channel selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I_{1-}	Interferer is reference signal at -2 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	-11.4	—	dB
Alternate selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I_2	Interferer is reference signal at ± 4 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	-40.3	—	dB
Alternate selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I_3	Interferer is reference signal at ± 6 MHz offset. Desired frequency 2404 MHz ≤ Fc ≤ 2480 MHz	—	-45.1	—	dB
Selectivity to image frequency, 0.1% BER. Desired is reference signal at -67 dBm	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision	—	-7.6	—	dB
Selectivity to image frequency ± 2 MHz, 0.1% BER. Desired is reference signal at -67 dBm	C/I_{IM+1}	Interferer is reference signal at image frequency ± 2 MHz with 2 MHz precision	—	-40.30	—	dB
Intermodulation performance	IM	Per Core_4.1, Vol 6, Part A, Section 4.4 with n = 3	—	-18.4	—	dBm

Note:

1. Reference signal is defined 2GFSK at -67 dBm, Modulation index = 0.5, BT = 0.5, Bit rate = 2 Mbps, desired data = PRBS9; interferer data = PRBS15; frequency accuracy better than 1 ppm.

4.1.9 Oscillators

4.1.9.1 Low-Frequency Crystal Oscillator (LFXO)

Table 4.21. Low-Frequency Crystal Oscillator (LFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{LFXO}		—	32.768	—	kHz
Supported crystal equivalent series resistance (ESR)	ESR_{LFXO}		—	—	70	kΩ
Supported range of crystal load capacitance [1]	C_{LFXO_CL}		6	—	18	pF
On-chip tuning cap range [2]	C_{LFXO_T}	On each of LFXTAL_N and LFXTAL_P pins	8	—	40	pF
On-chip tuning cap step size	SS_{LFXO}		—	0.25	—	pF
Current consumption after startup [3]	I_{LFXO}	ESR = 70 kOhm, C_L = 7 pF, GAIN[4] = 2, AGC[4] = 1	—	273	—	nA
Start- up time	t_{LFXO}	ESR = 70 kOhm, C_L = 7 pF, GAIN[4] = 2	—	308	—	ms

Note:
1. Total load capacitance as seen by the crystal.
2. The effective load capacitance seen by the crystal will be C_{LFXO_T} /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.
3. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
4. In CMU_LFXOCTRL register.

4.1.9.2 High-Frequency Crystal Oscillator (HFXO)

Table 4.22. High-Frequency Crystal Oscillator (HFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{HFXO}	38.4 MHz required for radio trans-ciever operation	—	38.4	—	MHz
Frequency tolerance for the crystal	FT_{HFXO}		-40	—	40	ppm

4.1.9.3 Low-Frequency RC Oscillator (LFRCO)

Table 4.23. Low-Frequency RC Oscillator (LFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{LFRCO}	ENVREF[1] = 1	31.3	32.768	33.6	kHz
		ENVREF[1] = 0	31.3	32.768	33.4	kHz
Startup time	t_{LFRCO}		—	500	—	µs
Current consumption [2]	I_{LFRCO}	ENVREF = 1 in CMU_LFRCOCTRL	—	342	—	nA
		ENVREF = 0 in CMU_LFRCOCTRL	—	494	—	nA

Note:
1. In CMU_LFRCOCTRL register.
2. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.

4.1.9.4 Precision Low-Frequency RC Oscillator (PLFRCO)

Table 4.24. Precision Low-Frequency RC Oscillator (PLFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{PLFRCO}		—	32.768	—	kHz
Frequency accuracy	f_{PLFRCO_ACC}	Across operating temperature range	-500	—	+500	ppm
Startup time	t_{PLFRCO}		—	64.2	—	ms
Current consumption	I_{PLFRCO}	3.3 V supply, T = 25 °C, recalibration every 2 minutes	—	854	—	nA

4.1.9.5 High-Frequency RC Oscillator (HFRCO)

Table 4.25. High-Frequency RC Oscillator (HFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	f_{HFRCO_ACC}	At production calibrated frequencies, across supply voltage and temperature	-2.5	—	2.5	%
Start-up time	t_{HFRCO}	f_{HFRCO} ≥ 19 MHz	—	300	—	ns
		4 < f_{HFRCO} < 19 MHz	—	1	—	µs
		f_{HFRCO} ≤ 4 MHz	—	2.5	—	µs
Current consumption on all supplies	I_{HFRCO}	f_{HFRCO} = 38 MHz	—	267	299	µA
		f_{HFRCO} = 32 MHz	—	224	248	µA
		f_{HFRCO} = 26 MHz	—	189	211	µA
		f_{HFRCO} = 19 MHz	—	154	172	µA
		f_{HFRCO} = 16 MHz	—	133	148	µA
		f_{HFRCO} = 13 MHz	—	118	135	µA
		f_{HFRCO} = 7 MHz	—	89	100	µA
		f_{HFRCO} = 4 MHz	—	34	44	µA
		f_{HFRCO} = 2 MHz	—	29	40	µA
		f_{HFRCO} = 1 MHz	—	26	36	µA
Coarse trim step size (% of period)	SS_{HFRCO_COARSE}		—	0.8	—	%
Fine trim step size (% of period)	SS_{HFRCO_FINE}		—	0.1	—	%
Period jitter	PJ_{HFRCO}		—	0.2	—	% RMS
Frequency limits	f_{HFRCO_BAND}	FREQRANGE = 0, FINETUNINGEN = 0	3.47	—	6.15	MHz
		FREQRANGE = 3, FINETUNINGEN = 0	6.24	—	11.45	MHz
		FREQRANGE = 6, FINETUNINGEN = 0	11.3	—	19.8	MHz
		FREQRANGE = 7, FINETUNINGEN = 0	13.45	—	22.8	MHz
		FREQRANGE = 8, FINETUNINGEN = 0	16.5	—	29.0	MHz
		FREQRANGE = 10, FINETUNINGEN = 0	23.11	—	40.63	MHz
		FREQRANGE = 11, FINETUNINGEN = 0	27.27	—	48	MHz
		FREQRANGE = 12, FINETUNINGEN = 0	33.33	—	54	MHz

4.1.9.6 Ultra-low Frequency RC Oscillator (ULFRCO)

Table 4.26. Ultra-low Frequency RC Oscillator (ULFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{ULFRCO}		0.95	1	1.07	kHz

4.1.10 Flash Memory Characteristics[1]

Table 4.27. Flash Memory Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC_{FLASH}		10000	—	—	cycles
Flash data retention	RET_{FLASH}		10	—	—	years
Word (32-bit) programming time	t_{W_PROG}	Burst write, 128 words, average time per word	20	26.3	30	µs
		Single word	62	68.9	80	µs
Page erase time[2]	t_{PERASE}		20	29.5	40	ms
Mass erase time[3]	t_{MERASE}		20	30	40	ms
Device erase time[4] [5]	t_{DERASE}		—	56.2	70	ms
Erase current[6]	I_{ERASE}	Page Erase	—	—	2.0	mA
Write current[6]	I_{WRITE}		—	—	3.5	mA
Supply voltage during flash erase and write	V_{FLASH}		1.62	—	3.6	V

Note:

1. Flash data retention information is published in the Quarterly Quality and Reliability Report.
2. From setting the ERASEPAGE bit in MSC_WRITECMD to 1 until the BUSY bit in MSC_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
3. Mass erase is issued by the CPU and erases all flash.
4. Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW).
5. From setting the DEVICEERASE bit in AAP_CMD to 1 until the ERASEBUSY bit in AAP_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
6. Measured at 25 °C.

4.1.11 General-Purpose I/O (GPIO)

Table 4.28. General-Purpose I/O (GPIO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IL}	GPIO pins	—	—	IOVDD*0.3	V
Input high voltage	V_{IH}	GPIO pins	IOVDD*0.7	—	—	V
Output high voltage relative to IOVDD	V_{OH}	Sourcing 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.8	—	—	V
		Sourcing 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.6	—	—	V
		Sourcing 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.8	—	—	V
		Sourcing 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.6	—	—	V
Output low voltage relative to IOVDD	V_{OL}	Sinking 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK	—	—	IOVDD*0.2	V
		Sinking 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	—	—	IOVDD*0.4	V
		Sinking 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG	—	—	IOVDD*0.2	V
		Sinking 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	—	—	IOVDD*0.4	V
Input leakage current	I_{IOLEAK}	All GPIO except LFXO pins, GPIO ≤ IOVDD	—	0.1	30	nA
		LFXO Pins, GPIO ≤ IOVDD	—	0.1	50	nA
Input leakage current on 5VTOL pads above IOVDD	$I_{5VTOLLEAK}$	IOVDD < GPIO ≤ IOVDD + 2 V	—	3.3	15	µA
I/O pin pull-up/pull-down resistor	R_{PUD}		30	40	65	kΩ
Pulse width of pulses removed by the glitch suppression filter	$t_{IOGLITCH}$		15	25	45	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output fall time, From 70% to 30% of V_{IO}	t_{IOOF}	C_L = 50 pF, DRIVESTRENGTH[1] = STRONG, SLEWRATE[1] = 0x6	—	1.8	—	ns
		C_L = 50 pF, DRIVESTRENGTH[1] = WEAK, SLEWRATE[1] = 0x6	—	4.5	—	ns
Output rise time, From 30% to 70% of V_{IO}	t_{IOOR}	C_L = 50 pF, DRIVESTRENGTH[1] = STRONG, SLEWRATE = 0x6[1]	—	2.2	—	ns
		C_L = 50 pF, DRIVESTRENGTH[1] = WEAK, SLEWRATE[1] = 0x6	—	7.4	—	ns

Note:
1. In GPIO_Pn_CTRL register.

4.1.12 Voltage Monitor (VMON)

Table 4.29. Voltage Monitor (VMON)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current (including I_SENSE)	I_{VMON}	In EM0 or EM1, 1 active channel	—	6.3	8	μA
		In EM0 or EM1, All channels active	—	12.5	15	μA
		In EM2, EM3 or EM4, 1 channel active and above threshold	—	62	—	nA
		In EM2, EM3 or EM4, 1 channel active and below threshold	—	62	—	nA
		In EM2, EM3 or EM4, All channels active and above threshold	—	99	—	nA
		In EM2, EM3 or EM4, All channels active and below threshold	—	99	—	nA
Loading of monitored supply	I_{SENSE}	In EM0 or EM1	—	2	—	μA
		In EM2, EM3 or EM4	—	2	—	nA
Threshold range	V_{VMON_RANGE}		1.62	—	3.4	V
Threshold step size	N_{VMON_STESP}	Coarse	—	200	—	mV
		Fine	—	20	—	mV
Response time	t_{VMON_RES}	Supply drops at 1V/μs rate	—	460	—	ns
Hysteresis	V_{VMON_HYST}		—	26	—	mV

4.1.13 Analog to Digital Converter (ADC)

Specified at 1 Msps, ADCCLK = 16 MHz, BIASPROG = 0, GPBIASACC = 0, unless otherwise indicated.

Table 4.30. Analog to Digital Converter (ADC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	$V_{RESOLUTION}$		6	—	12	Bits
Input voltage range[1]	V_{ADCIN}	Single ended	—	—	V_{FS}	V
		Differential	$-V_{FS}/2$	—	$V_{FS}/2$	V
Input range of external reference voltage, single ended and differential	$V_{ADCREFIN\_P}$		1	—	V_{AVDD}	V
Power supply rejection[2]	$PSRR_{ADC}$	At DC	—	80	—	dB
Analog input common mode rejection ratio	$CMRR_{ADC}$	At DC	—	80	—	dB
Current from all supplies, using internal reference buffer. Continuous operation. WARMUPMODE[3] = KEEPADCWARM	$I_{ADC\_CONTINUOUS\_LP}$	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [4]	—	270	290	µA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 1 [4]	—	125	—	µA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 1 [4]	—	80	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[3] = NORMAL	$I_{ADC\_NORMAL\_LP}$	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [4]	—	45	—	µA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 1 [4]	—	8	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[3] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADC\_STANDBY\_LP}$	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [4]	—	105	—	µA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [4]	—	70	—	µA
Current from all supplies, using internal reference buffer. Continuous operation. WARMUPMODE[3] = KEEPADCWARM	$I_{ADC\_CONTINUOUS\_HP}$	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [4]	—	325	—	µA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 0 [4]	—	175	—	µA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 0 [4]	—	125	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[3] = NORMAL	$I_{ADC\_NORMAL\_HP}$	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [4]	—	85	—	µA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 0 [4]	—	16	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[3] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADC\_STANDBY\_HP}$	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [4]	—	160	—	µA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [4]	—	125	—	µA
Current from HFPERCLK	I_{ADC_CLK}	HFPERCLK = 16 MHz	—	140	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC clock frequency	f_{ADCCLK}		—	—	16	MHz
Throughput rate	$f_{ADCRATE}$		—	—	1	Msps
Conversion time[5]	$t_{ADCCONV}$	6 bit	—	7	—	cycles
		8 bit	—	9	—	cycles
		12 bit	—	13	—	cycles
Startup time of reference generator and ADC core	$t_{ADCSTART}$	WARMUPMODE[3] = NORMAL	—	—	5	μs
		WARMUPMODE[3] = KEEPIN-STANDBY	—	—	2	μs
		WARMUPMODE[3] = KEEPINSLO-WACC	—	—	1	μs
SNDR at 1Msps and f_{IN} = 10kHz	$SNDR_{ADC}$	Internal reference[6], differential measurement	58	67	—	dB
		External reference[7], differential measurement	—	68	—	dB
Spurious-free dynamic range (SFDR)	$SFDR_{ADC}$	1 MSamples/s, 10 kHz full-scale sine wave	—	75	—	dB
Differential non-linearity (DNL)	DNL_{ADC}	12 bit resolution, No missing co-des	-1	—	2	LSB
Integral non-linearity (INL), End point method	INL_{ADC}	12 bit resolution	-6	—	6	LSB
Offset error	$V_{ADCOFFSETERR}$		-3	0	3	LSB
Gain error in ADC	$V_{ADCGAIN}$	Using internal reference	—	-0.2	3.5	%
		Using external reference	—	-1	—	%
Temperature sensor slope	V_{TS_SLOPE}		—	-1.84	—	mV/°C

Note:

1. The absolute voltage allowed at any ADC input is dictated by the power rail supplied to on-chip circuitry, and may be lower than the effective full scale voltage. All ADC inputs are limited to the ADC supply (AVDD or DVDD depending on EMU_PWRCTRL_ANASW). Any ADC input routed through the APORT will further be limited by the IOVDD supply to the pin.
2. PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU_PWRCTRL.
3. In ADCn_CNTL register.
4. In ADCn_BIASPROG register.
5. Derived from ADCCLK.
6. Internal reference option used corresponds to selection 2V5 in the SINGLECTRL_REF or SCANCTRL_REF register field. The differential input range with this configuration is ± 1.25 V. Typical value is characterized using full-scale sine wave input. Minimum value is production-tested using sine wave input at 1.5 dB lower than full scale.
7. External reference is 1.25 V applied externally to ADCnEXTREFP, with the selection CONF in the SINGLECTRL_REF or SCANCTRL_REF register field and VREFP in the SINGLECTRLX_VREFSEL or SCANCTRLX_VREFSEL field. The differential input range with this configuration is ± 1.25 V.

4.1.14 Analog Comparator (ACMP)

Table 4.31. Analog Comparator (ACMP)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{ACMPIN}	ACMPVDD = ACMPn_CTRL_PWRSEL [1]	—	—	$V_{ACMPVDD}$	V
Supply voltage	$V_{ACMPVDD}$	BIASPROG[2] ≤ 0x10 or FULL-BIAS[2] = 0	1.8	—	$V_{VREGVDD\_MAX}$	V
		0x10 < BIASPROG[2] ≤ 0x20 and FULLBIAS[2] = 1	2.1	—	$V_{VREGVDD\_MAX}$	V
Active current not including voltage reference[3]	I_{ACMP}	BIASPROG[2] = 1, FULLBIAS[2] = 0	—	50	—	nA
		BIASPROG[2] = 0x10, FULLBIAS[2] = 0	—	306	—	nA
		BIASPROG[2] = 0x02, FULLBIAS[2] = 1	—	6.1	11	µA
		BIASPROG[2] = 0x20, FULLBIAS[2] = 1	—	74	92	µA
Current consumption of internal voltage reference[3]	$I_{ACMPREF}$	VLP selected as input using 2.5 V Reference / 4 (0.625 V)	—	50	—	nA
		VLP selected as input using VDD	—	20	—	nA
		VBDIV selected as input using 1.25 V reference / 1	—	4.1	—	µA
		VADIV selected as input using VDD/1	—	2.4	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Hysteresis (V_{CM} = 1.25 V, BIASPROG[2] = 0x10, FULLBIAS[2] = 1)	$V_{ACMPHYST}$	HYSTSEL[4] = HYST0	-3	0	3	mV
		HYSTSEL[4] = HYST1	5	18	27	mV
		HYSTSEL[4] = HYST2	12	33	50	mV
		HYSTSEL[4] = HYST3	17	46	67	mV
		HYSTSEL[4] = HYST4	23	57	86	mV
		HYSTSEL[4] = HYST5	26	68	104	mV
		HYSTSEL[4] = HYST6	30	79	130	mV
		HYSTSEL[4] = HYST7	34	90	155	mV
		HYSTSEL[4] = HYST8	-3	0	3	mV
		HYSTSEL[4] = HYST9	-27	-18	-5	mV
		HYSTSEL[4] = HYST10	-50	-33	-12	mV
		HYSTSEL[4] = HYST11	-67	-45	-17	mV
		HYSTSEL[4] = HYST12	-86	-57	-23	mV
		HYSTSEL[4] = HYST13	-104	-67	-26	mV
		HYSTSEL[4] = HYST14	-130	-78	-30	mV
		HYSTSEL[4] = HYST15	-155	-88	-34	mV
Comparator delay[5]	$t_{ACMPDELAY}$	BIASPROG[2] = 1, FULLBIAS[2] = 0	—	30	95	µs
		BIASPROG[2] = 0x10, FULLBIAS[2] = 0	—	3.7	10	µs
		BIASPROG[2] = 0x02, FULLBIAS[2] = 1	—	360	1000	ns
		BIASPROG[2] = 0x20, FULLBIAS[2] = 1	—	35	—	ns
Offset voltage	$V_{ACMPOFFSET}$	BIASPROG[2] =0x10, FULLBIAS[2] = 1	-35	—	35	mV
Reference voltage	$V_{ACMPREF}$	Internal 1.25 V reference	1	1.25	1.47	V
		Internal 2.5 V reference	1.98	2.5	2.8	V
Capacitive sense internal resistance	R_{CSRES}	CSRESSEL[6] = 0	—	infinite	—	kΩ
		CSRESSEL[6] = 1	—	15	—	kΩ
		CSRESSEL[6] = 2	—	27	—	kΩ
		CSRESSEL[6] = 3	—	39	—	kΩ
		CSRESSEL[6] = 4	—	51	—	kΩ
		CSRESSEL[6] = 5	—	102	—	kΩ
		CSRESSEL[6] = 6	—	164	—	kΩ
		CSRESSEL[6] = 7	—	239	—	kΩ

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:
1. ACMPVDD is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD.
2. In ACMPn_CTRL register.
3. The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference. $I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$.
4. In ACMPn_HYSTERESIS registers.
5. ± 100 mV differential drive.
6. In ACMPn_INPUTSEL register.

4.1.15 Digital to Analog Converter (VDAC)

DRIVESTRENGTH = 2 unless otherwise specified. Primary VDAC output.

Table 4.32. Digital to Analog Converter (VDAC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output voltage	V_{DACOUT}	Single-Ended	0	—	V_{VREF}	V
		Differential[1]	$-V_{VREF}$	—	V_{VREF}	V
Current consumption including references (2 channels)[2]	I_{DAC}	500 ksps, 12-bit, DRIVESTRENGTH = 2, REFSEL = 4	—	396	—	µA
		44.1 ksps, 12-bit, DRIVESTRENGTH = 1, REFSEL = 4	—	72	—	µA
		200 Hz refresh rate, 12-bit Sample-Off mode in EM2, DRIVESTRENGTH = 2, BGRREQTIME = 1, EM2REFENTIME = 9, REFSEL = 4, SETTLETIME = 0x0A, WARMUPTIME = 0x02	—	1.2	—	µA
Current from HFPERCLK[3]	I_{DAC_CLK}		—	5.8	—	µA/MHz
Sample rate	SR_{DAC}		—	—	500	ksps
DAC clock frequency	f_{DAC}		—	—	1	MHz
Conversion time	$t_{DACCONV}$	f_{DAC} = 1MHz	2	—	—	µs
Settling time	$t_{DACSETTLE}$	50% fs step settling to 5 LSB	—	2.5	—	µs
Startup time	$t_{DACSTARTUP}$	Enable to 90% fs output, settling to 10 LSB	—	—	12	µs
Output impedance	R_{OUT}	DRIVESTRENGTH = 2, 0.4 V ≤ V_{OUT} ≤ V_{OPA} - 0.4 V, -8 mA < I_{OUT} < 8 mA, Full supply range	—	2	—	Ω
		DRIVESTRENGTH = 0 or 1, 0.4 V ≤ V_{OUT} ≤ V_{OPA} - 0.4 V, -400 µA < I_{OUT} < 400 µA, Full supply range	—	2	—	Ω
		DRIVESTRENGTH = 2, 0.1 V ≤ V_{OUT} ≤ V_{OPA} - 0.1 V, -2 mA < I_{OUT} < 2 mA, Full supply range	—	2	—	Ω
		DRIVESTRENGTH = 0 or 1, 0.1 V ≤ V_{OUT} ≤ V_{OPA} - 0.1 V, -100 µA < I_{OUT} < 100 µA, Full supply range	—	2	—	Ω
Power supply rejection ratio[4]	PSRR	Vout = 50% fs. DC	—	65.5	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 250 kHz	$SNDR_{DAC}$	500 ksps, single-ended, internal 1.25V reference	—	60.4	—	dB
		500 ksps, single-ended, internal 2.5V reference	—	61.6	—	dB
		500 ksps, single-ended, 3.3V VDD reference	—	64.0	—	dB
		500 ksps, differential, internal 1.25V reference	—	63.3	—	dB
		500 ksps, differential, internal 2.5V reference	—	64.4	—	dB
		500 ksps, differential, 3.3V VDD reference	—	65.8	—	dB
Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 22 kHz	$SNDR_{DAC\_BAND}$	500 ksps, single-ended, internal 1.25V reference	—	65.3	—	dB
		500 ksps, single-ended, internal 2.5V reference	—	66.7	—	dB
		500 ksps, single-ended, 3.3V VDD reference	—	70.0	—	dB
		500 ksps, differential, internal 1.25V reference	—	67.8	—	dB
		500 ksps, differential, internal 2.5V reference	—	69.0	—	dB
		500 ksps, differential, 3.3V VDD reference	—	68.5	—	dB
Total harmonic distortion	THD		—	70.2	—	dB
Differential non-linearity[5]	DNL_{DAC}		-0.99	—	1	LSB
Intergral non-linearity	INL_{DAC}		-4	—	4	LSB
Offset error[6]	V_{OFFSET}	T = 25 °C	-8	—	8	mV
		Across operating temperature range	-25	—	25	mV
Gain error[6]	V_{GAIN}	T = 25 °C, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN)	-2.5	—	2.5	%
		T = 25 °C, Internal reference (REFSEL = 1V25 or 2V5)	-5	—	5	%
		T = 25 °C, External reference (REFSEL = VDD or EXT)	-1.8	—	1.8	%
		Across operating temperature range, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN)	-3.5	—	3.5	%
		Across operating temperature range, Internal reference (REFSEL = 1V25 or 2V5)	-7.5	—	7.5	%
		Across operating temperature range, External reference (REFSEL = VDD or EXT)	-2.0	—	2.0	%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External load capactiance, OUTSCALE=0	C_{LOAD}		—	—	75	pF

Note:

1. In differential mode, the output is defined as the difference between two single-ended outputs. Absolute voltage on each output is limited to the single-ended range.
2. Supply current specifications are for VDAC circuitry operating with static output only and do not include current required to drive the load.
3. Current from HFPERCLK is dependent on HFPERCLK frequency. This current contributes to the total supply current used when the clock to the DAC module is enabled in the CMU.
4. PSRR calculated as 20 * $\log_{10}(\Delta VDD / \Delta V_{OUT})$, VDAC output at 90% of full scale
5. Entire range is monotonic and has no missing codes.
6. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.

4.1.16 Current Digital to Analog Converter (IDAC)

Table 4.33. Current Digital to Analog Converter (IDAC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Number of ranges	N_{IDAC_RANGES}		—	4	—	ranges
Output current	I_{IDAC_OUT}	RANGSEL[1] = RANGE0	0.05	—	1.6	µA
		RANGSEL[1] = RANGE1	1.6	—	4.7	µA
		RANGSEL[1] = RANGE2	0.5	—	16	µA
		RANGSEL[1] = RANGE3	2	—	64	µA
Linear steps within each range	N_{IDAC_STEPS}		—	32	—	steps
Step size	SS_{IDAC}	RANGSEL[1] = RANGE0	—	50	—	nA
		RANGSEL[1] = RANGE1	—	100	—	nA
		RANGSEL[1] = RANGE2	—	500	—	nA
		RANGSEL[1] = RANGE3	—	2	—	µA
Total accuracy, STEPSEL[1] = 0x10	ACC_{IDAC}	EM0 or EM1, AVDD=3.3 V, T = 25 °C	-3	—	3	%
		EM0 or EM1, Across operating temperature range	-18	—	22	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE0, AVDD=3.3 V, T = 25 °C	—	-2	—	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE1, AVDD=3.3 V, T = 25 °C	—	-1.7	—	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE2, AVDD=3.3 V, T = 25 °C	—	-0.8	—	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE3, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
		EM2 or EM3, Sink mode, RANG-SEL[1] = RANGE0, AVDD=3.3 V, T = 25 °C	—	-0.7	—	%
		EM2 or EM3, Sink mode, RANG-SEL[1] = RANGE1, AVDD=3.3 V, T = 25 °C	—	-0.6	—	%
		EM2 or EM3, Sink mode, RANG-SEL[1] = RANGE2, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
		EM2 or EM3, Sink mode, RANG-SEL[1] = RANGE3, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
Start up time	t_{IDAC_SU}	Output within 1% of steady state value	—	5	—	µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Settling time, (output settled within 1% of steady state value),	t_{IDAC_SETTLE}	Range setting is changed	—	5	—	µs
		Step value is changed	—	1	—	µs
Current consumption[2]	I_{IDAC}	EM0 or EM1 Source mode, excluding output current, Across operating temperature range	—	11	15	µA
		EM0 or EM1 Sink mode, excluding output current, Across operating temperature range	—	13	18	µA
		EM2 or EM3 Source mode, excluding output current, T = 25 °C	—	0.023	—	µA
		EM2 or EM3 Sink mode, excluding output current, T = 25 °C	—	0.041	—	µA
		EM2 or EM3 Source mode, excluding output current, T ≥ 85 °C	—	11	—	µA
		EM2 or EM3 Sink mode, excluding output current, T ≥ 85 °C	—	13	—	µA
Output voltage compliance in source mode, source current change relative to current sourced at 0 V	I_{COMP_SRC}	RANGESEL1=0, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-100 mV)	—	0.11	—	%
		RANGESEL1=1, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-100 mV)	—	0.06	—	%
		RANGESEL1=2, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-150 mV)	—	0.04	—	%
		RANGESEL1=3, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-250 mV)	—	0.03	—	%
Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD	I_{COMP_SINK}	RANGESEL1=0, output voltage = 100 mV	—	0.12	—	%
		RANGESEL1=1, output voltage = 100 mV	—	0.05	—	%
		RANGESEL1=2, output voltage = 150 mV	—	0.04	—	%
		RANGESEL1=3, output voltage = 250 mV	—	0.03	—	%

Note:

1. In IDAC_CURPROG register.
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRSEL in the IDAC_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

4.1.17 Capacitive Sense (CSEN)

Table 4.34. Capacitive Sense (CSEN)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single conversion time (1x accumulation)	t_{CNV}	12-bit SAR Conversions	—	20.2	—	µs
		16-bit SAR Conversions	—	26.4	—	µs
		Delta Modulation Conversion (single comparison)	—	1.55	—	µs
Maximum external capacitive load	C_{EXTMAX}	IREFPROG=7 (Gain = 1x), including routing parasitics	—	68	—	pF
		IREFPROG=0 (Gain = 10x), including routing parasitics	—	680	—	pF
Maximum external series impedance	R_{EXTMAX}		—	1	—	kΩ
Supply current, EM2 bonded conversions, WARMUPMODE=NORMAL, WARMUPCNT=0	I_{CSEN_BOND}	12-bit SAR conversions, 20 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)[1]	—	326	—	nA
		Delta Modulation conversions, 20 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)[1]	—	226	—	nA
		12-bit SAR conversions, 200 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)[1]	—	33	—	nA
		Delta Modulation conversions, 200 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)[1]	—	25	—	nA
Supply current, EM2 scan conversions, WARMUPMODE=NORMAL, WARMUPCNT=0	I_{CSEN_EM2}	12-bit SAR conversions, 20 ms scan rate, IREFPROG=0 (Gain = 10x), 8 samples per scan[1]	—	690	—	nA
		Delta Modulation conversions, 20 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), IREFPROG=0 (Gain = 10x), 8 samples per scan[1]	—	515	—	nA
		12-bit SAR conversions, 200 ms scan rate, IREFPROG=0 (Gain = 10x), 8 samples per scan[1]	—	79	—	nA
		Delta Modulation conversions, 200 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), IREFPROG=0 (Gain = 10x), 8 samples per scan[1]	—	57	—	nA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current, continuous conversions, WARMUP-MODE=KEEPCSENWARM	I_{CSEN_ACTIVE}	SAR or Delta Modulation conversions of 33 pF capacitor, IREFPROG=0 (Gain = 10x), always on	—	90.5	—	µA
HFPERCLK supply current	$I_{CSEN\_HFPERCLK}$	Current contribution from HFPERCLK when clock to CSEN block is enabled.	—	2.25	—	µA/MHz

Note:

1. Current is specified with a total external capacitance of 33 pF per channel. Average current is dependent on how long the module is actively sampling channels within the scan period, and scales with the number of samples acquired. Supply current for a specific application can be estimated by multiplying the current per sample by the total number of samples per period (total_current = single_sample_current * (number_of_channels * accumulation)).

4.1.18 Operational Amplifier (OPAMP)

Unless otherwise indicated, specified conditions are: Non-inverting input configuration, VDD = 3.3 V, DRIVESTRENGTH = 2, MAINOUTEN = 1, C_{LOAD} = 75 pF with OUTSCALE = 0, or C_{LOAD} = 37.5 pF with OUTSCALE = 1. Unit gain buffer and 3X-gain connection as specified in table footnotes[1] [2].

Table 4.35. Operational Amplifier (OPAMP)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply voltage (from AVDD)	V_{OPA}	HCMDIS = 0, Rail-to-rail input range	2	—	3.8	V
		HCMDIS = 1	1.62	—	3.8	V
Input voltage	V_{IN}	HCMDIS = 0, Rail-to-rail input range	V_{VSS}	—	V_{OPA}	V
		HCMDIS = 1	V_{VSS}	—	V_{OPA}-1.2	V
Input impedance	R_{IN}		100	—	—	MΩ
Output voltage	V_{OUT}		V_{VSS}	—	V_{OPA}	V
Load capacitance[3]	C_{LOAD}	OUTSCALE = 0	—	—	75	pF
		OUTSCALE = 1	—	—	37.5	pF
Output impedance	R_{OUT}	DRIVESTRENGTH = 2 or 3, 0.4 V ≤ V_{OUT} ≤ V_{OPA} - 0.4 V, -8 mA < I_{OUT} < 8 mA, Buffer connection, Full supply range	—	0.25	—	Ω
		DRIVESTRENGTH = 0 or 1, 0.4 V ≤ V_{OUT} ≤ V_{OPA} - 0.4 V, -400 µA < I_{OUT} < 400 µA, Buffer connection, Full supply range	—	0.6	—	Ω
		DRIVESTRENGTH = 2 or 3, 0.1 V ≤ V_{OUT} ≤ V_{OPA} - 0.1 V, -2 mA < I_{OUT} < 2 mA, Buffer connection, Full supply range	—	0.4	—	Ω
		DRIVESTRENGTH = 0 or 1, 0.1 V ≤ V_{OUT} ≤ V_{OPA} - 0.1 V, -100 µA < I_{OUT} < 100 µA, Buffer connection, Full supply range	—	1	—	Ω
Internal closed-loop gain	G_{CL}	Buffer connection	0.99	1	1.01	-
		3x Gain connection	2.93	2.99	3.05	-
		16x Gain connection	15.07	15.7	16.33	-
Active current[4]	I_{OPA}	DRIVESTRENGTH = 3, OUTSCALE = 0	—	580	—	µA
		DRIVESTRENGTH = 2, OUTSCALE = 0	—	176	—	µA
		DRIVESTRENGTH = 1, OUTSCALE = 0	—	13	—	µA
		DRIVESTRENGTH = 0, OUTSCALE = 0	—	4.7	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Open-loop gain	G_{OL}	DRIVESTRENGTH = 3	—	135	—	dB
		DRIVESTRENGTH = 2	—	137	—	dB
		DRIVESTRENGTH = 1	—	121	—	dB
		DRIVESTRENGTH = 0	—	109	—	dB
Loop unit-gain frequency[5]	UGF	DRIVESTRENGTH = 3, Buffer connection	—	3.38	—	MHz
		DRIVESTRENGTH = 2, Buffer connection	—	0.9	—	MHz
		DRIVESTRENGTH = 1, Buffer connection	—	132	—	kHz
		DRIVESTRENGTH = 0, Buffer connection	—	34	—	kHz
		DRIVESTRENGTH = 3, 3x Gain connection	—	2.57	—	MHz
		DRIVESTRENGTH = 2, 3x Gain connection	—	0.71	—	MHz
		DRIVESTRENGTH = 1, 3x Gain connection	—	113	—	kHz
		DRIVESTRENGTH = 0, 3x Gain connection	—	28	—	kHz
Phase margin	PM	DRIVESTRENGTH = 3, Buffer connection	—	67	—	°
		DRIVESTRENGTH = 2, Buffer connection	—	69	—	°
		DRIVESTRENGTH = 1, Buffer connection	—	63	—	°
		DRIVESTRENGTH = 0, Buffer connection	—	68	—	°
Output voltage noise	N_{OUT}	DRIVESTRENGTH = 3, Buffer connection, 10 Hz - 10 MHz	—	146	—	µVrms
		DRIVESTRENGTH = 2, Buffer connection, 10 Hz - 10 MHz	—	163	—	µVrms
		DRIVESTRENGTH = 1, Buffer connection, 10 Hz - 1 MHz	—	170	—	µVrms
		DRIVESTRENGTH = 0, Buffer connection, 10 Hz - 1 MHz	—	176	—	µVrms
		DRIVESTRENGTH = 3, 3x Gain connection, 10 Hz - 10 MHz	—	313	—	µVrms
		DRIVESTRENGTH = 2, 3x Gain connection, 10 Hz - 10 MHz	—	271	—	µVrms
		DRIVESTRENGTH = 1, 3x Gain connection, 10 Hz - 1 MHz	—	247	—	µVrms
		DRIVESTRENGTH = 0, 3x Gain connection, 10 Hz - 1 MHz	—	245	—	µVrms

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Slew rate[6]	SR	DRIVESTRENGTH = 3, INCBW=1[7]	—	4.7	—	V/µs
		DRIVESTRENGTH = 3, INCBW=0	—	1.5	—	V/µs
		DRIVESTRENGTH = 2, INCBW=1[7]	—	1.27	—	V/µs
		DRIVESTRENGTH = 2, INCBW=0	—	0.42	—	V/µs
		DRIVESTRENGTH = 1, INCBW=1[7]	—	0.17	—	V/µs
		DRIVESTRENGTH = 1, INCBW=0	—	0.058	—	V/µs
		DRIVESTRENGTH = 0, INCBW=1[7]	—	0.044	—	V/µs
		DRIVESTRENGTH = 0, INCBW=0	—	0.015	—	V/µs
Startup time[8]	T_{START}	DRIVESTRENGTH = 2	—	—	12	µs
Input offset voltage	V_{OSI}	DRIVESTRENGTH = 2 or 3, T = 25 °C	-2	—	2	mV
		DRIVESTRENGTH = 1 or 0, T = 25 °C	-2	—	2	mV
		DRIVESTRENGTH = 2 or 3, across operating temperature range	-12	—	12	mV
		DRIVESTRENGTH = 1 or 0, across operating temperature range	-30	—	30	mV
DC power supply rejection ratio[9]	$PSRR_{DC}$	Input referred	—	70	—	dB
DC common-mode rejection ratio[9]	$CMRR_{DC}$	Input referred	—	70	—	dB
Total harmonic distortion	THD_{OPA}	DRIVESTRENGTH = 2, 3x Gain connection, 1 kHz, V_{OUT} = 0.1 V to V_{OPA} - 0.1 V	—	90	—	dB
		DRIVESTRENGTH = 0, 3x Gain connection, 0.1 kHz, V_{OUT} = 0.1 V to V_{OPA} - 0.1 V	—	90	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Specified configuration for Unit gain buffer configuration is: INCBW = 0, HCMDIS = 0, RESINSEL = DISABLE. V_{INPUT} = 0.5 V, V_{OUTPUT} = 0.5 V.
2. Specified configuration for 3X-Gain configuration is: INCBW = 1, HCMDIS = 1, RESINSEL = VSS, V_{INPUT} = 0.5 V, V_{OUTPUT} = 1.5 V. Nominal voltage gain is 3.
3. If the maximum C_{LOAD} is exceeded, an isolation resistor is required for stability. See AN0038 for more information.
4. Current into the load resistor is excluded. When the OPAMP is connected with closed-loop gain > 1, there will be extra current to drive the resistor feedback network. The internal resistor feedback network has total resistance of 143.5 kOhm, which will cause another ~10 µA current when the OPAMP drives 1.5 V between output and ground.
5. In unit gain connection, UGF is the gain-bandwidth product of the OPAMP. In 3x Gain connection, UGF is the gain-bandwidth product of the OPAMP and 1/3 attenuation of the feedback network.
6. Step between 0.2V and V_{OPA}-0.2V, 10%-90% rising/falling range.
7. When INCBW is set to 1 the OPAMP bandwidth is increased. This is allowed only when the non-inverting close-loop gain is ≥ 3, or the OPAMP may not be stable.
8. From enable to output settled. In sample-and-off mode, RC network after OPAMP will contribute extra delay. Settling error < 1mV.
9. When HCMDIS=1 and input common mode transitions the region from V_{OPA}-1.4V to V_{OPA}-1V, input offset will change. PSRR and CMRR specifications do not apply to this transition region.

4.1.19 Pulse Counter (PCNT)

Table 4.36. Pulse Counter (PCNT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input frequency	F_{IN}	Asynchronous Single and Quadrature Modes	—	—	10	MHz
		Sampled Modes with Debounce filter set to 0.	—	—	8	kHz

4.1.20 Analog Port (APORT)

Table 4.37. Analog Port (APORT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current[1 2]	I_{APORT}	Operation in EM0/EM1	—	7	—	µA
		Operation in EM2/EM3	—	63	—	nA

Note:

1. Supply current increase that occurs when an analog peripheral requests access to APORT. This current is not included in reported module currents. Additional peripherals requesting access to APORT do not incur further current.
2. Specified current is for continuous APORT operation. In applications where the APORT is not requested continuously (e.g. periodic ACMP requests from LESENSE in EM2), the average current requirements can be estimated by mutiplying the duty cycle of the requests by the specified continuous current number.

4.1.21 I2C

4.1.21.1 I2C Standard-mode (Sm)[1]

Table 4.38. I2C Standard-mode (Sm)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	100	kHz
SCL clock low time	t_{LOW}		4.7	—	—	µs
SCL clock high time	t_{HIGH}		4	—	—	µs
SDA set-up time	t_{SU_DAT}		250	—	—	ns
SDA hold time[3]	t_{HD_DAT}		100	—	3450	ns
Repeated START condition set-up time	t_{SU_STA}		4.7	—	—	µs
(Repeated) START condition hold time	t_{HD_STA}		4	—	—	µs
STOP condition set-up time	t_{SU_STO}		4	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	—	µs

Note:

1. For CLHR set to 0 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time (t_{HD_DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

4.1.21.2 I2C Fast-mode (Fm)[1]

Table 4.39. I2C Fast-mode (Fm)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	400	kHz
SCL clock low time	t_{LOW}		1.3	—	—	µs
SCL clock high time	t_{HIGH}		0.6	—	—	µs
SDA set-up time	t_{SU_DAT}		100	—	—	ns
SDA hold time[3]	t_{HD_DAT}		100	—	900	ns
Repeated START condition set-up time	t_{SU_STA}		0.6	—	—	µs
(Repeated) START condition hold time	t_{HD_STA}		0.6	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.6	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		1.3	—	—	µs

Note:

1. For CLHR set to 1 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

4.1.21.3 I2C Fast-mode Plus (Fm+)[1]

Table 4.40. I2C Fast-mode Plus (Fm+)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	1000	kHz
SCL clock low time	t_{LOW}		0.5	—	—	µs
SCL clock high time	t_{HIGH}		0.26	—	—	µs
SDA set-up time	t_{SU_DAT}		50	—	—	ns
SDA hold time	t_{HD_DAT}		100	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		0.26	—	—	µs
(Repeated) START condition hold time	t_{HD_STA}		0.26	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.26	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		0.5	—	—	µs

Note:

1. For CLHR set to 0 or 1 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual.

4.1.22 USART SPI

SPI Master Timing

Table 4.41. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1,2,3]	t_{SCLK}		2 * $t_{HFPERCLK}$	—	—	ns
CS to MOSI [1,2]	t_{CS_MO}		-12.5	—	14	ns
SCLK to MOSI [1,2]	t_{SCLK_MO}		-8.5	—	10.5	ns
MISO setup time [1,2]	t_{SU_MI}	IOVDD = 1.62 V	90	—	—	ns
		IOVDD = 3.0 V	42	—	—	ns
MISO hold time [1,2]	t_{H_MI}		-9	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).
3. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.

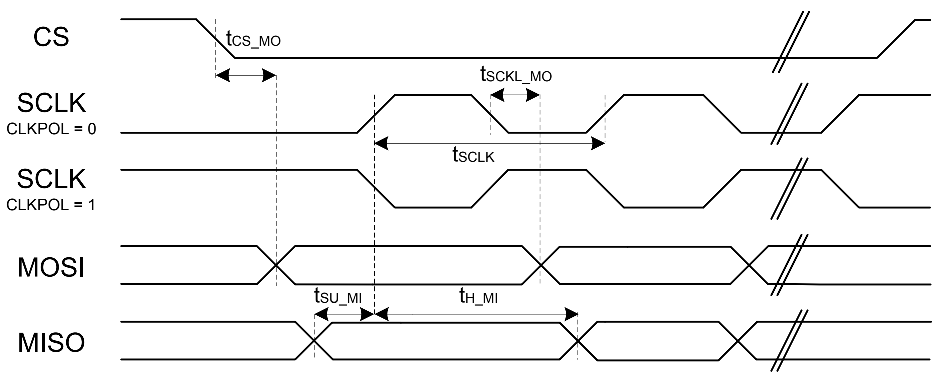


Figure 4.1. SPI Master Timing Diagram

SPI Slave Timing

Table 4.42. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1 2 3]	t_{SCLK}		6 * $t_{HFPERCLK}$	—	—	ns
SCLK high time[1 2 3]	t_{SCLK_HI}		2.5 * $t_{HFPERCLK}$	—	—	ns
SCLK low time[1 2 3]	t_{SCLK_LO}		2.5 * $t_{HFPERCLK}$	—	—	ns
CS active to MISO [1 2]	$t_{CS\_ACT\_MI}$		4	—	70	ns
CS disable to MISO [1 2]	$t_{CS\_DIS\_MI}$		4	—	50	ns
MOSI setup time [1 2]	t_{SU_MO}		12.5	—	—	ns
MOSI hold time [1 2 3]	t_{H_MO}		13	—	—	ns
SCLK to MISO [1 2 3]	t_{SCLK_MI}		6 + 1.5 * $t_{HFPERCLK}$	—	45 + 2.5 * $t_{HFPERCLK}$	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).
3. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.

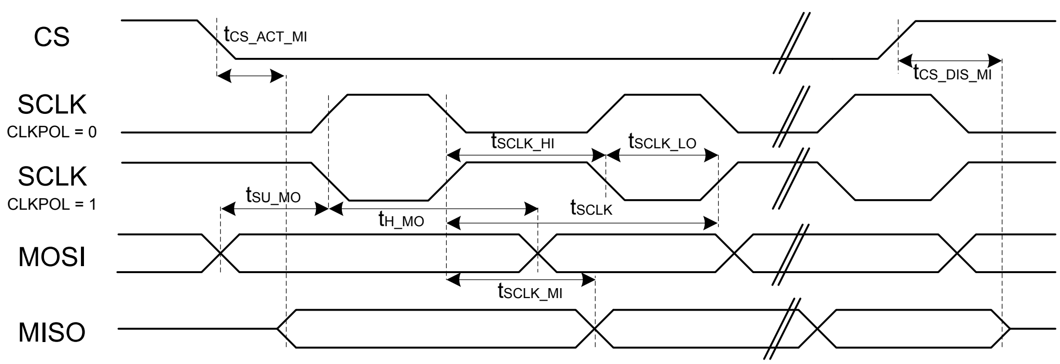


Figure 4.2. SPI Slave Timing Diagram

5. Typical Connection Diagrams

5.1 Typical BGM13S Connections

Typical connections for the BGM13S module are shown in Figure 5.1 Typical Connections for BGM13S with UART Network Co-Processor on page 66. This diagram shows connections for:

- Power supplies
- Antenna loop for internal antenna usage or external antenna connection - The RF and ANTENNA pins should be tied together for correct operation of the module. An optional 0R resistor can be added between RF and ANTENNA, making it possible to measure the signal between these pins.
- Reset line
- UART connection to an external host for Network Co-Processor (NCP) usage (optional)
- 32.768 kHz crystal - Required in applications that must meet 500 ppm Bluetooth Sleep Clock accuracy requirement. More accurate crystals can be used to reduce the listening window and thereby reduce overall current consumption. Recommended crystal is KDS part number *1TJG125DP1A0012* or equivalent.

Note: It is recommended to connect the RESETn line to the host CPU when NCP mode is used.

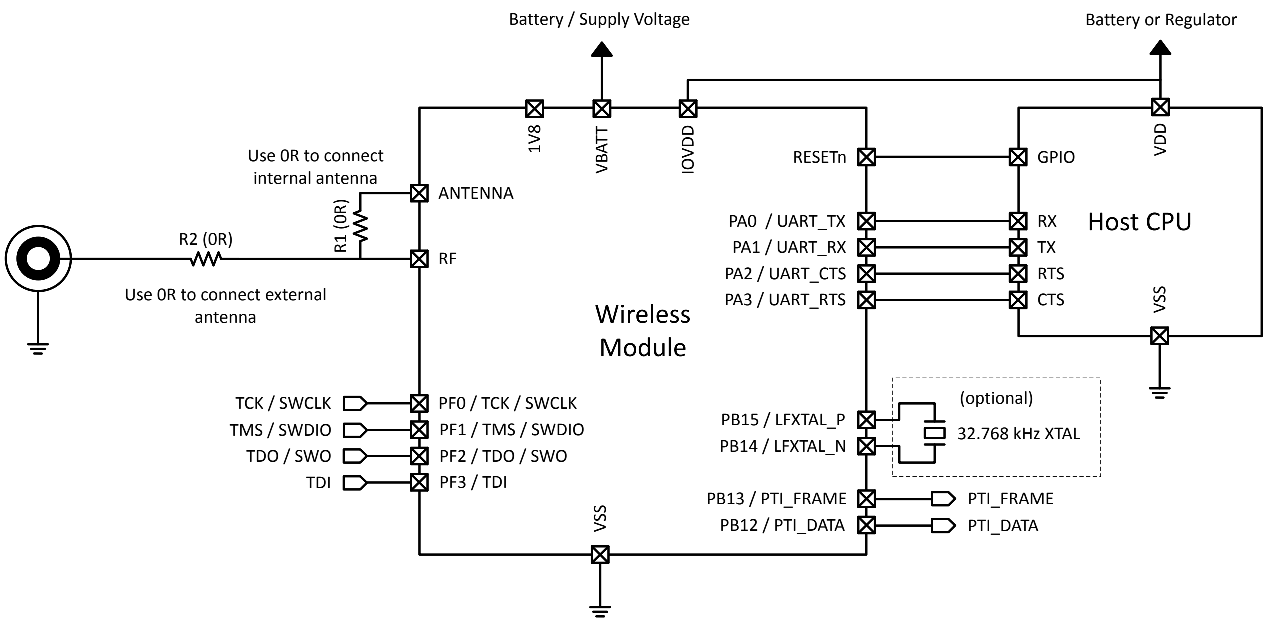


Figure 5.1. Typical Connections for BGM13S with UART Network Co-Processor

Note: It is possible to power the IOVDD pin at 1.8 V from the DC-DC output (1V8). However, the 1V8 output is off by default, and IOVDD must be powered when programming the device. Any system that powers IOVDD directly from 1V8 must power IOVDD externally during initial programming.

Two common debug interface options are shown in Figure 5.2 Common Debug Connections on page 67. Refer to AN958 for more information and additional options.

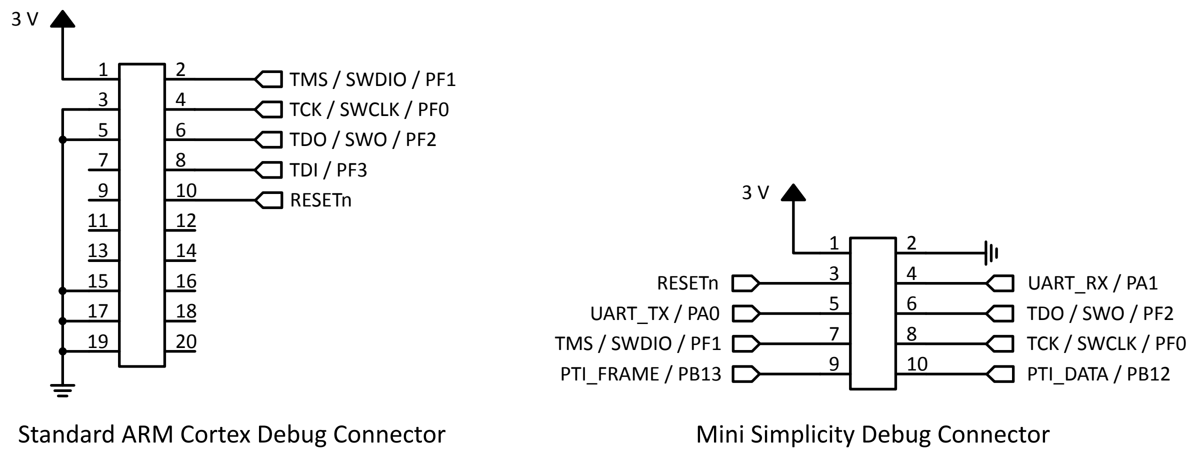


Figure 5.2. Common Debug Connections

6. Layout Guidelines

For optimal performance of the BGM13S, please follow the PCB layout guidelines and ground plane recommendations indicated in this section.

6.1 Layout Guidelines

This section contains generic PCB layout and design guidelines for the BGM13S module. For optimal performance:

- Place the module at the edge of the PCB, as shown in the figures in this chapter.
- Do not place any metal (traces, components, etc.) in the antenna clearance area.
- Connect all ground pads directly to a solid ground plane.
- Place the ground vias as close to the ground pads as possible.

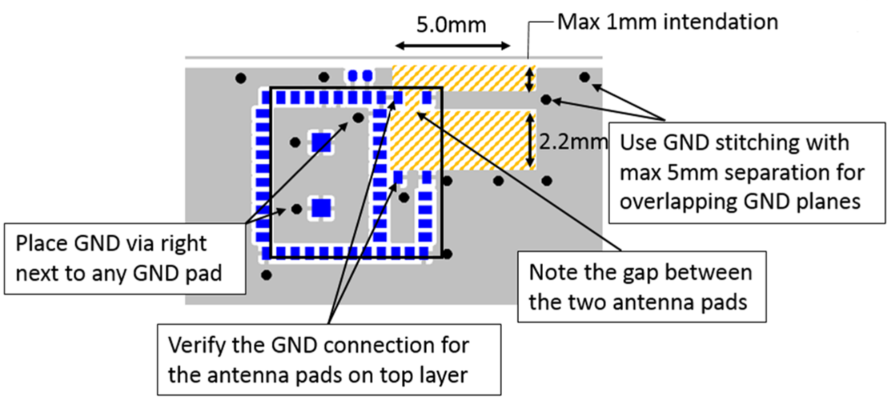


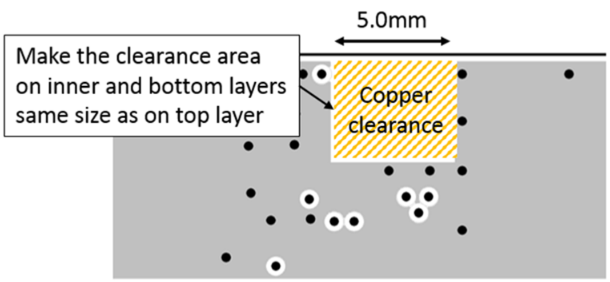
Figure 6.1. BGM13S PCB Top Layer Design

The following rules are recommended for the PCB design:

- Trace to copper clearance 150um
- PTH drill size 300um
- PTH annular ring 150um

Important:

The antenna area must align with the pads precisely. Please refer to the recommended PCB land pattern for exact dimensions.



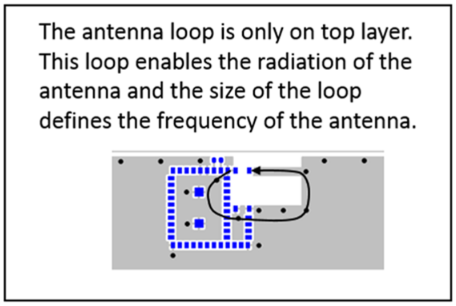


Figure 6.2. BGM13S PCB Middle and Bottom Layer Design

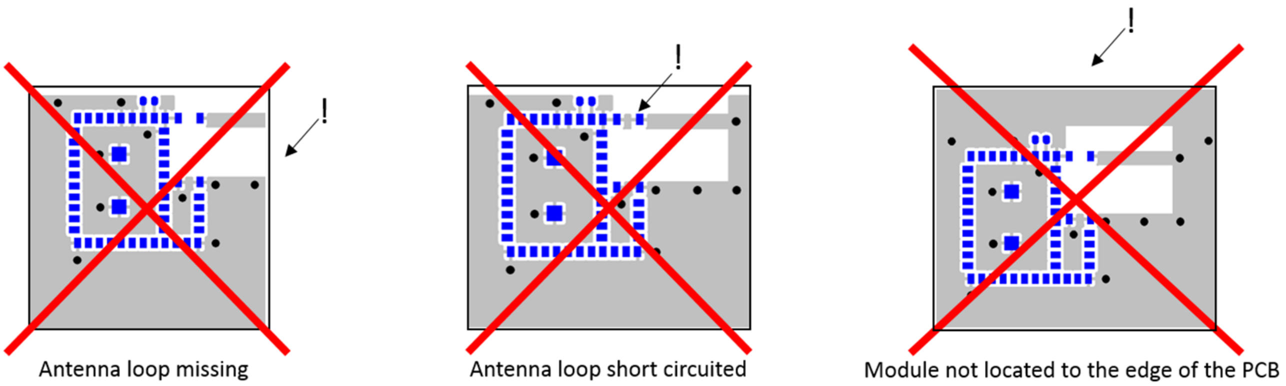


Figure 6.3. Poor Layout Designs for the BGM13S

Layout checklist for BGM13S:

1. Antenna area is aligned relative to the module pads as shown in the recommended PCB land pattern.
2. Clearance area within the inner layers and bottom layer is covering the whole antenna area as shown in the layout guidelines.
3. The antenna loop is implemented on the top layer as shown in the layoyt guidelines.
4. All dimensions within the antenna area are precisely as shown in the recommended PCB land pattern.
5. The module is placed near the edge of the PCB with max 1mm indentation.
6. The module is not placed in the corner of the PCB.

6.2 Effect of PCB Width

The BGM13S module should be placed at the center of the PCB edge. The width of the board has an impact to the radiated efficiency and, more importantly, there should be enough ground plane on both sides of the module for optimal antenna performance. Figure 6.4 BGM13S PCB Top Layer Design on page 69 gives an indcation of ground plane size vs. maximum achievable range.

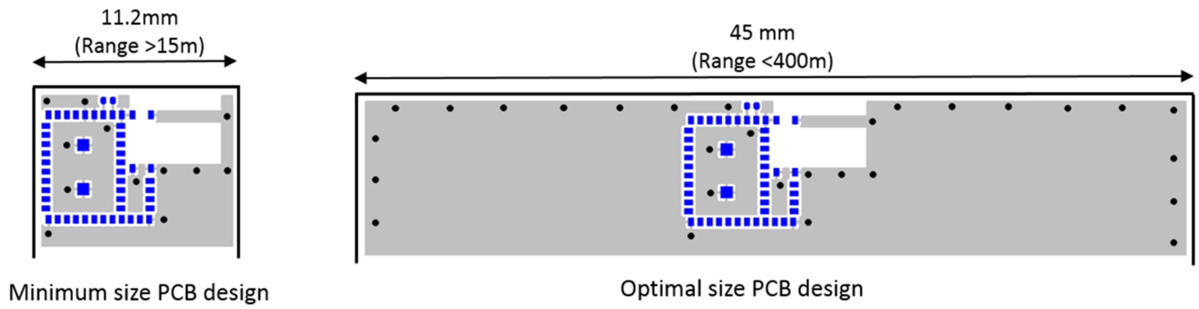


Figure 6.4. BGM13S PCB Top Layer Design

The impact of the board size to the radiated performance is a generic feature of all PCB and chip antennas and it is not a unique feature of the BGM13S. For the BGM13S the depth of the board is not important and does not impact the radiated performance.

6.3 Effect of Plastic and Metal Materials

The antenna on the BGM13S is insensitive to the effects of nearby plastic and other materials with low dielectric constant. No separation between the BGM13S and plastic or other materials is needed. The board thickness does not have any impact on the module either.

Any metal within the antenna area or in close proximity to the antenna area may detune the antenna. In this case it is possible to retune the antenna by adjusting the width of the antenna loop. To avoid detuning of the antenna, the minimum distance to any metal should be more than 3 mm. Encapsulating the module inside metal casing will prevent the radiation of the antenna.

Figure 6.5 Antenna Tuning on page 70 shows how it is possible to adjust the frequency of the antenna by adjusting the width of the antenna loop. The antenna is extremely robust against any objects in close proximity or in direct contact with the antenna and it is recommended not to adjust the dimensions of the antenna area unless it is clear that a metal object, such as a coin cell battery, within the antenna area is detuning the antenna.

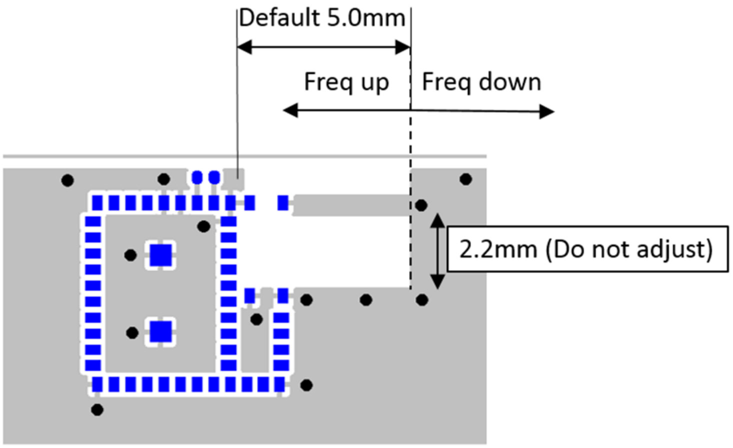


Figure 6.5. Antenna Tuning

6.4 Effects of Human Body

Placing the module in contact with or very close to the human body will negatively impact antenna efficiency and reduce range.

6.5 2D Radiation Pattern Plots

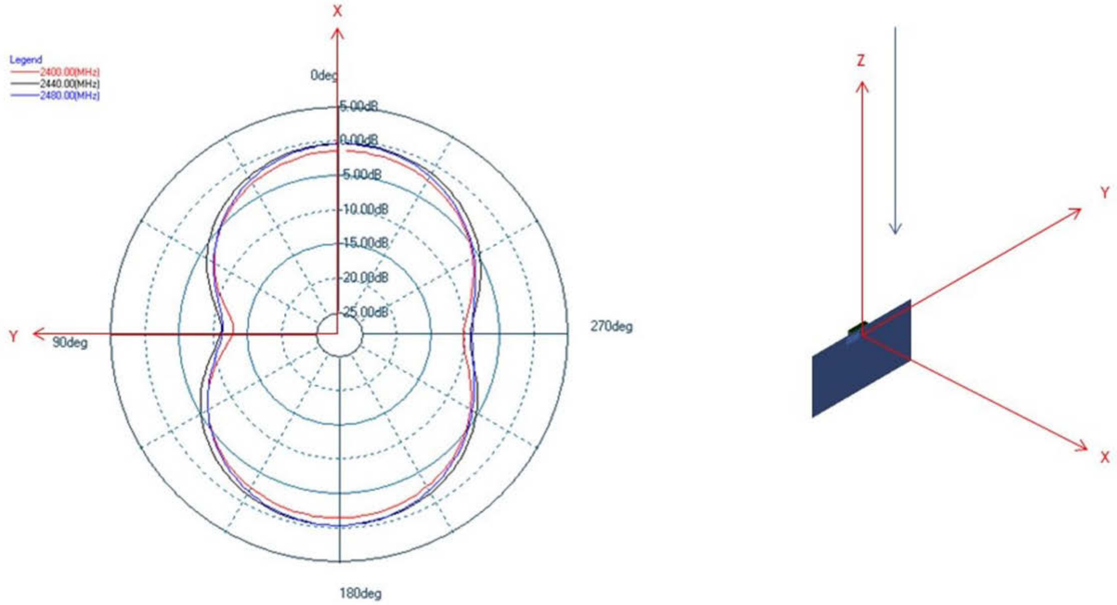


Figure 6.6. Typical 2D Radiation Pattern – Front View

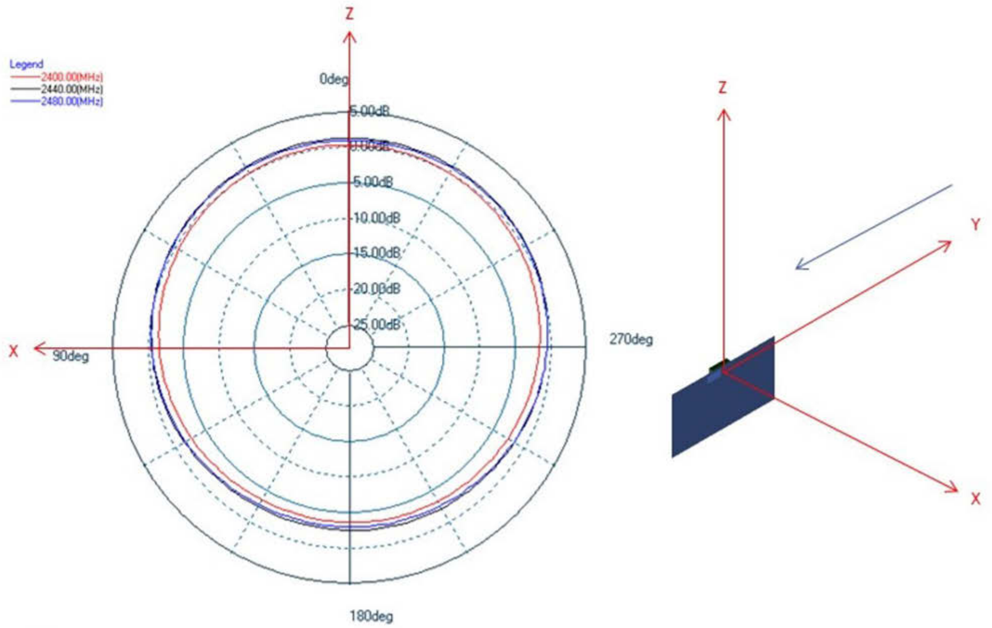


Figure 6.7. Typical 2D Radiation Pattern – Side View

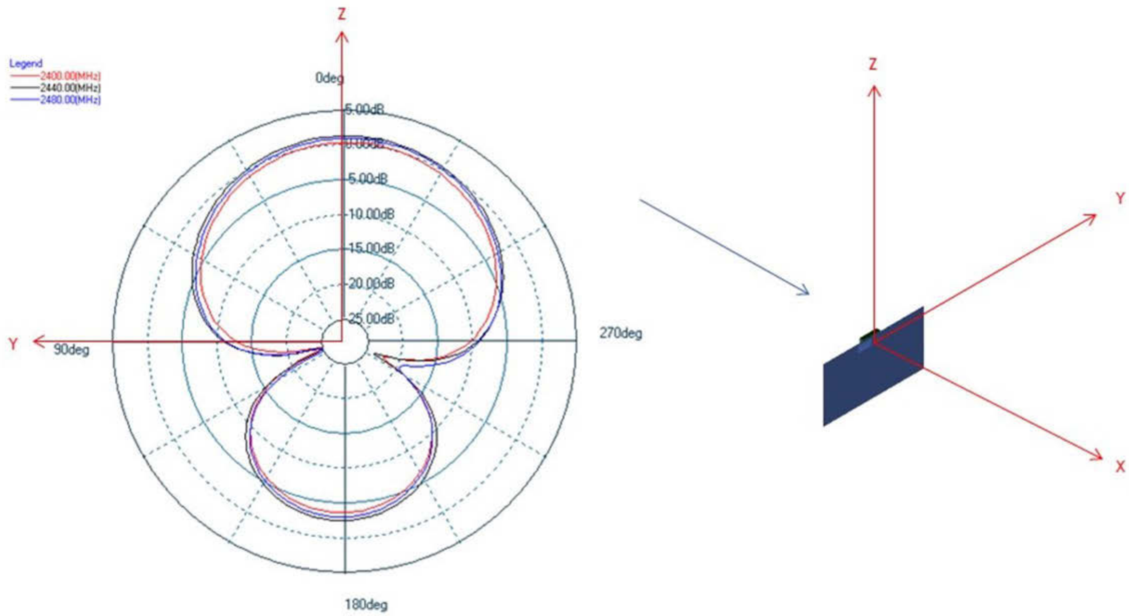


Figure 6.8. Typical 2D Radiation Pattern – Top View

7. Pin Definitions

7.1 BGM13S Device Pinout

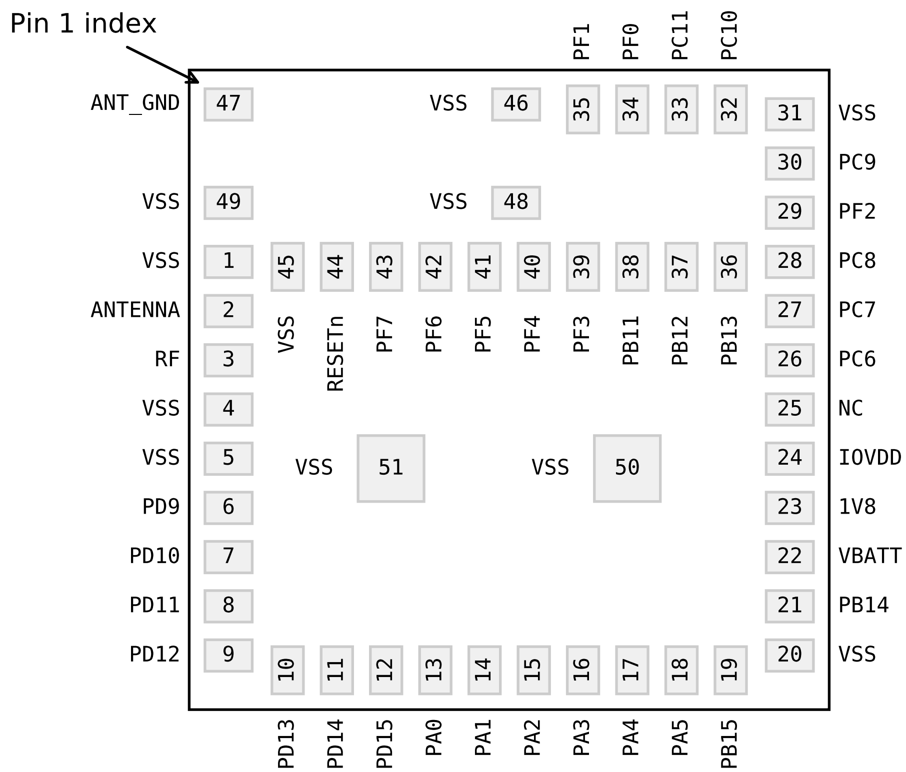


Figure 7.1. BGM13S Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 7.2 GPIO Functionality Table or 7.3 Alternate Functionality Overview.

Table 7.1. BGM13S Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	1 4 5 20 31 45 46 48 49 50 51	Ground	ANTENNA	2	50 Ohm input pin for internal antenna.
RF	3	50 Ohm I/O for external antenna connection.	PD9	6	GPIO (5V)
PD10	7	GPIO (5V)	PD11	8	GPIO (5V)
PD12	9	GPIO (5V)	PD13	10	GPIO
PD14	11	GPIO	PD15	12	GPIO
PA0	13	GPIO	PA1	14	GPIO
PA2	15	GPIO	PA3	16	GPIO
PA4	17	GPIO	PA5	18	GPIO (5V)
PB15	19	GPIO	PB14	21	GPIO
VBATT	22	Battery supply voltage input to the internal DC-DC and analog supply.	1V8	23	1.8V output of the internal DC-DC converter. Internally decoupled - do not add external decoupling.
IOVDD	24	Digital IO power supply.	NC	25	No Connect.
PC6	26	GPIO (5V)	PC7	27	GPIO (5V)
PC8	28	GPIO (5V)	PF2	29	GPIO (5V)
PC9	30	GPIO (5V)	PC10	32	GPIO (5V)
PC11	33	GPIO (5V)	PF0	34	GPIO (5V)
PF1	35	GPIO (5V)	PB13	36	GPIO
PB12	37	GPIO	PB11	38	GPIO
PF3	39	GPIO (5V)	PF4	40	GPIO (5V)
PF5	41	GPIO (5V)	PF6	42	GPIO (5V)
PF7	43	GPIO (5V)	RESETn	44	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
ANT_GND	47	Antenna ground.			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

7.2 GPIO Functionality Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of each GPIO pin, followed by the functionality available on that pin. Refer to 7.3 Alternate Functionality Overview for a list of GPIO locations available for each function.

Table 7.2. GPIO Functionality Table

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PA0	BUSDY BUSCX ADC0_EXTN	TIM0_CC0 #0 TIM0_CC1 #31 TIM0_CC2 #30 TIM0_CDTI0 #29 TIM0_CDTI1 #28 TIM0_CDTI2 #27 TIM1_CC0 #0 TIM1_CC1 #31 TIM1_CC2 #30 TIM1_CC3 #29 WTIM0_CC0 #0 LE-TIM0_OUT0 #0 LE-TIM0_OUT1 #31 PCNT0_S0IN #0 PCNT0_S1IN #31	US0_TX #0 US0_RX #31 US0_CLK #30 US0_CS #29 US0_CTS #28 US0_RTS #27 US1_TX #0 US1_RX #31 US1_CLK #30 US1_CS #29 US1_CTS #28 US1_RTS #27 LEU0_TX #0 LEU0_RX #31 I2C0_SDA #0 I2C0_SCL #31	FRC_DCLK #0 FRC_DOUT #31 FRC_DFRAME #30 MODEM_DCLK #0 MODEM_DIN #31 MODEM_DOUT #30	CMU_CLK1 #0 PRS_CH6 #0 PRS_CH7 #10 PRS_CH8 #9 PRS_CH9 #8 ACMP0_O #0 ACMP1_O #0 LES_CH8
PA1	BUSCY BUSDX ADC0_EXTP VDAC0_EXT	TIM0_CC0 #1 TIM0_CC1 #0 TIM0_CC2 #31 TIM0_CDTI0 #30 TIM0_CDTI1 #29 TIM0_CDTI2 #28 TIM1_CC0 #1 TIM1_CC1 #0 TIM1_CC2 #31 TIM1_CC3 #30 WTIM0_CC0 #1 LE-TIM0_OUT0 #1 LE-TIM0_OUT1 #0 PCNT0_S0IN #1 PCNT0_S1IN #0	US0_TX #1 US0_RX #0 US0_CLK #31 US0_CS #30 US0_CTS #29 US0_RTS #28 US1_TX #1 US1_RX #0 US1_CLK #31 US1_CS #30 US1_CTS #29 US1_RTS #28 LEU0_TX #1 LEU0_RX #0 I2C0_SDA #1 I2C0_SCL #0	FRC_DCLK #1 FRC_DOUT #0 FRC_DFRAME #31 MODEM_DCLK #1 MODEM_DIN #0 MODEM_DOUT #31	CMU_CLK0 #0 PRS_CH6 #1 PRS_CH7 #0 PRS_CH8 #10 PRS_CH9 #9 ACMP0_O #1 ACMP1_O #1 LES_CH9
PA2	VDAC0_OUT1ALT / OPA1_OUTALT #1 BUSDY BUSCX OPA0_P	TIM0_CC0 #2 TIM0_CC1 #1 TIM0_CC2 #0 TIM0_CDTI0 #31 TIM0_CDTI1 #30 TIM0_CDTI2 #29 TIM1_CC0 #2 TIM1_CC1 #1 TIM1_CC2 #0 TIM1_CC3 #31 WTIM0_CC0 #2 WTIM0_CC1 #0 LE-TIM0_OUT0 #2 LE-TIM0_OUT1 #1 PCNT0_S0IN #2 PCNT0_S1IN #1	US0_TX #2 US0_RX #1 US0_CLK #0 US0_CS #31 US0_CTS #30 US0_RTS #29 US1_TX #2 US1_RX #1 US1_CLK #0 US1_CS #31 US1_CTS #30 US1_RTS #29 LEU0_TX #2 LEU0_RX #1 I2C0_SDA #2 I2C0_SCL #1	FRC_DCLK #2 FRC_DOUT #1 FRC_DFRAME #0 MODEM_DCLK #2 MODEM_DIN #1 MODEM_DOUT #0	PRS_CH6 #2 PRS_CH7 #1 PRS_CH8 #0 PRS_CH9 #10 ACMP0_O #2 ACMP1_O #2 LES_CH10

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PA3	BUSCY BUSDX VDAC0_OUT0 / OPA0_OUT	TIM0_CC0 #3 TIM0_CC1 #2 TIM0_CC2 #1 TIM0_CDTI0 #0 TIM0_CDTI1 #31 TIM0_CDTI2 #30 TIM1_CC0 #3 TIM1_CC1 #2 TIM1_CC2 #1 TIM1_CC3 #0 WTIM0_CC0 #3 WTIM0_CC1 #1 LE-TIM0_OUT0 #3 LE-TIM0_OUT1 #2 PCNT0_S0IN #3 PCNT0_S1IN #2	US0_TX #3 US0_RX #2 US0_CLK #1 US0_CS #0 US0_CTS #31 US0_RTS #30 US1_TX #3 US1_RX #2 US1_CLK #1 US1_CS #0 US1_CTS #31 US1_RTS #30 LEU0_TX #3 LEU0_RX #2 I2C0_SDA #3 I2C0_SCL #2	FRC_DCLK #3 FRC_DOUT #2 FRC_DFRAME #1 MODEM_DCLK #3 MODEM_DIN #2 MODEM_DOUT #1	PRS_CH6 #3 PRS_CH7 #2 PRS_CH8 #1 PRS_CH9 #0 ACMP0_O #3 ACMP1_O #3 LES_CH11 GPIO_EM4WU8
PA4	VDAC0_OUT1ALT / OPA1_OUTALT #2 BUSDY BUSCX OPA0_N	TIM0_CC0 #4 TIM0_CC1 #3 TIM0_CC2 #2 TIM0_CDTI0 #1 TIM0_CDTI1 #0 TIM0_CDTI2 #31 TIM1_CC0 #4 TIM1_CC1 #3 TIM1_CC2 #2 TIM1_CC3 #1 WTIM0_CC0 #4 WTIM0_CC1 #2 WTIM0_CC2 #0 LE-TIM0_OUT0 #4 LE-TIM0_OUT1 #3 PCNT0_S0IN #4 PCNT0_S1IN #3	US0_TX #4 US0_RX #3 US0_CLK #2 US0_CS #1 US0_CTS #0 US0_RTS #31 US1_TX #4 US1_RX #3 US1_CLK #2 US1_CS #1 US1_CTS #0 US1_RTS #31 LEU0_TX #4 LEU0_RX #3 I2C0_SDA #4 I2C0_SCL #3	FRC_DCLK #4 FRC_DOUT #3 FRC_DFRAME #2 MODEM_DCLK #4 MODEM_DIN #3 MODEM_DOUT #2	PRS_CH6 #4 PRS_CH7 #3 PRS_CH8 #2 PRS_CH9 #1 ACMP0_O #4 ACMP1_O #4 LES_CH12
PA5	VDAC0_OUT0ALT / OPA0_OUTALT #0 BUSCY BUSDX	TIM0_CC0 #5 TIM0_CC1 #4 TIM0_CC2 #3 TIM0_CDTI0 #2 TIM0_CDTI1 #1 TIM0_CDTI2 #0 TIM1_CC0 #5 TIM1_CC1 #4 TIM1_CC2 #3 TIM1_CC3 #2 WTIM0_CC0 #5 WTIM0_CC1 #3 WTIM0_CC2 #1 LE-TIM0_OUT0 #5 LE-TIM0_OUT1 #4 PCNT0_S0IN #5 PCNT0_S1IN #4	US0_TX #5 US0_RX #4 US0_CLK #3 US0_CS #2 US0_CTS #1 US0_RTS #0 US1_TX #5 US1_RX #4 US1_CLK #3 US1_CS #2 US1_CTS #1 US1_RTS #0 US2_TX #0 US2_RX #31 US2_CLK #30 US2_CS #29 US2_CTS #28 US2_RTS #27 LEU0_TX #5 LEU0_RX #4 I2C0_SDA #5 I2C0_SCL #4	FRC_DCLK #5 FRC_DOUT #4 FRC_DFRAME #3 MODEM_DCLK #5 MODEM_DIN #4 MODEM_DOUT #3	CMU_CLKI0 #4 PRS_CH6 #5 PRS_CH7 #4 PRS_CH8 #3 PRS_CH9 #2 ACMP0_O #5 ACMP1_O #5 LES_CH13 ETM_TCLK #1

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PB11	BUSCY BUSDX OPA2_P	TIM0_CC0 #6 TIM0_CC1 #5 TIM0_CC2 #4 TIM0_CDTI0 #3 TIM0_CDTI1 #2 TIM0_CDTI2 #1 TIM1_CC0 #6 TIM1_CC1 #5 TIM1_CC2 #4 TIM1_CC3 #3 WTIM0_CC0 #15 WTIM0_CC1 #13 WTIM0_CC2 #11 WTIM0_CDTI0 #7 WTIM0_CDTI1 #5 WTIM0_CDTI2 #3 LETIM0_OUT0 #6 LETIM0_OUT1 #5 PCNT0_S0IN #6 PCNT0_S1IN #5	US0_TX #6 US0_RX #5 US0_CLK #4 US0_CS #3 US0_CTS #2 US0_RTS #1 US1_TX #6 US1_RX #5 US1_CLK #4 US1_CS #3 US1_CTS #2 US1_RTS #1 LEU0_TX #6 LEU0_RX #5 I2C0_SDA #6 I2C0_SCL #5	FRC_DCLK #6 FRC_DOUT #5 FRC_DFRAME #4 MODEM_DCLK #6 MODEM_DIN #5 MODEM_DOUT #4	PRS_CH6 #6 PRS_CH7 #5 PRS_CH8 #4 PRS_CH9 #3 ACMP0_O #6 ACMP1_O #6
PB12	BUSDY BUSCX OPA2_OUT	TIM0_CC0 #7 TIM0_CC1 #6 TIM0_CC2 #5 TIM0_CDTI0 #4 TIM0_CDTI1 #3 TIM0_CDTI2 #2 TIM1_CC0 #7 TIM1_CC1 #6 TIM1_CC2 #5 TIM1_CC3 #4 WTIM0_CC0 #16 WTIM0_CC1 #14 WTIM0_CC2 #12 WTIM0_CDTI0 #8 WTIM0_CDTI1 #6 WTIM0_CDTI2 #4 LETIM0_OUT0 #7 LETIM0_OUT1 #6 PCNT0_S0IN #7 PCNT0_S1IN #6	US0_TX #7 US0_RX #6 US0_CLK #5 US0_CS #4 US0_CTS #3 US0_RTS #2 US1_TX #7 US1_RX #6 US1_CLK #5 US1_CS #4 US1_CTS #3 US1_RTS #2 LEU0_TX #7 LEU0_RX #6 I2C0_SDA #7 I2C0_SCL #6	FRC_DCLK #7 FRC_DOUT #6 FRC_DFRAME #5 MODEM_DCLK #7 MODEM_DIN #6 MODEM_DOUT #5	PRS_CH6 #7 PRS_CH7 #6 PRS_CH8 #5 PRS_CH9 #4 ACMP0_O #7 ACMP1_O #7
PB13	BUSCY BUSDX OPA2_N	TIM0_CC0 #8 TIM0_CC1 #7 TIM0_CC2 #6 TIM0_CDTI0 #5 TIM0_CDTI1 #4 TIM0_CDTI2 #3 TIM1_CC0 #8 TIM1_CC1 #7 TIM1_CC2 #6 TIM1_CC3 #5 WTIM0_CC0 #17 WTIM0_CC1 #15 WTIM0_CC2 #13 WTIM0_CDTI0 #9 WTIM0_CDTI1 #7 WTIM0_CDTI2 #5 LETIM0_OUT0 #8 LETIM0_OUT1 #7 PCNT0_S0IN #8 PCNT0_S1IN #7	US0_TX #8 US0_RX #7 US0_CLK #6 US0_CS #5 US0_CTS #4 US0_RTS #3 US1_TX #8 US1_RX #7 US1_CLK #6 US1_CS #5 US1_CTS #4 US1_RTS #3 LEU0_TX #8 LEU0_RX #7 I2C0_SDA #8 I2C0_SCL #7	FRC_DCLK #8 FRC_DOUT #7 FRC_DFRAME #6 MODEM_DCLK #8 MODEM_DIN #7 MODEM_DOUT #6	CMU_CLKI0 #0 PRS_CH6 #8 PRS_CH7 #7 PRS_CH8 #6 PRS_CH9 #5 ACMP0_O #8 ACMP1_O #8 DBG_SWO #1 GPIO_EM4WU9

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PB14	BUSDY BUSCX LFXTAL_N	TIM0_CC0 #9 TIM0_CC1 #8 TIM0_CC2 #7 TIM0_CDTI0 #6 TIM0_CDTI1 #5 TIM0_CDTI2 #4 TIM1_CC0 #9 TIM1_CC1 #8 TIM1_CC2 #7 TIM1_CC3 #6 WTIM0_CC0 #18 WTIM0_CC1 #16 WTIM0_CC2 #14 WTIM0_CDTI0 #10 WTIM0_CDTI1 #8 WTIM0_CDTI2 #6 LETIM0_OUT0 #9 LETIM0_OUT1 #8 PCNT0_S0IN #9 PCNT0_S1IN #8	US0_TX #9 US0_RX #8 US0_CLK #7 US0_CS #6 US0_CTS #5 US0_RTS #4 US1_TX #9 US1_RX #8 US1_CLK #7 US1_CS #6 US1_CTS #5 US1_RTS #4 LEU0_TX #9 LEU0_RX #8 I2C0_SDA #9 I2C0_SCL #8	FRC_DCLK #9 FRC_DOUT #8 FRC_DFRAME #7 MODEM_DCLK #9 MODEM_DIN #8 MODEM_DOUT #7	CMU_CLK1 #1 PRS_CH6 #9 PRS_CH7 #8 PRS_CH8 #7 PRS_CH9 #6 ACMP0_O #9 ACMP1_O #9
PB15	BUSCY BUSDX LFXTAL_P	TIM0_CC0 #10 TIM0_CC1 #9 TIM0_CC2 #8 TIM0_CDTI0 #7 TIM0_CDTI1 #6 TIM0_CDTI2 #5 TIM1_CC0 #10 TIM1_CC1 #9 TIM1_CC2 #8 TIM1_CC3 #7 WTIM0_CC0 #19 WTIM0_CC1 #17 WTIM0_CC2 #15 WTIM0_CDTI0 #11 WTIM0_CDTI1 #9 WTIM0_CDTI2 #7 LETIM0_OUT0 #10 LETIM0_OUT1 #9 PCNT0_S0IN #10 PCNT0_S1IN #9	US0_TX #10 US0_RX #9 US0_CLK #8 US0_CS #7 US0_CTS #6 US0_RTS #5 US1_TX #10 US1_RX #9 US1_CLK #8 US1_CS #7 US1_CTS #6 US1_RTS #5 LEU0_TX #10 LEU0_RX #9 I2C0_SDA #10 I2C0_SCL #9	FRC_DCLK #10 FRC_DOUT #9 FRC_DFRAME #8 MODEM_DCLK #10 MODEM_DIN #9 MODEM_DOUT #8	CMU_CLK0 #1 PRS_CH6 #10 PRS_CH7 #9 PRS_CH8 #8 PRS_CH9 #7 ACMP0_O #10 ACMP1_O #10
PC6	BUSBY BUSAX	TIM0_CC0 #11 TIM0_CC1 #10 TIM0_CC2 #9 TIM0_CDTI0 #8 TIM0_CDTI1 #7 TIM0_CDTI2 #6 TIM1_CC0 #11 TIM1_CC1 #10 TIM1_CC2 #9 TIM1_CC3 #8 WTIM0_CC0 #26 WTIM0_CC1 #24 WTIM0_CC2 #22 WTIM0_CDTI0 #18 WTIM0_CDTI1 #16 WTIM0_CDTI2 #14 LETIM0_OUT0 #11 LETIM0_OUT1 #10 PCNT0_S0IN #11 PCNT0_S1IN #10	US0_TX #11 US0_RX #10 US0_CLK #9 US0_CS #8 US0_CTS #7 US0_RTS #6 US1_TX #11 US1_RX #10 US1_CLK #9 US1_CS #8 US1_CTS #7 US1_RTS #6 LEU0_TX #11 LEU0_RX #10 I2C0_SDA #11 I2C0_SCL #10	FRC_DCLK #11 FRC_DOUT #10 FRC_DFRAME #9 MODEM_DCLK #11 MODEM_DIN #10 MODEM_DOUT #9	CMU_CLK0 #2 CMU_CLKI0 #2 PRS_CH0 #8 PRS_CH9 #11 PRS_CH10 #0 PRS_CH11 #5 ACMP0_O #11 ACMP1_O #11 ETM_TCLK #3

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PC7	BUSAY BUSBX	TIM0_CC0 #12 TIM0_CC1 #11 TIM0_CC2 #10 TIM0_CDTI0 #9 TIM0_CDTI1 #8 TIM0_CDTI2 #7 TIM1_CC0 #12 TIM1_CC1 #11 TIM1_CC2 #10 TIM1_CC3 #9 WTIM0_CC0 #27 WTIM0_CC1 #25 WTIM0_CC2 #23 WTIM0_CDTI0 #19 WTIM0_CDTI1 #17 WTIM0_CDTI2 #15 LETIM0_OUT0 #12 LETIM0_OUT1 #11 PCNT0_S0IN #12 PCNT0_S1IN #11	US0_TX #12 US0_RX #11 US0_CLK #10 US0_CS #9 US0_CTS #8 US0_RTS #7 US1_TX #12 US1_RX #11 US1_CLK #10 US1_CS #9 US1_CTS #8 US1_RTS #7 LEU0_TX #12 LEU0_RX #11 I2C0_SDA #12 I2C0_SCL #11	FRC_DCLK #12 FRC_DOUT #11 FRC_DFRAME #10 MODEM_DCLK #12 MODEM_DIN #11 MODEM_DOUT #10	CMU_CLK1 #2 PRS_CH0 #9 PRS_CH9 #12 PRS_CH10 #1 PRS_CH11 #0 ACMP0_O #12 ACMP1_O #12 ETM_TD0
PC8	BUSBY BUSAX	TIM0_CC0 #13 TIM0_CC1 #12 TIM0_CC2 #11 TIM0_CDTI0 #10 TIM0_CDTI1 #9 TIM0_CDTI2 #8 TIM1_CC0 #13 TIM1_CC1 #12 TIM1_CC2 #11 TIM1_CC3 #10 WTIM0_CC0 #28 WTIM0_CC1 #26 WTIM0_CC2 #24 WTIM0_CDTI0 #20 WTIM0_CDTI1 #18 WTIM0_CDTI2 #16 LETIM0_OUT0 #13 LETIM0_OUT1 #12 PCNT0_S0IN #13 PCNT0_S1IN #12	US0_TX #13 US0_RX #12 US0_CLK #11 US0_CS #10 US0_CTS #9 US0_RTS #8 US1_TX #13 US1_RX #12 US1_CLK #11 US1_CS #10 US1_CTS #9 US1_RTS #8 LEU0_TX #13 LEU0_RX #12 I2C0_SDA #13 I2C0_SCL #12	FRC_DCLK #13 FRC_DOUT #12 FRC_DFRAME #11 MODEM_DCLK #13 MODEM_DIN #12 MODEM_DOUT #11	PRS_CH0 #10 PRS_CH9 #13 PRS_CH10 #2 PRS_CH11 #1 ACMP0_O #13 ACMP1_O #13 ETM_TD1
PC9	BUSAY BUSBX	TIM0_CC0 #14 TIM0_CC1 #13 TIM0_CC2 #12 TIM0_CDTI0 #11 TIM0_CDTI1 #10 TIM0_CDTI2 #9 TIM1_CC0 #14 TIM1_CC1 #13 TIM1_CC2 #12 TIM1_CC3 #11 WTIM0_CC0 #29 WTIM0_CC1 #27 WTIM0_CC2 #25 WTIM0_CDTI0 #21 WTIM0_CDTI1 #19 WTIM0_CDTI2 #17 LETIM0_OUT0 #14 LETIM0_OUT1 #13 PCNT0_S0IN #14 PCNT0_S1IN #13	US0_TX #14 US0_RX #13 US0_CLK #12 US0_CS #11 US0_CTS #10 US0_RTS #9 US1_TX #14 US1_RX #13 US1_CLK #12 US1_CS #11 US1_CTS #10 US1_RTS #9 LEU0_TX #14 LEU0_RX #13 I2C0_SDA #14 I2C0_SCL #13	FRC_DCLK #14 FRC_DOUT #13 FRC_DFRAME #12 MODEM_DCLK #14 MODEM_DIN #13 MODEM_DOUT #12	PRS_CH0 #11 PRS_CH9 #14 PRS_CH10 #3 PRS_CH11 #2 ACMP0_O #14 ACMP1_O #14 ETM_TD2

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PC10	BUSBY BUSAX	TIM0_CC0 #15 TIM0_CC1 #14 TIM0_CC2 #13 TIM0_CDTI0 #12 TIM0_CDTI1 #11 TIM0_CDTI2 #10 TIM1_CC0 #15 TIM1_CC1 #14 TIM1_CC2 #13 TIM1_CC3 #12 WTIM0_CC0 #30 WTIM0_CC1 #28 WTIM0_CC2 #26 WTIM0_CDTI0 #22 WTIM0_CDTI1 #20 WTIM0_CDTI2 #18 LETIM0_OUT0 #15 LETIM0_OUT1 #14 PCNT0_S0IN #15 PCNT0_S1IN #14	US0_TX #15 US0_RX #14 US0_CLK #13 US0_CS #12 US0_CTS #11 US0_RTS #10 US1_TX #15 US1_RX #14 US1_CLK #13 US1_CS #12 US1_CTS #11 US1_RTS #10 LEU0_TX #15 LEU0_RX #14 I2C0_SDA #15 I2C0_SCL #14 I2C1_SDA #19 I2C1_SCL #18	FRC_DCLK #15 FRC_DOUT #14 FRC_DFRAME #13 MODEM_DCLK #15 MODEM_DIN #14 MODEM_DOUT #13	CMU_CLK1 #3 PRS_CH0 #12 PRS_CH9 #15 PRS_CH10 #4 PRS_CH11 #3 ACMP0_O #15 ACMP1_O #15 ETM_TD3 GPIO_EM4WU12
PC11	BUSAY BUSBX	TIM0_CC0 #16 TIM0_CC1 #15 TIM0_CC2 #14 TIM0_CDTI0 #13 TIM0_CDTI1 #12 TIM0_CDTI2 #11 TIM1_CC0 #16 TIM1_CC1 #15 TIM1_CC2 #14 TIM1_CC3 #13 WTIM0_CC0 #31 WTIM0_CC1 #29 WTIM0_CC2 #27 WTIM0_CDTI0 #23 WTIM0_CDTI1 #21 WTIM0_CDTI2 #19 LETIM0_OUT0 #16 LETIM0_OUT1 #15 PCNT0_S0IN #16 PCNT0_S1IN #15	US0_TX #16 US0_RX #15 US0_CLK #14 US0_CS #13 US0_CTS #12 US0_RTS #11 US1_TX #16 US1_RX #15 US1_CLK #14 US1_CS #13 US1_CTS #12 US1_RTS #11 LEU0_TX #16 LEU0_RX #15 I2C0_SDA #16 I2C0_SCL #15 I2C1_SDA #20 I2C1_SCL #19	FRC_DCLK #16 FRC_DOUT #15 FRC_DFRAME #14 MODEM_DCLK #16 MODEM_DIN #15 MODEM_DOUT #14	CMU_CLK0 #3 PRS_CH0 #13 PRS_CH9 #16 PRS_CH10 #5 PRS_CH11 #4 ACMP0_O #16 ACMP1_O #16 DBG_SWO #3
PD9	BUSCY BUSDX	TIM0_CC0 #17 TIM0_CC1 #16 TIM0_CC2 #15 TIM0_CDTI0 #14 TIM0_CDTI1 #13 TIM0_CDTI2 #12 TIM1_CC0 #17 TIM1_CC1 #16 TIM1_CC2 #15 TIM1_CC3 #14 WTIM0_CC1 #31 WTIM0_CC2 #29 WTIM0_CDTI0 #25 WTIM0_CDTI1 #23 WTIM0_CDTI2 #21 LETIM0_OUT0 #17 LETIM0_OUT1 #16 PCNT0_S0IN #17 PCNT0_S1IN #16	US0_TX #17 US0_RX #16 US0_CLK #15 US0_CS #14 US0_CTS #13 US0_RTS #12 US1_TX #17 US1_RX #16 US1_CLK #15 US1_CS #14 US1_CTS #13 US1_RTS #12 LEU0_TX #17 LEU0_RX #16 I2C0_SDA #17 I2C0_SCL #16	FRC_DCLK #17 FRC_DOUT #16 FRC_DFRAME #15 MODEM_DCLK #17 MODEM_DIN #16 MODEM_DOUT #15	CMU_CLK0 #4 PRS_CH3 #8 PRS_CH4 #0 PRS_CH5 #6 PRS_CH6 #11 ACMP0_O #17 ACMP1_O #17 LES_CH1

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PD10	BUSDY BUSCX	TIM0_CC0 #18 TIM0_CC1 #17 TIM0_CC2 #16 TIM0_CDTI0 #15 TIM0_CDTI1 #14 TIM0_CDTI2 #13 TIM1_CC0 #18 TIM1_CC1 #17 TIM1_CC2 #16 TIM1_CC3 #15 WTIM0_CC2 #30 WTIM0_CDTI0 #26 WTIM0_CDTI1 #24 WTIM0_CDTI2 #22 LETIM0_OUT0 #18 LETIM0_OUT1 #17 PCNT0_S0IN #18 PCNT0_S1IN #17	US0_TX #18 US0_RX #17 US0_CLK #16 US0_CS #15 US0_CTS #14 US0_RTS #13 US1_TX #18 US1_RX #17 US1_CLK #16 US1_CS #15 US1_CTS #14 US1_RTS #13 LEU0_TX #18 LEU0_RX #17 I2C0_SDA #18 I2C0_SCL #17	FRC_DCLK #18 FRC_DOUT #17 FRC_DFRAME #16 MODEM_DCLK #18 MODEM_DIN #17 MODEM_DOUT #16	CMU_CLK1 #4 PRS_CH3 #9 PRS_CH4 #1 PRS_CH5 #0 PRS_CH6 #12 ACMP0_O #18 ACMP1_O #18 LES_CH2
PD11	BUSCY BUSDX	TIM0_CC0 #19 TIM0_CC1 #18 TIM0_CC2 #17 TIM0_CDTI0 #16 TIM0_CDTI1 #15 TIM0_CDTI2 #14 TIM1_CC0 #19 TIM1_CC1 #18 TIM1_CC2 #17 TIM1_CC3 #16 WTIM0_CC2 #31 WTIM0_CDTI0 #27 WTIM0_CDTI1 #25 WTIM0_CDTI2 #23 LETIM0_OUT0 #19 LETIM0_OUT1 #18 PCNT0_S0IN #19 PCNT0_S1IN #18	US0_TX #19 US0_RX #18 US0_CLK #17 US0_CS #16 US0_CTS #15 US0_RTS #14 US1_TX #19 US1_RX #18 US1_CLK #17 US1_CS #16 US1_CTS #15 US1_RTS #14 LEU0_TX #19 LEU0_RX #18 I2C0_SDA #19 I2C0_SCL #18	FRC_DCLK #19 FRC_DOUT #18 FRC_DFRAME #17 MODEM_DCLK #19 MODEM_DIN #18 MODEM_DOUT #17	PRS_CH3 #10 PRS_CH4 #2 PRS_CH5 #1 PRS_CH6 #13 ACMP0_O #19 ACMP1_O #19 LES_CH3
PD12	VDAC0_OUT1ALT / OPA1_OUTALT #0 BUSDY BUSCX	TIM0_CC0 #20 TIM0_CC1 #19 TIM0_CC2 #18 TIM0_CDTI0 #17 TIM0_CDTI1 #16 TIM0_CDTI2 #15 TIM1_CC0 #20 TIM1_CC1 #19 TIM1_CC2 #18 TIM1_CC3 #17 WTIM0_CDTI0 #28 WTIM0_CDTI1 #26 WTIM0_CDTI2 #24 LETIM0_OUT0 #20 LETIM0_OUT1 #19 PCNT0_S0IN #20 PCNT0_S1IN #19	US0_TX #20 US0_RX #19 US0_CLK #18 US0_CS #17 US0_CTS #16 US0_RTS #15 US1_TX #20 US1_RX #19 US1_CLK #18 US1_CS #17 US1_CTS #16 US1_RTS #15 LEU0_TX #20 LEU0_RX #19 I2C0_SDA #20 I2C0_SCL #19	FRC_DCLK #20 FRC_DOUT #19 FRC_DFRAME #18 MODEM_DCLK #20 MODEM_DIN #19 MODEM_DOUT #18	PRS_CH3 #11 PRS_CH4 #3 PRS_CH5 #2 PRS_CH6 #14 ACMP0_O #20 ACMP1_O #20 LES_CH4

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PD13	VDAC0_OUT0ALT / OPA0_OUTALT #1 BUSCY BUSDX OPA1_P	TIM0_CC0 #21 TIM0_CC1 #20 TIM0_CC2 #19 TIM0_CDTI0 #18 TIM0_CDTI1 #17 TIM0_CDTI2 #16 TIM1_CC0 #21 TIM1_CC1 #20 TIM1_CC2 #19 TIM1_CC3 #18 WTIM0_CDTI0 #29 WTIM0_CDTI1 #27 WTIM0_CDTI2 #25 LETIM0_OUT0 #21 LETIM0_OUT1 #20 PCNT0_S0IN #21 PCNT0_S1IN #20	US0_TX #21 US0_RX #20 US0_CLK #19 US0_CS #18 US0_CTS #17 US0_RTS #16 US1_TX #21 US1_RX #20 US1_CLK #19 US1_CS #18 US1_CTS #17 US1_RTS #16 LEU0_TX #21 LEU0_RX #20 I2C0_SDA #21 I2C0_SCL #20	FRC_DCLK #21 FRC_DOUT #20 FRC_DFRAME #19 MODEM_DCLK #21 MODEM_DIN #20 MODEM_DOUT #19	PRS_CH3 #12 PRS_CH4 #4 PRS_CH5 #3 PRS_CH6 #15 ACMP0_O #21 ACMP1_O #21 LES_CH5
PD14	BUSDY BUSCX VDAC0_OUT1 / OPA1_OUT	TIM0_CC0 #22 TIM0_CC1 #21 TIM0_CC2 #20 TIM0_CDTI0 #19 TIM0_CDTI1 #18 TIM0_CDTI2 #17 TIM1_CC0 #22 TIM1_CC1 #21 TIM1_CC2 #20 TIM1_CC3 #19 WTIM0_CDTI0 #30 WTIM0_CDTI1 #28 WTIM0_CDTI2 #26 LETIM0_OUT0 #22 LETIM0_OUT1 #21 PCNT0_S0IN #22 PCNT0_S1IN #21	US0_TX #22 US0_RX #21 US0_CLK #20 US0_CS #19 US0_CTS #18 US0_RTS #17 US1_TX #22 US1_RX #21 US1_CLK #20 US1_CS #19 US1_CTS #18 US1_RTS #17 LEU0_TX #22 LEU0_RX #21 I2C0_SDA #22 I2C0_SCL #21	FRC_DCLK #22 FRC_DOUT #21 FRC_DFRAME #20 MODEM_DCLK #22 MODEM_DIN #21 MODEM_DOUT #20	CMU_CLK0 #5 PRS_CH3 #13 PRS_CH4 #5 PRS_CH5 #4 PRS_CH6 #16 ACMP0_O #22 ACMP1_O #22 LES_CH6 GPIO_EM4WU4
PD15	VDAC0_OUT0ALT / OPA0_OUTALT #2 BUSCY BUSDX OPA1_N	TIM0_CC0 #23 TIM0_CC1 #22 TIM0_CC2 #21 TIM0_CDTI0 #20 TIM0_CDTI1 #19 TIM0_CDTI2 #18 TIM1_CC0 #23 TIM1_CC1 #22 TIM1_CC2 #21 TIM1_CC3 #20 WTIM0_CDTI0 #31 WTIM0_CDTI1 #29 WTIM0_CDTI2 #27 LETIM0_OUT0 #23 LETIM0_OUT1 #22 PCNT0_S0IN #23 PCNT0_S1IN #22	US0_TX #23 US0_RX #22 US0_CLK #21 US0_CS #20 US0_CTS #19 US0_RTS #18 US1_TX #23 US1_RX #22 US1_CLK #21 US1_CS #20 US1_CTS #19 US1_RTS #18 LEU0_TX #23 LEU0_RX #22 I2C0_SDA #23 I2C0_SCL #22	FRC_DCLK #23 FRC_DOUT #22 FRC_DFRAME #21 MODEM_DCLK #23 MODEM_DIN #22 MODEM_DOUT #21	CMU_CLK1 #5 PRS_CH3 #14 PRS_CH4 #6 PRS_CH5 #5 PRS_CH6 #17 ACMP0_O #23 ACMP1_O #23 LES_CH7 DBG_SWO #2

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PF0	BUSBY BUSAX	TIM0_CC0 #24 TIM0_CC1 #23 TIM0_CC2 #22 TIM0_CDTI0 #21 TIM0_CDTI1 #20 TIM0_CDTI2 #19 TIM1_CC0 #24 TIM1_CC1 #23 TIM1_CC2 #22 TIM1_CC3 #21 WTIM0_CDTI1 #30 WTIM0_CDTI2 #28 LETIM0_OUT0 #24 LETIM0_OUT1 #23 PCNT0_S0IN #24 PCNT0_S1IN #23	US0_TX #24 US0_RX #23 US0_CLK #22 US0_CS #21 US0_CTS #20 US0_RTS #19 US1_TX #24 US1_RX #23 US1_CLK #22 US1_CS #21 US1_CTS #20 US1_RTS #19 US2_TX #14 US2_RX #13 US2_CLK #12 US2_CS #11 US2_CTS #10 US2_RTS #9 LEU0_TX #24 LEU0_RX #23 I2C0_SDA #24 I2C0_SCL #23	FRC_DCLK #24 FRC_DOUT #23 FRC_DFRAME #22 MODEM_DCLK #24 MODEM_DIN #23 MODEM_DOUT #22	PRS_CH0 #0 PRS_CH1 #7 PRS_CH2 #6 PRS_CH3 #5 ACMP0_O #24 ACMP1_O #24 DBG_SWCLKTCK BOOT_TX
PF1	BUSAY BUSBX	TIM0_CC0 #25 TIM0_CC1 #24 TIM0_CC2 #23 TIM0_CDTI0 #22 TIM0_CDTI1 #21 TIM0_CDTI2 #20 TIM1_CC0 #25 TIM1_CC1 #24 TIM1_CC2 #23 TIM1_CC3 #22 WTIM0_CDTI1 #31 WTIM0_CDTI2 #29 LETIM0_OUT0 #25 LETIM0_OUT1 #24 PCNT0_S0IN #25 PCNT0_S1IN #24	US0_TX #25 US0_RX #24 US0_CLK #23 US0_CS #22 US0_CTS #21 US0_RTS #20 US1_TX #25 US1_RX #24 US1_CLK #23 US1_CS #22 US1_CTS #21 US1_RTS #20 US2_TX #15 US2_RX #14 US2_CLK #13 US2_CS #12 US2_CTS #11 US2_RTS #10 LEU0_TX #25 LEU0_RX #24 I2C0_SDA #25 I2C0_SCL #24	FRC_DCLK #25 FRC_DOUT #24 FRC_DFRAME #23 MODEM_DCLK #25 MODEM_DIN #24 MODEM_DOUT #23	PRS_CH0 #1 PRS_CH1 #0 PRS_CH2 #7 PRS_CH3 #6 ACMP0_O #25 ACMP1_O #25 DBG_SWDIOTMS BOOT_RX
PF2	BUSBY BUSAX	TIM0_CC0 #26 TIM0_CC1 #25 TIM0_CC2 #24 TIM0_CDTI0 #23 TIM0_CDTI1 #22 TIM0_CDTI2 #21 TIM1_CC0 #26 TIM1_CC1 #25 TIM1_CC2 #24 TIM1_CC3 #23 WTIM0_CDTI2 #30 LETIM0_OUT0 #26 LETIM0_OUT1 #25 PCNT0_S0IN #26 PCNT0_S1IN #25	US0_TX #26 US0_RX #25 US0_CLK #24 US0_CS #23 US0_CTS #22 US0_RTS #21 US1_TX #26 US1_RX #25 US1_CLK #24 US1_CS #23 US1_CTS #22 US1_RTS #21 LEU0_TX #26 LEU0_RX #25 I2C0_SDA #26 I2C0_SCL #25	FRC_DCLK #26 FRC_DOUT #25 FRC_DFRAME #24 MODEM_DCLK #26 MODEM_DIN #25 MODEM_DOUT #24	CMU_CLK0 #6 PRS_CH0 #2 PRS_CH1 #1 PRS_CH2 #0 PRS_CH3 #7 ACMP0_O #26 ACMP1_O #26 DBG_TDO DBG_SWO #0 GPIO_EM4WU0

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PF3	BUSAY BUSBX	TIM0_CC0 #27 TIM0_CC1 #26 TIM0_CC2 #25 TIM0_CDTI0 #24 TIM0_CDTI1 #23 TIM0_CDTI2 #22 TIM1_CC0 #27 TIM1_CC1 #26 TIM1_CC2 #25 TIM1_CC3 #24 WTIM0_CDTI2 #31 LETIM0_OUT0 #27 LETIM0_OUT1 #26 PCNT0_S0IN #27 PCNT0_S1IN #26	US0_TX #27 US0_RX #26 US0_CLK #25 US0_CS #24 US0_CTS #23 US0_RTS #22 US1_TX #27 US1_RX #26 US1_CLK #25 US1_CS #24 US1_CTS #23 US1_RTS #22 US2_TX #16 US2_RX #15 US2_CLK #14 US2_CS #13 US2_CTS #12 US2_RTS #11 LEU0_TX #27 LEU0_RX #26 I2C0_SDA #27 I2C0_SCL #26	FRC_DCLK #27 FRC_DOUT #26 FRC_DFRAME #25 MODEM_DCLK #27 MODEM_DIN #26 MODEM_DOUT #25	CMU_CLK1 #6 PRS_CH0 #3 PRS_CH1 #2 PRS_CH2 #1 PRS_CH3 #0 ACMP0_O #27 ACMP1_O #27 DBG_TDI
PF4	BUSBY BUSAX	TIM0_CC0 #28 TIM0_CC1 #27 TIM0_CC2 #26 TIM0_CDTI0 #25 TIM0_CDTI1 #24 TIM0_CDTI2 #23 TIM1_CC0 #28 TIM1_CC1 #27 TIM1_CC2 #26 TIM1_CC3 #25 LE- TIM0_OUT0 #28 LE- TIM0_OUT1 #27 PCNT0_S0IN #28 PCNT0_S1IN #27	US0_TX #28 US0_RX #27 US0_CLK #26 US0_CS #25 US0_CTS #24 US0_RTS #23 US1_TX #28 US1_RX #27 US1_CLK #26 US1_CS #25 US1_CTS #24 US1_RTS #23 US2_TX #17 US2_RX #16 US2_CLK #15 US2_CS #14 US2_CTS #13 US2_RTS #12 LEU0_TX #28 LEU0_RX #27 I2C0_SDA #28 I2C0_SCL #27	FRC_DCLK #28 FRC_DOUT #27 FRC_DFRAME #26 MODEM_DCLK #28 MODEM_DIN #27 MODEM_DOUT #26	PRS_CH0 #4 PRS_CH1 #3 PRS_CH2 #2 PRS_CH3 #1 ACMP0_O #28 ACMP1_O #28

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PF5	BUSAY BUSBX	TIM0_CC0 #29 TIM0_CC1 #28 TIM0_CC2 #27 TIM0_CDTI0 #26 TIM0_CDTI1 #25 TIM0_CDTI2 #24 TIM1_CC0 #29 TIM1_CC1 #28 TIM1_CC2 #27 TIM1_CC3 #26 LE- TIM0_OUT0 #29 LE- TIM0_OUT1 #28 PCNT0_S0IN #29 PCNT0_S1IN #28	US0_TX #29 US0_RX #28 US0_CLK #27 US0_CS #26 US0_CTS #25 US0_RTS #24 US1_TX #29 US1_RX #28 US1_CLK #27 US1_CS #26 US1_CTS #25 US1_RTS #24 US2_TX #18 US2_RX #17 US2_CLK #16 US2_CS #15 US2_CTS #14 US2_RTS #13 LEU0_TX #29 LEU0_RX #28 I2C0_SDA #29 I2C0_SCL #28	FRC_DCLK #29 FRC_DOUT #28 FRC_DFRAME #27 MODEM_DCLK #29 MODEM_DIN #28 MODEM_DOUT #27	PRS_CH0 #5 PRS_CH1 #4 PRS_CH2 #3 PRS_CH3 #2 ACMP0_O #29 ACMP1_O #29
PF6	BUSBY BUSAX	TIM0_CC0 #30 TIM0_CC1 #29 TIM0_CC2 #28 TIM0_CDTI0 #27 TIM0_CDTI1 #26 TIM0_CDTI2 #25 TIM1_CC0 #30 TIM1_CC1 #29 TIM1_CC2 #28 TIM1_CC3 #27 LE- TIM0_OUT0 #30 LE- TIM0_OUT1 #29 PCNT0_S0IN #30 PCNT0_S1IN #29	US0_TX #30 US0_RX #29 US0_CLK #28 US0_CS #27 US0_CTS #26 US0_RTS #25 US1_TX #30 US1_RX #29 US1_CLK #28 US1_CS #27 US1_CTS #26 US1_RTS #25 US2_TX #19 US2_RX #18 US2_CLK #17 US2_CS #16 US2_CTS #15 US2_RTS #14 LEU0_TX #30 LEU0_RX #29 I2C0_SDA #30 I2C0_SCL #29	FRC_DCLK #30 FRC_DOUT #29 FRC_DFRAME #28 MODEM_DCLK #30 MODEM_DIN #29 MODEM_DOUT #28	CMU_CLK1 #7 PRS_CH0 #6 PRS_CH1 #5 PRS_CH2 #4 PRS_CH3 #3 ACMP0_O #30 ACMP1_O #30

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PF7	BUSAY BUSBX	TIM0_CC0 #31 TIM0_CC1 #30 TIM0_CC2 #29 TIM0_CDTI0 #28 TIM0_CDTI1 #27 TIM0_CDTI2 #26 TIM1_CC0 #31 TIM1_CC1 #30 TIM1_CC2 #29 TIM1_CC3 #28 LE-TIM0_OUT0 #31 LE-TIM0_OUT1 #30 PCNT0_S0IN #31 PCNT0_S1IN #30	US0_TX #31 US0_RX #30 US0_CLK #29 US0_CS #28 US0_CTS #27 US0_RTS #26 US1_TX #31 US1_RX #30 US1_CLK #29 US1_CS #28 US1_CTS #27 US1_RTS #26 US2_TX #20 US2_RX #19 US2_CLK #18 US2_CS #17 US2_CTS #16 US2_RTS #15 LEU0_TX #31 LEU0_RX #30 I2C0_SDA #31 I2C0_SCL #30	FRC_DCLK #31 FRC_DOUT #30 FRC_DFRAME #29 MODEM_DCLK #31 MODEM_DIN #30 MODEM_DOUT #29	CMU_CLKI0 #1 CMU_CLK0 #7 PRS_CH0 #7 PRS_CH1 #6 PRS_CH2 #5 PRS_CH3 #4 ACMP0_O #31 ACMP1_O #31 GPIO_EM4WU1

7.3 Alternate Functionality Overview

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings and the associated GPIO pin. Refer to 7.2 GPIO Functionality Table for a list of functions available on each GPIO pin.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 7.3. Alternate Functionality Overview

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
ACMP0_O	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Analog comparator ACMP0, digital output.
ACMP1_O	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Analog comparator ACMP1, digital output.
ADC0_EXTN	0: PA0								Analog to digital converter ADC0 external reference input negative pin.
ADC0_EXTP	0: PA1								Analog to digital converter ADC0 external reference input positive pin.
BOOT_RX	0: PF1								Bootloader RX.
BOOT_TX	0: PF0								Bootloader TX.
CMU_CLK0	0: PA1 1: PB15 2: PC6 3: PC11	4: PD9 5: PD14 6: PF2 7: PF7							Clock Management Unit, clock output number 0.
CMU_CLK1	0: PA0 1: PB14 2: PC7 3: PC10	4: PD10 5: PD15 6: PF3 7: PF6							Clock Management Unit, clock output number 1.
CMU_CLKI0	0: PB13 1: PF7 2: PC6	4: PA5							Clock Management Unit, clock input number 0.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
DBG_SWCLKTCK	0: PF0								Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down.
DBG_SWDIOTMS	0: PF1								Debug-interface Serial Wire data input / output and JTAG Test Mode Select. Note that this function is enabled to the pin out of reset, and has a built-in pull up.
DBG_SWO	0: PF2 1: PB13 2: PD15 3: PC11								Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
DBG_TDI	0: PF3								Debug-interface JTAG Test Data In. Note that this function becomes available after the first valid JTAG command is received, and has a built-in pull up when JTAG is active.
DBG_TDO	0: PF2								Debug-interface JTAG Test Data Out. Note that this function becomes available after the first valid JTAG command is received.
ETM_TCLK	1: PA5 3: PC6								Embedded Trace Module ETM clock .
ETM_TD0	3: PC7								Embedded Trace Module ETM data 0.

Alternate	LOCATION							
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
ETM_TD1	3: PC8								Embedded Trace Module ETM data 1.
ETM_TD2	3: PC9								Embedded Trace Module ETM data 2.
ETM_TD3	3: PC10								Embedded Trace Module ETM data 3.
FRC_DCLK	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Frame Controller, Data Sniffer Clock.
FRC_DFRAME	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Frame Controller, Data Sniffer Frame active
FRC_DOUT	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Frame Controller, Data Sniffer Output.
GPIO_EM4WU0	0: PF2								Pin can be used to wake the system up from EM4
GPIO_EM4WU1	0: PF7								Pin can be used to wake the system up from EM4
GPIO_EM4WU4	0: PD14								Pin can be used to wake the system up from EM4
GPIO_EM4WU8	0: PA3								Pin can be used to wake the system up from EM4
GPIO_EM4WU9	0: PB13								Pin can be used to wake the system up from EM4
GPIO_EM4WU12	0: PC10								Pin can be used to wake the system up from EM4
I2C0_SCL	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	I2C0 Serial Clock Line input / output.

Alternate	LOCATION								
Functionality	**0 - 3**	**4 - 7**	**8 - 11**	**12 - 15**	**16 - 19**	**20 - 23**	**24 - 27**	**28 - 31**	**Description**
I2C0_SDA	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	I2C0 Serial Data input / output.
I2C1_SCL					18: PC10 19: PC11				I2C1 Serial Clock Line input / output.
I2C1_SDA					19: PC10	20: PC11			I2C1 Serial Data input / output.
LES_CH1	0: PD9								LESENSE channel 1.
LES_CH2	0: PD10								LESENSE channel 2.
LES_CH3	0: PD11								LESENSE channel 3.
LES_CH4	0: PD12								LESENSE channel 4.
LES_CH5	0: PD13								LESENSE channel 5.
LES_CH6	0: PD14								LESENSE channel 6.
LES_CH7	0: PD15								LESENSE channel 7.
LES_CH8	0: PA0								LESENSE channel 8.
LES_CH9	0: PA1								LESENSE channel 9.
LES_CH10	0: PA2								LESENSE channel 10.
LES_CH11	0: PA3								LESENSE channel 11.
LES_CH12	0: PA4								LESENSE channel 12.
LES_CH13	0: PA5								LESENSE channel 13.
LETIM0_OUT0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Low Energy Timer LETIM0, output channel 1.

Alternate	LOCATION								
Functionality	**0 - 3**	**4 - 7**	**8 - 11**	**12 - 15**	**16 - 19**	**20 - 23**	**24 - 27**	**28 - 31**	**Description**
LEU0_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	LEUART0 Receive input.
LEU0_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	0: PB14								Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	0: PB15								Low Frequency Crystal (typically 32.768 kHz) positive pin.
MODEM_DCLK	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	MODEM data clock out.
MODEM_DIN	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	MODEM data in.
MODEM_DOUT	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	MODEM data out.
OPA0_N	0: PA4								Operational Amplifier 0 external negative input.
OPA0_P	0: PA2								Operational Amplifier 0 external positive input.
OPA1_N	0: PD15								Operational Amplifier 1 external negative input.
OPA1_P	0: PD13								Operational Amplifier 1 external positive input.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
OPA2_N	0: PB13								Operational Amplifier 2 external negative input.
OPA2_OUT	0: PB12								Operational Amplifier 2 output.
OPA2_P	0: PB11								Operational Amplifier 2 external positive input.
PCNT0_S0IN	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Pulse Counter PCNT0 input number 1.
PRS_CH0	0: PF0 1: PF1 2: PF2 3: PF3	4: PF4 5: PF5 6: PF6 7: PF7	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11					Peripheral Reflex System PRS, channel 0.
PRS_CH1	0: PF1 1: PF2 2: PF3 3: PF4	4: PF5 5: PF6 6: PF7 7: PF0							Peripheral Reflex System PRS, channel 1.
PRS_CH2	0: PF2 1: PF3 2: PF4 3: PF5	4: PF6 5: PF7 6: PF0 7: PF1							Peripheral Reflex System PRS, channel 2.
PRS_CH3	0: PF3 1: PF4 2: PF5 3: PF6	4: PF7 5: PF0 6: PF1 7: PF2	8: PD9 9: PD10 10: PD11 11: PD12	12: PD13 13: PD14 14: PD15					Peripheral Reflex System PRS, channel 3.
PRS_CH4	0: PD9 1: PD10 2: PD11 3: PD12	4: PD13 5: PD14 6: PD15							Peripheral Reflex System PRS, channel 4.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
PRS_CH5	0: PD10 1: PD11 2: PD12 3: PD13	4: PD14 5: PD15 6: PD9							Peripheral Reflex System PRS, channel 5.
PRS_CH6	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PD9	12: PD10 13: PD11 14: PD12 15: PD13	16: PD14 17: PD15				Peripheral Reflex System PRS, channel 6.
PRS_CH7	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PA0						Peripheral Reflex System PRS, channel 7.
PRS_CH8	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PA0 10: PA1						Peripheral Reflex System PRS, channel 8.
PRS_CH9	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PA0 9: PA1 10: PA2 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11				Peripheral Reflex System PRS, channel 9.
PRS_CH10	0: PC6 1: PC7 2: PC8 3: PC9	4: PC10 5: PC11							Peripheral Reflex System PRS, channel 10.
PRS_CH11	0: PC7 1: PC8 2: PC9 3: PC10	4: PC11 5: PC6							Peripheral Reflex System PRS, channel 11.
TIM0_CC0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Timer 0 Capture Compare input / output channel 1.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
TIM0_CC2	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD9 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	Timer 0 Complimentary Dead Time Insertion channel 0.
TIM0_CDTI1	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 13: PD9 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	Timer 0 Complimentary Dead Time Insertion channel 1.
TIM0_CDTI2	0: PA5 1: PB11 2: PB12 3: PB13	4: PB14 5: PB15 6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11	12: PD9 13: PD10 14: PD11 15: PD12	16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	Timer 0 Complimentary Dead Time Insertion channel 2.
TIM1_CC0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Timer 1 Capture Compare input / output channel 2.
TIM1_CC3	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD9 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	Timer 1 Capture Compare input / output channel 3.
US0_CLK	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	USART0 clock input / output.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
US0_CS	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD9 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	USART0 chip select input / output.
US0_CTS	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 13: PD9 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	USART0 Clear To Send hardware flow control input.
US0_RTS	0: PA5 1: PB11 2: PB12 3: PB13	4: PB14 5: PB15 6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11	12: PD9 13: PD10 14: PD11 15: PD12	16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	USART0 Request To Send hardware flow control output.
US0_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	USART1 clock input / output.
US1_CS	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD9 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	USART1 chip select input / output.
US1_CTS	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 13: PD9 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	USART1 Clear To Send hardware flow control input.

Alternate	LOCATION								
Functionality	**0 - 3**	**4 - 7**	**8 - 11**	**12 - 15**	**16 - 19**	**20 - 23**	**24 - 27**	**28 - 31**	**Description**
US1_RTS	0: PA5 1: PB11 2: PB12 3: PB13	4: PB14 5: PB15 6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11	12: PD9 13: PD10 14: PD11 15: PD12	16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	USART1 Request To Send hardware flow control output.
US1_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK				12: PF0 13: PF1 14: PF3 15: PF4	16: PF5 17: PF6 18: PF7			30: PA5	USART2 clock input / output.
US2_CS			11: PF0	12: PF1 13: PF3 14: PF4 15: PF5	16: PF6 17: PF7			29: PA5	USART2 chip select input / output.
US2_CTS			10: PF0 11: PF1	12: PF3 13: PF4 14: PF5 15: PF6	16: PF7			28: PA5	USART2 Clear To Send hardware flow control input.
US2_RTS			9: PF0 10: PF1 11: PF3	12: PF4 13: PF5 14: PF6 15: PF7			27: PA5		USART2 Request To Send hardware flow control output.
US2_RX				13: PF0 14: PF1 15: PF3	16: PF4 17: PF5 18: PF6 19: PF7			31: PA5	USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
US2_TX	0: PA5			14: PF0 15: PF1	16: PF3 17: PF4 18: PF5 19: PF6	20: PF7			USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
VDAC0_EXT	0: PA1								Digital to analog converter VDAC0 external reference input pin.
VDAC0_OUT0 / OPA0_OUT	0: PA3								Digital to Analog Converter DAC0 output channel number 0.
VDAC0_OUT0ALT / OPA0_OUT-ALT	0: PA5 1: PD13 2: PD15								Digital to Analog Converter DAC0 alternative output for channel 0.
VDAC0_OUT1 / OPA1_OUT	0: PD14								Digital to Analog Converter DAC0 output channel number 1.
VDAC0_OUT1ALT / OPA1_OUT-ALT	0: PD12 1: PA2 2: PA4								Digital to Analog Converter DAC0 alternative output for channel 1.
WTIM0_CC0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5		15: PB11	16: PB12 17: PB13 18: PB14 19: PB15		26: PC6 27: PC7	28: PC8 29: PC9 30: PC10 31: PC11	Wide timer 0 Capture Compare input / output channel 0.
WTIM0_CC1	0: PA2 1: PA3 2: PA4 3: PA5			13: PB11 14: PB12 15: PB13	16: PB14 17: PB15		24: PC6 25: PC7 26: PC8 27: PC9	28: PC10 29: PC11 31: PD9	Wide timer 0 Capture Compare input / output channel 1.
WTIM0_CC2	0: PA4 1: PA5		11: PB11	12: PB12 13: PB13 14: PB14 15: PB15		22: PC6 23: PC7	24: PC8 25: PC9 26: PC10 27: PC11	29: PD9 30: PD10 31: PD11	Wide timer 0 Capture Compare input / output channel 2.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
WTIM0_CDTI0		7: PB11	8: PB12 9: PB13 10: PB14 11: PB15		18: PC6 19: PC7	20: PC8 21: PC9 22: PC10 23: PC11	25: PD9 26: PD10 27: PD11	28: PD12 29: PD13 30: PD14 31: PD15	Wide timer 0 Complimentary Dead Time Insertion channel 0.
WTIM0_CDTI1		5: PB11 6: PB12 7: PB13	8: PB14 9: PB15		16: PC6 17: PC7 18: PC8 19: PC9	20: PC10 21: PC11 23: PD9	24: PD10 25: PD11 26: PD12 27: PD13	28: PD14 29: PD15 30: PF0 31: PF1	Wide timer 0 Complimentary Dead Time Insertion channel 1.
WTIM0_CDTI2	3: PB11	4: PB12 5: PB13 6: PB14 7: PB15		14: PC6 15: PC7	16: PC8 17: PC9 18: PC10 19: PC11	21: PD9 22: PD10 23: PD11	24: PD12 25: PD13 26: PD14 27: PD15	28: PF0 29: PF1 30: PF2 31: PF3	Wide timer 0 Complimentary Dead Time Insertion channel 2.

7.4 Analog Port (APORT) Client Maps

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, DACs, etc. The APORT consists of a set of shared buses, switches, and control logic needed to configurably implement the signal routing. Figure 7.2 APORT Connection Diagram on page 99 shows the APORT routing for this device family (note that available features may vary by part number). A complete description of APORT functionality can be found in the Reference Manual.

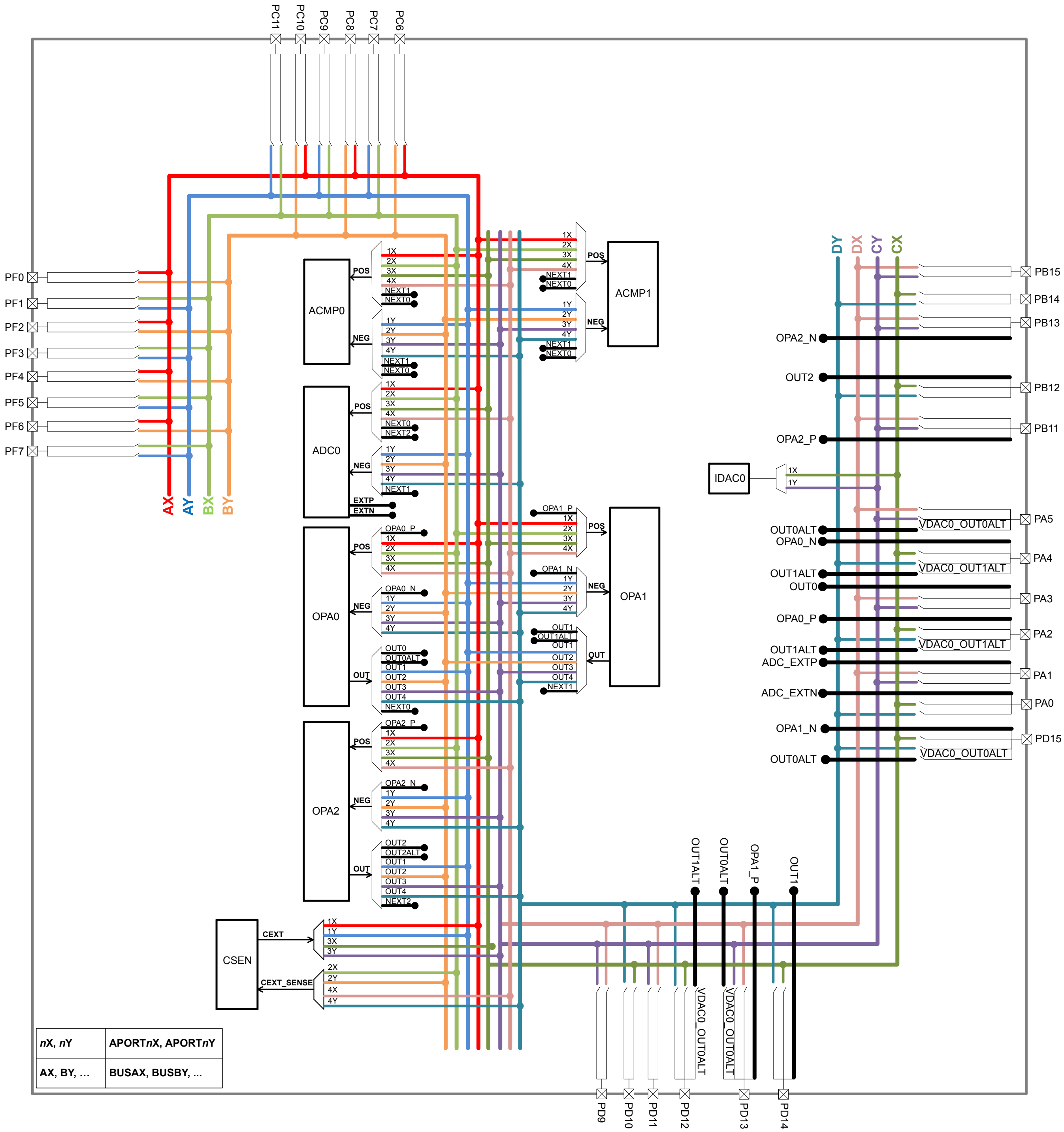


Figure 7.2. APORT Connection Diagram

Client maps for each analog circuit using the APORT are shown in the following tables. The maps are organized by bus, and show the peripheral's port connection, the shared bus, and the connection from specific bus channel numbers to GPIO pins.

In general, enumerations for the pin selection field in an analog peripheral's register can be determined by finding the desired pin connection in the table and then combining the value in the Port column (APORT__), and the channel identifier (CH__). For example, if pin PF7 is available on port APORT2X as CH23, the register field enumeration to connect to PF7 would be APORT2XCH23. The shared bus used by this connection is indicated in the Bus column.

Table 7.4. ACMP0 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT1X	BUSAX										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT1Y	BUSAY									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2X	BUSBX									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2Y	BUSBY										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT3X	BUSCX		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		
APORT3Y	BUSCY	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4X	BUSDX	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		

Table 7.5. ACMP1 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT1X	BUSAX										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT1Y	BUSAY									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2X	BUSBX									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2Y	BUSBY										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT3X	BUSCX		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		
APORT3Y	BUSCY	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4X	BUSDX	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		

Table 7.6. ADC0 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT1X	BUSAX										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT1Y	BUSAY									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2X	BUSBX									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2Y	BUSBY										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT3X	BUSCX		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		
APORT3Y	BUSCY	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4X	BUSDX	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		

Table 7.7. CSEN Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
CEXT																																	
APORT1X	BUSAX										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT1Y	BUSAY									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT3X	BUSCX		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		
APORT3Y	BUSCY	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
CEXT_SENSE																																	
APORT2X	BUSBX									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2Y	BUSBY										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT4X	BUSDX	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		

Table 7.8. IDAC0 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT1X	BUSCX		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		
APORT1Y	BUSCY	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	

Table 7.9. VDAC0 / OPA Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
OPA0_N																																	
APORT1Y	BUSAY									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2Y	BUSBY										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT3Y	BUSCY	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		
OPA0_P																																	
APORT1X	BUSAX										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT2X	BUSBX									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT3X	BUSCX		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		
APORT4X	BUSDX	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
OPA1_N																																	
APORT1Y	BUSAY									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2Y	BUSBY										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT3Y	BUSCY	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		
OPA1_P																																	
APORT1X	BUSAX										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT2X	BUSBX									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT3X	BUSCX		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		
APORT4X	BUSDX	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
OPA2_N																																	
APORT1Y	BUSAY									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2Y	BUSBY										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT3Y	BUSCY	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
OPA2_OUT																																	
APORT1Y	BUSAY									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2Y	BUSBY										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT3Y	BUSCY	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		
OPA2_P																																	
APORT1X	BUSAX										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT2X	BUSBX									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT3X	BUSCX		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		
APORT4X	BUSDX	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
VDAC0_OUT0 / OPA0_OUT																																	
APORT1Y	BUSAY									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2Y	BUSBY										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT3Y	BUSCY	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
VDAC0_OUT1 / OPA1_OUT																																	
APORT1Y	BUSAY									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2Y	BUSBY										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT3Y	BUSCY	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		

8. Package Specifications

8.1 BGM13S Package Dimensions

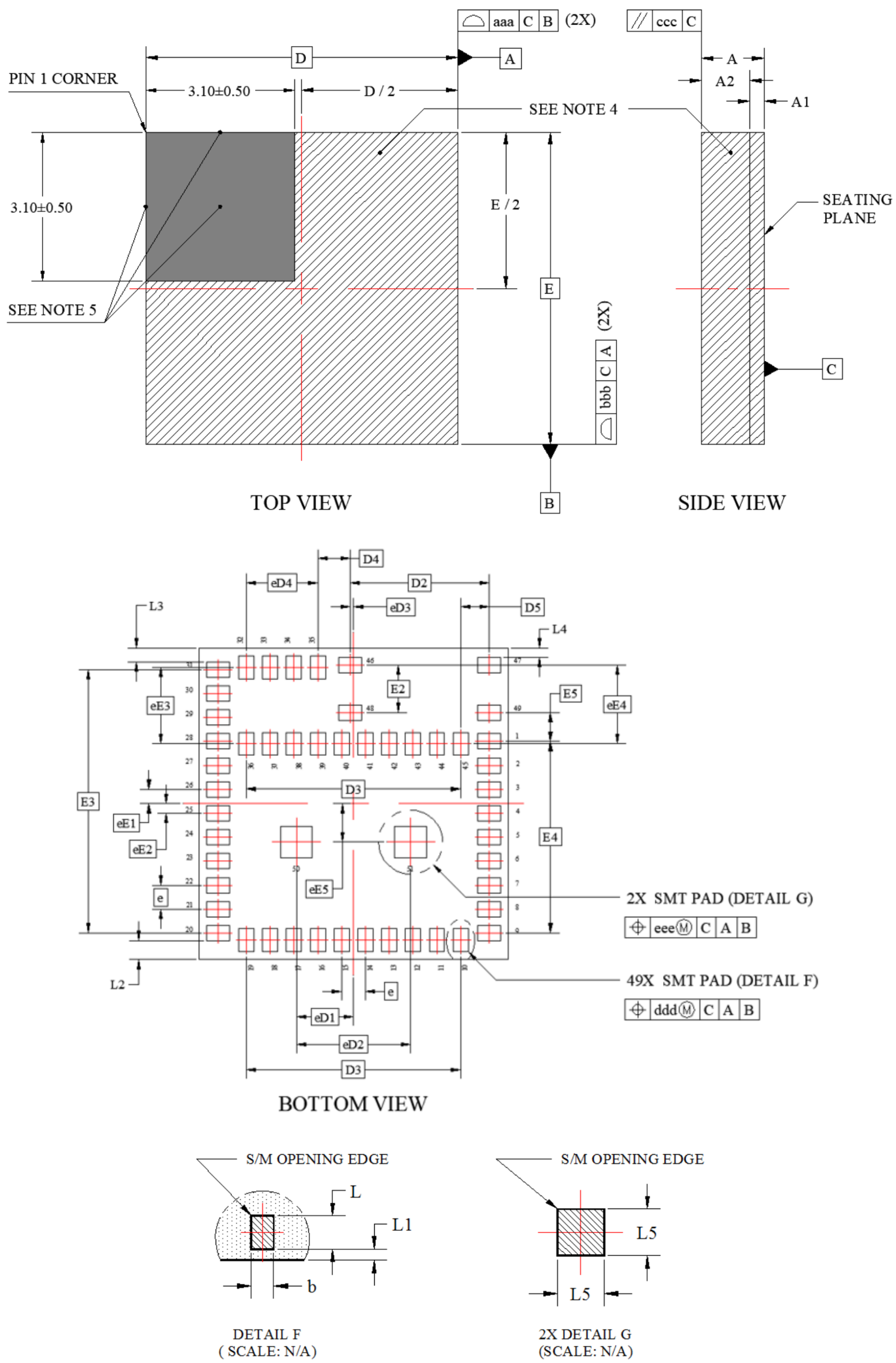


Figure 8.1. BGM13S Package Dimensions

Dimension	MIN	NOM	MAX
A	1.20	1.30	1.40
A1	0.26	0.30	0.34
A2	0.95	1.00	1.05
b	0.27	0.32	0.37

Dimension	MIN	NOM	MAX
D		6.50 BSC	
D2		2.92 BSC	
D3		4.50 BSC	
D4		0.68 BSC	
D5		0.60 BSC	
e		0.50 BSC	
E		6.50 BSC	
E2		1.00 BSC	
E3		5.50 BSC	
E4		4.00 BSC	
E5		0.60 BSC	
L	0.43	0.48	0.53
L1	0.11	0.16	0.21
L2	0.34	0.39	0.44
L3	0.24	0.29	0.34
L4	0.14	0.19	0.24
L5	0.62	0.67	0.72
eD1		1.20 BSC	
eD2		2.40 BSC	
eD3		0.07 BSC	
eD4		1.50 BSC	
eE1		0.30 BSC	
eE2		0.20 BSC	
eE3		1.60 BSC	
eE4		1.65 BSC	
eE5		0.80 BSC	
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.10	
eee		0.10	

Dimension	MIN	NOM	MAX
Note: 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Tolerances are: a. Decimal: X.X = ±0.1 X.XX = ±0.05 X.XXX = ±0.03 b. Angular: ±0.1 Degrees 3. Dimensioning and Tolerancing per ANSI Y14.5M-1994. 4. This drawing conforms to the JEDEC Solid State Outline MO-220. 5. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components. 6. Hatching lines means package shielding area. 7. Solid pattern (3.1x3.1mm) shows non-shielding area including its side walls. For side wall, borderline between shielding area and not-shielding area could not be defined clearly like top side.			

8.2 BGM13S Recommeded PCB Land Pattern

This section describes the recommended PCB land pattern for the BGM13S. The antenna copper clearance area is shown in Figure 8.2 BGM13S Recommended Antenna Clearance on page 111, while the X-Y cordinates of pads relative to the origin are shown in Table 8.1 BGM13S Pad Coordinates and Sizing on page 112. The origin is the center point of pin number 47. It is very important to align the antenna area relative to the module pads precisely.

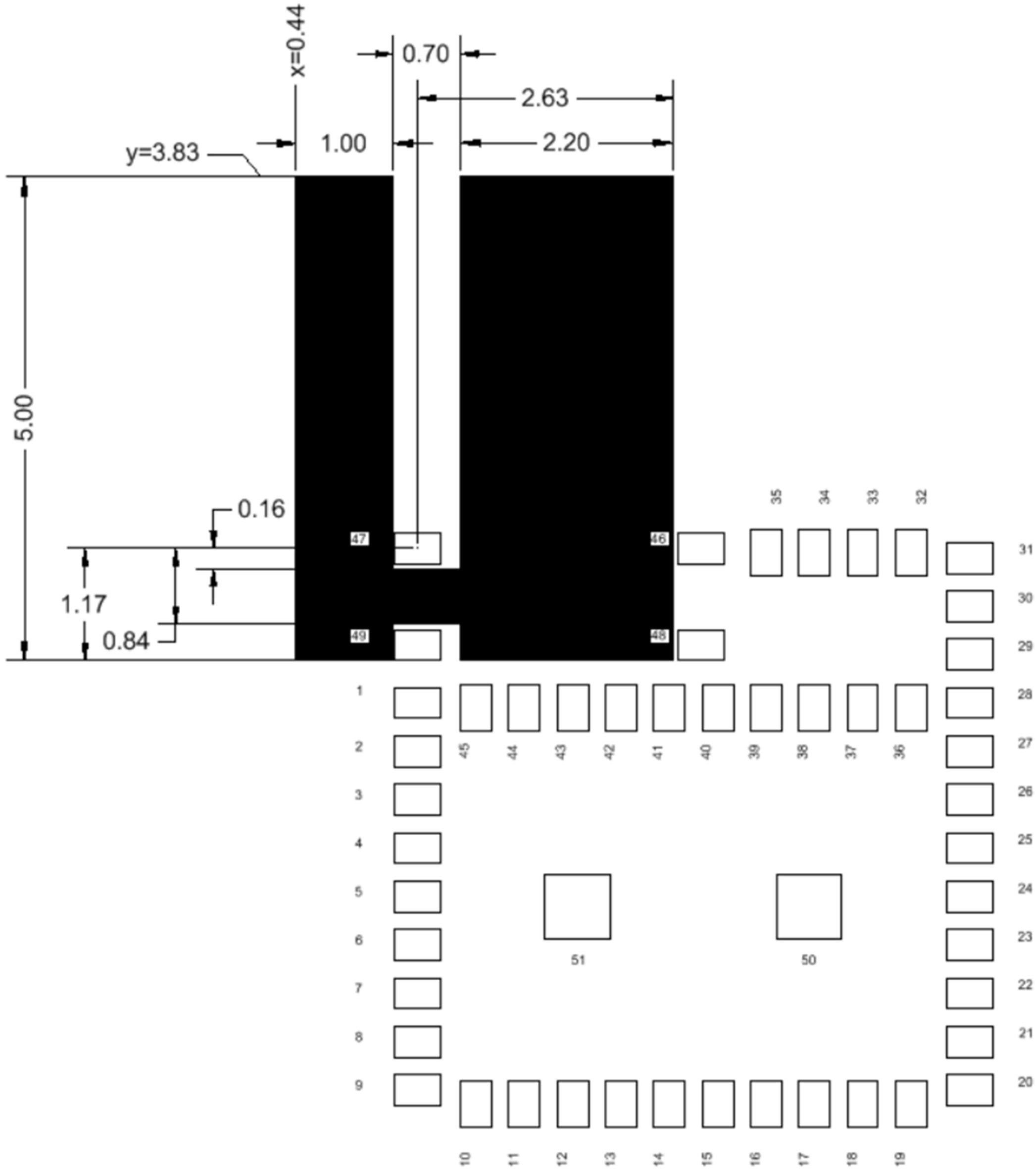


Figure 8.2. BGM13S Recommended Antenna Clearance

Table 8.1. BGM13S Pad Coordinates and Sizing

Pad No.	Pad coordinates (X,Y)	Pad size (mm)
47	Pad Center, Origin (0,0)	0.32 x 0.48
1	(0,-1.60)	
2	(0,-2.10)	
9	(0,-5.60)	
10	(0.60,-5.75)	
19	(5.10,-5.75)	
20	(5.70,-5.60)	
31	(5.70,-0.10)	
32	(5.10,-0.05)	
36	(5.10,-1.65)	
45	(0.60,-1.65)	
49	(0,-1.00)	
46	(2.92,0)	
50	1.65,-3.70)	0.67 x 0.67
51	4.05,-3.70)	

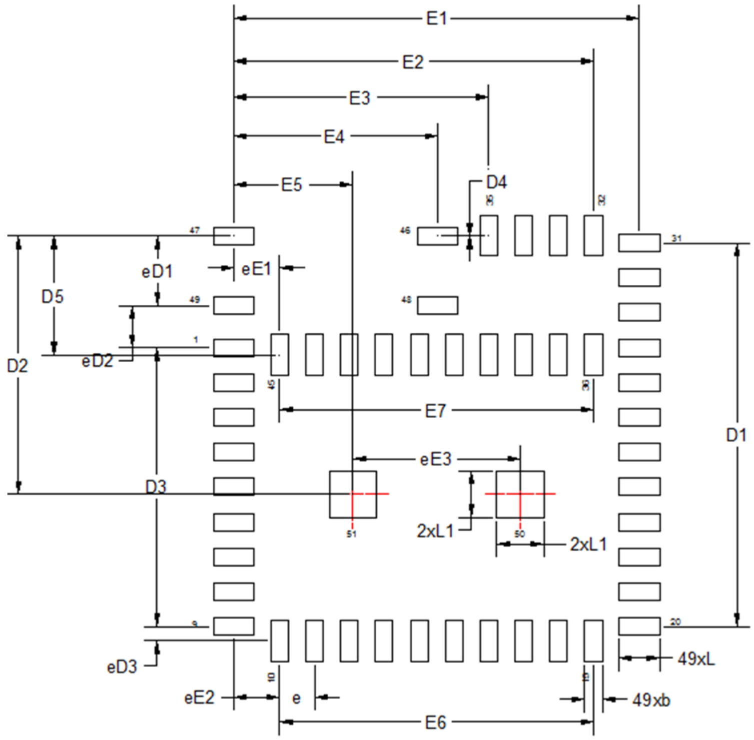


Figure 8.3. BGM13S Recommended PCB Land Pattern

Table 8.2. BGM13S Recommended PCB Land Pattern

Symbol	NOM (mm)
b	0.32 BSC
D1	5.50 BSC
D2	3.70 BSC
D3	4.00 BSC
D4	0.05 BSC
D5	1.65 BSC
eD1	1.00 BSC
eD2	0.60 BSC
eD3	0.15 BSC
e	0.50 BSC
E1	5.70 BSC
E2	5.10 BSC
E3	3.60 BSC
E4	2.92 BSC
E5	1.65 BSC
E6	4.50 BSC
E7	4.50 BSC
L	0.48 BSC

Symbol	NOM (mm)
L1	0.67 BSC
eE1	0.60 BSC
eE2	0.60 BSC
eE3	2.40 BSC

Notes:

1. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05mm is assumed.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
4. The stencil thickness should be 0.100mm (4 mils).
5. The stencil aperture to land pad size recommendation is 70% paste coverage.
6. Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.

8.3 BGM13S Package Marking

The figure below shows the package markings printed on the module.

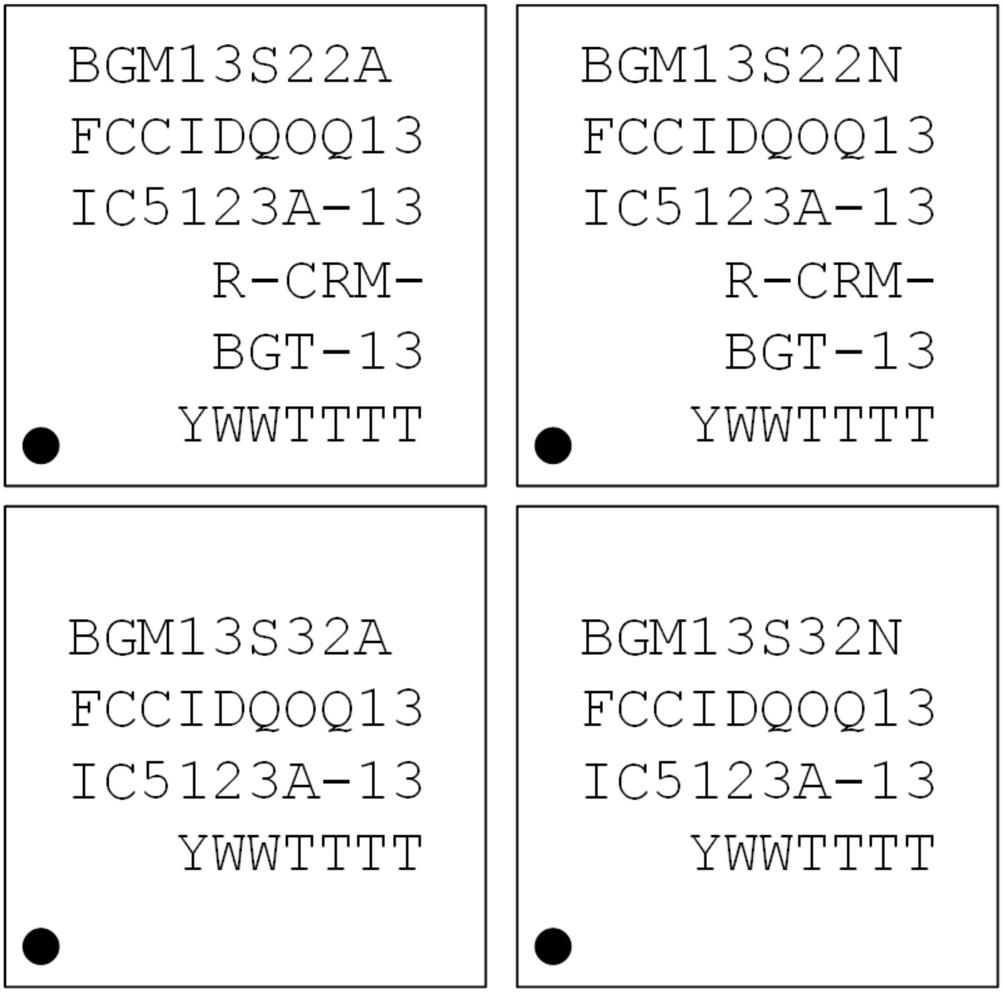


Figure 8.4. BGM13S Package Marking

Explanations:

Marking	Explanation
BGM13Sxxx	Model Number
FCCIDQOQ13	FCC Certification ID
IC5123A-13	IC5123A-13
R-CRM-BGT-13	KC (Korea) Certification ID
YWWTTTT	1. Y = Manufacturing Year 2. WW = Manufacturing Work Week 3. TTTT = Trace Code

9. Soldering Recommendations

9.1 Soldering Recommendations

The BGM13S is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven, and particular type of solder paste used.

- Refer to technical documentations of particular solder paste for profile configurations.
- Avoid usining more than two reflow cycles.
- A no-clean, type-3 solder paste is recommended.
- A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- Recommended stencil thickness is 0.100mm (4 mils).
- Refer to the recommended PCB land pattern for an example stencil aperture size.
- For further recommendation, please refer to the JEDEC/IPC J-STD-020, IPC-SM-782 and IPC 7351 guidelines.
- Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.

10. Certifications

10.1 Qualified Antenna Types

The BGM13S variants supporting an external antenna have been designed to operate with a standard 2.14 dBi dipole antenna. Any antenna of a different type or with a gain higher than 2.14 dBi is strictly prohibited for use with this device. Using an antenna of a different type or gain more than 2.14 dBi will require additional testing for FCC, CE and IC. The required antenna impedance is 50 Ω.

Table 10.1. Qualified Antennas for BGM13S

Antenna Type	Maximum Gain
Dipole	2.14 dBi

10.2 Bluetooth

The BGM13S is pre-qualified as a Low Energy RF-PHY tested component, having Declaration ID of TBD and QDID of TBD. For the qualification of an end product embedding the BGM13S, the above should be combined with the most up to date Wireless Gecko Link Layer and Host components.

10.3 CE

The BGM13S22 module is in conformity with the essential requirements and other relevant requirements of the Radio Equipment Directive (RED) (2014/53/EU). Please note that every application using the BGM13S22 will need to perform the radio EMC tests on the end product, according to EN 301 489-17. It is ultimately the responsibility of the manufacturer to ensure the compliance of the end-product. The specific product assembly may have an impact to RF radiated characteristics, and manufacturers should carefully consider RF radiated testing with the end-product assembly. A formal DoC is available via www.silabs.com

The BGM13S32 module is in conformity with the essential requirements and other relevant requirements of the Radio Equipment Directive(RED) at nominal 10 dBm transmit power.

The transmit power of the module is not limited and when an end product is using BGM13S32, the end product manufacturer is responsible that the end product is in conformity of all relevant requirements of the RED.

10.4 FCC

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesirable operation.

Any changes or modifications not expressly approved by Silicon Labs could void the user's authority to operate the equipment.

FCC RF Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure compliance. This transmitter meets both portable and mobile limits as demonstrated in the RF Exposure Analysis. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

OEM Responsibilities to comply with FCC Regulations:

OEM integrator is responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

- With BGM13S32 the antenna(s) must be installed such that a minimum separation distance of 50.5 mm is maintained between the radiator (antenna) and all persons at all times.
- With BGM13S22 the antenna(s) must be installed such that a minimum separation distance of 0 mm is maintained between the radiator (antenna) and all persons at all times.
- The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

Important Note:

In the event that the above conditions cannot be met (for certain configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End Product Labeling

The variants of BGM13S Modules are labeled with their own FCC ID. If the FCC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final end product must be labeled in a visible area with the following:

"Contains Transmitter Module FCC ID: QOQ13"

Or

"Contains FCC ID: QOQ13"

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product.

10.5 ISED Canada

ISEDC

This radio transmitter (IC: 5123A-13) has been approved by Industry Canada to operate with the antenna types listed above, with the maximum permissible gain indicared. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

This device complies with Industry Canada's license-exempt RSS standards. Operation is subject to the following two conditions:

1. This device may not cause interference; and
2. This device must accept any interference, including interference that may cause undesired operation of the device

RF Exposure Statement

Exception from routine SAR evaluation limits are given in RSS-102 Issue 5.

The models BGM13S32A and BGM13S32N meet the given requirements when the minimum separation distance to human body is 40 mm.

The models BGM13S22A and BGM13S22N meet the given requirements when the minimum separation distance to human body is 20 mm.

RF exposure or SAR evaluation is not required when the separation distance is same or more than stated above. If the separation distance is less than stated above the OEM integrator is responsible for evaluating the SAR.

OEM Responsibilities to comply with IC Regulations

The BGM13S modules have been certified for integration into products only by OEM integrators under the following conditions:

- The antenna(s) must be installed such that a minimum separation distance as stated above is maintained between the radiator (antenna) and all persons at all times.
- The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter.

As long as the two conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

IMPORTANT NOTE

In the event that these conditions cannot be met (for certain configurations or co-location with another transmitter), then the ISEDC authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate ISEDC authorization.

End Product Labeling

The BGM13S module is labeled with its own IC ID. If the IC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final end product must be labeled in a visible area with the following:

"**Contains Transmitter Module IC: 5123A-13** "

or

"**Contains IC: 5123A-13"**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product.

ISEDC (Français)

Industrie Canada a approuvé l'utilisation de cet émetteur radio (IC: 5123A-13) en conjonction avec des antennes de type dipolaire à 2.14dBi ou des antennes embarquées, intégrée au produit. L'utilisation de tout autre type d'antenne avec ce composant est proscrite.

Ce composant est conforme aux normes RSS, exonérées de licence d'Industrie Canada. Son mode de fonctionnement est soumis aux deux conditions suivantes:

1. Ce composant ne doit pas générer d'interférences.
2. Ce composant doit pouvoir est soumis à tout type de perturbation y compris celle pouvant nuire à son bon fonctionnement.

Déclaration d'exposition RF

L'exception tirée des limites courantes d'évaluation SAR est donnée dans le document RSS-102 Issue 5.

Les modules BGM13S32A and BGM13S32N répondent aux exigences requises lorsque la distance minimale de séparation avec le corps humain est de 40 mm.

Les modules BGM13S22A and BGM13S22N répondent aux exigences requises lorsque la distance minimale de séparation avec le corps humain est de 20 mm.

La déclaration d'exposition RF ou l'évaluation SAR n'est pas nécessaire lorsque la distance de séparation est identique ou supérieure à celle indiquée ci-dessus. Si la distance de séparation est inférieure à celle mentionnées plus haut, il incombe à l'intégrateur OEM de procédé à une évaluation SAR.

Responsabilités des OEM pour une mise en conformité avec le Règlement du Circuit Intégré

Le module BGM13S a été approuvé pour l'intégration dans des produits finaux exclusivement réalisés par des OEM sous les conditions suivantes:

- L'antenne (s) doit être installée de sorte qu'une distance de séparation minimale indiquée ci-dessus soit maintenue entre le radiateur (antenne) et toutes les personnes avoisinante, ce à tout moment.
- Le module émetteur ne doit pas être localisé ou fonctionner avec une autre antenne ou un autre transmetteur que celle indiquée plus haut.

Tant que les deux conditions ci-dessus sont respectées, il n'est pas nécessaire de tester ce transmetteur de façon plus poussée. Cependant, il incombe à l'intégrateur OEM de s'assurer de la bonne conformité du produit fini avec les autres normes auxquelles il pourrait être soumis de fait de l'utilisation de ce module (par exemple, les émissions des périphériques numériques, les exigences de périphériques PC, etc.).

REMARQUE IMPORTANTE

ans le cas où ces conditions ne peuvent être satisfaites (pour certaines configurations ou co-implantation avec un autre émetteur), l'autorisation ISEDC n'est plus considérée comme valide et le numéro d'identification ID IC ne peut pas être apposé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera responsable de la réévaluation du produit final (y compris le transmetteur) et de l'obtention d'une autorisation ISEDC distincte.

Étiquetage des produits finis

Les modules BGM13S sont étiquetés avec leur propre ID IC. Si l'ID IC n'est pas visible lorsque le module est intégré au sein d'un autre produit, cet autre produit dans lequel le module est installé devra porter une étiquette faisant apparaitre les référence du module intégré. Dans un tel cas, sur le produit final doit se trouver une étiquette aisément lisible sur laquelle figurent les informations suivantes:

"**Contient le module transmetteur: 5123A-13** "

or

"**Contient le circuit: 5123A-13"**

L'intégrateur OEM doit être conscient qu'il ne doit pas fournir, dans le manuel d'utilisation, d'informations relatives à la façon d'installer ou de d'enlever ce module RF ainsi que sur la procédure à suivre pour modifier les paramètres liés à la radio.

10.6 Japan

The BGM13S22A and BGM13S22N are certified in Japan with certification number TBD.

Since September 1, 2014 it is allowed (and highly recommended) that a manufacturer who integrates a radio module in their host equipment can place the certification mark and certification number (the same marking/number as depicted on the label of the radio module) on the outside of the host equipment. The certification mark and certification number must be placed close to the text in the Japanese language which is provided below. This change in the Radio Law has been made in order to enable users of the combination of host and radio module to verify if they are actually using a radio device which is approved for use in Japan.

Certification Text to be Placed on the Outside Surface of the Host Equipment:

当該機器には電波法に基づく、技術基準適合証明等を受けた特定無線設備を装着している。

Translation of the text:

“This equipment contains specified radio equipment that has been certified to the Technical Regulation Conformity Certification under the Radio Law.”

The "Giteki" marking shown in the figures below must be affixed to an easily noticeable section of the specified radio equipment. Note that additional information may be required if the device is also subject to a telecom approval.

Figure 10.1. GITEKI Mark and ID

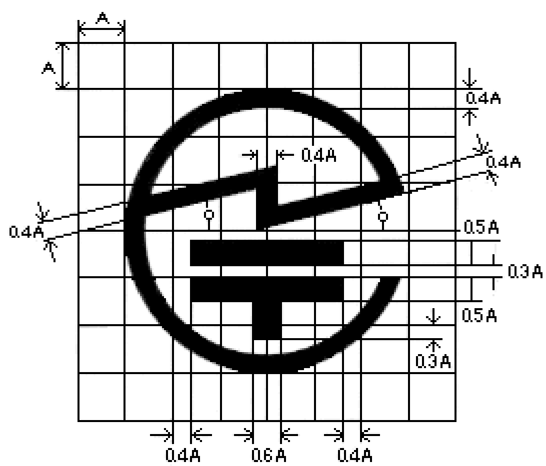


Figure 10.2. GITEKI Mark

11. Revision History

Revision 1.0

October 2018

- Added PLFRCO back to block diagrams and overview.
- Added Electrical Specifications Tables for PLFRCO, VDAC, CSEN, OPAMP, PCNT and APORT.
- 5.1 Typical BGM13S Connections: Updated diagram to show IOVDD connection to Host CPU supply.
- Table 7.2 GPIO Functionality Table on page 75: Sorted by GPIO name.
- Removed unbonded I/O from APORT mapping tables.
- Packaging figures updated with latest annotations.
- Removed tape and reel specifications section.
- Added package marking specifications in 8.3 BGM13S Package Marking.
- Added certification chapter .

Revision 0.5

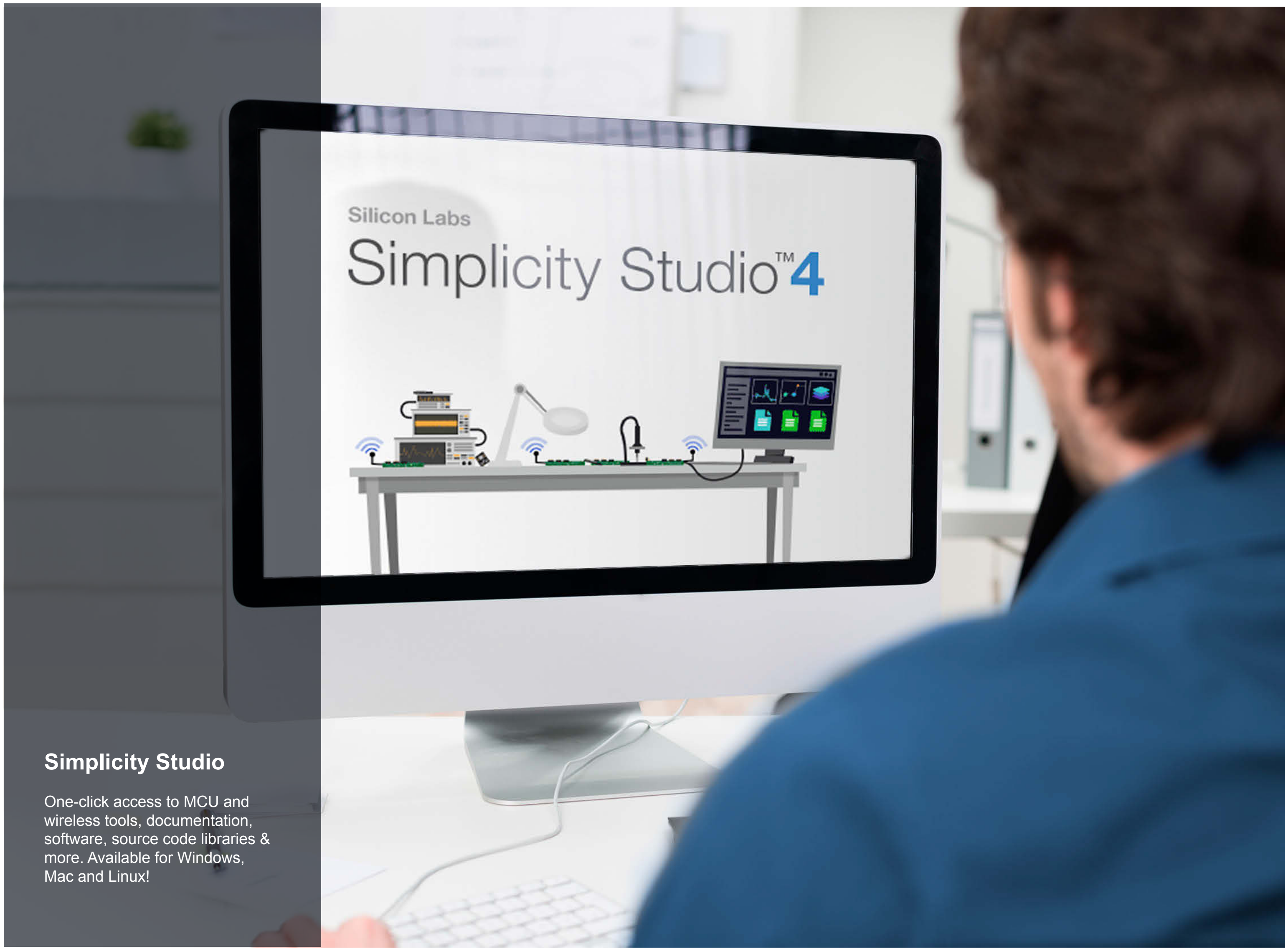
April 2018

- Removed PLFRCO content.
- Added V2 part numbers to Table 2.1 Ordering Information on page 3.
- Updated 4.1 Electrical Characteristics with latest characterization data and test limits.
- 5.1 Typical BGM13S Connections: Added optional 32.768 kHz crystal connection.
- 5.1 Typical BGM13S Connections: Corrected RTS/CTS naming on Host CPU for UART connection.
- 5.1 Typical BGM13S Connections: Corrected TCK/TMS order on standard ARM Cortex debug connector.
- 7.1 BGM13S Device Pinout: Changed pin 47 name from VSS to ANT_GND.
- 7.1 BGM13S Device Pinout: Corrected numbering of pins 50 and 51.
- Updated 8.2 BGM13S Recommeded PCB Land Pattern with latest drawings and dimension recommendations.

Revision 0.1

July 10, 2017

- Initial Release.



IoT Portfolio	SW/HW	Quality	Support and Community
www.silabs.com/IoT	*www.silabs.com/simplicity*	*www.silabs.com/quality*	*community.silabs.com*

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com